8-Channel, High-Bandwidth, Analog Front-End

Check for Samples: PGA5807A

FEATURES

- **8-Channel Complete AFE:**
  - **LNA, PGA, and LPF**
  - **Full-Channel Gain: 12 dB to 30 dB**
  - **Input-Referred Noise: 2.1 nV/$\sqrt{Hz}$**
- **LNA:**
  - **Gain: 12 dB**
  - **Fully Differential**
  - **Wide Input Common-Mode Support: 2.1 ± 200 mV**
  - **Maximum Linear Input Range: 500 mV_{PP}**
- **PGA Gain: 0 dB to 18 dB**
  - **With 3-dB Gain Steps**
  - **Programmable via Either Serial Interface or External Pins**
- **Maximum Total Channel Gain: 30 dB**
- **Programmable LPF:**
  - **Corner Frequency: 75 MHz, 60 MHz**
- **Power (Full-Chain):**
  - **60 mW per Channel**
- **Fast and Consistent Overload Recovery**
- **Small Package: 9-mm × 9-mm QFN-64**

APPLICATIONS

- **Data Acquisition Front Ends**
- **Ultrasound Imaging**

DESCRIPTION

The PGA5807A is an 8-channel, high-bandwidth, analog front-end (AFE). The device functions on a single 3.3-V analog supply. The device supports high-bandwidth input frequencies with a total power of 60 mW per channel. The PGA5807A consists of a low-noise amplifier (LNA), a programmable gain amplifier (PGA), and a programmable low-pass filter (LPF). The LNA has a fixed 12-dB gain (the differential amplifier supports both direct and capacitive input coupling) and supports a maximum linear input range of 500 mV_{PP}.

The device provides gain options from 0 dB to 18 dB, in 3-dB gain steps. This 18-dB PGA gain can be programmed using either the serial interface or external pins. The PGA5807A integrates an antialiasing filter in the form of an LPF to reduce noise. The device is available in a very small, 9-mm × 9-mm QFN-64 package and is specified for operation over the –40°C to +85°C temperature range.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR
PGA5807A	QFN-64	RGC

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.(1)

		VALUE	UNIT
Supply voltage range	AVDD	–0.3 to 3.9	V
Voltage at analog input and digital input		–0.3 to minimum (3.6, AVDD + 0.3)	V
Temperature range	Operating, T_A	–40 to +85	°C
	Storage, T_{stg}	–55 to +150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)	1	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
AVDD	Analog voltage supply	3.15		3.6	V
T_A	Operating temperature	–40		+85	°C
	Input common-mode voltage range	1.9		2.3	V

THERMAL INFORMATION

THERMAL METRIC(1)		PGA5807 RGC (QFN) 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	22.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	6.9	
θ_{JB}	Junction-to-board thermal resistance	2.4	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	2.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

Typical values are at T_A = +25°C, AVDD = 3.3 V, input dc-coupled with a 2.1-V common-mode voltage, LNA gain = 12 dB, PGA gain = 18 dB, total channel gain = 30 dB, bandwidth = high, and V_{OUT} = –1 dBFS, unless otherwise specified. Minimum and maximum values are specified across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C with AVDD = 3.3 V.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input-referred noise		f = 25 MHz, total channel gain = 30 dB		2.1		nV/√Hz
	Noise figure		R_S = 100 Ω, differential		6.4		dB
	Maximum linear input voltage		Total channel gain = 12 dB, differential		500		mV_{PP}
	Maximum linear output swing				2		V_{PP}
G_{LNA}	LNA gain				12		dB
	Maximum channel gain			29	30	31	dB
	PGA gain range			0		18	dB
	Gain step				3		dB
	Total output-referred noise		Total channel gain = 30 dB		450		µV
	Input resistance				5		kΩ
C_i	Input capacitance				3		pF
	LPF –3-dB cutoff frequency				75		MHz
	Gain matching		Across devices, T_A = +25°C	–1		1	dB
			Across channels in the same device		±0.25		dB
V_{ICR}	Input common-mode voltage range			1.9		2.3	V
	Output offset			–50		50	mV
V_{OCR}	Output common-mode voltage				950		mV
HD2	Harmonic distortion	Second	f = 25 MHz, V_{OUT} = –1 dBFS		–55		dBc
HD3		Third	f = 25 MHz, V_{OUT} = –1 dBFS		–50		dBc
THD		Total	f = 25 MHz, V_{OUT} = –1 dBFS		–48		dBc
IMD3	Intermodulation distortion		f_1 = 25 MHz at –7 dBFS, f_2 = 25 MHz, 1 MHz at –7 dBFS, for all PGA gains		–45		dBc
	Fundamental crosstalk		f = 25 MHz, V_{OUT} = –1 dBFS		–50		dBc
P_D	Power dissipation	Total, per channel			60	69	mW/ch
		Power-down mode	Partial power-down		4.2		mW/ch
			Complete power-down			2.5	mW/ch
	AVDD current (3.3 V)				145		mA
	Settling time for overload recovery		For 12-dB higher signal than linear input		–30		ns
	Power-up response time		Partial power-down		1		µs
			Full power-down		1		ms
PSRR	Power-supply rejection ratio		f = 10 kHz, gain = 30 dB		–40		dBc
			f = 10 kHz, gain = 12 dB		–38		dBc

DIGITAL CHARACTERISTICS

Typical values are at T_A = +25°C and AVDD = 3.3 V, unless otherwise specified. Minimum and maximum values are specified across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{IH}	Logic high input voltage		2			V
V_{IL}	Logic low input voltage		0			V
I_{IH}	Logic high input current			200		µA
I_{IL}	Logic low input current			200		µA
C_i	Input capacitance			5		pF
V_{OH}	Logic high output voltage	SDOUT pin		AVDD		V
V_{OL}	Logic low output voltage	SDOUT pin		0		V

PIN CONFIGURATION

RGC PACKAGE
QFN-64
(TOP VIEW)

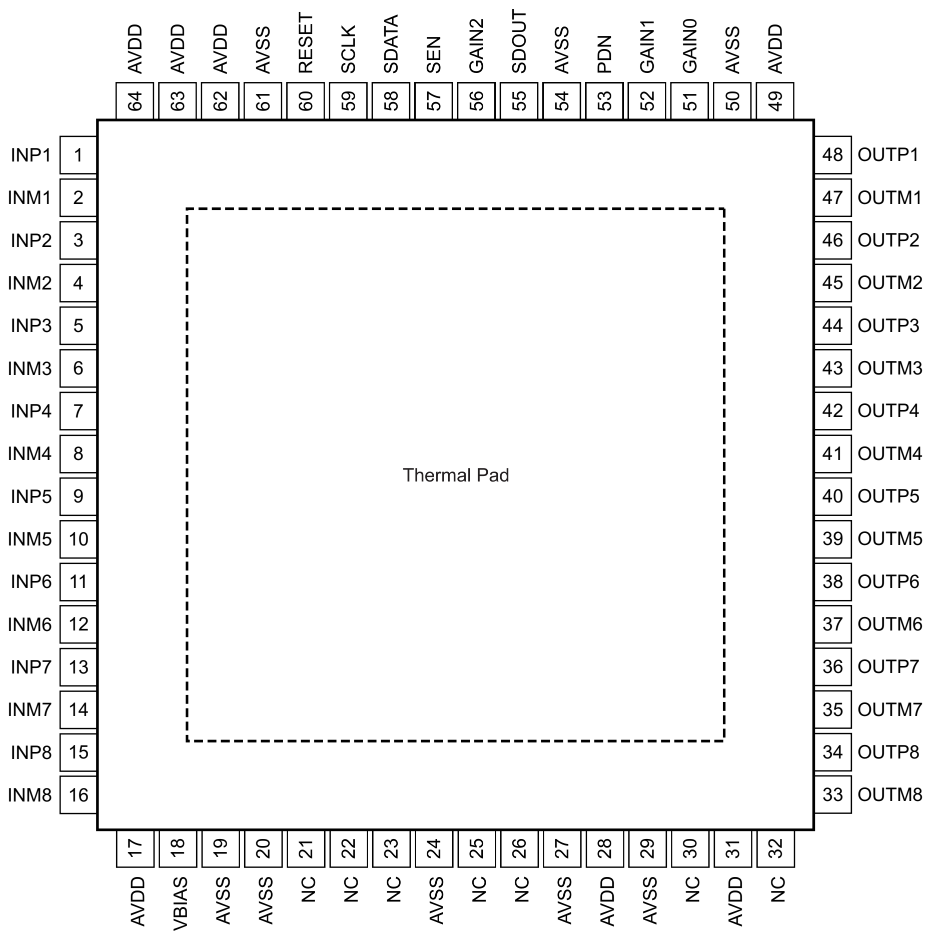


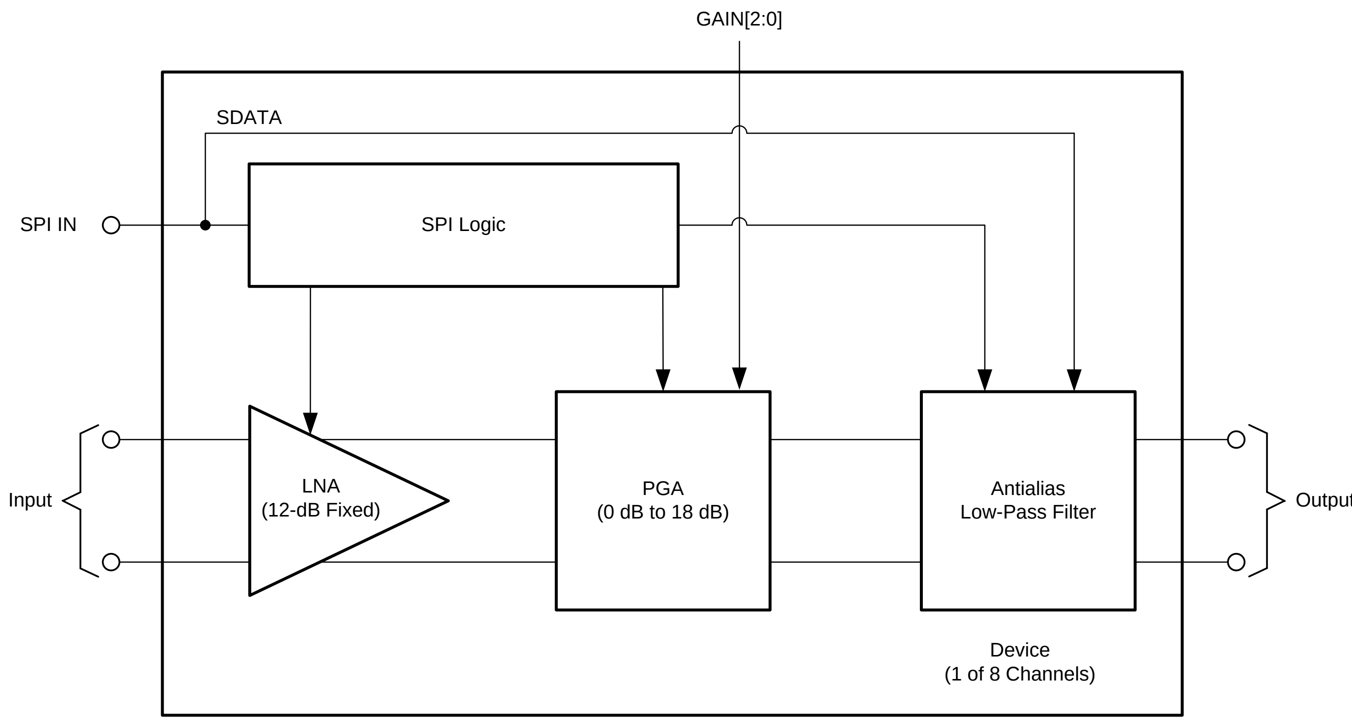
Table 1. PIN FUNCTIONS

NAME	NO.	FUNCTION	DESCRIPTION	
AVDD	17, 28, 31, 49, 62-64	Supply	Analog supply pin, 3.3 V	
AVSS	19, 20, 24, 27, 29, 50, 54, 61	Ground	Analog ground	
GAIN0	51	Digital input	When RESET is high, this pin is used to program the PGA gain. Refer to Table 2 for more details. Note: Use 3.3-V logic.	
GAIN1	52	Digital input	When RESET is high, this pin is used to program the PGA gain. Refer to Table 2 for more details. Note: Use 3.3-V logic.	
GAIN2	56	Digital input	When RESET is high, this pin is used to program the PGA gain. Refer to Table 2 for more details. Note: Use 3.3-V logic.	
INM1	2	Input	Complimentary analog input for channel 1	The dc input common-mode can be 2.1 V ± 200 mV.
INP1	1	Input	Analog input for channel 1	
INM2	4	Input	Complimentary analog input for channel 2	
INP2	3	Input	Analog input for channel 2	
INM3	6	Input	Complimentary analog input for channel 3	
INP3	5	Input	Analog input for channel 3	
INM4	8	Input	Complimentary analog input for channel 4	
INP4	7	Input	Analog input for channel 4	
INM5	10	Input	Complimentary analog input for channel 5	
INP5	9	Input	Analog input for channel 5	
INM6	12	Input	Complimentary analog input for channel 6	
INP6	11	Input	Analog input for channel 6	
INM7	14	Input	Complimentary analog input for channel 7	
INP7	13	Input	Analog input for channel 7	
INM8	16	Input	Complimentary analog input for channel 8	
INP8	15	Input	Analog input for channel 8	
NC	21-23, 25, 26, 30, 32	—	Unused pins; do not connect	
OUTM1	47	Output	Complimentary output pin for channel 1	The common-mode voltage is 0.95 V.
OUTP1	48	Output	Output pin for channel 1	
OUTM2	45	Output	Complimentary output pin for channel 2	
OUTP2	46	Output	Output pin for channel 2	
OUTM3	43	Output	Complimentary output pin for channel 3	
OUTP3	44	Output	Output pin for channel 3	
OUTM4	41	Output	Complimentary output pin for channel 4	
OUTP4	42	Output	Output pin for channel 4	
OUTM5	39	Output	Complimentary output pin for channel 5	
OUTP5	40	Output	Output pin for channel 5	
OUTM6	37	Output	Complimentary output pin for channel 6	
OUTP6	38	Output	Output pin for channel 6	
OUTM7	35	Output	Complimentary output pin for channel 7	
OUTP7	36	Output	Output pin for channel 7	
OUTM8	33	Output	Complimentary output pin for channel 8	
OUTP8	34	Output	Output pin for channel 8	
PDN	53	Digital input	Partial power-down control pin for the entire device with an internal 20-kΩ pull-down resistor; active high. Note: Use 3.3-V logic.	
RESET	60	Digital input	Logic hardware reset pin. Note: Use 3.3-V logic.	
SCLK	59	Digital input	Serial interface clock pin with an internal 20-kΩ pull-down resistor. Note: Use 3.3-V logic.	
SDATA	58	Digital input	Serial interface data input with an internal 20-kΩ pull-down resistor. When RESET is high, the corner frequency for the antialias filter can be programmed to a lower frequency (60 MHz) by setting this pin high. Note: Use 3.3-V logic.	
SDOUT	55	Digital output	Serial interface readout pin	
SEN	57	Digital input	Serial interface enabled for channels 1 to 8 with an internal 20-kΩ pull-up resistor; active low. Note: Use 3.3-V logic.	
VBIAS	18	Decap	Bias voltage; bypass to ground with a 1-µF capacitor or greater	

Table 2. PGA Gain Control

GAIN[2:0]	PGA_GAIN (dB)
000	18
001	15
010	12
011	9
100	6
101	3
110	0

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = 3.3 V, input dc-coupled with 2.1-V input common-mode, LNA gain = 12 dB, PGA gain = 18 dB, total channel gain = 30 dB, GAIN[2:0] = 000, f_{IN} = 5 MHz, default LPF filter corner, and V_{OUT} = –1 dBFS, unless otherwise noted.

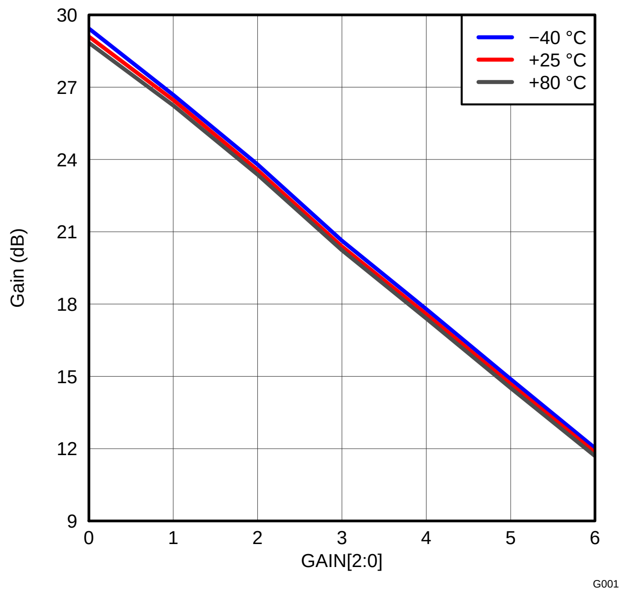


Figure 1. GAIN vs GAIN[2:0] ACROSS TEMPERATURE

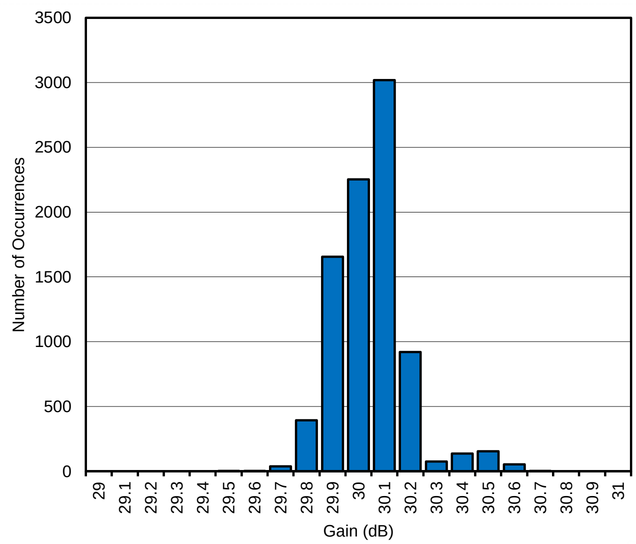


Figure 2. GAIN-MATCHING HISTOGRAM (Gain = 30 dB)

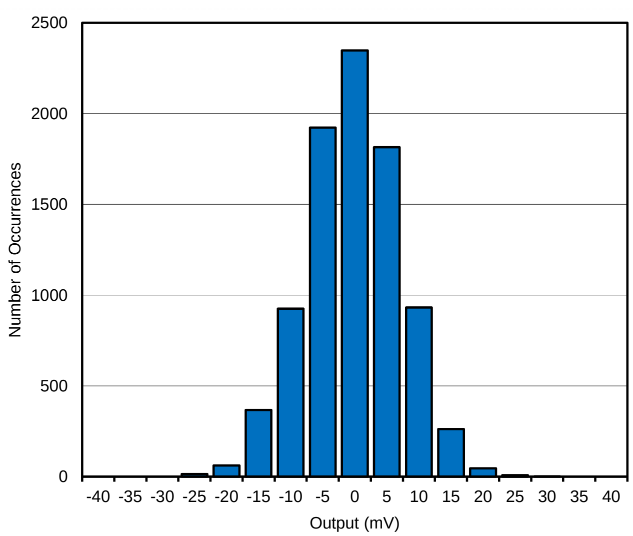


Figure 3. OUTPUT OFFSET HISTOGRAM (Gain = 30 dB)

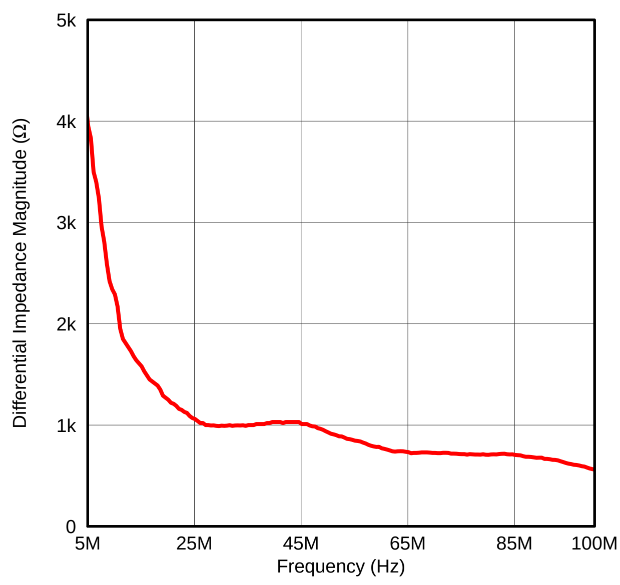


Figure 4. INPUT IMPEDANCE MAGNITUDE

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3.3 V, input dc-coupled with 2.1-V input common-mode, LNA gain = 12 dB, PGA gain = 18 dB, total channel gain = 30 dB, GAIN[2:0] = 000, f_{IN} = 5 MHz, default LPF filter corner, and V_{OUT} = –1 dBFS, unless otherwise noted.

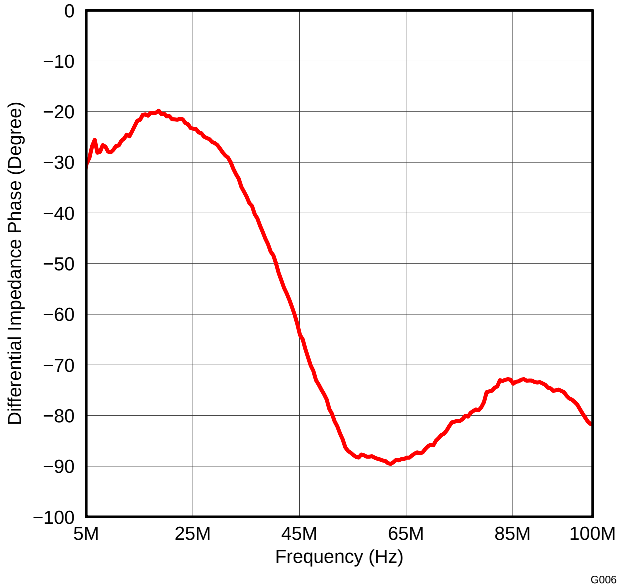


Figure 5. INPUT IMPEDANCE PHASE

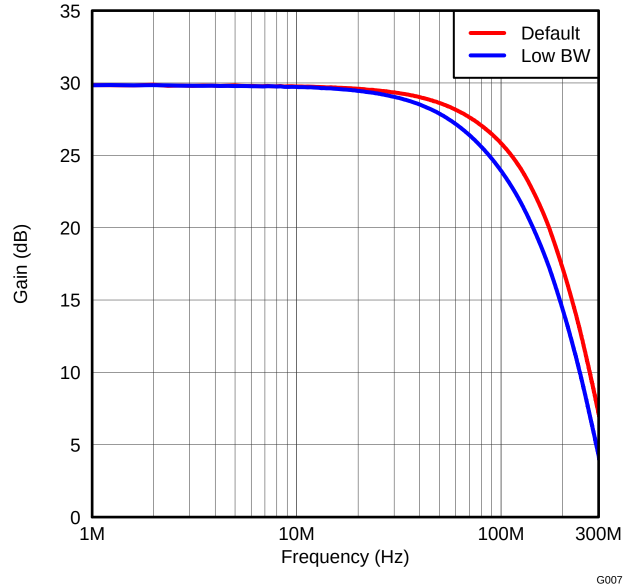


Figure 6. LOW-PASS FILTER RESPONSE

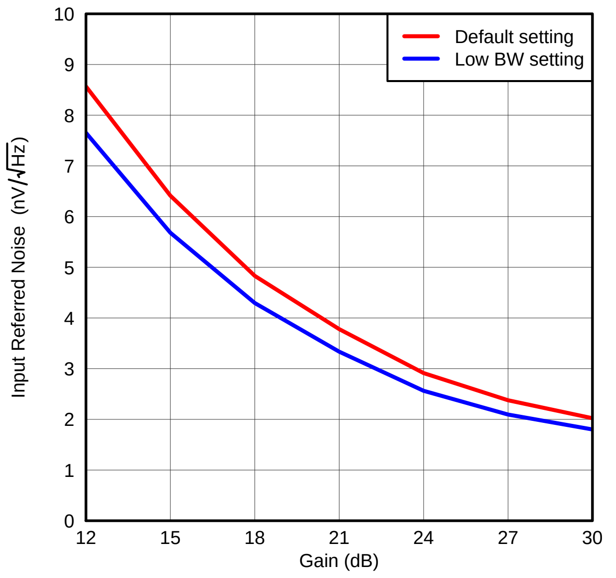


Figure 7. INPUT-REFERRED NOISE vs GAIN

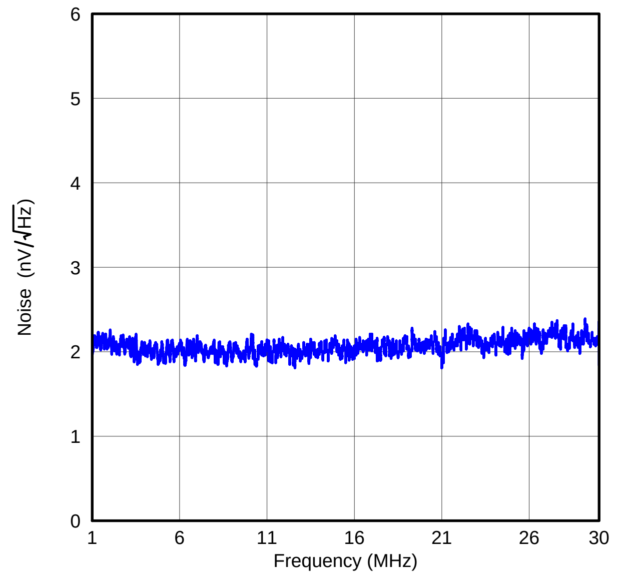


Figure 8. INPUT-REFERRED NOISE vs FREQUENCY (Gain = 30 dB)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3.3 V, input dc-coupled with 2.1-V input common-mode, LNA gain = 12 dB, PGA gain = 18 dB, total channel gain = 30 dB, GAIN[2:0] = 000, f_{IN} = 5 MHz, default LPF filter corner, and V_{OUT} = –1 dBFS, unless otherwise noted.

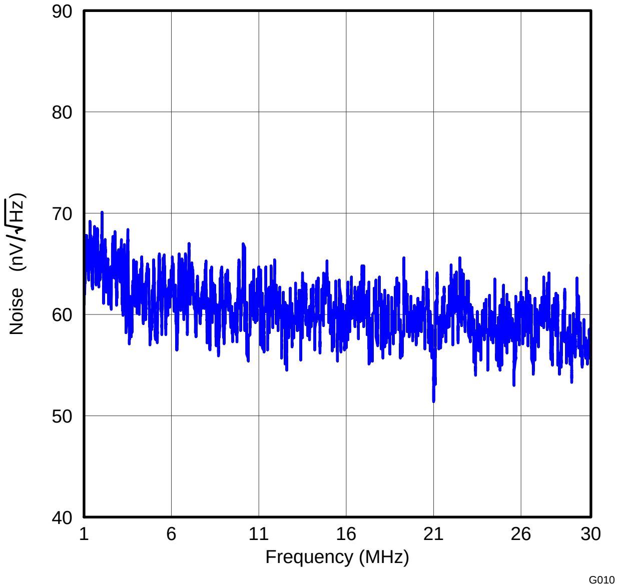


Figure 9. OUTPUT-REFERRED NOISE vs FREQUENCY (Gain = 30 dB)

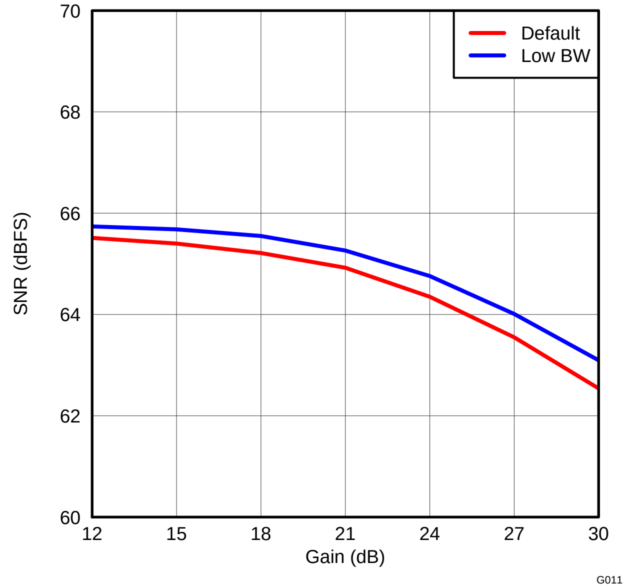


Figure 10. SIGNAL-TO-NOISE RATIO vs GAIN ACROSS BANDWIDTH MODE

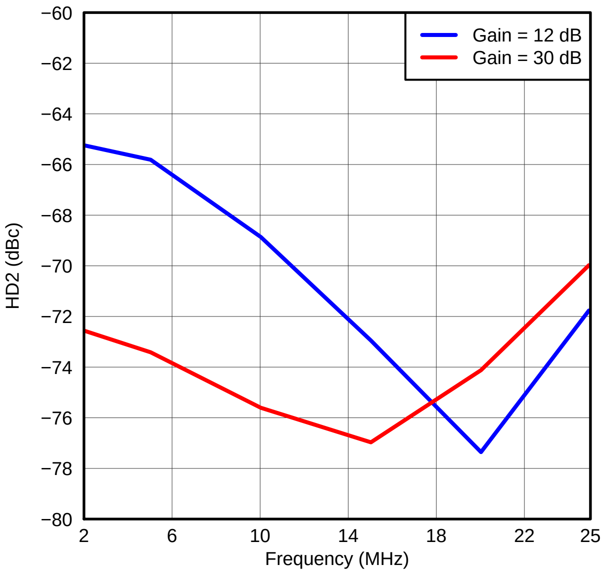


Figure 11. SECOND-HARMONIC DISTORTION vs FREQUENCY

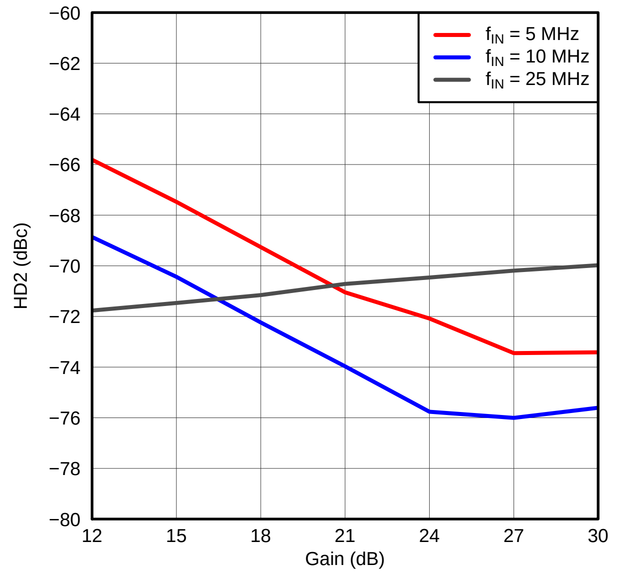


Figure 12. SECOND-HARMONIC DISTORTION vs GAIN

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3.3 V, input dc-coupled with 2.1-V input common-mode, LNA gain = 12 dB, PGA gain = 18 dB, total channel gain = 30 dB, GAIN[2:0] = 000, f_{IN} = 5 MHz, default LPF filter corner, and V_{OUT} = –1 dBFS, unless otherwise noted.

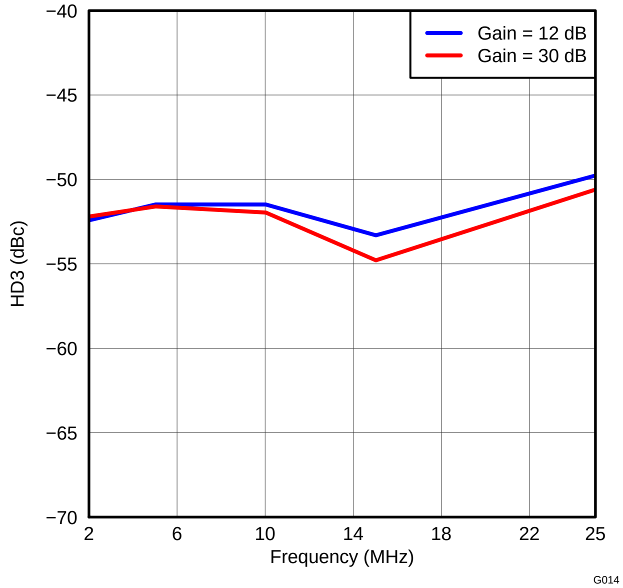


Figure 13. THIRD-HARMONIC DISTORTION vs FREQUENCY

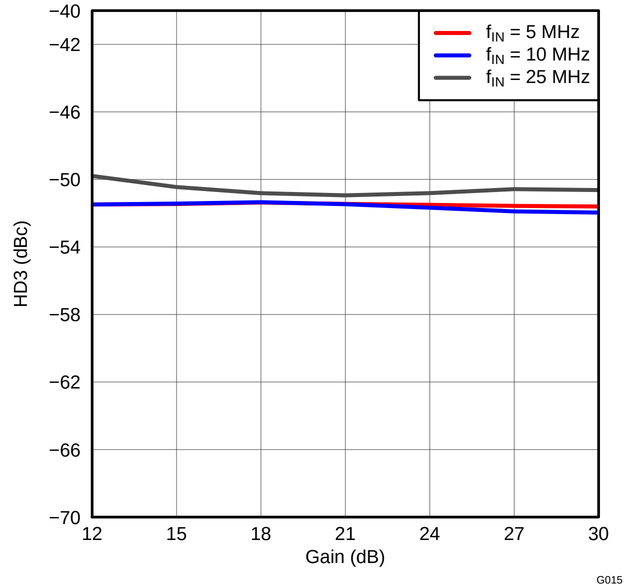


Figure 14. THIRD-HARMONIC DISTORTION vs GAIN

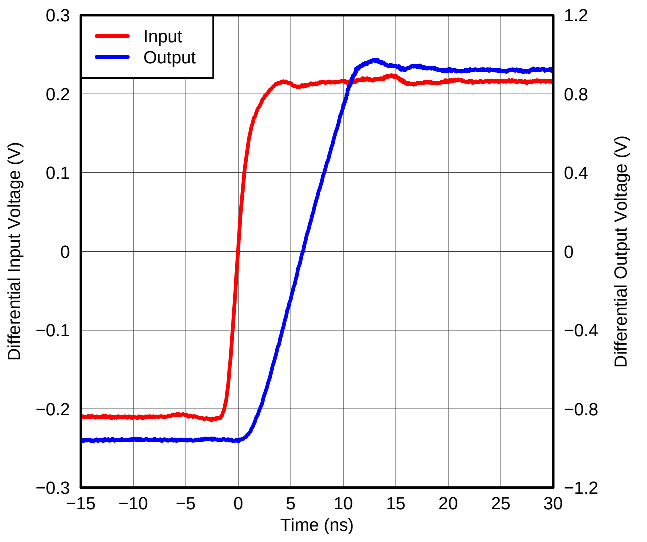


Figure 15. DIFFERENTIAL OUTPUT RESPONSE FOR AN INPUT STEP (12-dB Total Channel Gain)

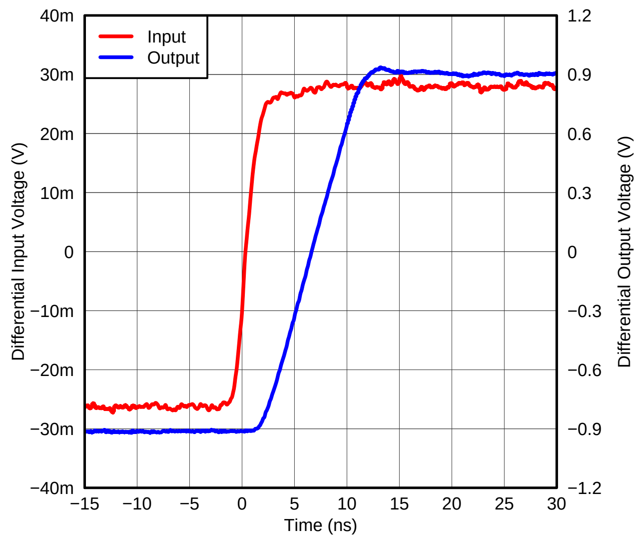


Figure 16. DIFFERENTIAL OUTPUT RESPONSE FOR AN INPUT STEP (30-dB Total Channel Gain)

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = 3.3 V, input dc-coupled with 2.1-V input common-mode, LNA gain = 12 dB, PGA gain = 18 dB, total channel gain = 30 dB, GAIN[2:0] = 000, f_{IN} = 5 MHz, default LPF filter corner, and V_{OUT} = –1 dBFS, unless otherwise noted.

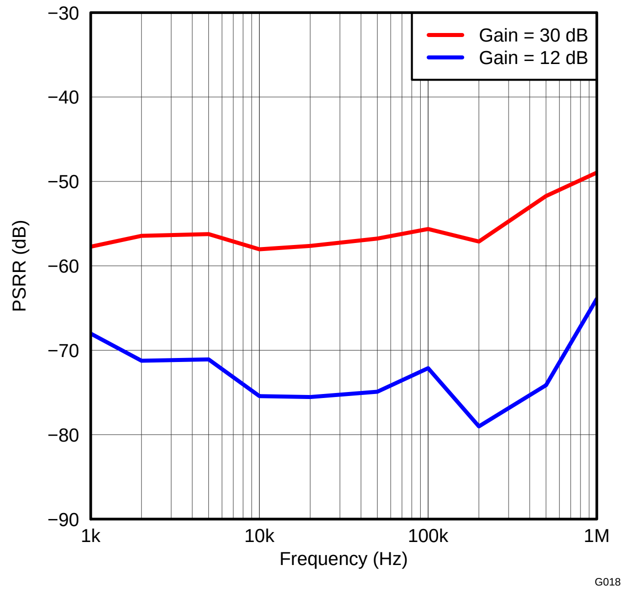


Figure 17. POWER-SUPPLY REJECTION RATIO (100-mV$_{PP}$ Supply Noise with Different Frequencies)

SERIAL REGISTER TIMING

SERIAL REGISTER WRITE DESCRIPTION

Programming different modes can be accomplished through the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and RESET pins. Each of these pins has a 20-kΩ pull-down resistor to GND. Serially shifting bits into the device is enabled when SEN is low. SDATA serial data are latched at every SCLK rising edge when SEN is active (low). Serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse (an internal counter counts groups of 24 clocks after the SEN falling edge). The interface can function with SCLK frequencies from 20 MHz down to low speeds (of a few Hertz) and even with a non-50% duty cycle SCLK. Data are divided into two main portions to load on the addressed register: a register address (eight bits) and the actual data (16 bits). When writing to a register with unused bits, these bits should be set to '0'. Figure 18 shows a timing diagram of the write operation. Table 3 lists the serial interface timing characteristics.

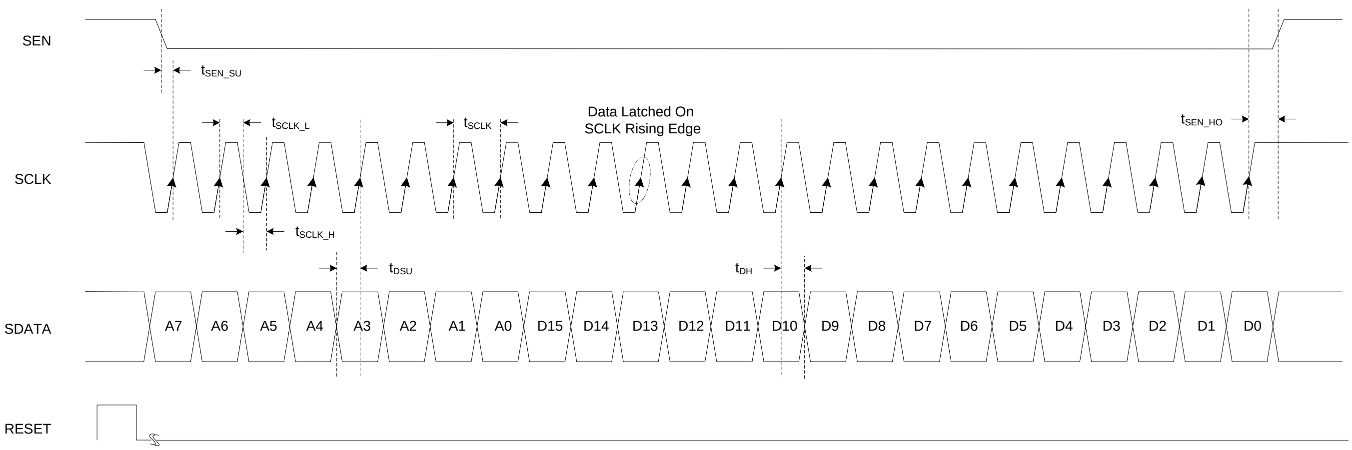


Figure 18. Serial Interface Timing Diagram

Table 3. Serial Interface Timing Characteristics(1)

PARAMETER		MIN	TYP	MAX	UNIT
t_{SCLK}	SCLK period	50			ns
t_{SCLK_H}	SCLK high time	20			ns
t_{SCLK_L}	SCLK low time	20			ns
t_{DSU}	Data setup time	5			ns
t_{DHO}	Data hold time	5			ns
t_{SEN_SU}	SEN falling edge to SCLK rising edge	8			ns
t_{SEN_HO}	Time between last SCLK rising edge to SEN rising edge	8			ns
t_{OUT_DV}(2)	Delay from SCLK falling edge to SDOUT valid	12	20	28	ns

(1) Minimum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C and AVDD = 3.3 V.
(2) See Figure 19.

REGISTER READOUT

The device includes an option where the contents of the internal registers can be read back. This readout may be useful as a diagnostic test to verify the serial interface communication between the external controller and the AFE. First, the REGISTER READOUT ENABLE bit (bit 1, register 00h) must be set to '1'. Then, initiate a serial interface cycle specifying the register address (A[7:0]) to be read. The data bits are *don't care*. The device outputs the contents (D[15:0]) of the selected register on the SDOUT pin. SDOUT has a typical 20-ns delay (t_{OUT_DV}) from the SCLK falling edge. For a lower speed SCLK, SDOUT can be latched on the SCLK rising edge. For a higher speed SCLK (for example, with an SCLK period less than 60 ns), latching SDOUT at the next SCLK falling edge is preferable. Figure 19 shows the read operation timing diagram (timing specifications follow the same information provided in Table 3). In readout mode, REGISTER READOUT ENABLE can still be accessed through SDATA, SCLK, and SEN. To enable serial register writes, set the REGISTER READOUT ENABLE bit back to '0'.

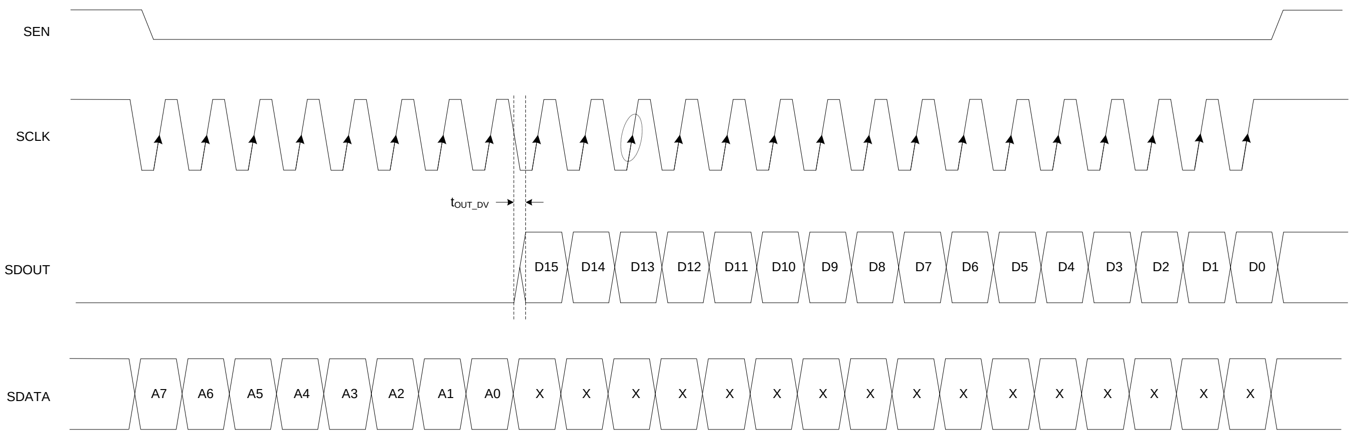


Figure 19. Serial Interface Register Read Timing Diagram

REGISTER MAP

A reset process is required at the device initialization stage. Initialization can be accomplished in one of two ways:

1. Through a hardware reset, by applying a positive pulse on the RESET pin, or
2. Through a software reset (using the serial interface), by setting the SW_RESET bit high. Setting this bit initializes the internal registers to the respective default values (all '0's) and then self-resets the SW_RESET bit low. In this case, the RESET pin can remain low (inactive).

After reset, all PGA registers are set to ‘0’ (default). During register programming, all reserved or unlisted register bits must be set to ‘0’. Register settings are maintained when the device is in either partial or complete power-down mode. Table 4 lists the PGA register map.

Table 4. PGA Register Map

REGISTER (Hex)	DECIMAL VALUE	Bit 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00	0	X[1]	X	X	X	X	X	X	X	X	X	X	X	X	X	REGISTER READOUT ENABLE[2]	SW_RESET
35	53	COMPLETE PDN	PARTIAL PDN	X	X	X	X	X	X	X	X	X	X	X	X	X	X
3B	59	X	X	X	X	X	X	X	X	LOW _ FILTER_BW	PGA_GAIN			X	X	X	X

(1) X = don't care.
(2) Shaded cells indicate used bits.

Register Descriptions

Table 5. Register 00h

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	X	X	REGISTER READOUT ENABLE	SW_RESET

Bits 15:2 **Don't care**

Default = 0.

Bit 1 **REGISTER READOUT ENABLE**

0 = Readout disabled (default)
1 = Register readout enabled at SDOUT pin

Bit 0 **SW_RESET**

0 = Normal operation (default)
1 = Resets the device and self-clears the bit to '0'

Table 6. Register 35h

15	14	13	12	11	10	9	8
COMPLETE PDN	PARTIAL PDN	X	X	X	X	X	X

7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X

Bit 15 **COMPLETE PDN**

Bit 14 **PARTIAL PDN**

0 = Normal operation (default)
1 = LNA and PGA powered down

Bits 13:0 **Don't care**

Default = 0.

Table 7. Register 3Bh

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X

7	6	5	4	3	2	1	0
LOW_FILTER_BW	PGA_GAIN			X	X	X	X

Bits 15:8 **Don't care**

Default = 0.

Bit 7 **LOW_FILTER_BW**

0 = 75-MHz bandwidth (default)
1 = 60-MHz bandwidth

Bits 6:4 **PGA_GAIN**

000 = 18-dB PGA gain (default)
001 = 15-dB PGA gain
010 = 12-dB PGA gain
011 = 9-dB PGA gain
100 = 6-dB PGA gain
101 = 3-dB PGA gain
110 = 0-dB PGA gain

Bits 3:0 **Don't care**

Default = 0.

APPLICATION INFORMATION

THEORY OF OPERATION

The PGA5807A is a programmable gain amplifier (PGA) for applications with input frequencies up to 25 MHz. The device includes a low-noise amplifier (LNA) with a fixed gain, followed by a PGA and an antialiasing filter to reduce noise. The LNA is a fully-differential amplifier with a 12-dB fixed gain and can support a 500-mV_{PP} maximum linear differential input swing. The PGA is implemented as an attenuator followed by a fixed-gain amplifier with 18-dB gain. The attenuator can provide attenuation from 0 dB to –18 dB in 3-dB steps. The attenuator can be controlled by the GAIN[2:0] pins or by using register 3Bh (bits 6 to 4). The antialiasing filter is combined with the fixed-gain amplifier. The filter has one active pole and a passive pole for a combined bandwidth of 75 MHz. For low-frequency applications, bandwidth can be reduced to 60 MHz where better noise can be achieved. The device can be programmed in this mode either by using the SDATA pin while RESET is high or by using bit 7 of register 3Bh. This device can directly drive ADCs such as the ADS5296.

Low-Noise Amplifier (LNA)

In most data-acquisition systems, an LNA is required at the front-end to obtain good noise performance. The PGA5807A has a fully-differential LNA with a 12-dB fixed gain. The LNA input-referred noise is 1.9 nV/$\sqrt{Hz}$, and supports a differential 500-mV_{PP} input swing. The LNA input can be applied either directly or through an ac-coupling capacitor. Internally, the LNA input is connected to a 2.1-V common-mode voltage via a large resistor (8 kΩ). For direct input coupling, the LNA supports an input common-mode range from 1.9 V to 2.3 V. The LNA input circuits are shown in Figure 20.

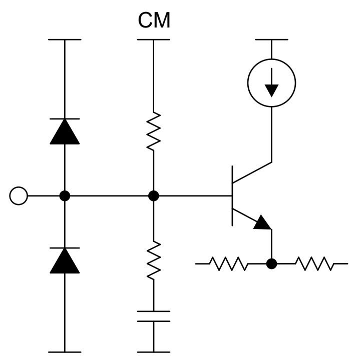


Figure 20. INP and INM Equivalent Circuits of LNA Inputs

Programmable Gain Amplifier (PGA) and Filter

The LNA output is transmitted to a PGA with a programmable gain from 0 dB to 18 dB in 3-dB steps. This gain can either be controlled through a serial interface or through pins, as explained in the *Serial Register Write Description* section. The PGA is implemented as a programmable attenuator and as a fixed-gain amplifier with an 18-dB gain. This architecture helps achieve the same bandwidth across different gain settings. The attenuator provides programmable attenuation from 0 dB to 18 dB.

The attenuator architecture is shown in Figure 21. There are six shunt resistors that can be connected or disconnected to achieve programmable attenuation. The network provides 0-dB attenuation when no shunt resistors are connected. When the first shunt resistor (RS_1) is turned on, an attenuation of 3 dB is obtained. For achieving 6-dB attenuation, both RS_1 and RS_2 are turned on. Similarly, by turning on additional resistors, greater attenuation can be achieved; by turning on all resistors, an effective 18-dB attenuation is achieved.

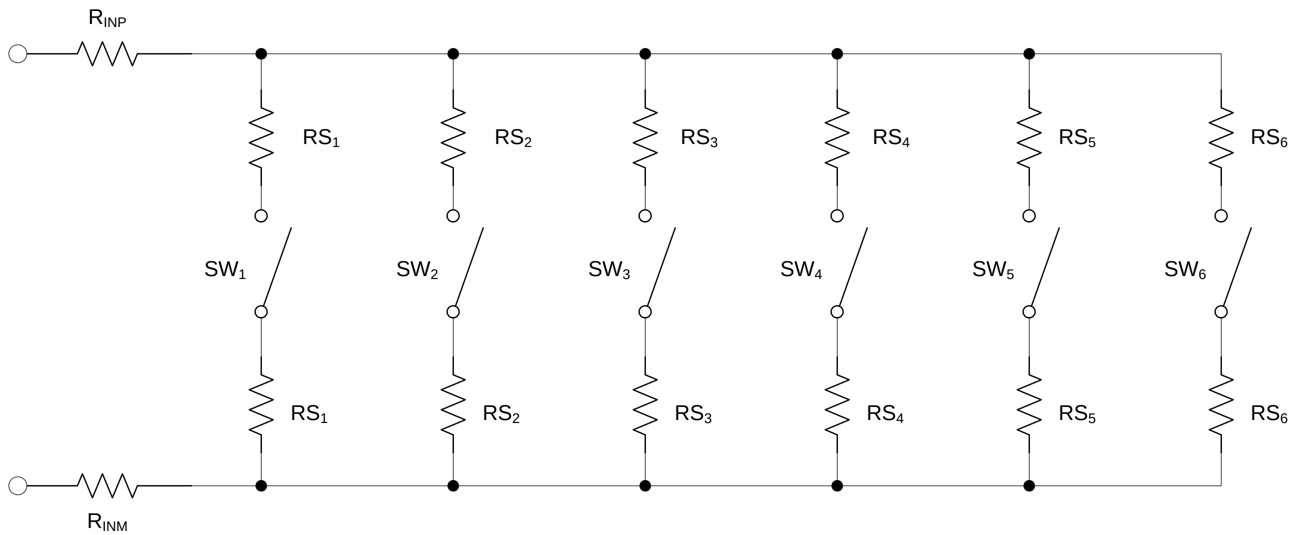


Figure 21. Programmable Attenuator

The attenuator is followed by a 18-dB fixed-gain amplifier. The amplifier is implemented as a voltage-to-current (V-to-I) converter followed by a current-to-voltage (I-to-V) converter. The I-to-V bandwidth is limited so that it functions as an LPF and is followed by a passive filter, as shown in Figure 22. Both the active and passive filters provide an antialiasing filter action, which helps reduce noise when the PGA output is sampled by an ADC. The architecture of the passive filter is selected to reduce the glitches that can occur when the PGA5807A output is sampled by an ADC. For example, the PGA5807A can be directly connected to ADC devices (such as the ADS5295 or ADS5296) without any external components between the ADC and PGA5807A. Figure 23 shows an example of the PGA5807A connected directly to the ADS5296.

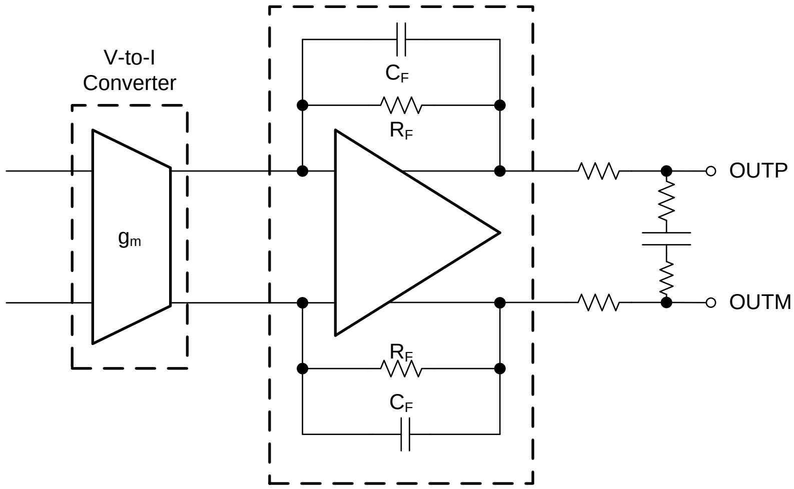


Figure 22. Antialias Filter

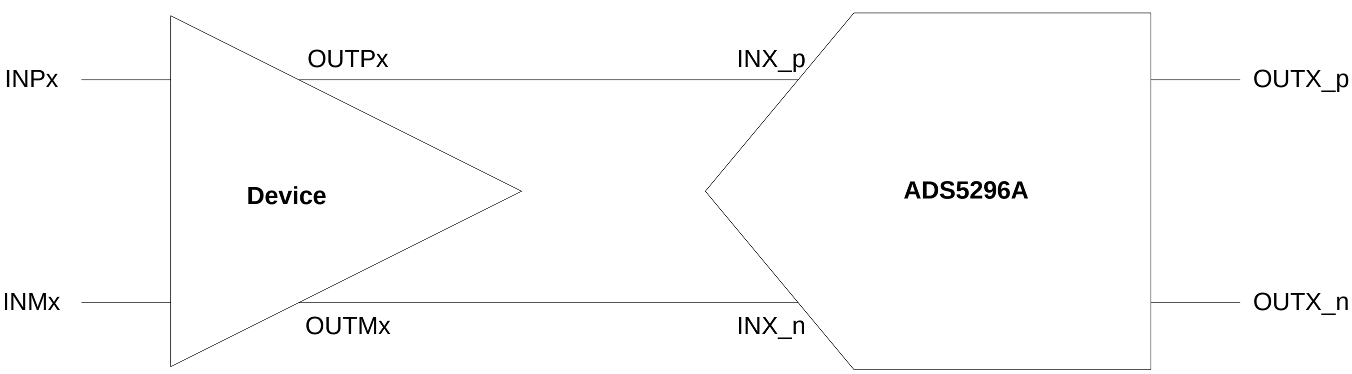


Figure 23. PGA Connected to an ADC

DEVICE CONFIGURATION USING SERIAL INTERFACE OR PARALLEL PINS

Different device modes (such as channel gain and bandwidth) can be programmed by either using the serial interface or external pins. The device can be configured via the serial interface only when the device RESET pin is pulsed and remains low. In this configuration, device gain can be programmed through register 3Bh (bits 6 to 4) and bandwidth can be programmed by register 3Bh (bit 7). When the RESET pin is connected to 3.3 V or is pulled high, the serial interface is unable to control the device. In this configuration, the GAIN[2:0] pins can be used to control gain and the SDATA pin can be used to control bandwidth.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA5807ARGCR	ACTIVE	VQFN	RGC	64	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	PGA5807	Samples
PGA5807ARGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	PGA5807	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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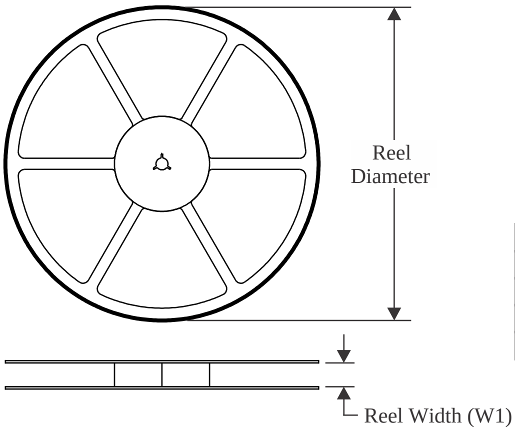
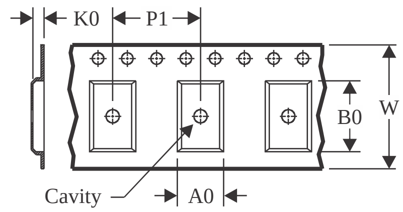
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

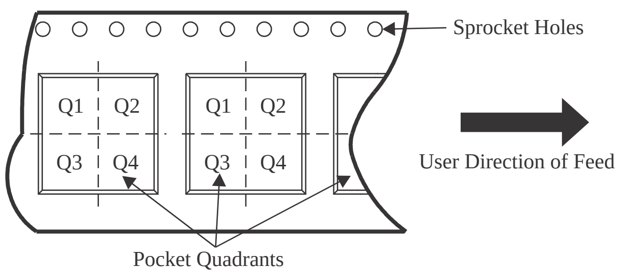


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

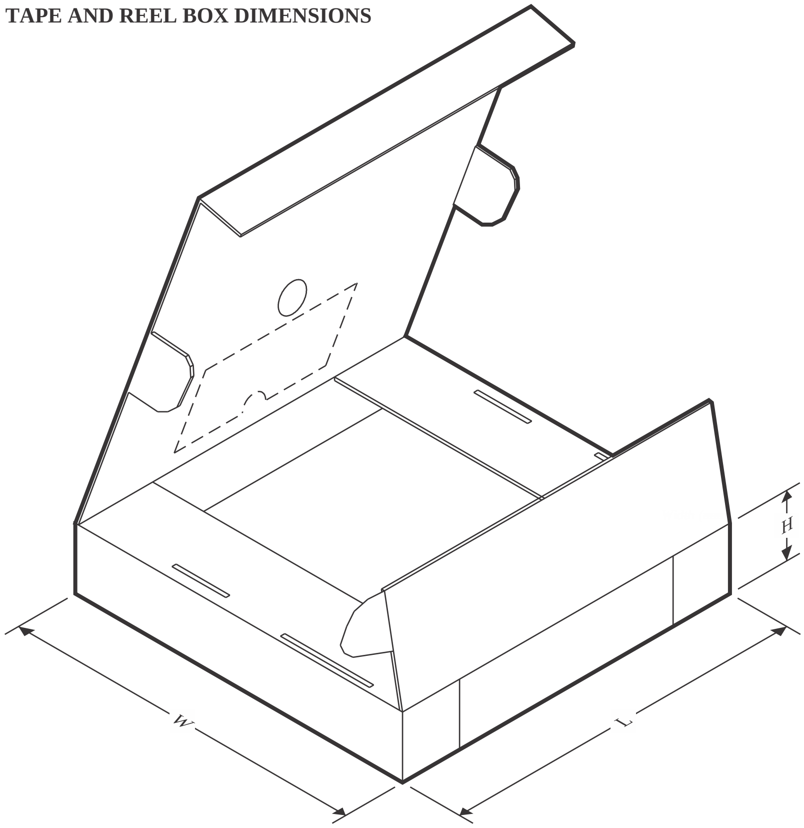
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA5807ARGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA5807ARGCR	VQFN	RGC	64	2000	350.0	350.0	43.0

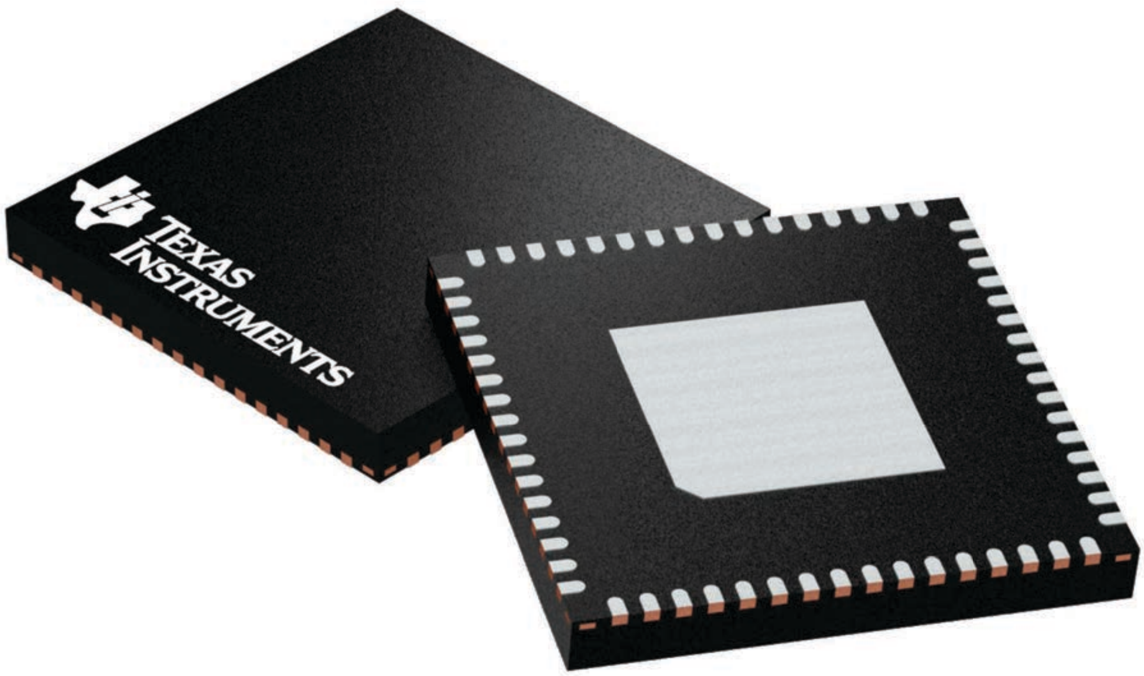
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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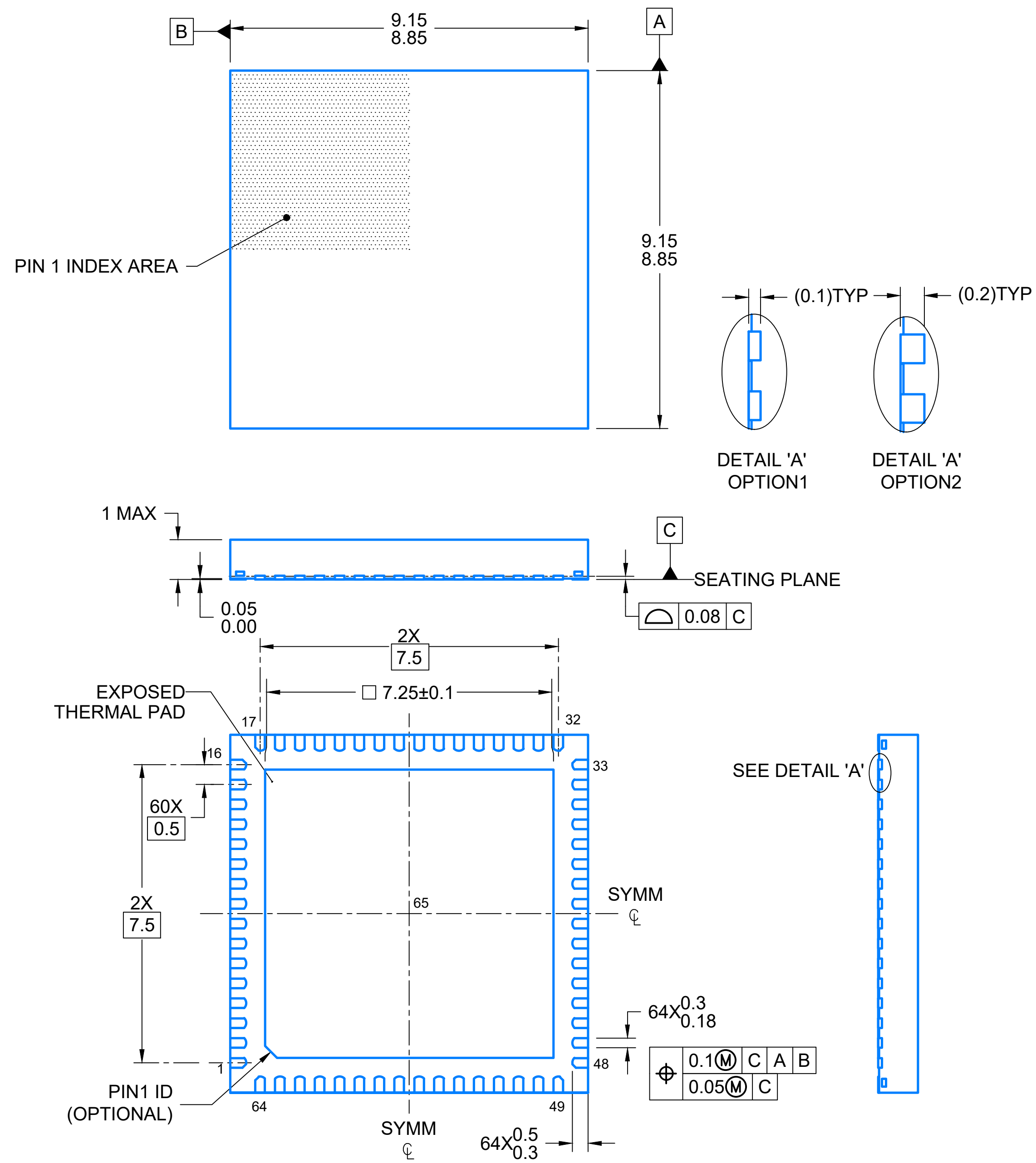

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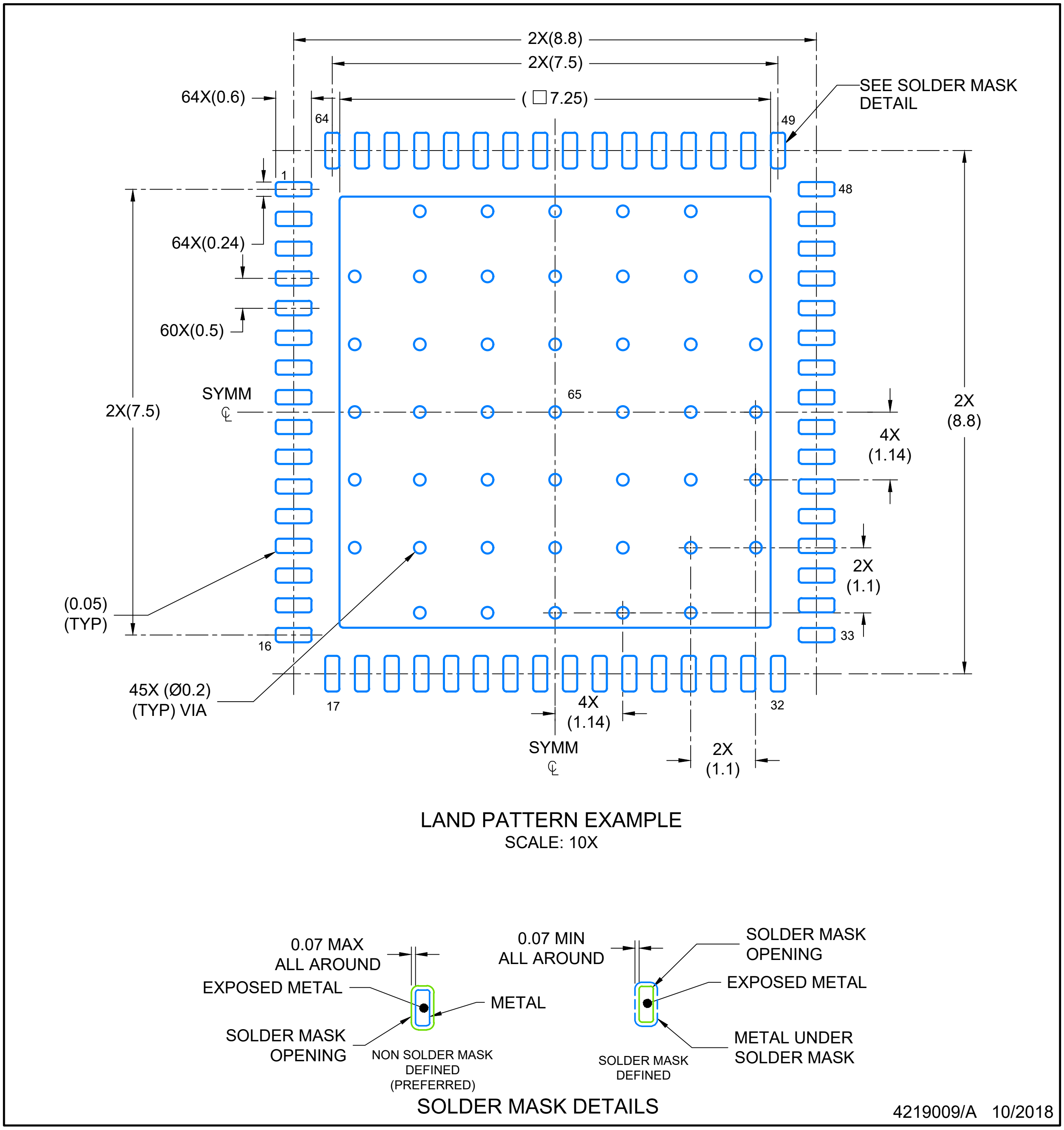
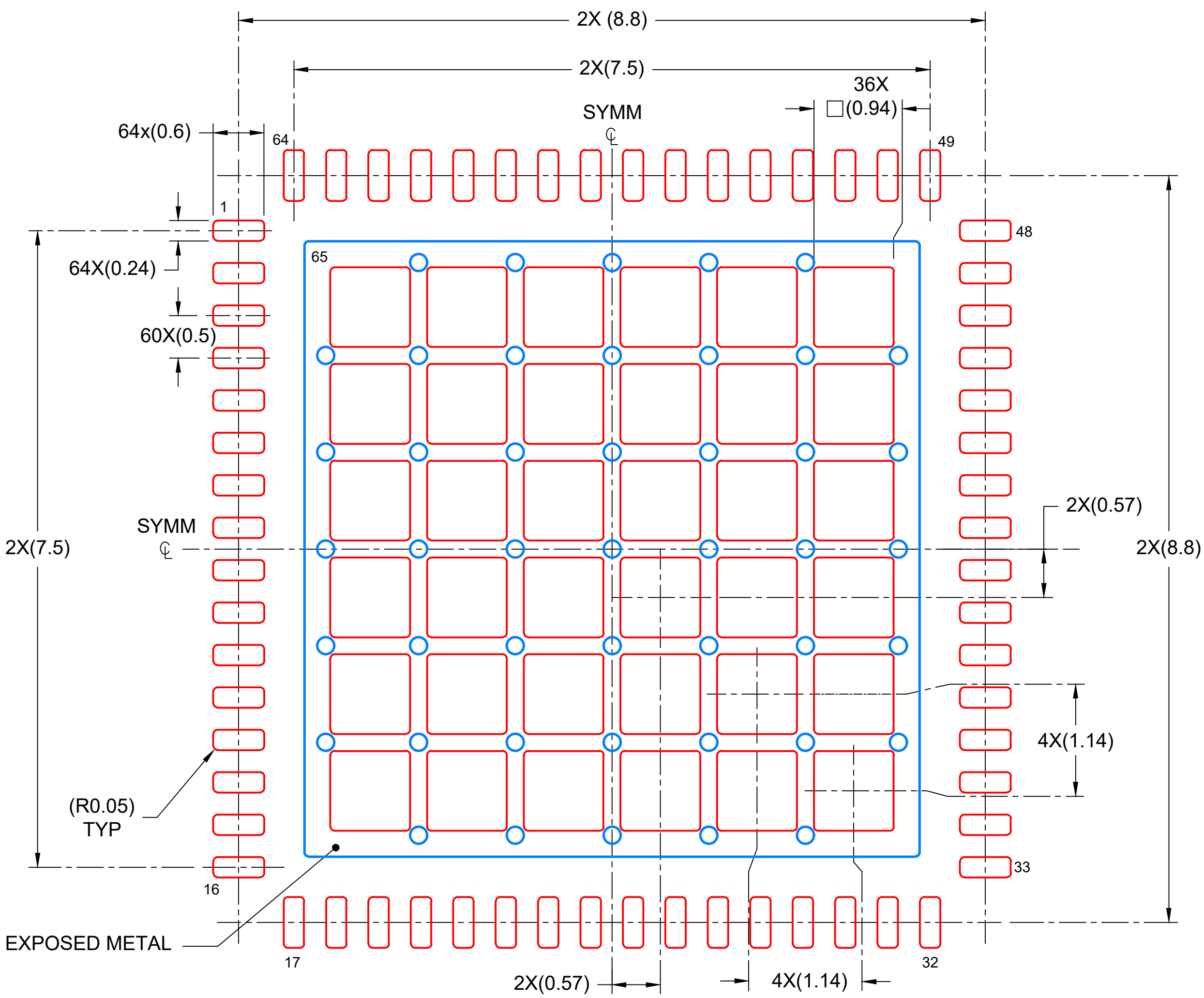
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60% PRINTED COVERAGE BY AREA
SCALE: 12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.