

## SNx4AHC08 Quadruple 2-Input Positive-AND Gates

### 1 Features

- 2V to 5.5V operating range
- Latch-up performance exceeds 250mA per JESD 17
- ESD protection exceeds JESD 22

### 2 Applications

- Servers
- Network Switches
- PCs and Notebooks
- Electronic Points of Sale

### 3 Description

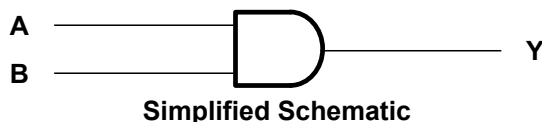
The SNx4AHC08 devices are quadruple 2-input positive-AND gates. These devices perform the Boolean function  $Y = A \cdot B$  or  $Y = \overline{A + B}$  in positive logic.

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE <sup>(2)</sup>
SN74AHC08	D (SOIC, 14)	8.65mm × 3.90mm
	DB (SSOP, 14)	6.20mm × 5.30mm
	DGV (TVSOP, 14)	3.60mm × 4.40mm
	N (PDIP, 14)	19.30mm × 6.35mm
	NS (SO, 14)	10.30mm × 5.30mm
	PW (TSSOP, 14)	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm
	BQA (WQFN, 14)	3mm × 2.5mm
SN54AHC08	FK (LCCC, 20)	8.89mm × 8.89mm

(1) For more information, see [Section 11](#).

(2) The body size (length × width) is a nominal value and does not include pins.



## Table of Contents

<b>1 Features</b> .....	1	7.1 Overview.....	12
<b>2 Applications</b> .....	1	7.2 Functional Block Diagram.....	12
<b>3 Description</b> .....	1	7.3 Feature Description.....	12
<b>4 Pin Configuration and Functions</b> .....	3	7.4 Device Functional Modes.....	12
<b>5 Specifications</b> .....	5	<b>8 Application and Implementation</b> .....	13
5.1 Absolute Maximum Ratings.....	5	8.1 Application Information.....	13
5.2 ESD Ratings.....	5	8.2 Typical Application.....	13
5.3 Recommended Operating Conditions.....	5	8.3 Layout.....	15
5.4 Thermal Information.....	6	<b>9 Device and Documentation Support</b> .....	16
5.5 Electrical Characteristics, $T_A = 25^\circ\text{C}$ .....	6	9.1 Documentation Support.....	16
5.6 Electrical Characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$ .....	7	9.2 Receiving Notification of Documentation Updates....	16
5.7 Electrical Characteristics, $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ .....	7	9.3 Support Resources.....	16
5.8 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	8	9.4 Trademarks.....	16
5.9 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	8	9.5 Electrostatic Discharge Caution.....	16
5.10 Noise Characteristics.....	9	9.6 Glossary.....	16
5.11 Operating Characteristics.....	9	<b>10 Revision History</b> .....	16
5.12 Typical Characteristics.....	10	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	17
<b>6 Parameter Measurement Information</b> .....	11		
<b>7 Detailed Description</b> .....	12		

### 4 Pin Configuration and Functions

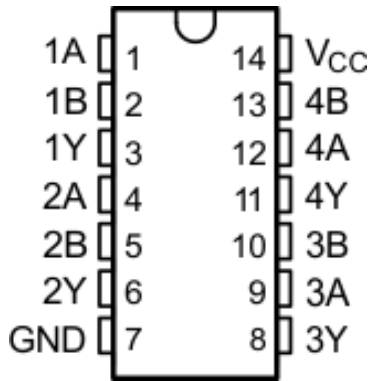


Figure 4-1. D, DB, DGV, N, NS, PW, or W Package 14-Pin SOIC, SSOP, TVSOP, PDIP, SO, or TSSOP (Top View)

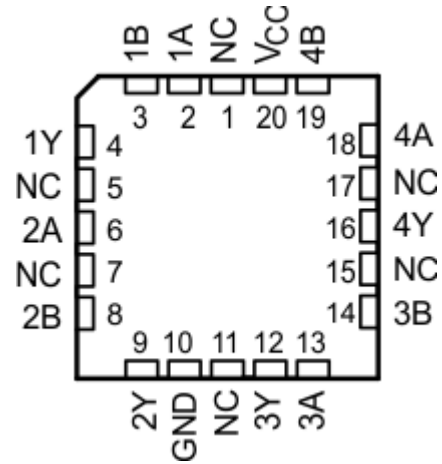


Figure 4-2. FK Package 20-Pin LCCC (Top View)

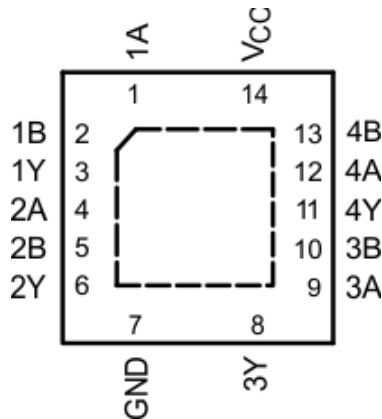


Figure 4-3. RGY or BQA Package 14-Pin VQFN or WQFN (Top View)

Table 4-1. Pin Functions

NAME	PIN			I/O	DESCRIPTION
	SOIC, SSOP, TVSOP, PDIP, SO, TSSOP	VQFN, WQFN	LCCC		
1A	1	1	2	I	1A Input
1B	2	2	3	I	1B Input
1Y	3	3	4	O	1Y Output
2A	4	4	6	I	2A Input
2B	5	5	8	I	2B Input
2Y	6	6	9	O	2Y Output
3Y	8	8	12	O	3Y Output
3A	9	9	13	I	3A Input
3B	10	10	14	I	3B Input
4Y	11	11	16	O	4Y Output
4A	12	12	18	I	4A Input
4B	13	13	19	I	4B Input
GND	7	7	10	—	Ground Pin
NC	—	—	1, 5, 7, 11, 15, 17	—	No Connection
V <sub>CC</sub>	14	14	20	—	Power Pin

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
V <sub>I</sub>	Input voltage <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage, V <sub>O</sub> <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
	Continuous current through V <sub>CC</sub> or GND			±50 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5		V
		V <sub>CC</sub> = 3 V	2.1		
		V <sub>CC</sub> = 5.5 V	3.85		
V <sub>IL</sub>	Low-level Input voltage	V <sub>CC</sub> = 2 V		0.5	V
		V <sub>CC</sub> = 3 V		0.9	
		V <sub>CC</sub> = 5.5 V		1.65	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V		-50	mA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		-4	
		V <sub>CC</sub> = 5 V ± 0.5 V		-8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V		50	mA
		V <sub>CC</sub> = 3.3 V ± 0.3 V		4	
		V <sub>CC</sub> = 5 V ± 0.5 V		8	
Δt/Δv	Input Transition rise or fall rate	V <sub>CC</sub> = 3.3 V ± 0.3 V		100	ns/V
		V <sub>CC</sub> = 5 V ± 0.5 V		20	

**SN54AHC08, SN74AHC08**

SCLS236L – OCTOBER 1995 – REVISED FEBRUARY 2024

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
T <sub>A</sub>	Operating free-air temperature	SN54AHC08	-55	125	°C
		SN74AHC08	-40	125	

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AHC08								UNIT	
	D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	RGY (VQFN)	BQA (WQFN)		
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	124.5	96	127	80	76	147.7	87.1	88.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics, T<sub>A</sub> = 25°C

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2	V	
		3 V	2.9	3		
		4.5 V	4.4	4.5		
	I <sub>OH</sub> = -4 mA	3 V	2.58			
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	V
		3 V			0.1	
		4.5 V			0.1	
	I <sub>OH</sub> = 4 mA	3 V			0.36	
	I <sub>OH</sub> = 8 mA	4.5 V			0.36	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10	pF

## 5.6 Electrical Characteristics, $T_A = -55^\circ\text{C}$ to $125^\circ\text{C}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	SN54AHC08		UNIT
			MIN	MAX	
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	2 V	1.9		V
		3 V	2.9		
		4.5 V	4.4		
	$I_{OH} = -4 \text{ mA}$	3 V	2.48		
	$I_{OH} = -8 \text{ mA}$	4.5 V	3.8		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	2 V		0.1	V
		3 V		0.1	
		4.5 V		0.1	
	$I_{OH} = 4 \text{ mA}$	3 V		0.5	
	$I_{OH} = 8 \text{ mA}$	4.5 V		0.5	
$I_I$	$V_I = 5.5 \text{ V}$ or GND	0 V to 5.5 V		$\pm 1^{(1)}$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		20	$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V			pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at  $V_{CC} = 0 \text{ V}$ .

## 5.7 Electrical Characteristics, $T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A$	SN74AHC08		UNIT	
				MIN	MAX		
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	2 V		1.9		V	
		3 V		2.9			
		4.5 V		4.4			
	$I_{OH} = -4 \text{ mA}$	3 V		2.48			
	$I_{OH} = -8 \text{ mA}$	4.5 V		3.8			
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	2 V			0.1	V	
		3 V			0.1		
		4.5 V			0.1		
	$I_{OH} = 4 \text{ mA}$	3 V	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		0.44		
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ Recommended		0.5		
	$I_{OH} = 8 \text{ mA}$	4.5 V	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		0.44		
			$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$ Recommended		0.5		
$I_I$	$V_I = 5.5 \text{ V}$ or GND	0 V to 5.5 V			$\pm 1$	$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20	$\mu\text{A}$	
$C_i$	$V_I = V_{CC}$ or GND	5 V	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		10	pF	

## 5.8 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A$	MIN	TYP	MAX	UNIT
$t_{PLH}, t_{PHL}$	A or B	Y	$C_L = 15 \text{ pF}$	$T_A = 25^\circ\text{C}$		6.2 <sup>(1)</sup>	8.8 <sup>(1)</sup>	ns
				$T_A = -55^\circ\text{C to } 125^\circ\text{C, SN54AHC08}$		1 <sup>(1)</sup>	10.5 <sup>(1)</sup>	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C, SN74AHC08}$		1	10.5	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended, SN74AHC08}$		1	10.5	
$t_{PLH}, t_{PHL}$	A or B	Y	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		8.7	12.3	ns
				$T_A = -55^\circ\text{C to } 125^\circ\text{C, SN54AHC08}$		1	14	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C, SN74AHC08}$		1	14	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended, SN74AHC08}$		1	14	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 5.9 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

 over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A$	MIN	TYP	MAX	UNIT
$t_{PLH}, t_{PHL}$	A or B	Y	$C_L = 15 \text{ pF}$	$T_A = 25^\circ\text{C}$		4.3 <sup>(1)</sup>	5.9 <sup>(1)</sup>	ns
				$T_A = -55^\circ\text{C to } 125^\circ\text{C, SN54AHC08}$		1 <sup>(1)</sup>	7 <sup>(1)</sup>	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C, SN74AHC08}$		1	7	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended, SN74AHC08}$		1	7	
$t_{PLH}, t_{PHL}$	A or B	Y	$C_L = 50 \text{ pF}$	$T_A = 25^\circ\text{C}$		5.8	7.9	ns
				$T_A = -55^\circ\text{C to } 125^\circ\text{C, SN54AHC08}$		1	9	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C, SN74AHC08}$		1	9	
				$T_A = -40^\circ\text{C to } 125^\circ\text{C Recommended, SN74AHC08}$		1	9	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.



## 5.10 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

		SN74AHC08		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$	4.4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

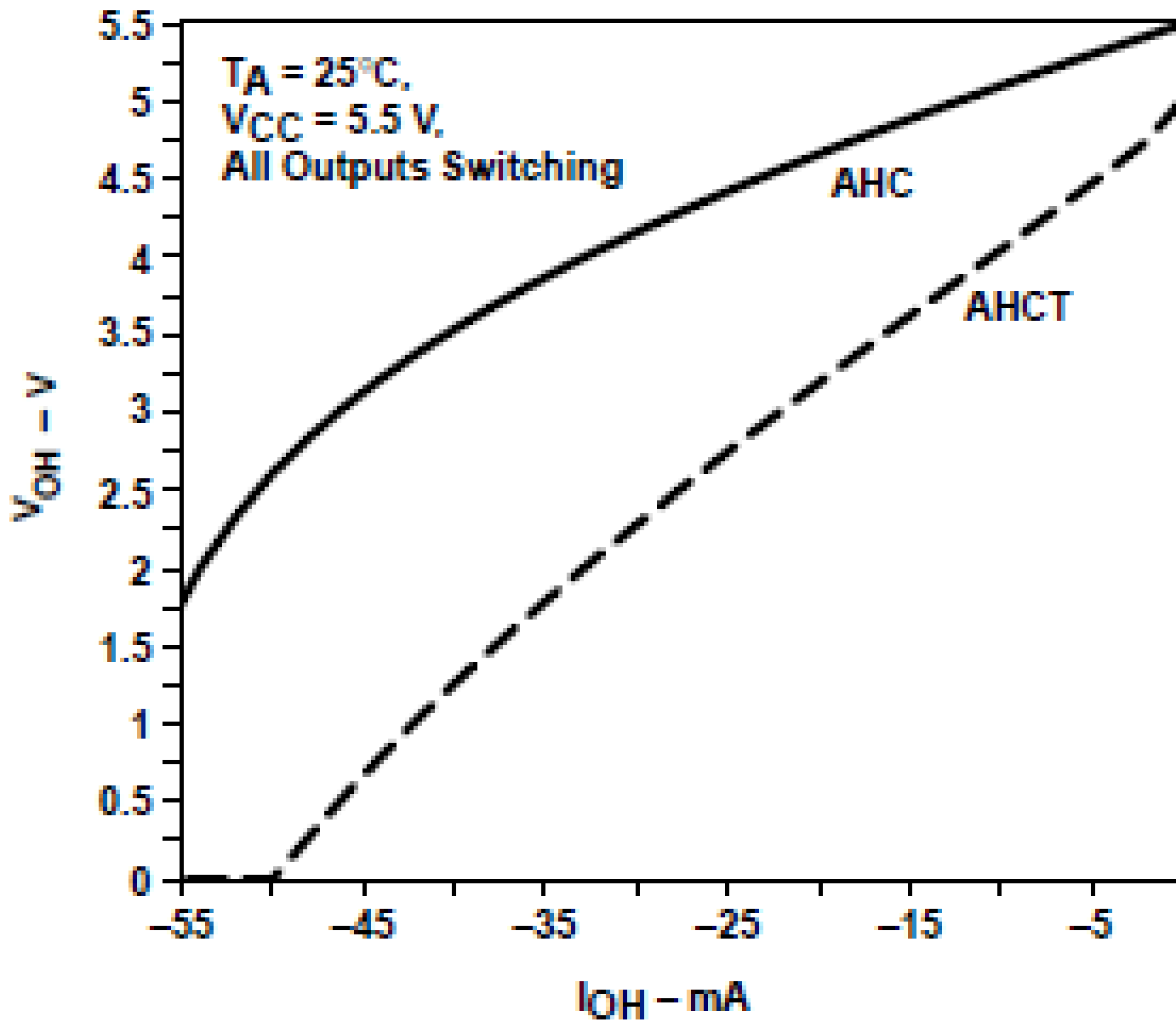
(1) Characteristics are for surface-mount packages only.

## 5.11 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	18	pF

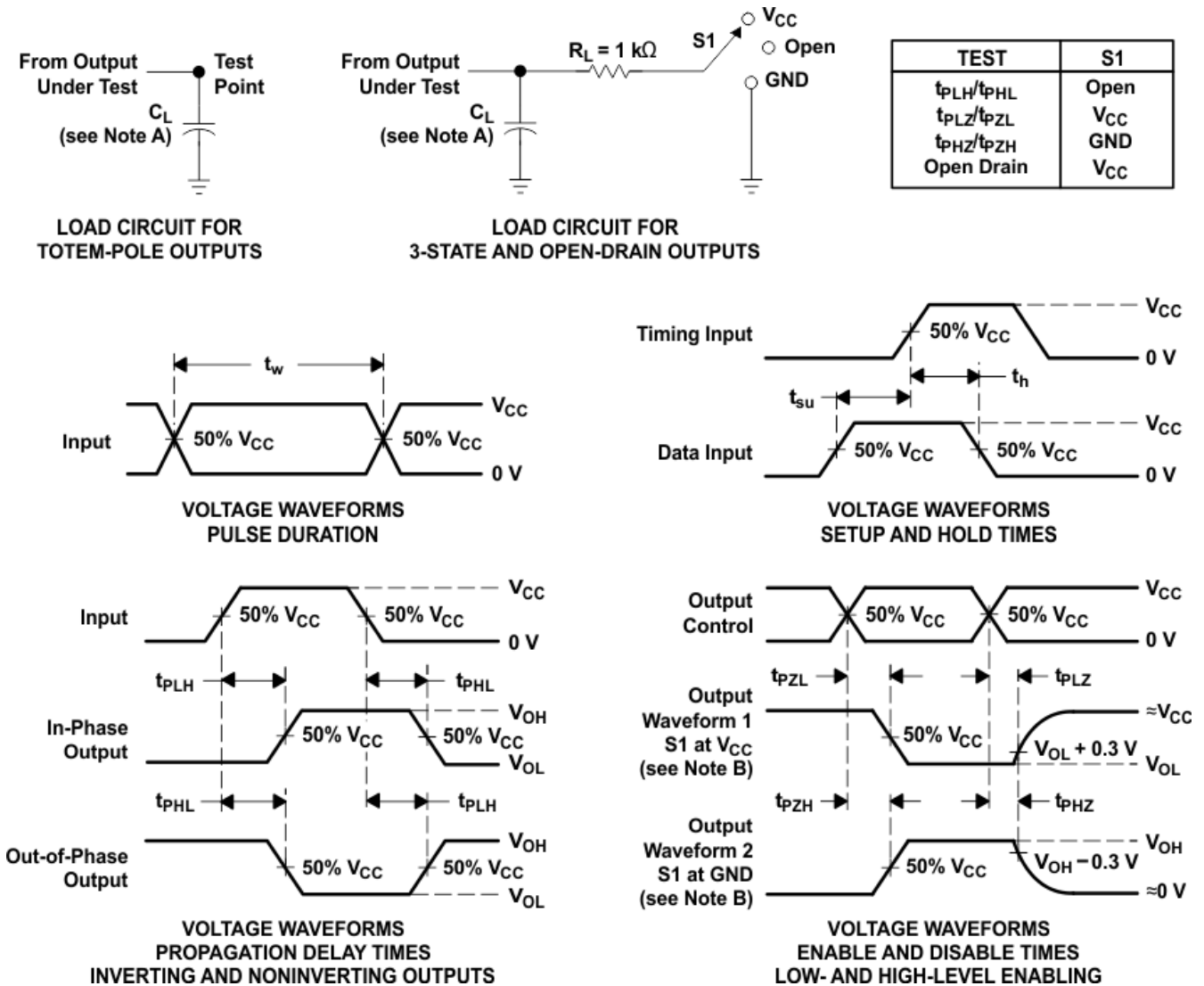
### 5.12 Typical Characteristics



$V_{CC} = 5.5\text{ V}$

Figure 5-1. AHC Family  $V_{OL}$  vs  $I_{OL}$

## 6 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

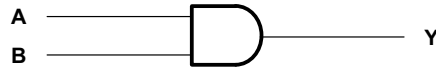
Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SNx4AHC08 devices are quadruple 2-input positive-AND gates with low drive that will produce slow rise and fall times. This slow transition reduces ringing on the output signal. The inputs are high impedance when  $V_{CC} = 0$  V.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

Slow rise and fall time on outputs allow for low-noise outputs.

### 7.4 Device Functional Modes

Table 7-1 is the function table for the SNx4AHC08.

**Table 7-1. Function Table  
(Each Gate)**

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

A common application for AND gates is the use in power sequencing. Power sequencing is often employed in applications that require a processor or other delicate device with specific voltage timing requirements in order to protect the device from malfunctioning. Using the SN74AHC08 to verify that the processor has turned on can protect it from harmful signals.

### 8.2 Typical Application

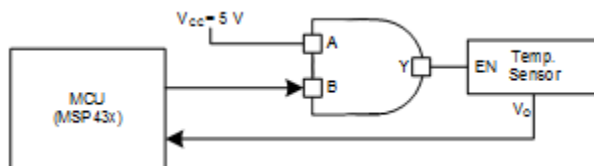


Figure 8-1. Typical Application Diagram

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions must be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

1. Recommended input conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta v)$  in the [Section 5.3](#) table.
  - Specified High and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Section 5.3](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$
2. Recommend output conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

### 8.2.3 Application Curve

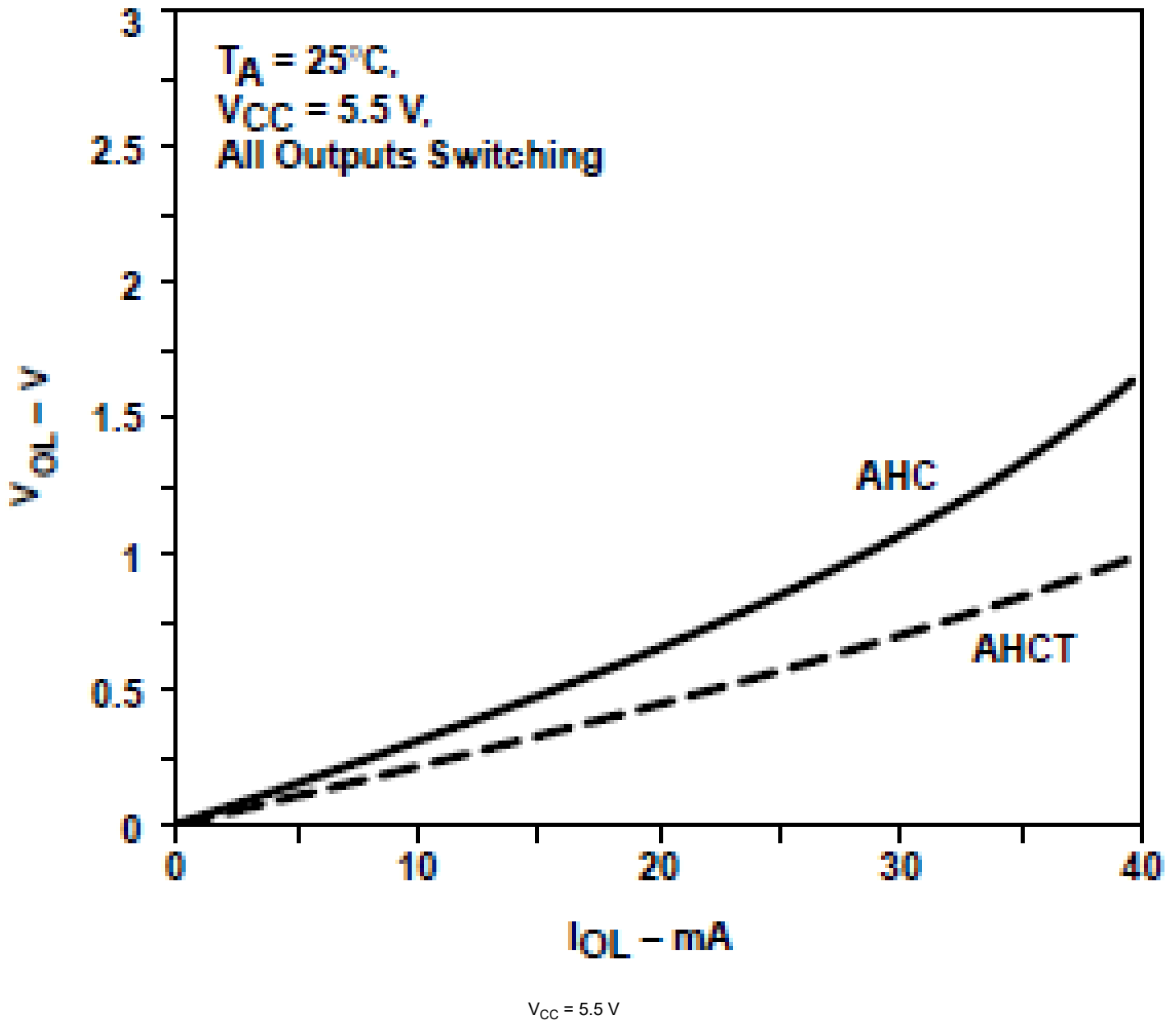


Figure 8-2. AHC Family  $V_{OH}$  vs  $I_{OH}$

### Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Section 5.1](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

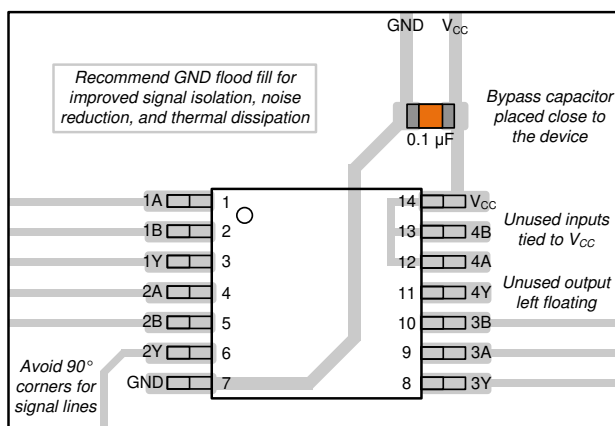
## 8.3 Layout

### 8.3.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Figure 8-3 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

#### 8.3.1.1 Layout Example



**Figure 8-3. Layout Example for the SNx4AHC08**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 9-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC08	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74AHC08	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision K (June 2023) to Revision L (February 2024)</b>	<b>Page</b>
• Updated RθJA value: RGY = 47 to 87.1, all values in °C/W .....	6

<b>Changes from Revision J (December 2015) to Revision K (June 2023)</b>	<b>Page</b>
• Added BQA package to <i>Device Information</i> table.....	1
• Updated RθJA values: D = 86 to 124.5, PW = 113 to 147.7 .....	6
• Added thermal value for RθJA: BQA = 88.3, all values in °C/W.....	6



## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9682001Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682001Q2A SNJ54AHC 08FK	<a href="#">Samples</a>
SN74AHC08BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08	<a href="#">Samples</a>
SN74AHC08D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	AHC08	
SN74AHC08DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	<a href="#">Samples</a>
SN74AHC08DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	<a href="#">Samples</a>
SN74AHC08DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08	<a href="#">Samples</a>
SN74AHC08N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC08N	<a href="#">Samples</a>
SN74AHC08NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC08	<a href="#">Samples</a>
SN74AHC08PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	HA08	
SN74AHC08PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HA08	<a href="#">Samples</a>
SN74AHC08PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	<a href="#">Samples</a>
SN74AHC08RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA08	<a href="#">Samples</a>
SNJ54AHC08FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9682001Q2A SNJ54AHC 08FK	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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#### OTHER QUALIFIED VERSIONS OF SN54AHC08, SN74AHC08 :

- Catalog : [SN74AHC08](#)
- Enhanced Product : [SN74AHC08-EP](#), [SN74AHC08-EP](#)
- Military : [SN54AHC08](#)

#### NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC08BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC08DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC08DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC08NSR	SO	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74AHC08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC08RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC08BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC08DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC08DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC08DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC08DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC08NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC08PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC08PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC08PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74AHC08PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC08PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC08RGYR	VQFN	RGY	14	3000	360.0	360.0	36.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9682001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74AHC08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC08N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC08FK	FK	LCCC	20	55	506.98	12.06	2030	NA

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

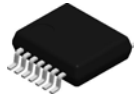
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

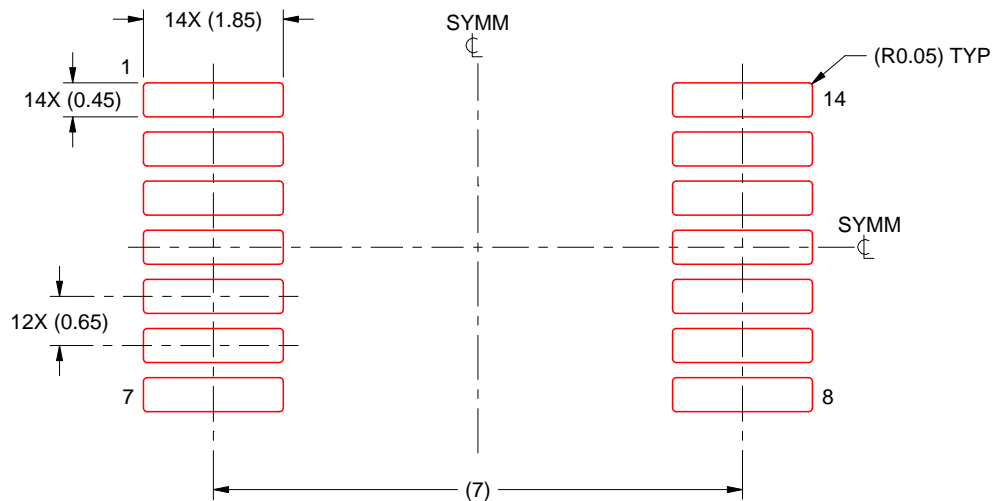
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

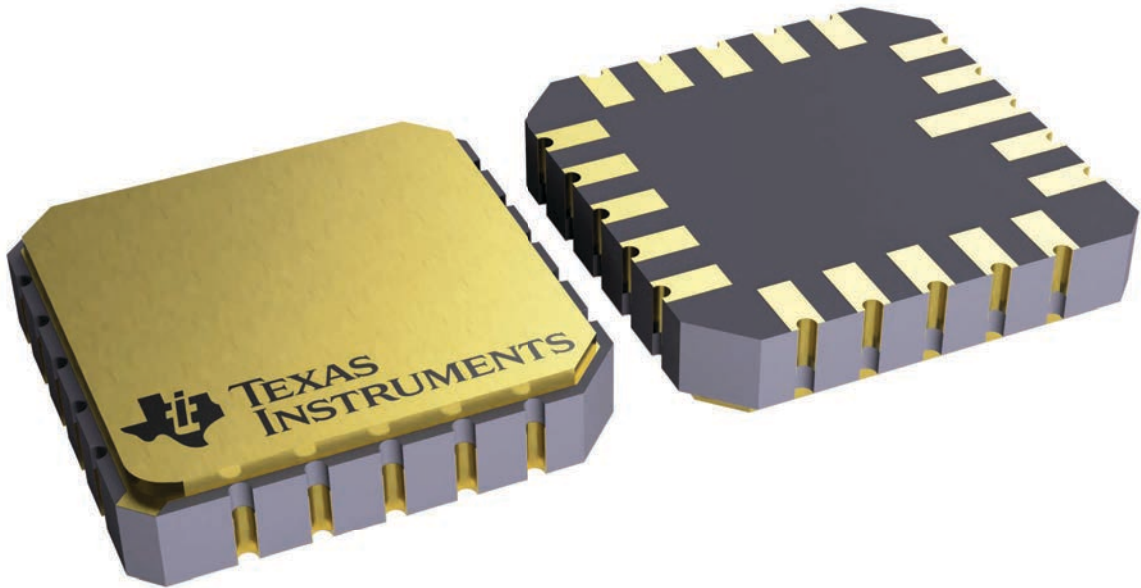
**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

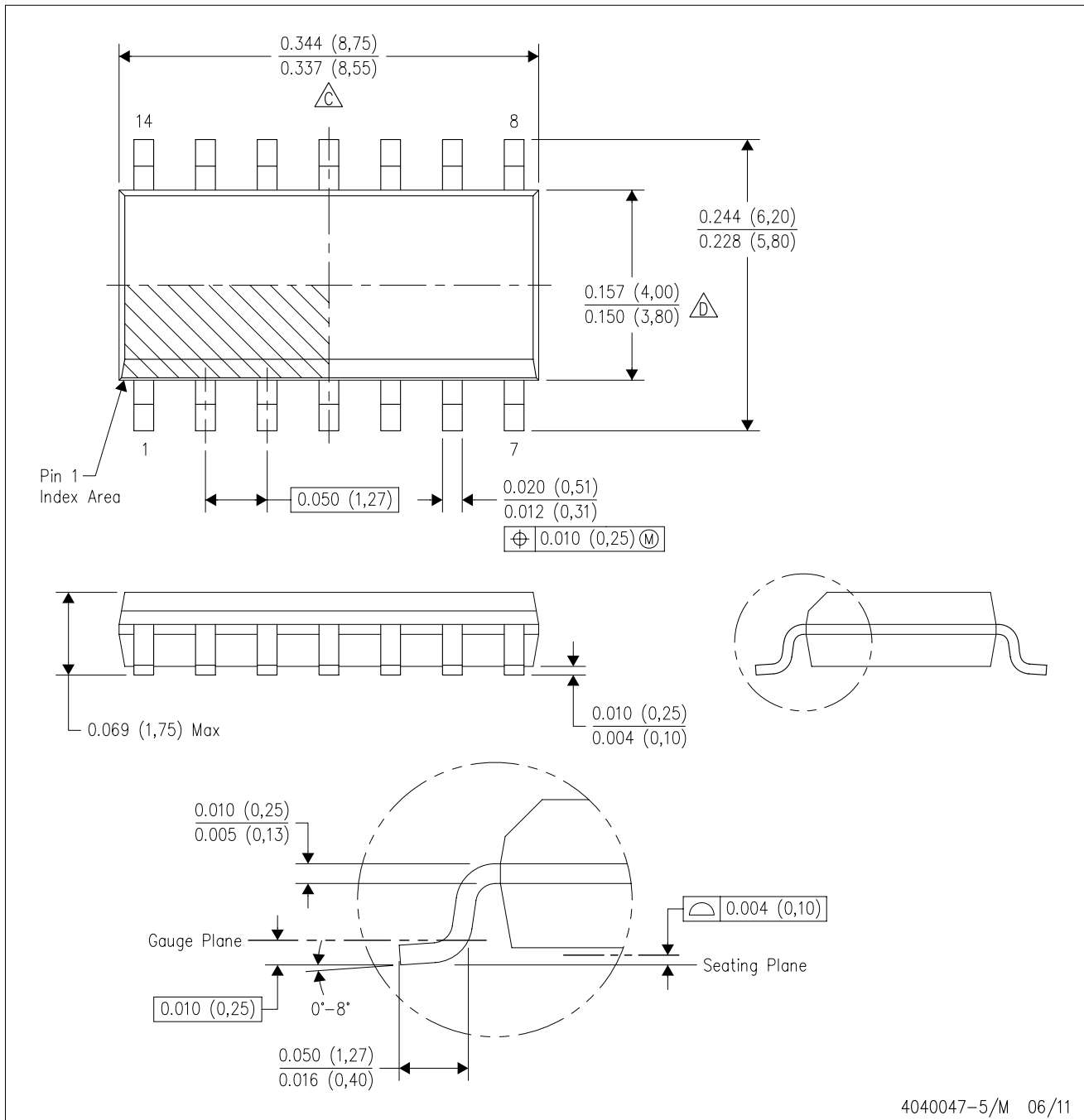
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

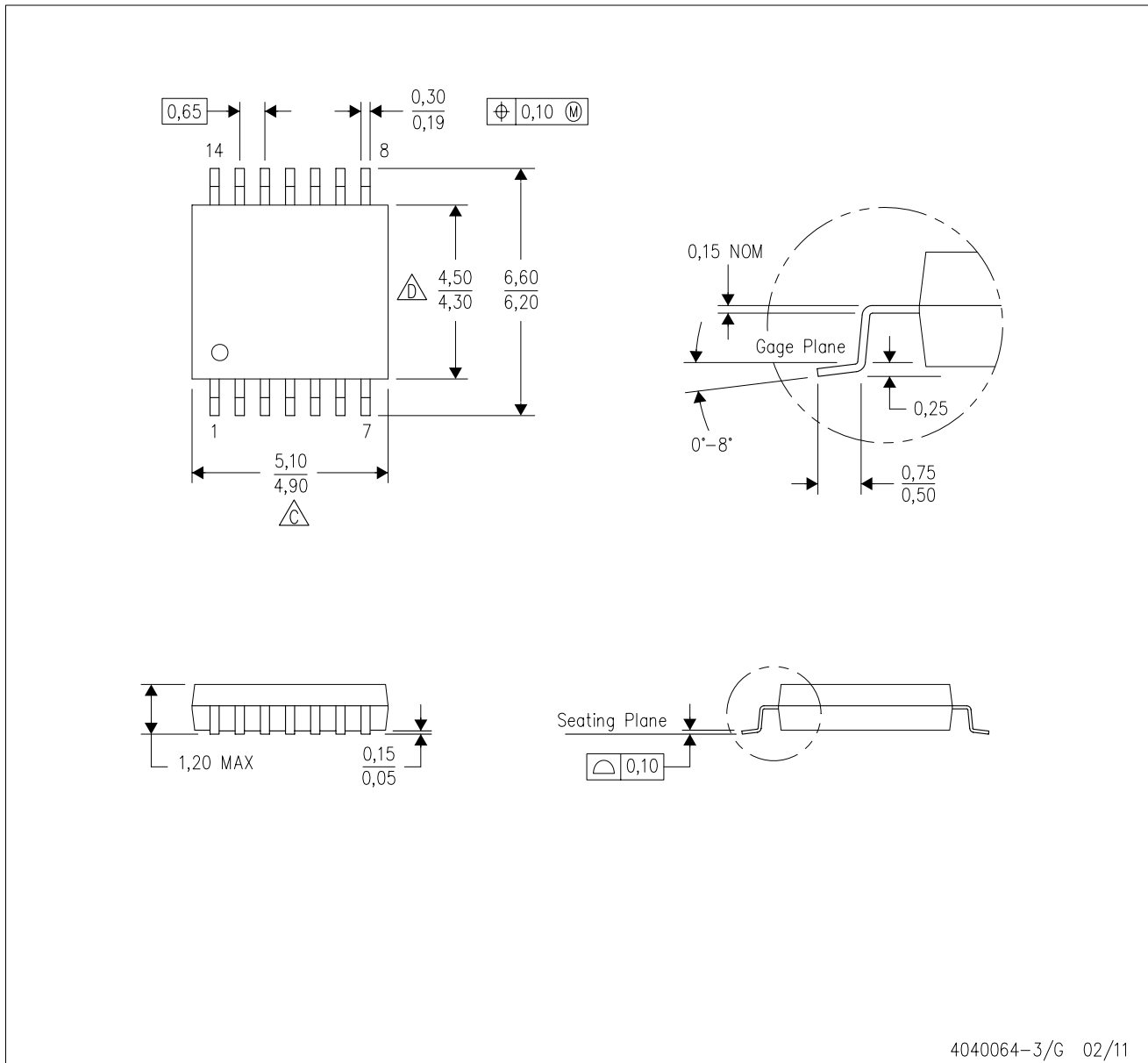


4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - $\triangle F$  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

## GENERIC PACKAGE VIEW

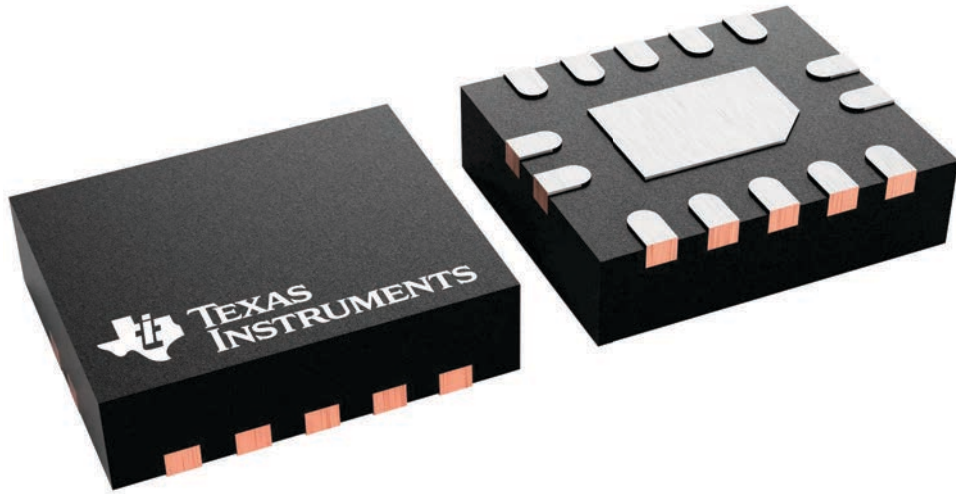
**BQA 14**

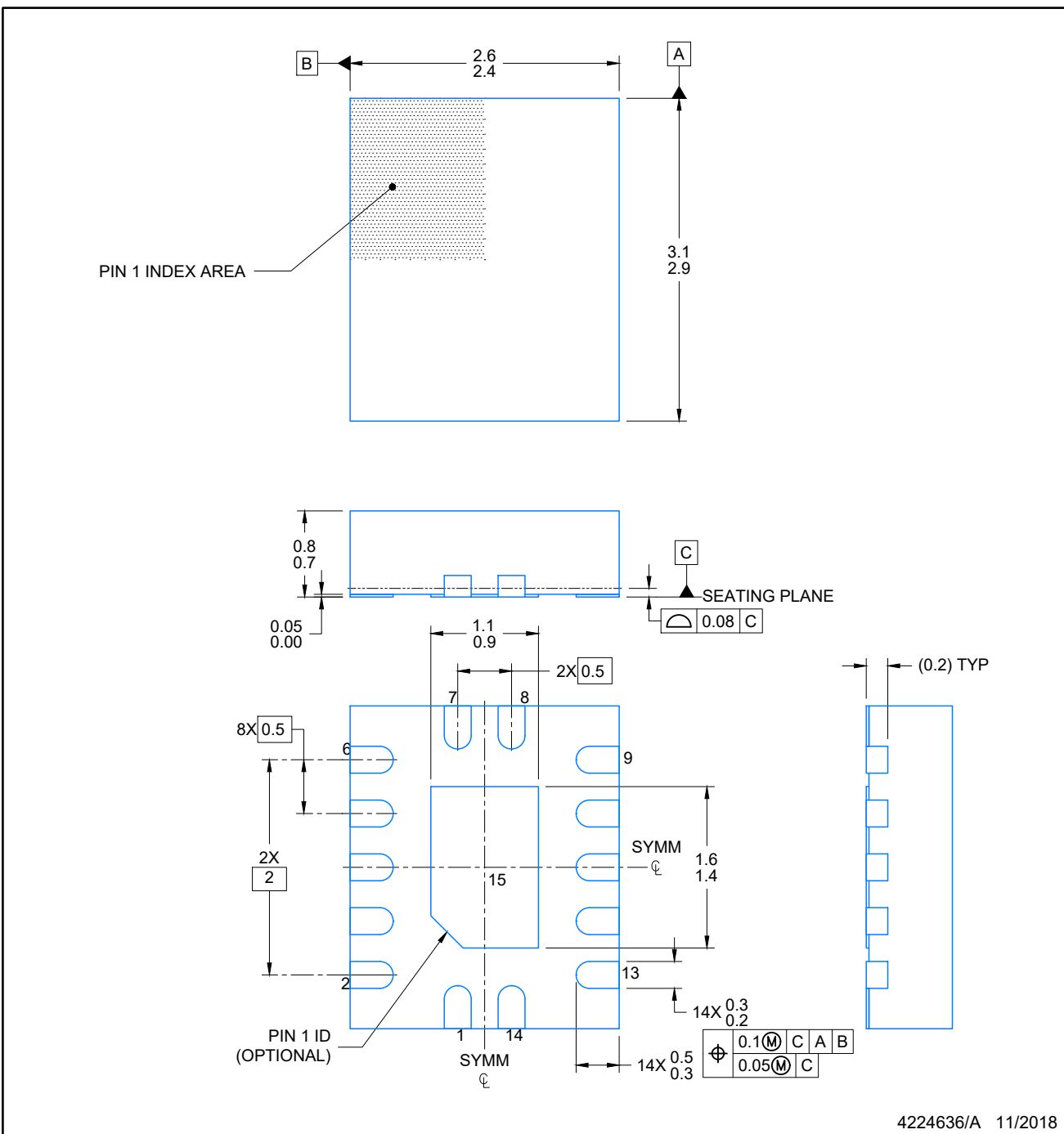
**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





**NOTES:**

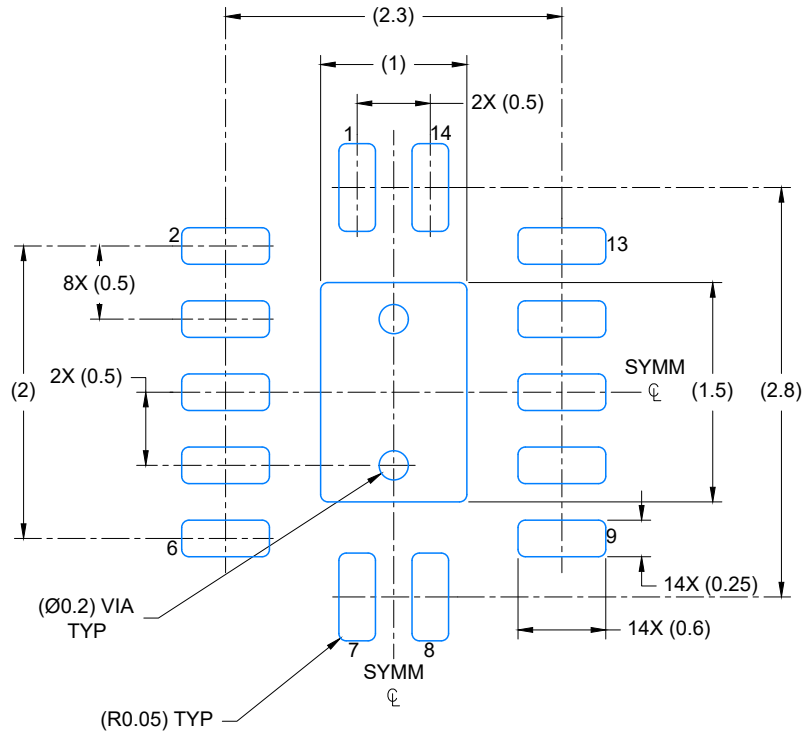
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

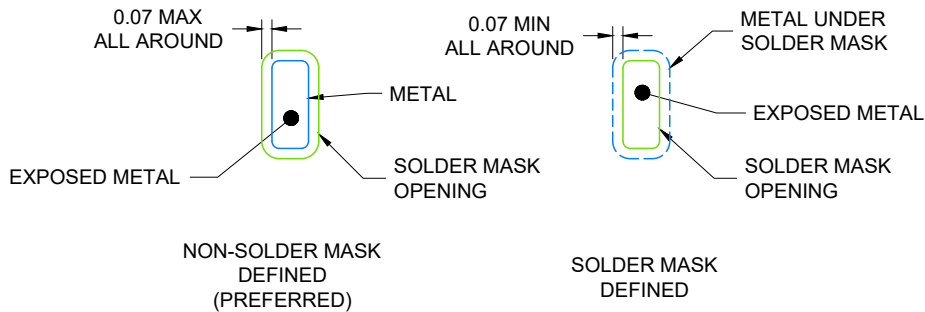
WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

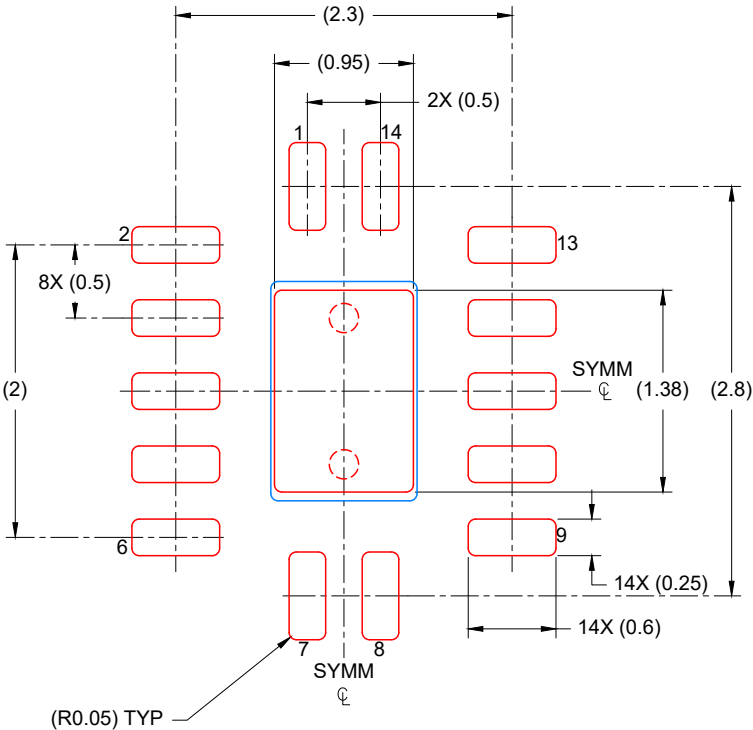
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**EXAMPLE STENCIL DESIGN**

**BQA0014A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 88% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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