

# SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCEIVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

- Three Differential Transceivers in One Package
- Signaling Rates† Up to 30 Mbps
- Low Power and High Speed
- Designed for TIA/EIA-485, TIA/EIA-422, ISO 8482, and ANSI X3.277 (HVD SCSI Fast–20) Applications
- Common-Mode Bus Voltage Range –7 V to 12 V
- ESD Protection on Bus Terminals Exceeds 12 kV
- Driver Output Current up to  $\pm 60$  mA
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Power-Up, Power-Down Glitch-Free Operation
- Pin-Compatible With the SN75ALS170
- Available in Shrink Small-Outline Package

## description

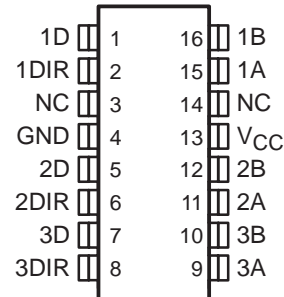
The SN65LBC170 and SN75LBC170 are monolithic integrated circuits designed for bidirectional data communication on multipoint bus-transmission lines. Potential applications include serial or parallel data transmission, cabled peripheral buses with twin axial, ribbon, or twisted-pair cabling. These devices are suitable for FAST-20 SCSI and can transmit or receive data pulses as short as 25 ns, with skew less than 3 ns.

These devices combine three 3-state differential line drivers and three differential input line receivers, all of which operate from a single 5-V power supply.

The driver differential outputs and the receiver differential inputs are connected internally to form three differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or  $V_{CC} = 0$ . These ports feature a wide common-mode voltage range making the device suitable for party-line applications over long cable runs.

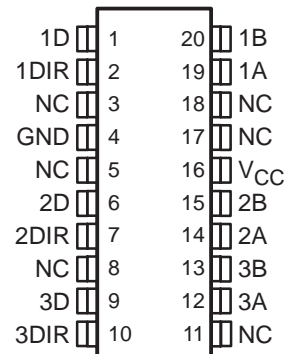
SN65LBC170DB (marked as BL170)  
SN75LBC170DB (marked as BL170)

(TOP VIEW)



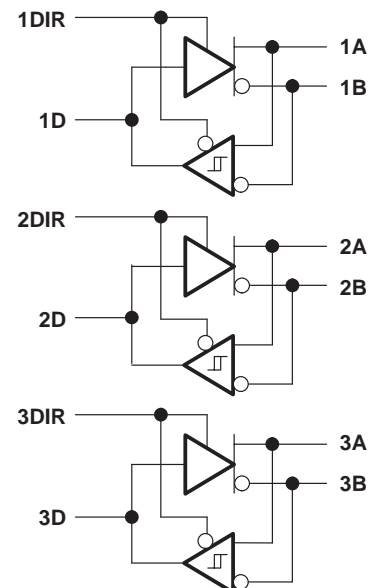
SN65LBC170DW (marked as 65LBC170)  
SN75LBC170DW (marked as 75LBC170)

(TOP VIEW)



NC – No internal connection

## logic diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002, Texas Instruments Incorporated

# SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCEIVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

## description (continued)

The driver's active-high enable and the receiver's active-low enable are tied together internally and provide a direction input for each driver/receiver pair.

The SN75LBC170 is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC170 is characterized for operation over the temperature range of -40°C to 85°C.

### AVAILABLE OPTIONS†

T <sub>A</sub>	PACKAGE	
	PLASTIC SHRINK SMALL-OUTLINE (JEDEC MO-150)	PLASTIC SMALL-OUTLINE (JEDEC MS-013)
0°C to 70°C	SN75LBC170DB	SN75LBC170DW
-40°C to 85°C	SN65LBC170DB	SN65LBC170DW

† Add R suffix for taped and reel

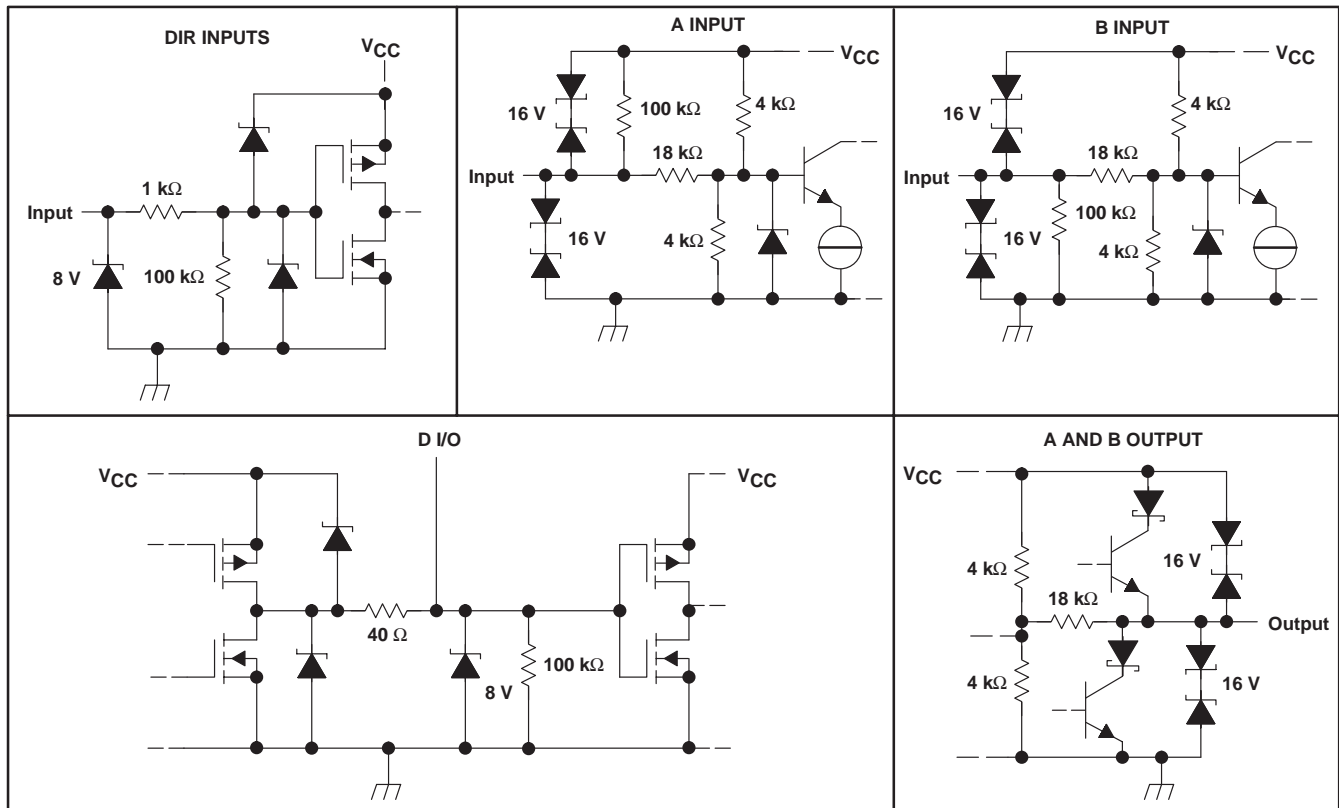
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### Function Tables

EACH DRIVER			EACH RECEIVER			
INPUT D	ENABLE DIR	OUTPUTS		DIFFERENTIAL INPUT (V <sub>A</sub> -V <sub>B</sub> )	ENABLE DIR	OUTPUT D
		A	B			
H	H	H	L	V <sub>ID</sub> ≥ 0.2 V	L	H
L	H	L	H	-0.2 V < V <sub>ID</sub> < 0.2 V	L	?
OPEN	H	L	H	V <sub>ID</sub> ≤ -0.2 V	L	L
X	L	Z	Z	X	H	Z
X	OPEN	X	X	OPEN	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

## equivalent input and output schematic diagrams



# SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCEIVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

## absolute maximum ratings<sup>†</sup> over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	–0.3 V to 6 V
Voltage range at any bus I/O terminal (steady state)	–10 V to 15 V
Voltage input range, A and B, (transient pulse through 100 $\Omega$ , see Figure 12)	–30 V to 30 V
Voltage range at any D or DIR terminal	–0.5 V to $V_{CC} + 0.5$ V
Receiver output current, $I_O$	$\pm 10$ mA
Electrostatic discharge: Human body model (A, B, GND) (see Note 2)	12 kV
All pins	5 kV
Charged-device model (all pins) (see Note 3)	1 kV
Continuous total power dissipation	See Power Dissipation Rating Table

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.  
 2. Tested in accordance with JEDEC Standard 22, Test Method A114–A.  
 3. Tested in accordance with JEDEC Standard 22, Test Method C101.

POWER DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR <sup>‡</sup> ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DB	995 mW	8.0 mW/ $^\circ\text{C}$	635 mW	515 mW
DW	1480 mW	11.8 mW/ $^\circ\text{C}$	950 mW	770 mW

<sup>‡</sup> This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus I/O terminal	A, B	–7		12	V
High-level input voltage, $V_{IH}$	D, DIR	2		$V_{CC}$	V
Low-level input voltage, $V_{IL}$		0		0.8	
Differential input voltage, $V_{ID}$	A with respect to B	–12		12	V
Output current	Driver	–60		60	mA
	Receiver	–8		8	
Operating free-air temperature, $T_A$	SN75LBC170	0		70	$^\circ\text{C}$
	SN65LBC170	–40		85	



# SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCEIVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

## DRIVER SECTION

### electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	D and DIR $I_I = 18 \text{ mA}$	-1.5	-0.7		V
$V_O$	Open-circuit output voltage (single-ended)	A or B, No load	0		$V_{CC}$	V
$ V_{OD(SS)} $	Steady-state differential output voltage magnitude‡	No load	3.8	4.3	$V_{CC}$	V
		$R_L = 54 \Omega$ , See Figure 1	1	1.6	2.4	
		With common-mode loading, See Figure 2	1	1.6	2.4	
$\Delta V_{OD}$	Change in differential output voltage magnitude, $ V_{OD(H)}  -  V_{OD(L)} $	$R_L = 54 \Omega$ , $C_L = 50 \text{ pF}$ See Figure 1	-0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage		2	2.4	2.8	
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage ( $V_{OC(H)} - V_{OC(L)}$ )		-0.2		0.2	
$I_I$	Input current	D, DIR	-100		100	$\mu\text{A}$
$I_O$	Output current with power off	$V_{CC} = 0 \text{ V}$ , $V_O = -7 \text{ V to } 12 \text{ V}$	-700		900	$\mu\text{A}$
$I_{OS}$	Short-circuit output current	$V_O = -7 \text{ V to } 12 \text{ V}$ , See Figure 7	-250		250	mA
$I_{CC}$	Supply current (driver enabled)	D at 0 V or $V_{CC}$ , DIR at $V_{CC}$ , No load		14	20	mA

† All typical values are at  $V_{CC} = 5 \text{ V}$  and  $T_A = 25^\circ\text{C}$ .

‡ The minimum  $V_{OD}$  may not fully comply with TIA/EIA-485-A at operating temperatures below  $0^\circ\text{C}$ . System designers should take the possibly lower output signal into account in determining the maximum signal-transmission distance.

### switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Differential output propagation delay, low-to-high	$R_L = 54 \Omega$ , $C_L = 50 \text{ pF}$ , See Figure 3	4	8.5	12	ns
$t_{PHL}$	Differential output propagation delay, high-to-low		4	8.5	11	
$t_r$	Differential output rise time		3	7.5	11	
$t_f$	Differential output fall time		3	7.5	11	
$t_{sk(p)}$	Pulse skew $ t_{PLH} - t_{PHL} $				2	
$t_{sk(o)}$	Output skew§				1.5	
$t_{sk(pp)}$	Part-to-part skew¶				2	
$t_{PLH}$	Differential output propagation delay, low-to-high	See Figure 4, (HVD SCSI double-terminated load)	3	7	10	ns
$t_{PHL}$	Differential output propagation delay, high-to-low		3	7.5	10	
$t_r$	Differential output rise time		3	7.5	12	
$t_f$	Differential output fall time		3	7.5	12	
$t_{sk(p)}$	Pulse skew $ t_{PLH} - t_{PHL} $				3	
$t_{sk(o)}$	Output skew§				1.5	
$t_{sk(pp)}$	Part-to-part skew¶				2.5	
$t_{pZH}$	Output enable time to high level	See Figure 5		15	25	ns
$t_{pHZ}$	Output disable time from high level			18	25	
$t_{pZL}$	Output enable time to low level	See Figure 6		10	25	ns
$t_{pLZ}$	Output disable time from low level			17	25	

§ Output skew ( $t_{sk(o)}$ ) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

¶ Part-to-part skew ( $t_{sk(pp)}$ ) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.



## RECEIVER SECTION

### electrical characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IT+}$	Positive-going differential input voltage threshold	See Figure 8			0.2	V
$V_{IT-}$	Negative-going differential input voltage threshold				-0.2	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )				40	mV
$V_{OH}$	High-level output voltage	$V_{ID} = 200$ mV, $I_{OH} = -8$ mA, See Figure 8	4	4.7	$V_{CC}$	V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200$ mV, $I_{OL} = -8$ mA, See Figure 8	0	0.2	0.4	
$I_I$	Line input current	Other input = 0 V			0.9	mA
					-0.7	
$R_I$	Input resistance	A, B	12			k $\Omega$
$I_{CC}$	Supply current (receiver enabled)	A, B, D, and DIR open			16	mA

† All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

### switching characteristics over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high level output	See Figure 9	7		16	ns
$t_{PHL}$	Propagation delay time, high-to-low level output		7		16	
$t_r$	Receiver output rise time			1.3	3	ns
$t_f$	Receiver output fall time			1.3	3	
$t_{PZH}$	Receiver output enable time to high level	See Figure 10		26	40	ns
$t_{PHZ}$	Receiver output disable time from high level				40	
$t_{PZL}$	Receiver output enable time to low level	See Figure 11		29	40	ns
$t_{PLZ}$	Receiver output enable time to high level				40	
$t_{sk(p)}$	Pulse skew ( $ t_{PLH} - t_{PHL} $ )				2	ns
$t_{sk(o)}$	Output skew‡				1.5	ns
$t_{sk(pp)}$	Part-to-part skew§				3	ns

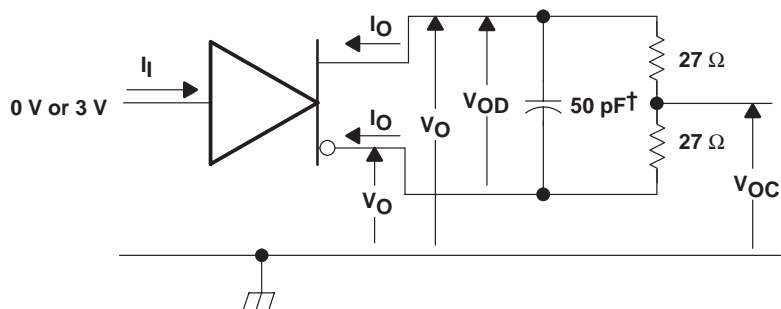
‡ Output skew ( $t_{sk(o)}$ ) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.

§ Part-to-part skew ( $t_{sk(pp)}$ ) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

# SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCIEVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

## PARAMETER MEASUREMENT INFORMATION



† Includes probe and jig capacitance

Figure 1. Driver Test Circuit,  $V_{OD}$  and  $V_{OC}$  Without Common-Mode Loading

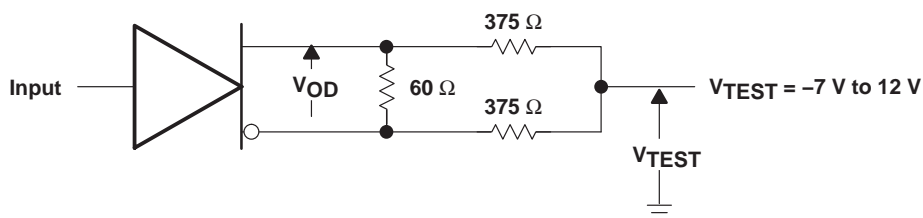
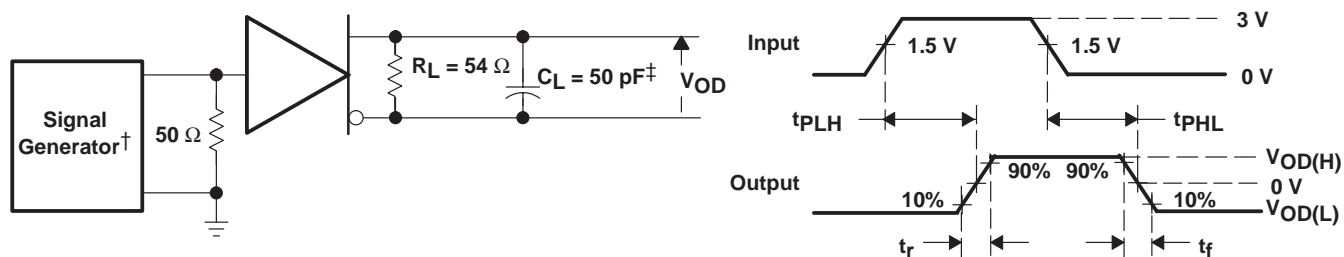


Figure 2. Driver Test Circuit,  $V_{OD}$  With Common-Mode Loading

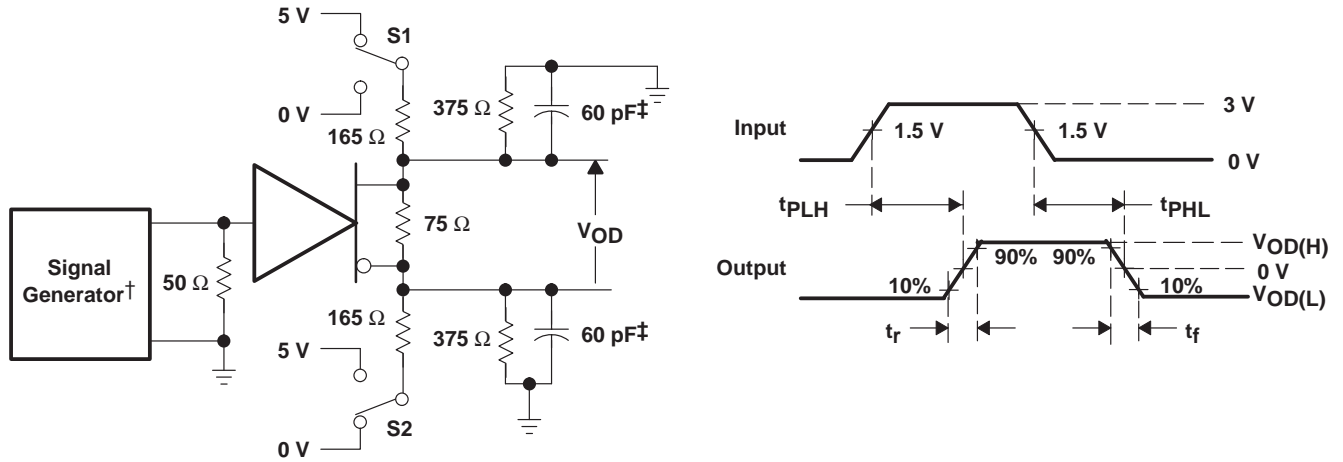


† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_0 = 50 \Omega$

‡ Includes probe and jig capacitance

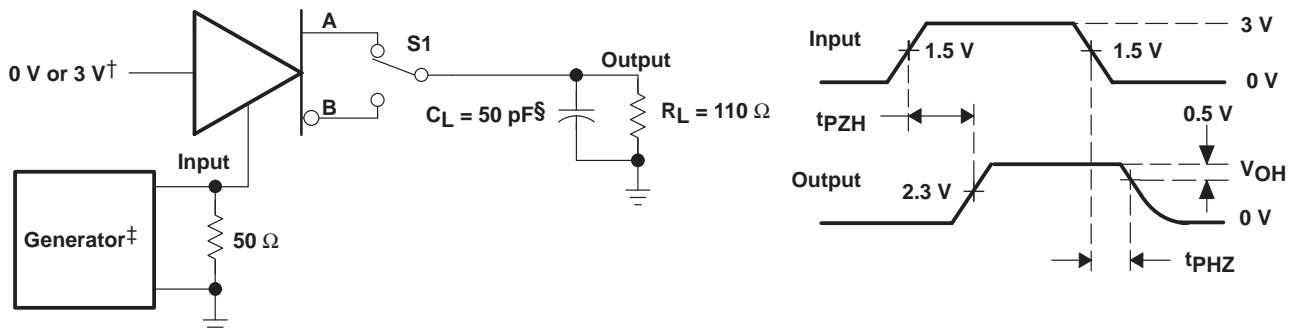
Figure 3. Driver Switching Test Circuit and Waveforms, 485-Loading

## PARAMETER MEASUREMENT INFORMATION



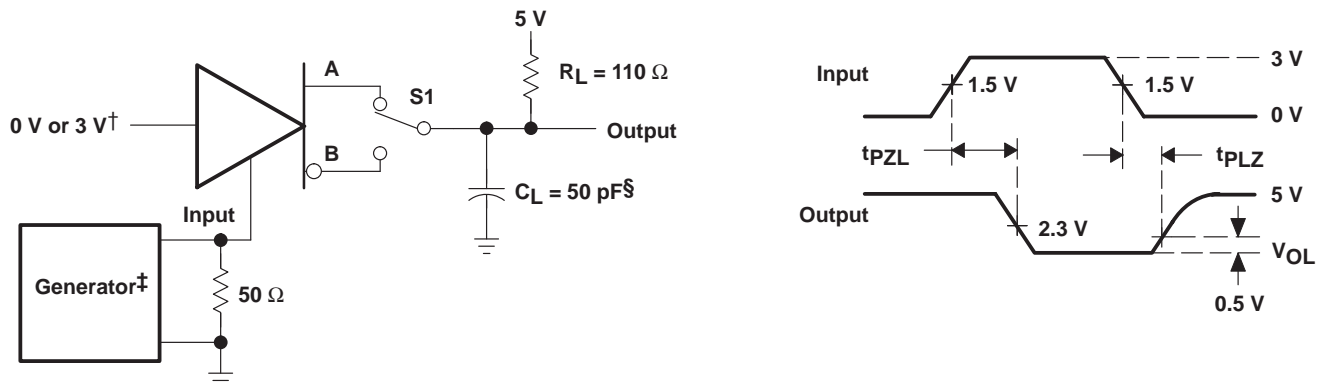
† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_0 = 50 \Omega$   
‡ Includes probe and jig capacitance

Figure 4. Driver Switching Test Circuit and Waveforms, HVD SCSI-Loading (double terminated)



† 3 V if testing A output, 0 V if testing B output  
‡ PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_0 = 50 \Omega$   
§ Includes probe and jig capacitance

Figure 5. Driver Enable/Disable Test, High Output



† 0 V if testing A output, 3 V if testing B output  
‡ PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_0 = 50 \Omega$   
§ Includes probe and jig capacitance

Figure 6. Driver Enable/Disable Test, Low Output

# SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCIEVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

## PARAMETER MEASUREMENT INFORMATION

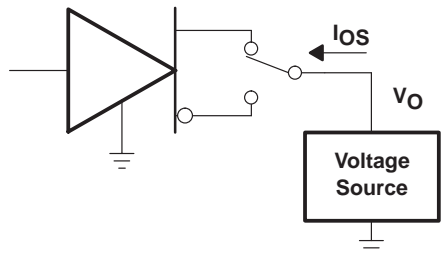


Figure 7. Driver Short-Circuit Test

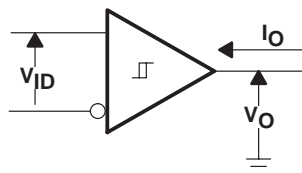
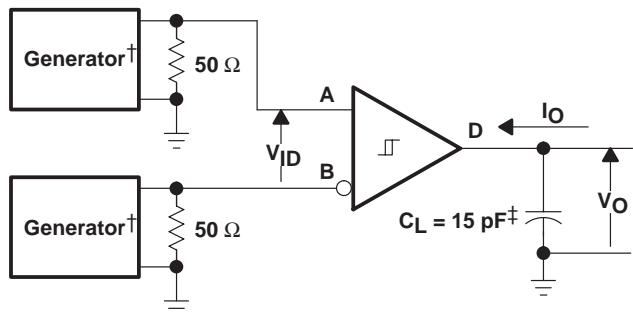
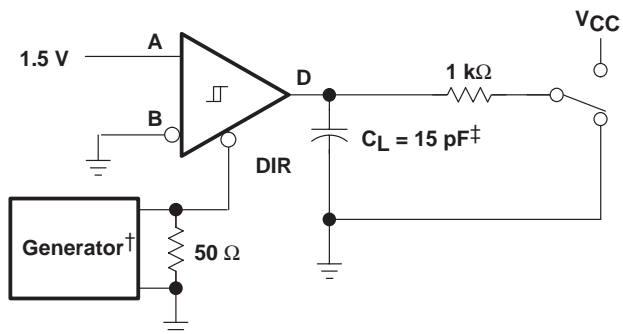


Figure 8. Receiver DC Parameters



† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_0 = 50 \Omega$   
‡ Includes probe and jig capacitance

Figure 9. Receiver Switching Test Circuit and Waveforms

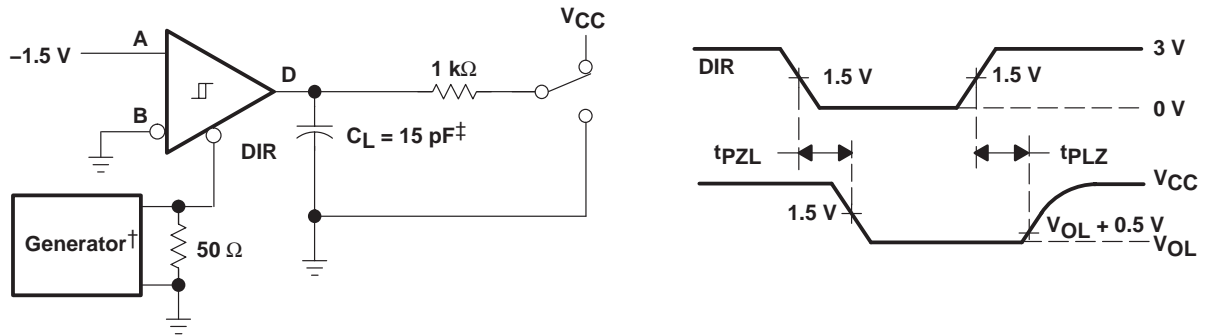


† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_0 = 50 \Omega$   
‡ Includes probe and jig capacitance

Figure 10. Receiver Enable/Disable Test, High Output



## PARAMETER MEASUREMENT INFORMATION



† PRR = 1 MHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_0 = 50 \Omega$   
 ‡ Includes probe and jig capacitance

Figure 11. Receiver Enable/Disable Test, Low Output

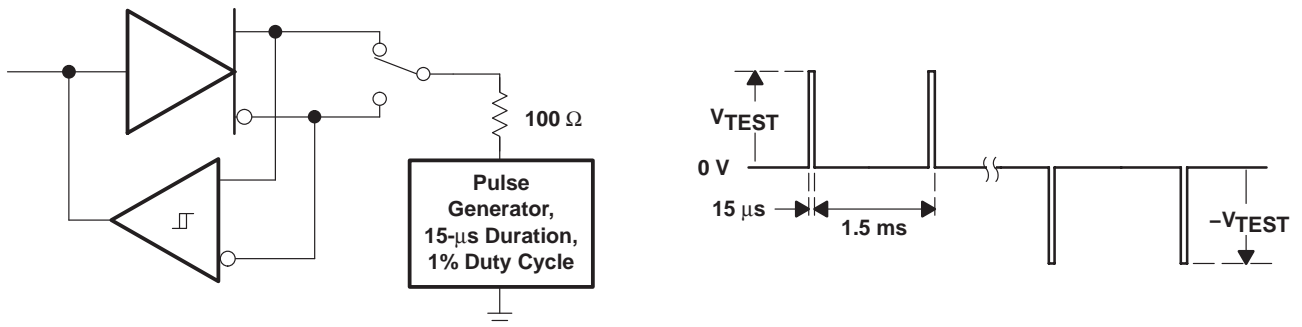


Figure 12. Test Circuit and Waveform, Transient Over Voltage Test

# SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCEIVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

## TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE  
vs  
OUTPUT CURRENT

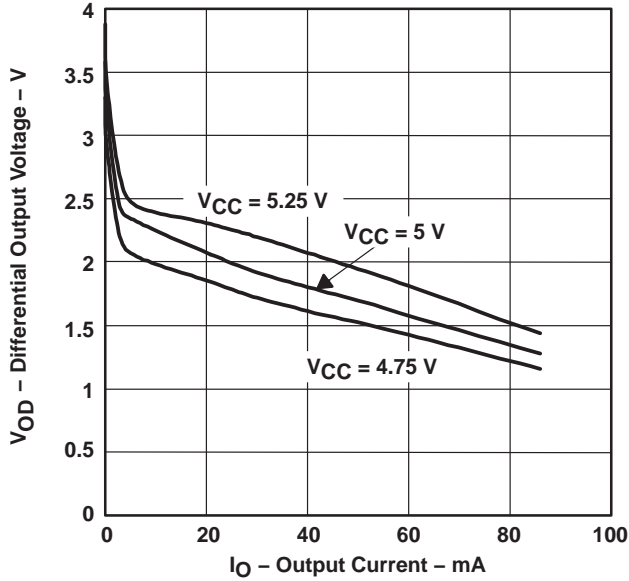


Figure 13

DIFFERENTIAL OUTPUT VOLTAGE  
vs  
FREE-AIR TEMPERATURE

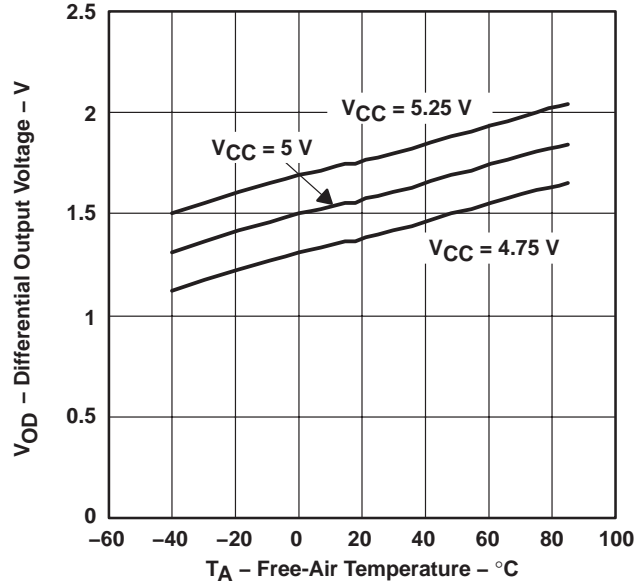


Figure 14

DRIVER PROPAGATION DELAY  
vs  
FREE-AIR TEMPERATURE

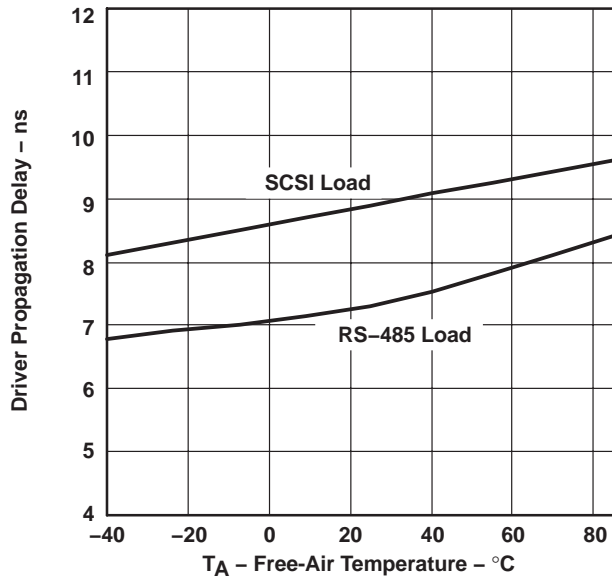


Figure 15

SUPPLY CURRENT  
vs  
SIGNALING RATE

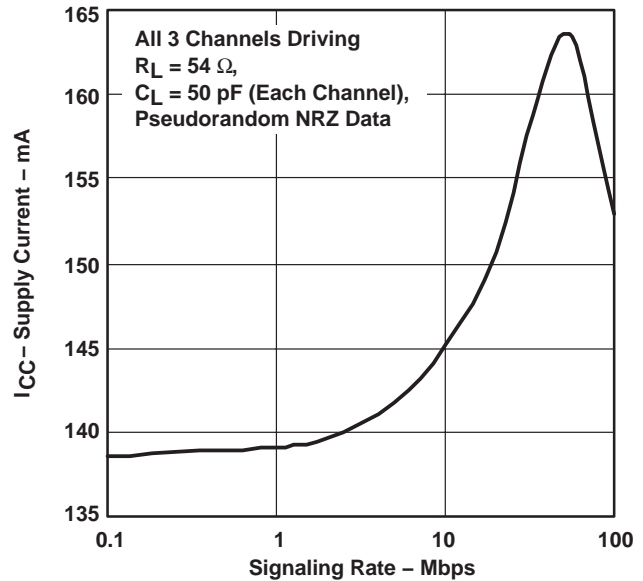


Figure 16



TYPICAL CHARACTERISTICS

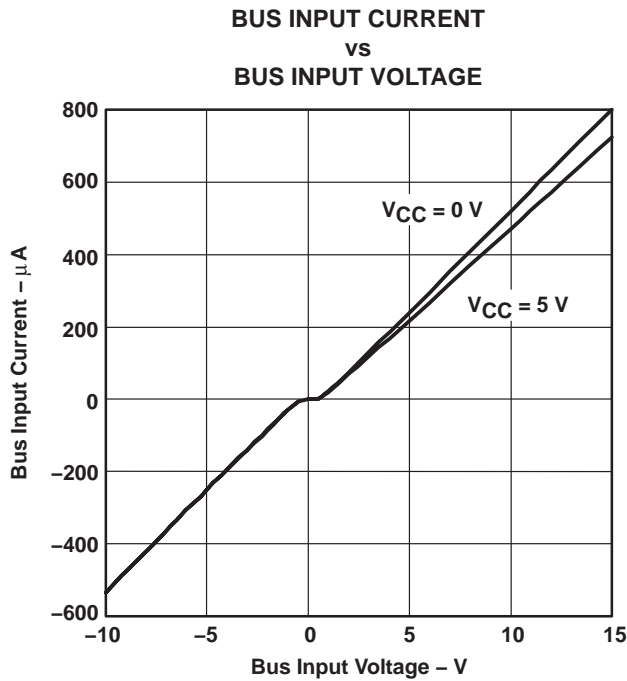


Figure 17

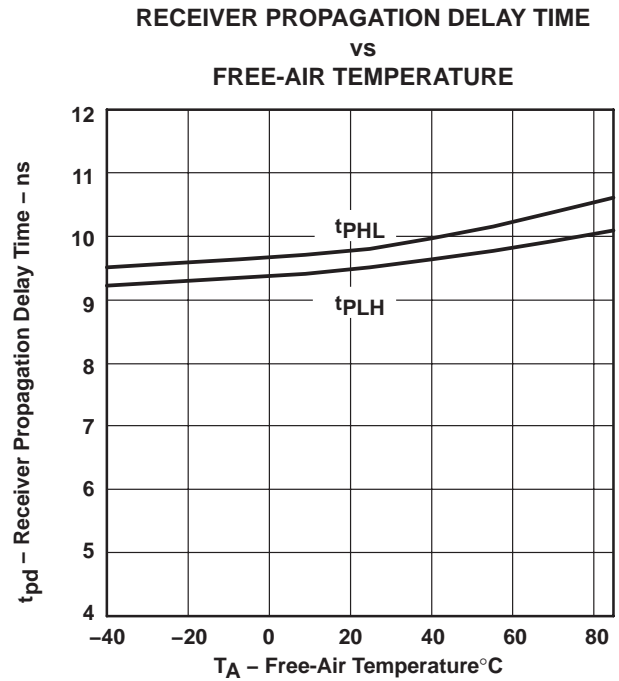


Figure 18

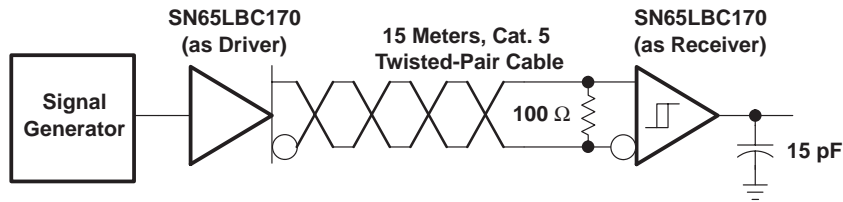


Figure 19. Circuit Diagram for Signaling Characteristics

# SN65LBC170, SN75LBC170 TRIPLE DIFFERENTIAL TRANSCEIVERS

SLLS459C – NOVEMBER 2000 – REVISED MARCH 2005

## TYPICAL CHARACTERISTICS

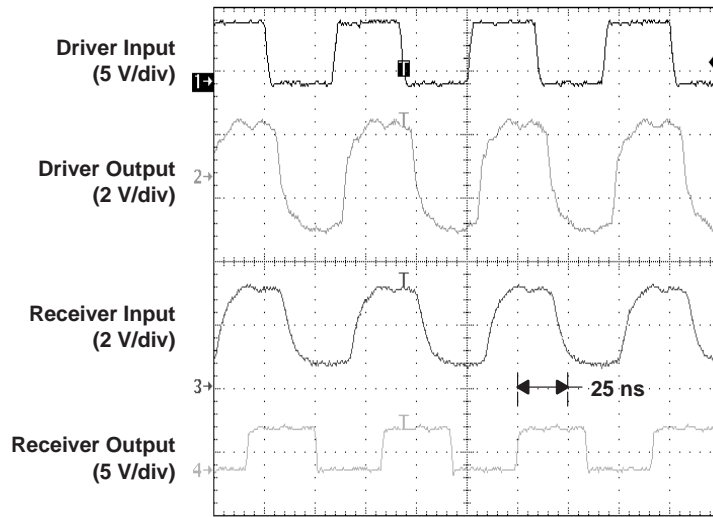


Figure 20. Signal Waveforms at 30 Mbps

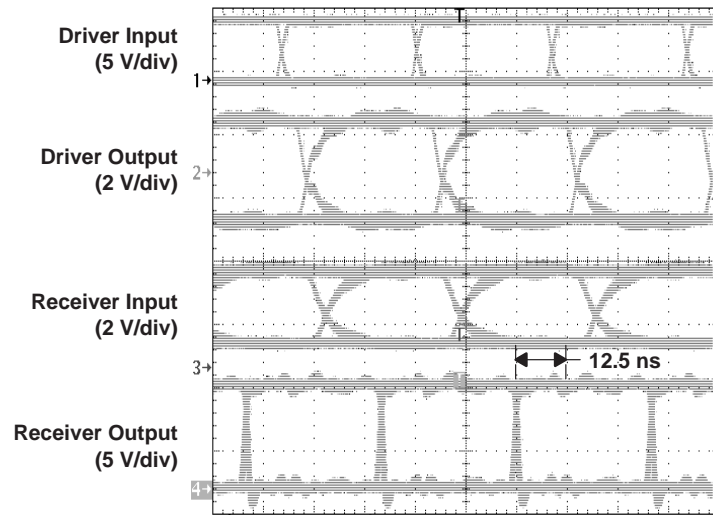


Figure 21. Eye Patterns, Pseudorandom Data at 30 Mbps

TYPICAL CHARACTERISTICS

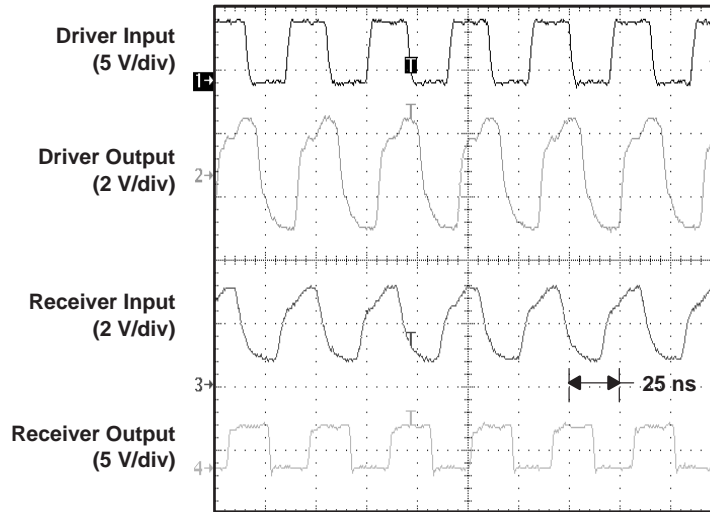


Figure 22. Signal Waveforms at 50 Mbps

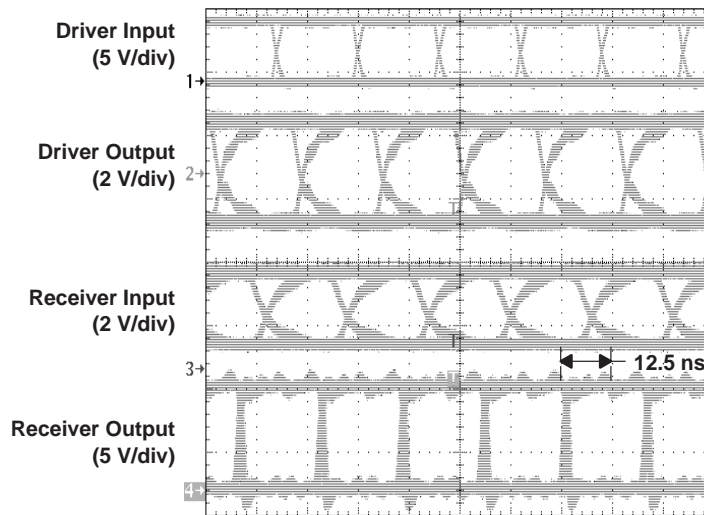


Figure 23. Eye Patterns, Pseudorandom Data at 50 Mbps

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC170DB	ACTIVE	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BL170	<a href="#">Samples</a>
SN65LBC170DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC170	<a href="#">Samples</a>
SN75LBC170DB	ACTIVE	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB170	<a href="#">Samples</a>
SN75LBC170DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LB170	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC170DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.5	12.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC170DBR	SSOP	DB	16	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65LBC170DB	DB	SSOP	16	80	530	10.5	4000	4.1
SN65LBC170DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC170DB	DB	SSOP	16	80	530	10.5	4000	4.1

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

**NOTES:**

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated