

SNx4AHC126 Quadruple Bus Buffer Gates with 3-State Outputs

1 Features

- Operating range 2V to 5.5V V_{CC}
- Low delay, 3.8 ns (typical with 5-V supply)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- [Drive indicator LEDs](#)
- [Drive transmission lines with logic](#)
- [Enable or disable a digital signal](#)

3 Description

The SNx4AHC126 devices are quadruple bus buffer gates featuring independent line drivers with 3-state outputs.

For the high-impedance state during power up or power down, OE can be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the drive.

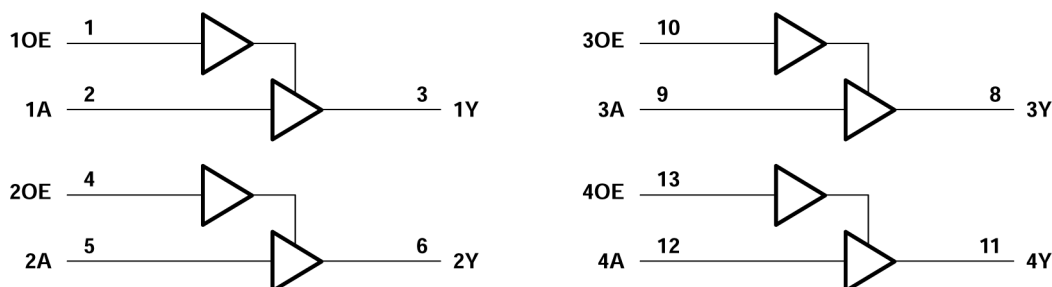
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SNx4AHC126	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	PW (TSSOP, 14)	5mm × 6.4mm	5mm × 4.4mm

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



Table of Contents

1 Features	1	7 Detailed Description	11
2 Applications	1	7.1 Overview.....	11
3 Description	1	7.2 Functional Block Diagram.....	11
4 Pin Configuration and Functions	3	7.3 Feature Description.....	11
5 Specifications	4	7.4 Device Functional Modes.....	12
5.1 Absolute Maximum Ratings.....	4	8 Device and Documentation Support	13
5.2 ESD Ratings.....	4	8.1 Documentation Support.....	13
5.3 Recommended Operating Conditions.....	5	8.2 Receiving Notification of Documentation Updates... 13	
5.4 Thermal Information.....	5	8.3 Support Resources.....	13
5.5 Electrical Characteristics.....	6	8.4 Trademarks.....	13
5.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	8.5 Electrostatic Discharge Caution.....	13
5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	7	8.6 Glossary.....	13
5.8 Noise Characteristics.....	7	9 Revision History	13
5.9 Operating Characteristics.....	7	10 Mechanical, Packaging, and Orderable	
5.10 Typical Characteristics.....	8	Information	13
6 Parameter Measurement Information	10		

4 Pin Configuration and Functions

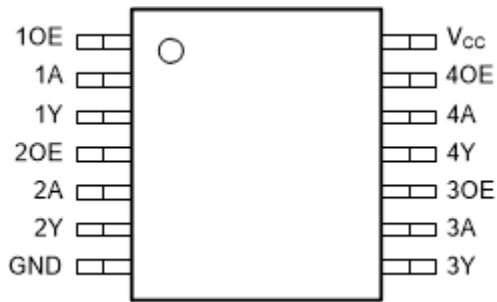


Figure 4-1. PW Package, 14-Pin (Top View)

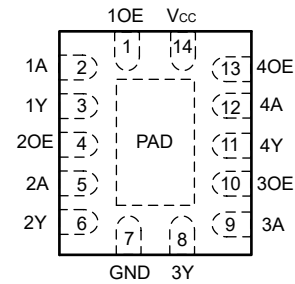


Figure 4-2. BQA Package, WQFN 14-Pin (Transparent Top View)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
10E	1	I	Channel 1, output enable
1A	2	I	Channel 1, A input
1Y	3	O	Channel 1, Y output
2OE	4	I	Channel 2, output enable
2A	5	I	Channel 2, A input
2Y	6	O	Channel 2, Y output
GND	7	G	Ground
3Y	8	O	Channel 3, Y output
3A	9	I	Channel 3, A input
3OE	10	I	Channel 3, OE input
4Y	11	O	Channel 4, Y output
4A	12	I	Channel 4, A input
4OE	13	I	Channel 4, OE input
V _{CC}	14	P	Positive supply
Thermal Pad ⁽²⁾		—	Thermal pad; connect to GND or leave floating

(1) I = input, O = output, P = power, G = ground

(2) BQA package only

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.5	7	V
V_I ⁽²⁾	Input voltage range	-0.5	7	V
V_O ⁽²⁾	Output voltage range	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	($V_I < 0$)	-20	mA
I_{OK}	Output clamp current	($V_O < 0$ or $V_O > V_{CC}$)	±20	mA
I_O	Continuous output current	($V_O = 0$ to V_{CC})	±25	mA
	Continuous current through V_{CC} or GND		±50	mA
T_{stg}	Storage temperature range	-65	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	2	5.5	V	
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V	
		V _{CC} = 3 V	2.1		
		V _{CC} = 5.5 V	3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V	
		V _{CC} = 3 V	0.9		
		V _{CC} = 5.5 V	1.65		
V _I ⁽¹⁾	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH} ⁽²⁾	High-level output current	V _{CC} = 2 V	-50	μA	
		V _{CC} = 3.3 V ± 0.3 V	-4	mA	
		V _{CC} = 5 V ± 0.5 V	-8		
I _{OL} ⁽²⁾	Low-level output current	V _{CC} = 2 V	50	μA	
		V _{CC} = 3.3 V ± 0.3 V	4	mA	
		V _{CC} = 5 V ± 0.5 V	8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	ns/V	
		V _{CC} = 5 V ± 0.5 V	20		
T _A	Operating free-air temperature	SN74AHC126	-40	85	°C
		SN54AHC126	-55	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) Recommended current values provided to maintain appropriate output state as per the relevant output voltage specification (V_{OL} for I_{OL}, V_{OH} for I_{OH}). See *Electrical Characteristics* table for details.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74AHC126						UNIT
	D	DB	DGV	N	NS	PW	
	14 PINS						
R _{θJA}	Junction-to-ambient thermal resistance	124.6				147.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	79.7				77.4	
R _{θJB}	Junction-to-board thermal resistance	81.2				90.9	
ψ _{JT}	Junction-to-top characterization parameter	39.3				27.2	
ψ _{JB}	Junction-to-board characterization parameter	80.8				90.2	
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25 °C			–40 to +85 °C		–55 to +125 °C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = –4 mA	3 V	2.58		2.48		2.48			
	I _{OH} = –8 mA	4.5 V	3.94		3.8		3.8			
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	0.1	V	
		3 V			0.1		0.1	0.1		
		4.5 V			0.1		0.1	0.1		
	I _{OL} = 4 mA	3 V			0.36		0.44	0.5		
	I _{OL} = 8 mA	4.5 V			0.36		0.44	0.5		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	±1 ⁽¹⁾	μA	
I _{OZ}	V _I = V _{CC} or GND	5.5 V			±0.25			±2.5	μA	
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4			40	μA	
C _i	V _I = V _{CC} or GND	5 V		4	10		10		pF	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Section 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25 °C			–40 to +85 °C		–55 to +125 °C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF	5.6 ⁽¹⁾	8 ⁽¹⁾		1	9.5	1 ⁽¹⁾	9.5 ⁽¹⁾	ns
t _{PHL}				5.6 ⁽¹⁾	8 ⁽¹⁾		1	9.5	1 ⁽¹⁾	9.5 ⁽¹⁾	
t _{PZH}	OE	Y	C _L = 15 pF	5.4 ⁽¹⁾	8 ⁽¹⁾		1	9.5	1 ⁽¹⁾	9.5 ⁽¹⁾	ns
t _{PZL}				5.4 ⁽¹⁾	8 ⁽¹⁾		1	9.5	1 ⁽¹⁾	9.5 ⁽¹⁾	
t _{PHZ}	OE	Y	C _L = 15 pF	7 ⁽¹⁾	9.7 ⁽¹⁾		1	11.5	1 ⁽¹⁾	11.5 ⁽¹⁾	ns
t _{PLZ}				7 ⁽¹⁾	9.7 ⁽¹⁾		1	11.5	1 ⁽¹⁾	11.5 ⁽¹⁾	
t _{PLH}	A	Y	C _L = 50 pF	8.1	11.5		1	13	1	13	ns
t _{PHL}				8.1	11.5		1	13	1	13	
t _{PZH}	OE	Y	C _L = 50 pF	7.9	11.5		1	13	1	13	ns
t _{PZL}				7.9	11.5		1	13	1	13	
t _{PHZ}	OE	Y	C _L = 50 pF	9.5	13.2		1	15	1	15	ns
t _{PLZ}				9.5	13.2		1	15	1	15	
t _{sk(o)}			C _L = 50 pF		1.5 ⁽²⁾			1.5		ns	

(1) (2)

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Section 6](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$-40\text{ to }+85^\circ\text{C}$		$-55\text{ to }+125^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.8 ⁽¹⁾	5.5 ⁽¹⁾	1	6.5	1 ⁽¹⁾	6.5 ⁽¹⁾	ns	
t_{PHL}				3.8 ⁽¹⁾	5.5 ⁽¹⁾	1	6.5	1 ⁽¹⁾	6.5 ⁽¹⁾		
t_{PZH}	OE	Y	$C_L = 15\text{ pF}$	3.6 ⁽¹⁾	5.1 ⁽¹⁾	1	6	1 ⁽¹⁾	6 ⁽¹⁾	ns	
t_{PZL}				3.6 ⁽¹⁾	5.1 ⁽¹⁾	1	6	1 ⁽¹⁾	6 ⁽¹⁾		
t_{PHZ}	OE	Y	$C_L = 15\text{ pF}$	4.6 ⁽¹⁾	6.8 ⁽¹⁾	1	8	1 ⁽¹⁾	8 ⁽¹⁾	ns	
t_{PLZ}				4.6 ⁽¹⁾	6.8 ⁽¹⁾	1	8	1 ⁽¹⁾	8 ⁽¹⁾		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.3	7.5	1	8.5	1	8.5	ns	
t_{PHL}				5.3	7.5	1	8.5	1	8.5		
t_{PZH}	OE	Y	$C_L = 50\text{ pF}$	5.1	7.1	1	8	1	8	ns	
t_{PZL}				5.1	7.1	1	8	1	8		
t_{PHZ}	OE	Y	$C_L = 50\text{ pF}$	6.1	8.8	1	10	1	10	ns	
t_{PLZ}				6.1	8.8	1	10	1	10		
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1 ⁽²⁾		1			ns	

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER	MIN	TYP	MAX	UNIT
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		0.2	0.8	V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}	-0.9	-0.2		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}	4.4	4.7		V
$V_{IH(D)}$ High-level dynamic input voltage	3.5			V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

- (1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF

5.10 Typical Characteristics

T_A = 25°C (unless otherwise noted)

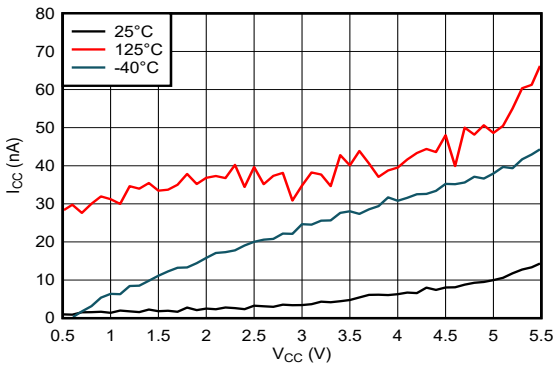


Figure 5-1. Supply Current Across Supply Voltage

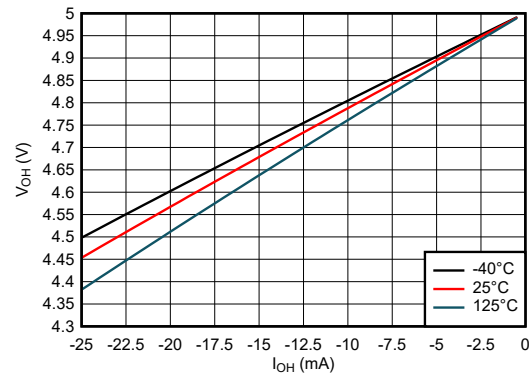


Figure 5-2. Output Voltage vs Current in HIGH State; 5-V Supply

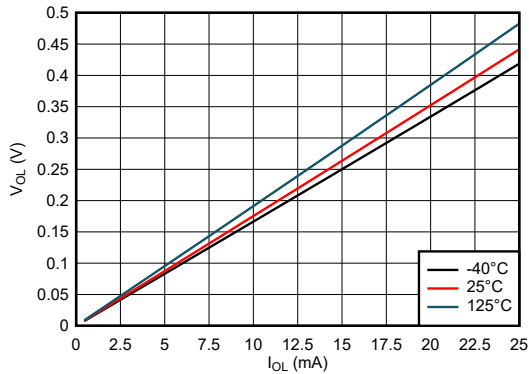


Figure 5-3. Output Voltage vs Current in LOW State; 5-V Supply

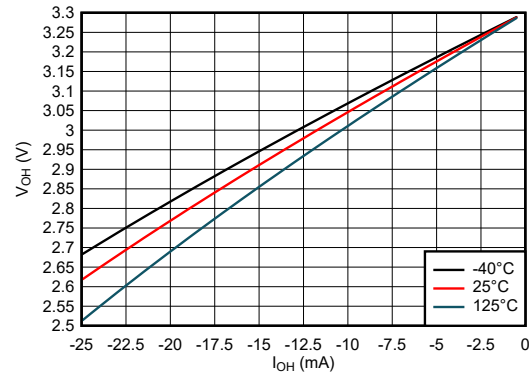


Figure 5-4. Output Voltage vs Current in HIGH State; 3.3-V Supply

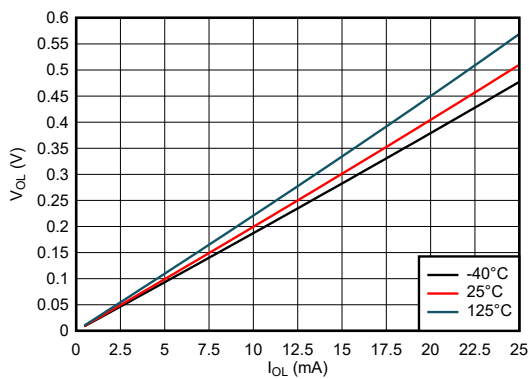


Figure 5-5. Output Voltage vs Current in LOW State; 3.3-V Supply

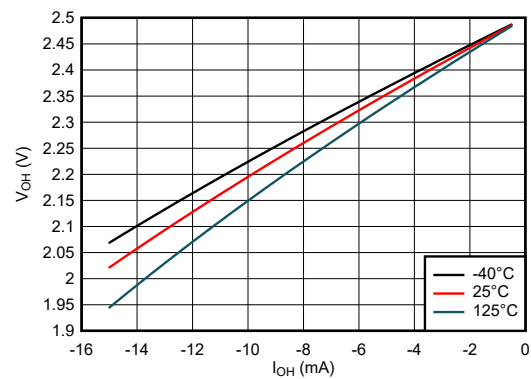


Figure 5-6. Output Voltage vs Current in HIGH State; 2.5-V Supply

5.10 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

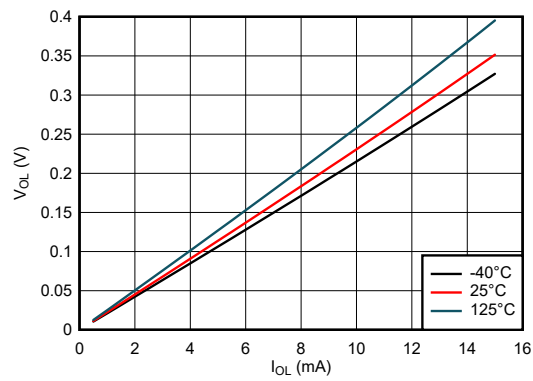


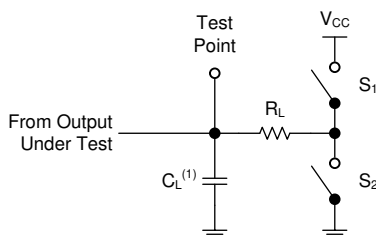
Figure 5-7. Output Voltage vs Current in LOW State; 2.5-V Supply

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t < 2.5 ns.

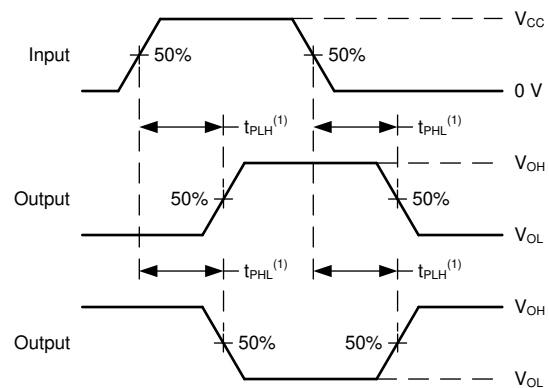
The outputs are measured individually with one input transition per measurement.

TEST	S1	S2	R _L	C _L	ΔV	V _{CC}
t _{PLH} , t _{PHL}	OPEN	OPEN	—	15pF, 50pF	—	ALL
t _{PLZ} , t _{PZL}	CLOSED	OPEN	1 kΩ	15pF, 50pF	0.15V	≤ 2.5V
t _{PHZ} , t _{PZH}	OPEN	CLOSED	1 kΩ	15pF, 50pF	0.15V	≤ 2.5V
t _{PLZ} , t _{PZL}	CLOSED	OPEN	1 kΩ	15pF, 50pF	0.3V	> 2.5V
t _{PHZ} , t _{PZH}	OPEN	CLOSED	1 kΩ	15pF, 50pF	0.3V	> 2.5V



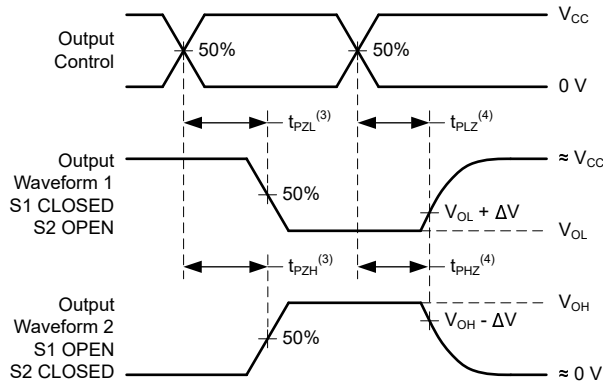
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

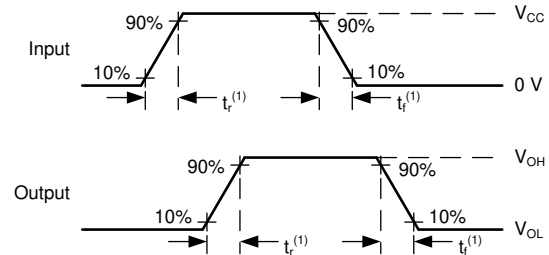
Figure 6-2. Voltage Waveforms Propagation Delays



(3) The greater between t_{PZL} and t_{PZH} is the same as t_{en}.

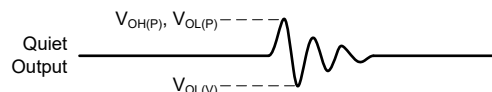
(4) The greater between t_{PLZ} and t_{PHZ} is the same as t_{dis}.

Figure 6-3. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

Figure 6-4. Voltage Waveforms, Input and Output Transition Times



Noise values measured with all other outputs simultaneously switching.

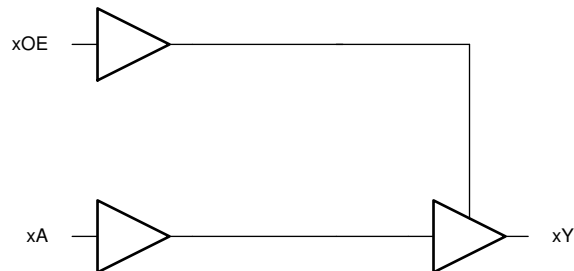
Figure 6-5. Voltage Waveforms, Noise

7 Detailed Description

7.1 Overview

This device contains four independent buffers with 3-state outputs. Each gate performs the Boolean function $Y = A$ in positive logic.

7.2 Functional Block Diagram



One of four channels

7.3 Feature Description

7.3.1 Balanced CMOS 3-State Outputs

This device includes balanced CMOS 3-state outputs. Driving high, driving low, and high impedance are the three states that these outputs can be in. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device can drive larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

When placed into the high-impedance state, the output will neither source nor sink current, with the exception of minor leakage current as defined in the *Electrical Characteristics* table. In the high-impedance state, the output voltage is not controlled by the device and is dependent on external factors. If no other drivers are connected to the node, then this is known as a floating node and the voltage is unknown. A pull-up or pull-down resistor can be connected to the output to provide a known voltage at the output while it is in the high-impedance state. The value of the resistor will depend on multiple factors, including parasitic capacitance and power consumption limitations. Typically, a 10-k Ω resistor can be used to meet these requirements.

Unused 3-state CMOS outputs should be left disconnected.

7.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-k Ω resistor, however, is recommended and will typically meet all requirements.

7.3.3 Clamp Diode Structure

As [Figure 7-1](#) shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

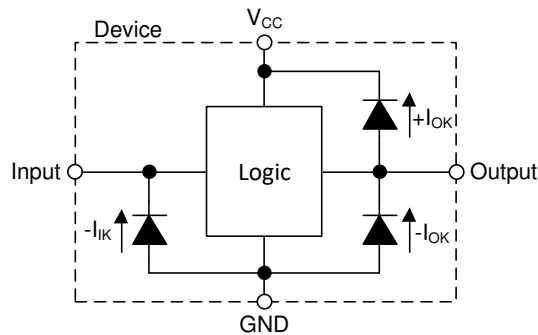


Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT
OE	A	Y
L	X	Z
H	L	L
H	H	H

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs](#)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (August 2023) to Revision N (February 2024) Page

- Added thermal values for D package: R θ JA = 124.6, R θ JC(top) = 79.7, R θ JB = 81.2, Ψ JT = 39.3, Ψ JB = 80.8, R θ JC(bot) = N/A, all values in °C/W5

Changes from Revision L (July 2003) to Revision M (August 2023) Page

- Changed the numbering format for tables, figures, and cross-references throughout the document..... 1
- Added the BQA package to the data sheet..... 1
- Deleted the J, W, D, DB, DGV, N, NS, and FK packages from the data sheet..... 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686201Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201Q2A SNJ54AHC 126FK	Samples
5962-9686201QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201QD A SNJ54AHC126W	Samples
SN74AHC126BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC126	Samples
SN74AHC126D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	AHC126	
SN74AHC126DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC126N	Samples
SN74AHC126NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC126	Samples
SN74AHC126PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	HA126	
SN74AHC126PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SN74AHC126PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA126	Samples
SNJ54AHC126FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201Q2A SNJ54AHC 126FK	Samples
SNJ54AHC126W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686201QD A SNJ54AHC126W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC126, SN74AHC126 :

- Catalog : [SN74AHC126](#)

- Automotive : [SN74AHC126-Q1](#), [SN74AHC126-Q1](#)

- Military : [SN54AHC126](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC126BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC126DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC126DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC126NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC126BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC126DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC126DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC126DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC126DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC126NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC126PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC126PWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9686201Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686201QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC126N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC126FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC126W	W	CFP	14	25	506.98	26.16	6220	NA

D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

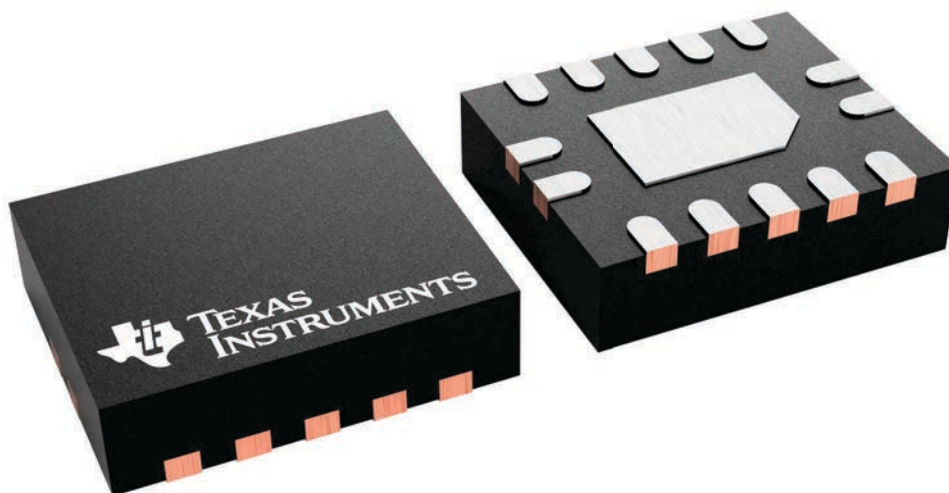
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 88% PRINTED COVERAGE BY AREA
 SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F14

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

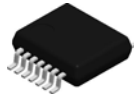
24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

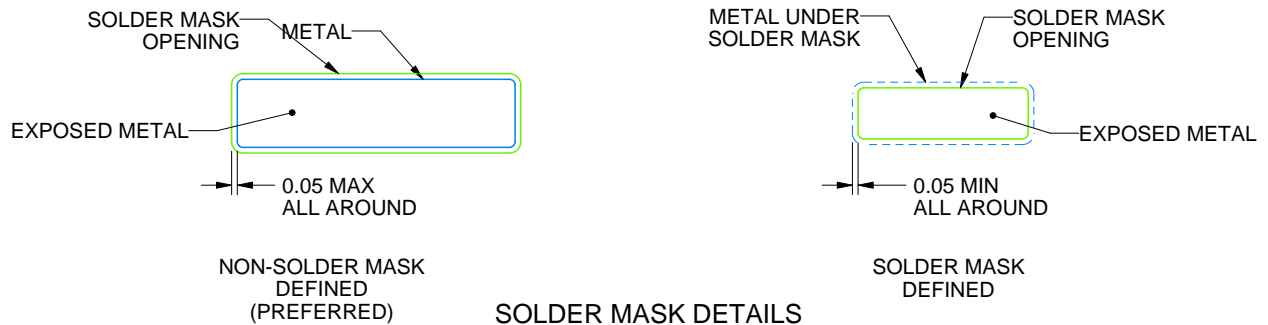
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated