

# SNx4AHCT573 Octal Transparent D-Type Latches With 3-State Outputs

## 1 Features

- Inputs are TTL-voltage compatible
- Latch-up performance exceeds 250mA per JESD 17
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

## 2 Applications

- Servers
- PCs and notebooks
- Network switches
- Wearable health and fitness devices
- Telecom infrastructures
- Electronic points-of-sale

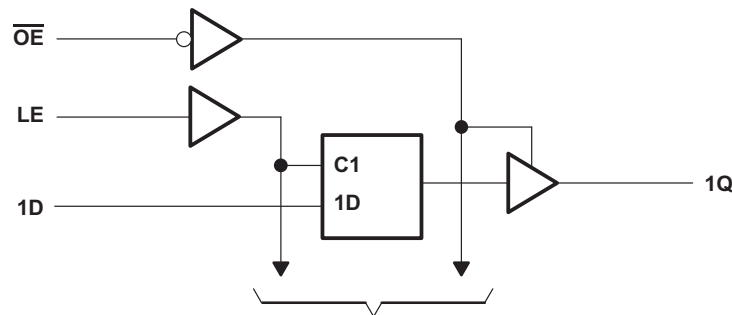
## 3 Description

The SNx4AHCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

### Device Information

PART NUMBER	RATING <sup>(1)</sup>	PACKAGE <sup>(1)</sup>
SN74AHCT573	Catalog	DB (SSOP, 20)
		DGV (TVSOP, 20)
		DW (SOIC, 20)
		N (PDIP, 20)
		PW (TSSOP, 20)
SN54AHCT573	Military	J (CDIP, 20)
		W (CFP, 20)

(1) For more information, see [Section 11](#).



To Seven Other Channels

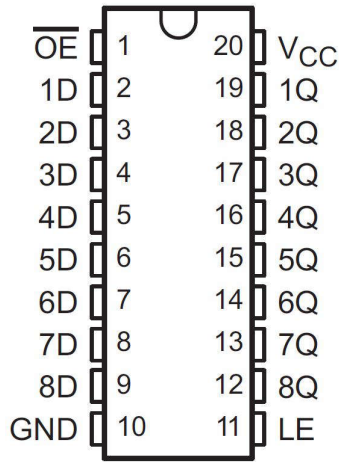
**Simplified Schematic**



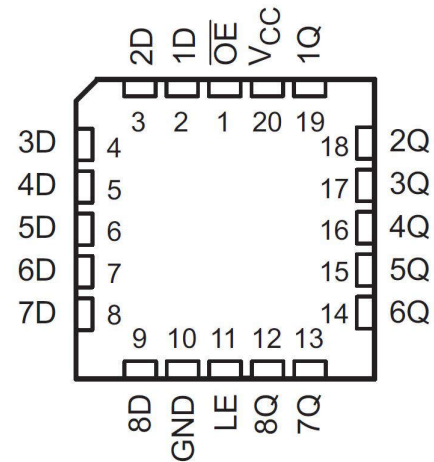
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## 4 Pin Configuration and Functions



**Figure 4-1. SN54AHCT573 J or W Package  
SN74AHCT573 DB, DGV, DW, N, NS, or PW  
Package (Top View)**



**Figure 4-2. SN54AHCT573 FK Package (Top View)**

**Table 4-1. Pin Functions**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Output Enable
2	1D	I	1D Input
3	2D	I	2D Input
4	3D	I	3D Input
5	4D	I	4D Input
6	5D	I	5D Input
7	6D	I	6D Input
8	7D	I	7D Input
9	8D	I	8D Input
10	GND	—	Ground
11	LE	I	Latch Enable
12	8Q	O	8Q Output
13	7Q	O	7Q Output
14	6Q	O	6Q Output
15	5Q	O	5Q Output
16	4Q	O	4Q Output
17	3Q	O	3Q Output
18	2Q	O	2Q Output
19	1Q	O	1Q Output
20	V <sub>CC</sub>	—	Power Pin

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-20 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>		±20 mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>		±25 mA
Continuous current through V <sub>CC</sub> or GND				±75 mA
T <sub>J</sub>	Junction temperature			150 °C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

			MIN	MAX	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>			±2000
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>			±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHCT573		SN74AHCT573		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level input voltage	0.8		0.8		V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	-8		-8		mA
I <sub>OL</sub>	Low-level output current	8		8		mA
Δt/Δv	Input transition rise or fall rate	20		20		ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHCT573						UNIT
		DW	DB	DGV	N	NS	PW	
		20 PINS						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	79.4	97.9	117.2	53.3	79.2	116.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	45.7	59.6	32.7	40.0	45.7	58.5	
R <sub>θJB</sub>	Junction-to-board thermal resistance	46.9	53.1	58.7	34.2	46.8	78.7	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.7	21.3	1.15	26.4	19.3	12.6	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	46.5	52.7	58.0	34.1	46.4	77.9	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			–55°C to 125°C SN54AHCT573		–40°C to 85°C SN74AHCT573		–40°C to 125°C SN74AHCT573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	4.5V	4.4	4.5		4.4		4.4		4.4		V
	I <sub>OH</sub> = –8mA		3.94			3.8		3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5V			0.1		0.1		0.1		0.1	V
	I <sub>OL</sub> = 8mA				0.36		0.44		0.44		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5V or GND	0V to 5.5V			±0.1		±1 <sup>(1)</sup>		±1		±2	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5V			±0.25		±2.5		±2.5		±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5V			4		40		40		40	μA
ΔI <sub>CC</sub> <sup>(2)</sup>	One input at 3.4V, Other inputs at V <sub>CC</sub> or GND	5.5V			1.35		1.5		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5V		2.5	10				10		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5V		3								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0V or V<sub>CC</sub>.

## 5.6 Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 5V ± 0.5V (unless otherwise noted) (see Section 6)

PARAMETER		T <sub>A</sub> = 25°C		–55°C to 125°C SN54AHCT573		–40°C to 85°C SN74AHCT573		–40°C to 125°C SN74AHCT573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration, LE high	5		5		5		5		ns
t <sub>su</sub>	Setup time, data before LE↓	3.5		3.5		3.5		3.5		ns
t <sub>h</sub>	Hold time, data after LE↓	1.5		1.5		1.5		1.5		ns

## 5.7 Switching Characteristics, SNx4AHCT573

over recommended operating free-air temperature range,  $V_{CC} = 5V \pm 0.5V$  (unless otherwise noted) (see Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$C_L = 15\text{pF}$										
$t_{pd}$	D	Q		5.1	7	1	9	1	9.5	ns
$t_{pd}$	LE	Q		5.6	7.5	1	9	1	9.5	ns
$t_{en}$	$\overline{OE}$	Q		5.5	7.5	1	10	1	11	ns
$t_{dis}$	$\overline{OE}$	Q		5.5	8	1	11	1	12	ns
$C_L = 50\text{pF}$										
$t_{pd}$	D	Q		6.1	8	1	10	1	10.5	ns
$t_{pd}$	LE	Q		6.6	8.5	1	10	1	10.5	ns
$t_{en}$	$\overline{OE}$	Q		6.5	8.5	1	11	1	11.5	ns
$t_{dis}$	$\overline{OE}$	Q		6.7	9	1	12	1	12.5	ns
$t_{sk(o)}$					1.5		1.5			ns

- (1) On products compliant to MIL-PRF-38535, this parameter is not production tested.  
 (2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 5.8 Switching Characteristics, SN54AHCT573

over recommended operating free-air temperature range,  $V_{CC} = 5V \pm 0.5V$  (unless otherwise noted) (see Section 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C to } 125^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$C_L = 15\text{pF}$								
$t_{pd}$	D	Q		5.1 <sup>(1)</sup>	7 <sup>(1)</sup>	1 <sup>(1)</sup>	9 <sup>(1)</sup>	ns
$t_{pd}$	LE	Q		5.6 <sup>(1)</sup>	7.5 <sup>(1)</sup>	1 <sup>(1)</sup>	9 <sup>(1)</sup>	ns
$t_{en}$	$\overline{OE}$	Q		5.5 <sup>(1)</sup>	7.5 <sup>(1)</sup>	1 <sup>(1)</sup>	9 <sup>(1)</sup>	ns
$t_{dis}$	$\overline{OE}$	Q		5.5 <sup>(1)</sup>	8 <sup>(1)</sup>	1 <sup>(1)</sup>	11 <sup>(1)</sup>	ns
$C_L = 50\text{pF}$								
$t_{pd}$	D	Q		6.1	8	1	10	ns
$t_{pd}$	LE	Q		6.6	8.5	1	10	ns
$t_{en}$	$\overline{OE}$	Q		6.5	8.5	1	11	ns
$t_{dis}$	$\overline{OE}$	Q		6.7	9	1	12	ns
$t_{sk(o)}$						1.5 <sup>(2)</sup>		ns

## 5.9 Operating Characteristics

$V_{CC} = 5V$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{MHz}$	16	pF

### 5.10 Typical Characteristics

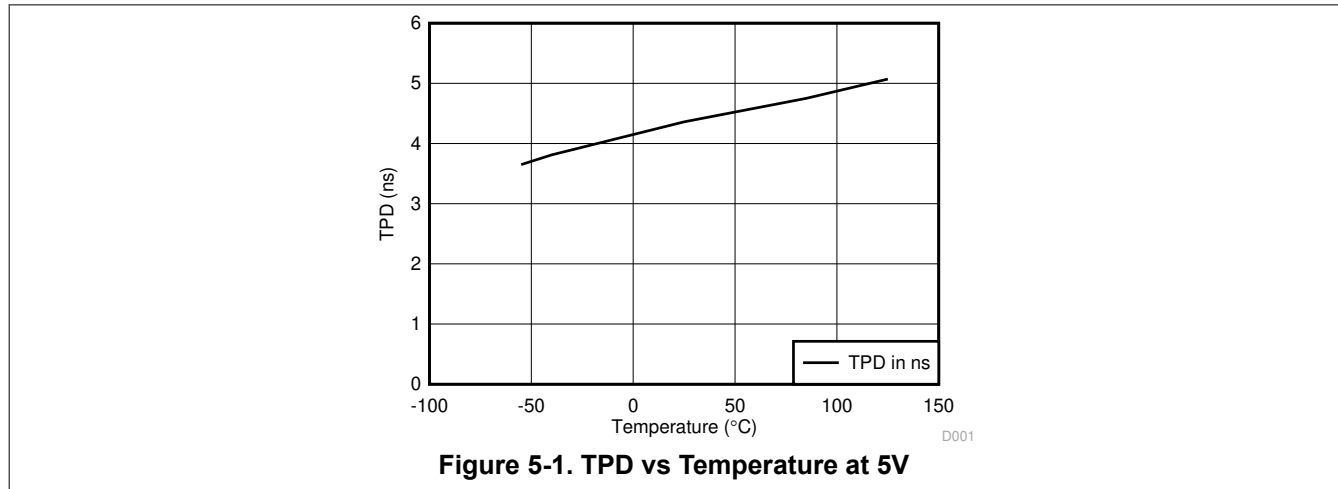


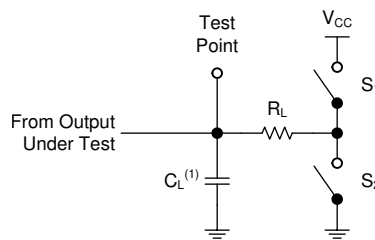
Figure 5-1. TPD vs Temperature at 5V

### 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z<sub>O</sub> = 50Ω, R<sub>L</sub> = 1kΩ, t<sub>t</sub> < 3ns, V<sub>t</sub> = 1.5V.

For clock inputs, f<sub>max</sub> is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C<sub>L</sub> includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for 3-State Outputs

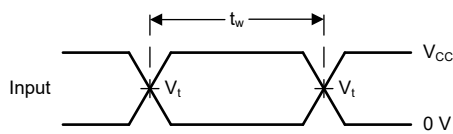


Figure 6-2. Voltage Waveforms, Pulse Duration

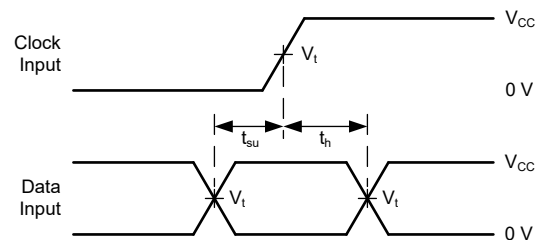
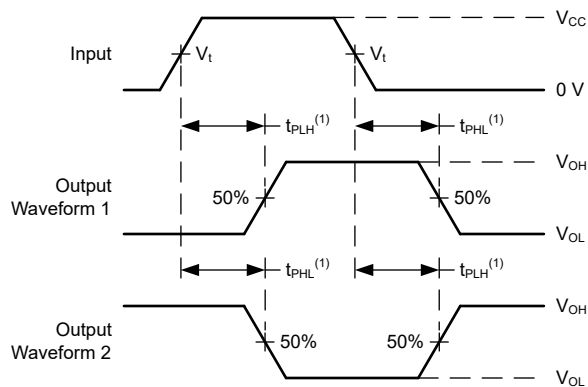
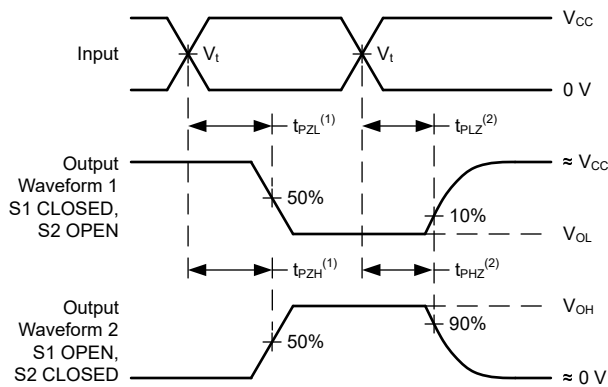


Figure 6-3. Voltage Waveforms, Setup and Hold Times



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

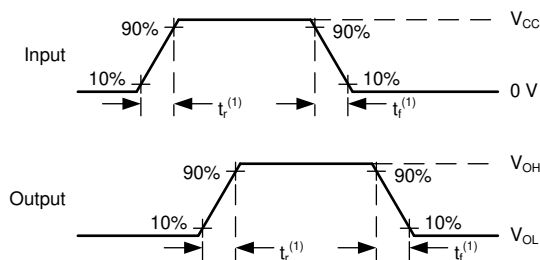
**Figure 6-4. Voltage Waveforms, Propagation Delays**



(1)  $t_{PZL}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(2)  $t_{PZL}$  and  $t_{PHZ}$  are the same as  $t_{en}$ .

**Figure 6-5. Voltage Waveforms, Propagation Delays for 3-State Outputs**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

**Figure 6-6. Voltage Waveforms, Input and Output Transition Times**

## 7 Detailed Description

### 7.1 Overview

The SNx4AHCT573 devices are octal transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

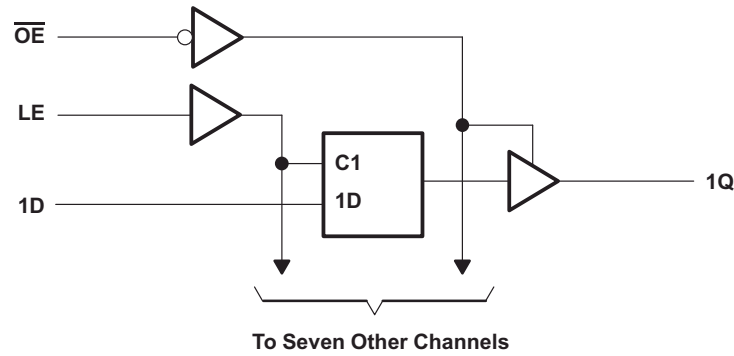
A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components.

To put the device in the high-impedance state during power up or power down, tie  $\overline{OE}$  to  $V_{CC}$  through a pull-up resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.



## 7.2 Functional Block Diagram



## 7.3 Feature Description

- TTL inputs
  - Lowered switching threshold allows up translation 3.3V to 5V
- Slow edges reduce output ringing

## 7.4 Device Functional Modes

**Table 7-1. Function Table (Each Latch)**

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The SN74AHCT573 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of  $0.8V_{IL}$  and  $2V_{IH}$ . This feature makes the device an excellent choice for translating up from 3.3V to 5V. [Figure 8-2](#) shows this type of translation.

### 8.2 Typical Application

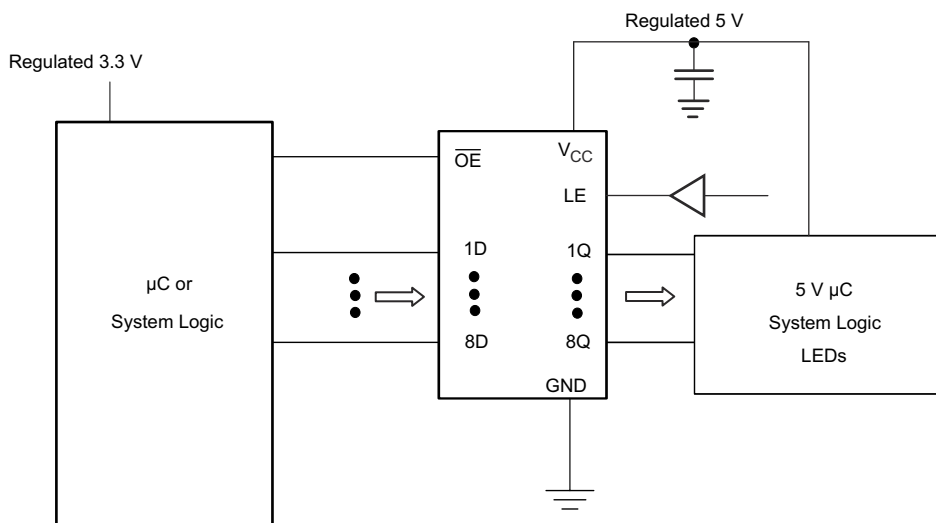


Figure 8-1. Typical Application Schematic

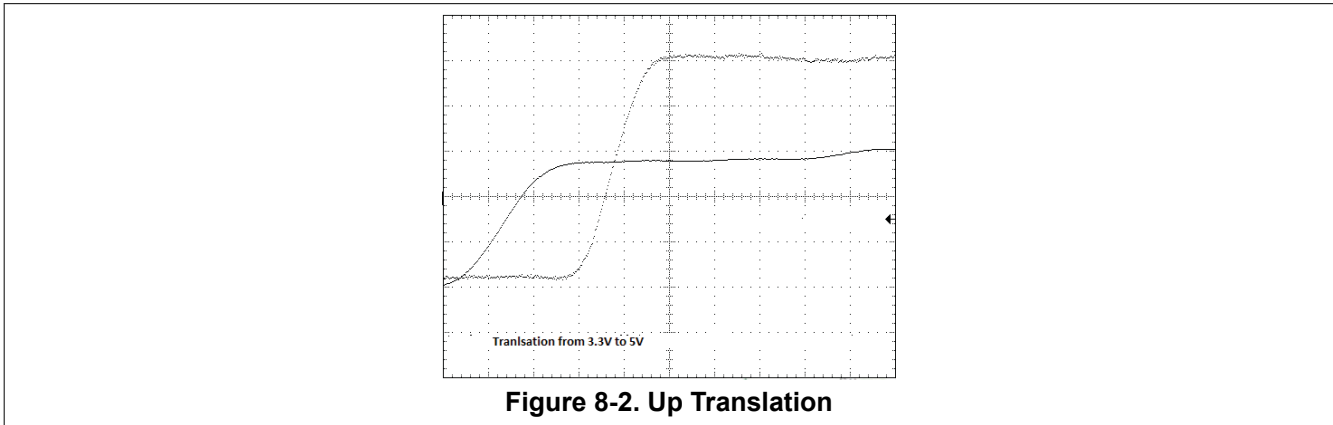
#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

1. Recommended input conditions:
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified High and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid  $V_{CC}$ .
2. Recommend output conditions
  - Load currents should not exceed 25mA per output and 75mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 8.2.3 Application Curves



### 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 $\mu$ F bypass capacitor is recommended. If there are multiple  $V_{CC}$  pins, 0.01 $\mu$ F or 0.022 $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 $\mu$ F and 1 $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 8.4 Layout

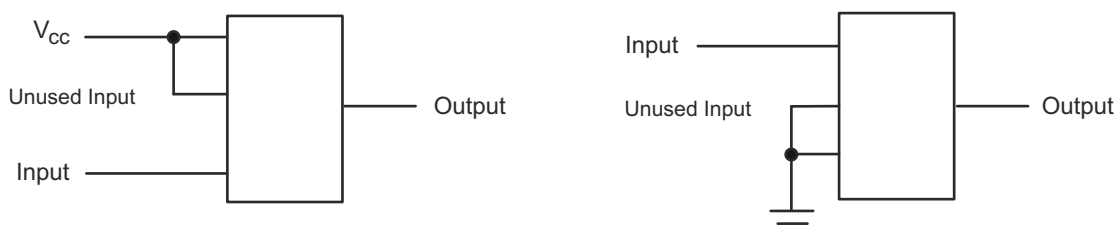
#### 8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 8-3](#) specifies the rules that must be observed under all circumstances.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, then it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they cannot float when disabled.

#### 8.4.2 Layout Example



**Figure 8-3. Layout Diagram**

## 9 Device and Documentation Support

### 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
 All trademarks are the property of their respective owners.

### 9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision P (April 2024) to Revision Q (July 2024)	Page
• Updated thermal values for PW package from RθJA = 103.3 to 116.8, RθJC(top) = 37.8 to 58.5, RθJB = 54.3 to 78.7, ΨJT = 2.9 to 12.6, ΨJB = 53.8 to 77.9, RθJC(bot) = N/A, all values in °C/W .....	5

Changes from Revision O (July 2014) to Revision P (April 2024)	Page
• Moved storage temperature from <i>Handling Ratings</i> table to <i>Absolute Maximum Ratings</i> table.....	4
• Changed Handling Ratings table to ESD Ratings table.....	4
• Added temperature range column labels in Electrical Characteristics table.....	5
• Added temperature range column labels in Timing Requirements table.....	5
• Changed $t_{PLH}$ and $t_{PHL}$ to be $t_{pd}$ , $t_{PZH}$ and $t_{PZL}$ to be $t_{en}$ , and $t_{PLZ}$ and $t_{PHZ}$ to be $t_{dis}$ .....	6
• Changed <i>Switching Characteristics</i> table to be two tables separating military and catalog device characteristics.....	6
• Changed parameter measurement information section images and tables to improve clarity and update formatting.....	7

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685501QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685501QR A SNJ54AHCT573J	<a href="#">Samples</a>
5962-9685501QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685501QS A SNJ54AHCT573W	<a href="#">Samples</a>
SN74AHCT573DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB573	<a href="#">Samples</a>
SN74AHCT573DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB573	<a href="#">Samples</a>
SN74AHCT573DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	AHCT573	
SN74AHCT573DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT573	<a href="#">Samples</a>
SN74AHCT573N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT573N	<a href="#">Samples</a>
SN74AHCT573PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 125	HB573	
SN74AHCT573PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HB573	<a href="#">Samples</a>
SN74AHCT573PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB573	<a href="#">Samples</a>
SN74AHCT573PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB573	<a href="#">Samples</a>
SNJ54AHCT573J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685501QR A SNJ54AHCT573J	<a href="#">Samples</a>
SNJ54AHCT573W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685501QS A SNJ54AHCT573W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AHCT573, SN74AHCT573 :**

● Catalog : [SN74AHCT573](#)

● Military : [SN54AHCT573](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT573DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT573DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT573PWGR4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT573DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHCT573DGVR	TVSOP	DGV	20	2000	356.0	356.0	35.0
SN74AHCT573DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT573PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHCT573PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9685501QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHCT573N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHCT573W	W	CFP	20	25	506.98	26.16	6220	NA

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

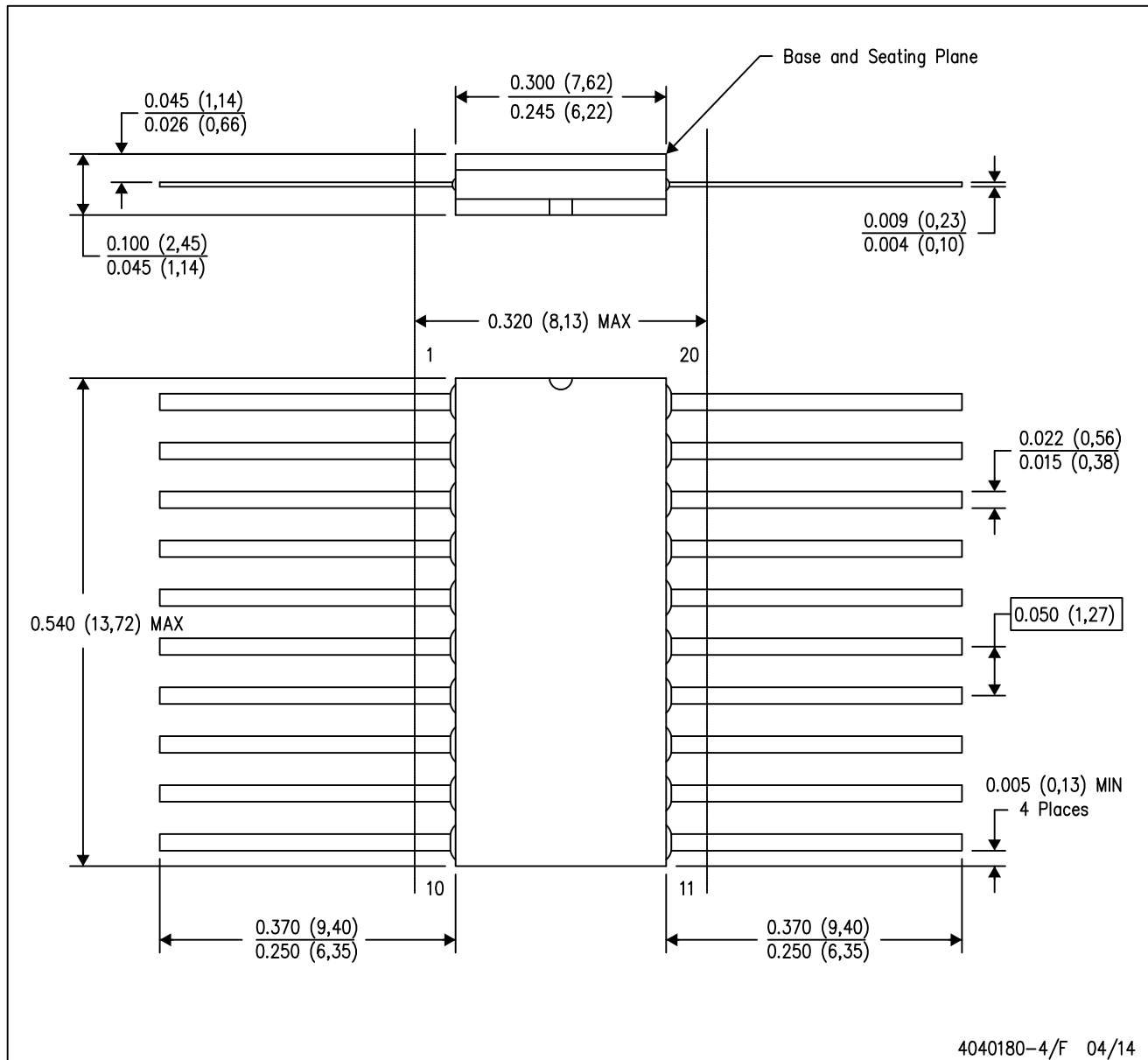
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

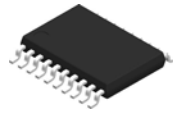
CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20



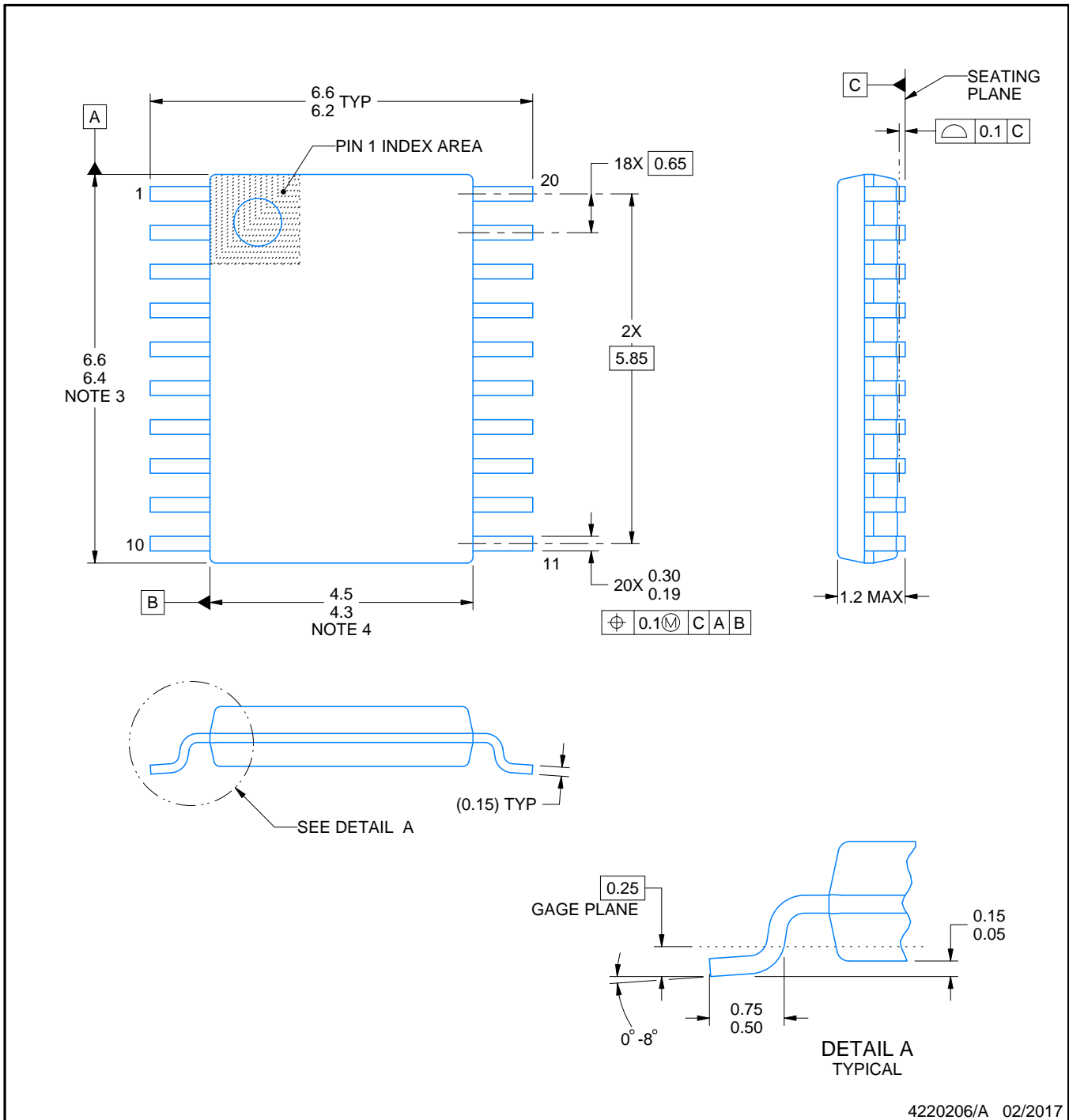
# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

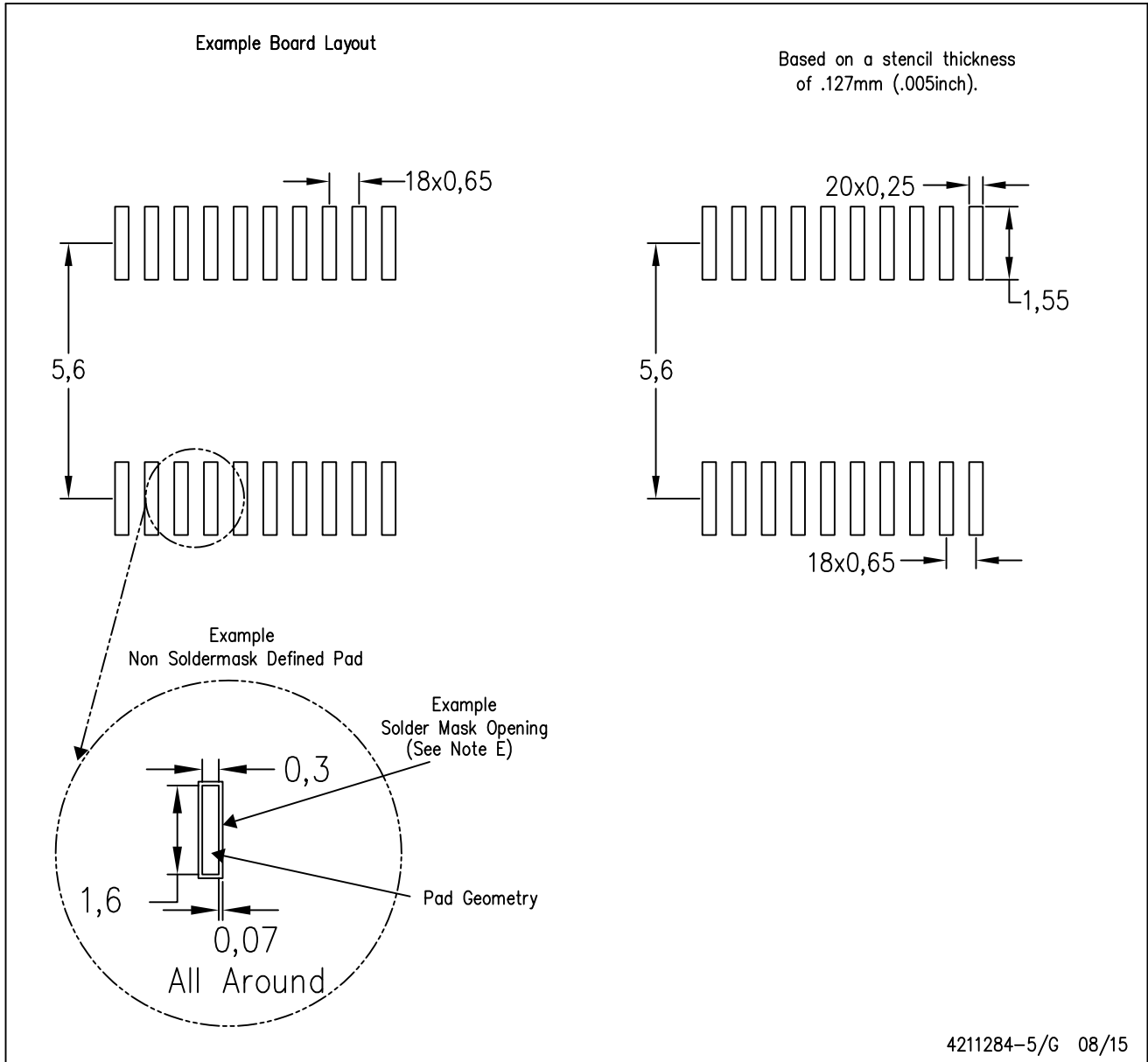
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

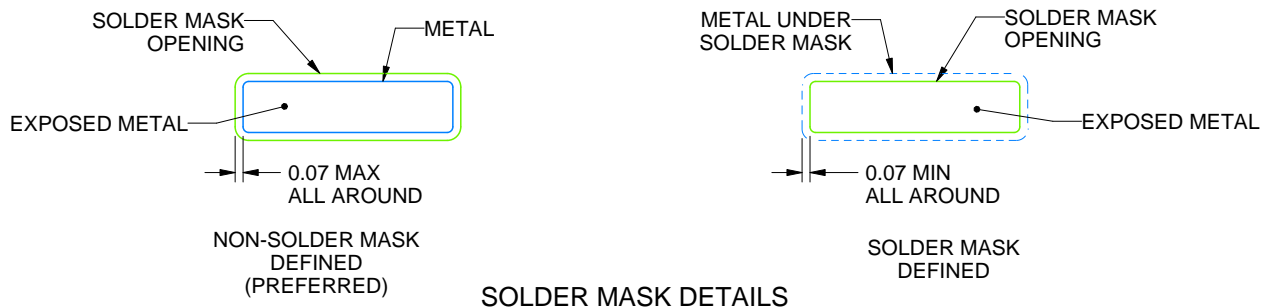
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

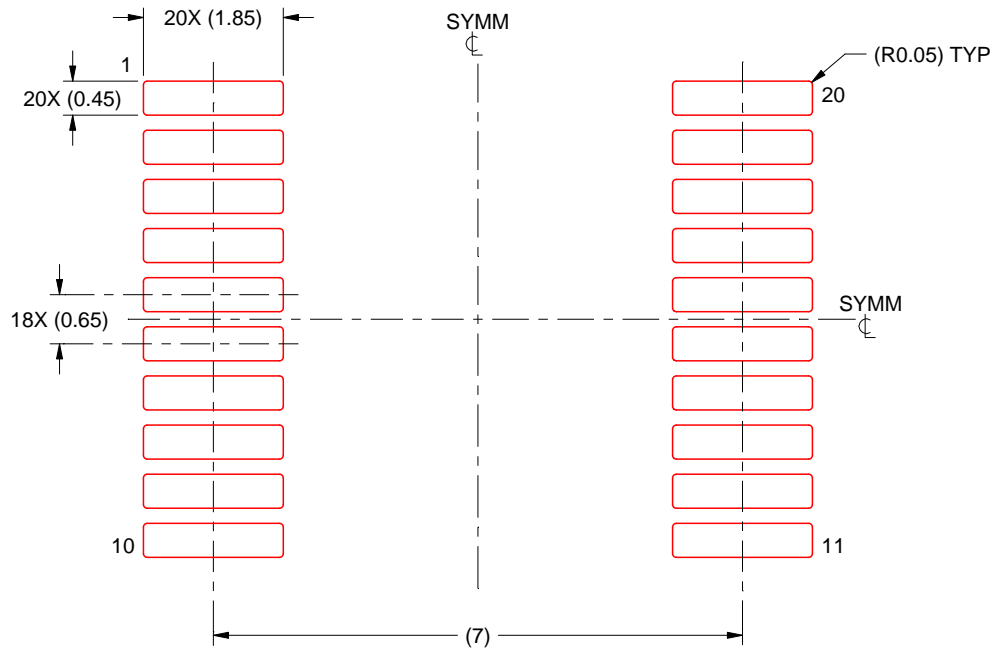
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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