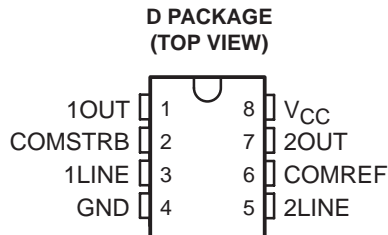


- Single 5-V Supply
- ± 100 -mV Sensitivity
- For Application as:
 - Single-Ended Line Receiver
 - Gated Oscillator
 - Level Comparator
- Adjustable Reference Voltage
- TTL Outputs
- TTL-Compatible Strobe
- Designed for Party-Line (Data-Bus) Applications
- Common Reference-Voltage Pin
- Common Strobe



description/ordering information

This device consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 V to 3.4 V, making it possible to optimize noise immunity for a given system design. Due to the low input current (less than 100 μ A), the device is suited ideally for party-line (data-bus) systems.

The SN74LS2323 has a common reference-voltage pin and a common strobe.

ORDERING INFORMATION

T _A	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube	SN74LS2323D
		Tape and reel	SN74LS2323DR
			LS2323

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each receiver)

LINE INPUT	STROBE	OUTPUT
$\leq (V_{REF} - 100 \text{ mV})$	L	H
$\geq (V_{REF} + 100 \text{ mV})$	X	L
X	H	L

H = high level, L = low level, X = irrelevant



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



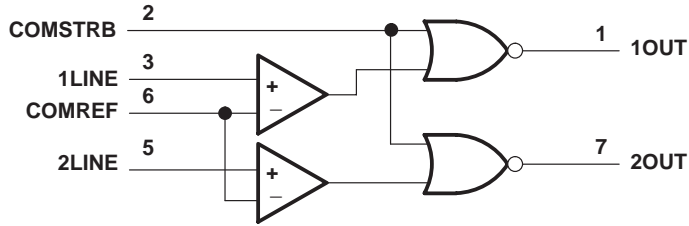
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

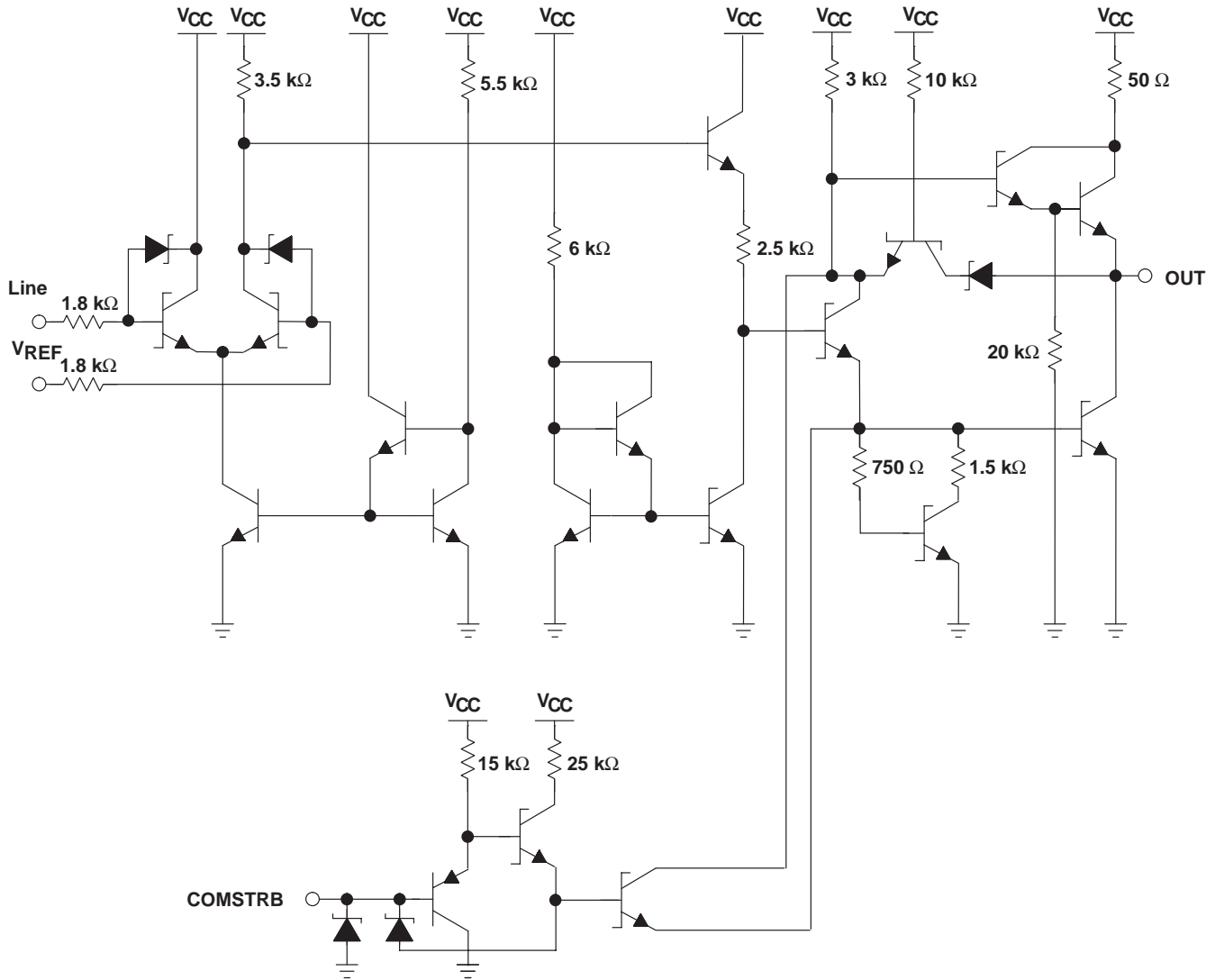
SN74LS2323 DUAL LINE RECEIVER

SDLS965 – OCTOBER 2004

logic diagram (positive logic)



schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Reference input voltage, V_{REF}	5.5 V
Line input voltage range with respect to GND	–2 V to 7 V
Line input voltage with respect to V_{REF}	±5 V
Strobe input voltage, $V_{I(S)}$	7 V
Package thermal impedance, θ_{JA} (see Note 2)	97°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Unless otherwise specified, voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{ref}	Reference input voltage	1.8		‡	V
$V_{I(L)}$	High-level line input voltage	0		$V_{CC} - 1$	V
$V_{I(S)}$	High-level strobe input voltage	0		7	V
T_A	Operating free-air temperature range	0		70	°C

‡ Max = $V_{CC} - 1.5\text{ V} > V_{REF} < 3.4\text{ V}$

SN74LS2323

DUAL LINE RECEIVER

SDLS965 – OCTOBER 2004

electrical characteristics over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{REF} = 1.5\text{ V to } 3.5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT	
$V_{IH(L)}$	High-level line input voltage	$V_{I(S)} = 0.8\text{ V}$, $I_{OL} = 12\text{ mA}$, $V_{REF} = 2.5\text{ V}$, $V_{OL} \leq 0.6\text{ V}$	$V_{CC} = 4.5\text{ V}$	2.62	6	V
		$V_{I(S)} = 0.8\text{ V}$, $I_{OL} = 16\text{ mA}$, $V_{REF} = 3.4\text{ V}$, $V_{OL} \leq 0.5\text{ V}$	$V_{CC} = 5.5\text{ V}$	3.5	7	
$V_{IL(L)}$	Low-level line input voltage	$V_{I(S)} = 0.8\text{ V}$, $I_{OH} = -0.4\text{ mA}$, $V_{REF} = 2.5\text{ V}$, $V_{OH} \geq 2\text{ V}$	$V_{CC} = 4.5\text{ V}$	-2	2.38	V
		$V_{I(S)} = 0.8\text{ V}$, $I_{OH} = -0.4\text{ mA}$, $V_{REF} = 3.4\text{ V}$, $V_{OH} \geq 3.2\text{ V}$	$V_{CC} = 5.5\text{ V}$	-2	3.3	
$V_{IH(S)}$	High-level output control input voltage	$V_{I(L)} = 1.8\text{ V}$, $V_{REF} = 2.5\text{ V}$, $V_O \leq 0.4\text{ V}$	$V_{CC} = 4.5\text{ V}$	2	V	
$V_{IL(S)}$	Low-level output control input voltage	$V_{I(L)} = 1.8\text{ V}$, $V_{REF} = 2.5\text{ V}$, $V_O \geq 2.4\text{ V}$	$V_{CC} = 4.5\text{ V}$	0.8	V	
V_{OH}	High-level output voltage	$V_{I(L)} = 1.4\text{ V}$, $V_{I(S)} = 0.8\text{ V}$, $I_{OH} = -1\text{ mA}$, $V_{REF} = 2.5\text{ V}$	$V_{CC} = 4.5\text{ V}$	2	V	
			$V_{CC} = 5\text{ V}$	2.7		
			$V_{CC} = 5.5\text{ V}$	2.7		
V_{OL}	Low-level output voltage	$V_{I(L)} = 3.8\text{ V}$, $V_{I(S)} = 0.8\text{ V}$, $V_{REF} = 2.5\text{ V}$	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 16\text{ mA}$	0.6	V	
			$V_{CC} = 5\text{ V}$, $I_{OL} = 24\text{ mA}$	0.5		
			$V_{CC} = 5.5\text{ V}$, $I_{OL} = 24\text{ mA}$	0.5		
$I_{IH(S)}$	High-level input current	$V_{I(L)} = 3.8\text{ V}$, $V_{REF} = 2.5\text{ V}$	$V_{CC} = 5.5\text{ V}$, $V_{I(S)} = 2.4\text{ V}$	20	μA	
			$V_{CC} = 5.5\text{ V}$, $V_{I(S)} = 7\text{ V}$	100		
$I_{IH(L)}$	High-level input current	$V_{I(S)} = 2.4\text{ V}$, $V_{REF} = 2.5\text{ V}$	$V_{CC} = 5\text{ V}$, $V_{I(L)} = 5\text{ V}$	100	μA	
			$V_{CC} = 5\text{ V}$, $V_{I(L)} = 5.5\text{ V}$	2	mA	
$I_{IH(REF)}$	High-level input current	$V_{I(S)} = 2.4\text{ V}$, $V_{REF} = 3.4\text{ V}$	$V_{CC} = 5.5\text{ V}$, $V_{I(L)} = 2.5\text{ V}$	500	μA	
$I_{IL(S)}$	Low-level input current	$V_{I(L)} = 1.8\text{ V}$, $V_{REF} = 0.1\text{ V}$	$V_{CC} = 5.5\text{ V}$, $V_{I(S)} = 0.4\text{ V}$	-400	μA	
$I_{IL(L)}$	Low-level input current at Line input	$V_{I(L)} = 0.1\text{ V}$, $V_{REF} = 1.8\text{ V}$	$V_{CC} = 5.5\text{ V}$, $V_{I(S)} = 0.4\text{ V}$	-100	μA	
$I_{IL(REF)}$	Low-level input current at REF pin	$V_{I(L)} = 1.8\text{ V}$, $V_{REF} = 0.1\text{ V}$	$V_{CC} = 5.5\text{ V}$, $V_{I(S)} = 0.4\text{ V}$	-100	μA	
I_{OS}	Short-circuit output current [†]	$V_{I(L)} = 1.8\text{ V}$, $V_{REF} = 2.8\text{ V}$	$V_{CC} = 5.5\text{ V}$, $V_{I(S)} = 0.4\text{ V}$	-30	-130	mA
I_{CCH}	Supply current, output high	$V_{I(S)} = 0$, $V_{CC} = 5.5\text{ V}$, $V_{I(L)} = V_{REF} - 100\text{ mV}$		12	mA	
I_{CCL}	Supply current, output low	$V_{I(S)} = 0$, $V_{CC} = 5.5\text{ V}$, $V_{I(L)} = V_{REF} + 100\text{ mV}$		16	mA	

[†] Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

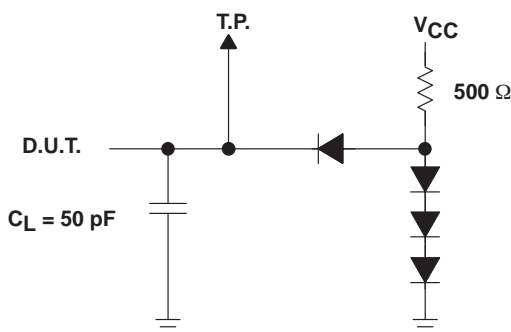


switching characteristics, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{REF} = 2.5\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C

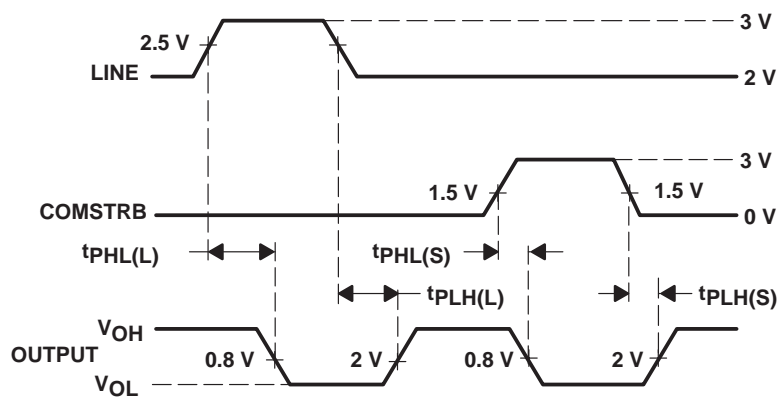
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{PLH(L)}$ Propagation delay time, low- to high-level output from LINE	$C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, See Figure 1	10	25	35	ns
$t_{PHL(L)}$ Propagation delay time, high- to low-level output from LINE	$C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, See Figure 1	10	25	35	ns
$t_{PLH(S)}$ Propagation delay time, low- to high-level output from COMSTRB	$C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, See Figure 1		11	22	ns
$t_{PHL(S)}$ Propagation delay time, high- to low-level output from COMSTRB	$C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, See Figure 1		8	15	ns

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, t_r and $t_f \leq 2\text{ ns}$, and duty cycle = 50%.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N914 (or equivalent).
 D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS2323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS2323DR	SOIC	D	8	2500	340.5	336.1	25.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated