

SN74LVC1G14 Single Schmitt-Trigger Inverter

1 Features

- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22
 - 2000V human-body model (A114-A)
 - 200V machine model (A115-A)
 - 1000V charged-device model (C101)
- Available in the Texas Instruments NanoFree™ package
- Supports 5V V_{CC} operation
- Inputs accept voltages to 5.5V
- Maximum t_{pd} of 4.6ns at 3.3V
- Low power consumption, 10 μ A maximum I_{CC}
- ± 24 mA output drive at 3.3V
- I_{off} supports partial-power-down mode operation

2 Applications

- AV receiver
- Audio dock: portable
- Blu-ray player and home theater
- Embedded PC
- MP3 player/recorder (portable audio)
- Personal Digital Assistant (PDA)
- Power: telecom/server AC/DC supply: single controller: analog and digital
- Solid State Drive (SSD): client and enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: enterprise
- Video analytics: server
- Wireless headset, keyboard, and mouse

3 Description

This single Schmitt-trigger inverter is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G14 device contains one inverter and performs the Boolean function $Y = \bar{A}$. The device functions as an independent inverter with Schmitt-trigger inputs, so the device has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals to provide hysteresis (ΔV_T) which makes the device tolerant to slow or noisy input signals.

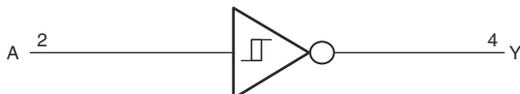
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾
SN74LVC1G14	DBV (SOT-23, 5)	2.90mm × 2.80mm	2.90mm × 1.60mm
	DCK (SC70, 5)	2.00mm × 2.10mm	2.00mm × 1.25mm
	DRL (SOT-5X3, 5)	1.60mm × 1.60mm	1.60mm × 1.20mm
	DRY (USON, 6)	1.45mm × 1.00mm	1.45mm × 1.00mm
	DSF (X2SON, 6)	1.00mm × 1.00mm	1.00mm × 1.00mm
	YZP (DSBGA, 5)	1.75mm × 1.75mm	1.39mm × 0.89mm
	YZV (DSBGA, 4)	1.25mm × 1.25mm	0.89mm × 0.89mm
	DPW (X2SON, 5)	0.80mm × 0.80mm	0.80mm × 0.80mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)
(DBV, DCK, DRL, DRY, DPW, and YZP Package)



Logic Diagram (Positive Logic)
(YZV Package)



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4 Pin Configuration and Functions

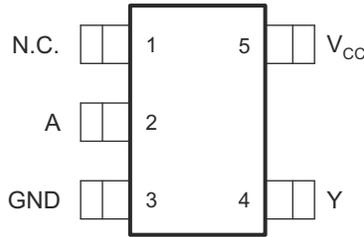


Figure 4-1. DBV Package 5-Pin SOT-23 Top View

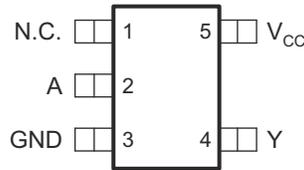


Figure 4-2. DCK Package 5-Pin SC70 Top View

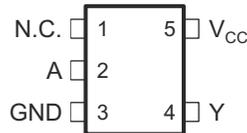


Figure 4-3. DRL Package 5-Pin SOT-5X3 Top View

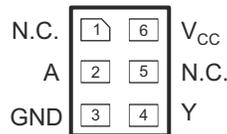
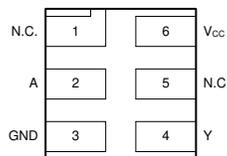


Figure 4-4. DRY Package 6-Pin SON Top View

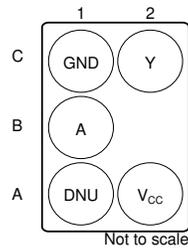


Figure 4-5. DPW Package 5-Pin X2SON Top View



See mechanical drawings for dimensions.
N.C. – No internal connection

Figure 4-6. DSF Package 6-Pin SON Top View



DNU – Do not use

Figure 4-7. YZP Package 5-Pin DSBGA Bottom View

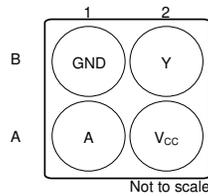


Figure 4-8. YZV Package 4-Pin DSBGA Bottom View

Table 4-1. Pin Functions

NAME	PIN				I/O	DESCRIPTION
	DBV, DCK, DRL, DPW	DRY, DSF	YZP	YZV		
A	2	2	B1	A1	I	Signal Input
GND	3	3	C1	B1	—	Ground
N.C.	1	1, 5	—	—	—	No internal connection ⁽¹⁾
DNU	—	—	A1	—	—	Do not use ⁽²⁾
V _{CC}	5	6	A2	A2	—	Positive Supply
Y	4	4	C2	B2	O	Signal Output

- (1) Pins labeled N.C. can be connected to any signal or voltage source, including ground. They should always be soldered to the board.
- (2) Pins labeled DNU should not be connected to any signal or voltage source, including ground. They should always be soldered to the board.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	6.5	V
V _I	Input voltage ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ^{(2) (3)}	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Maximum junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	1000
		Machine Model (A115-A)	200

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V		–4	mA
		V _{CC} = 2.3 V		–8	
		V _{CC} = 3 V		–16	
		V _{CC} = 4.5 V		–24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
		V _{CC} = 4.5 V		24	
T _A	Operating free-air temperature	YZP, YZV, and DPW packages	–40	85	°C
		All other packages	–40	125	

(1) All unused inputs of the device must be held at V_{CC} or GND to assure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC1G14							UNIT	
	DBV (SOT-23)	DCK (SC70)	DRL (SOT-5X3)	DRY (SON)	DPW (X2SON)	YZV (DSBGA)	YZP (DSBGA)		
	5 PINS	5 PINS	5 PINS	5 PINS	5 PINS	4 PINS	5 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	357.1	371.0	296.2	369.6	522.9	168.2	146.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	263.7	297.5	137.3	257.6	250.5	2.1	1.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	264.4	258.6	145.3	230.8	384.0	55.9	39.8	°C/W
ψ _{JT}	Junction-to-top characterization parameter	195.6	195.6	14.7	77.2	46.5	1.1	0.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	262.2	256.2	145.9	231.0	382.8	56.3	39.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	174.1	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40°C to 85°C			–40°C to 125°C ⁽²⁾			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP	MAX	
V _{T+} Positive-going input threshold voltage		1.65 V	0.79		1.16	.79		1.16	V
		2.3 V	1.11		1.56	1.11		1.56	
		3 V	1.5		1.87	1.5		1.87	
		4.5 V	2.16		2.74	2.16		2.74	
		5.5 V	2.61		3.33	2.61		3.33	
V _{T–} Negative- going input threshold voltage	DBV, DCK, DRL, DRY, DSF, YZV and YZP packages	1.65 V	0.39		0.62	.39		.64	V
		2.3 V	0.58		0.87	.58		.89	
		3 V	0.84		1.14	.84		1.16	
		4.5 V	1.41		1.79	1.41		1.79	
		5.5 V	1.87		2.29	1.87		2.29	
V _{T–} Negative- going input threshold voltage	DPW package	1.65 V	0.44		0.67				V
		2.3 V	0.63		0.92				
		3 V	0.89		1.19				
		4.5 V	1.46		1.84				
		5.5 V	1.92		2.34				
ΔV _T Hysteresis (V _{T+} – V _{T–})		1.65 V	0.37		0.62	0.37		0.62	V
		2.3 V	0.48		0.77	0.48		0.77	
		3 V	0.56		0.87	0.56		0.87	
		4.5 V	0.71		1.04	0.71		1.04	
		5.5 V	0.71		1.11	0.71		1.11	
V _{OH}	I _{OL} = –100 μA	1.65 V to 4.5 V	V _{CC} – 0.1		V _{CC} – 0.1				V
		1.65 V	1.2		1.2				
		2.3 V	1.9		1.9				
		3 V	2.4		2.4				
			2.3		2.3				
			3.8		3.8				
V _{OL}	I _{OL} = 100 μA	1.65 V to 4.5 V			0.1		0.1		V
		1.65 V			0.45		0.45		
		2.3 V			0.3		0.3		
		3 V			0.4		0.4		
					0.55		0.55		
					0.55		0.7		
I _I	A input V _I = 5.5 V or GND	0 to 5.5 V			±5		±5		μA
I _{off}	V _I or V _O = 5.5 V	0			±10		±10		μA
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10		10		μA
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V			500		500		μA
C _i	V _I = V _{CC} or GND	3.3 V	4.5				4.5		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) These specifications do not apply to DPW, YZV and YZP packages. DPW, YZV and YZP have a recommended operating free-air temperature range of –40°C to 85°C.

5.6 Switching Characteristics: –40°C to 85°C

over recommended operating free-air temperature range, (–40°C to 85°C unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	C _L = 15 pF		C _L = 30 pF or 50 pF		UNIT
				MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.8 V ± 0.15 V	2.8	9.9	3.8	11	ns
			2.5 V ± 0.2 V	1.6	5.5	2	6.5	
			3.3 V ± 0.3 V	1.5	4.6	1.8	5.5	
			5 V ± 0.5 V	0.9	4.4	1.2	5	

5.7 Switching Characteristics: –40°C to 125°C

over operating free-air temperature range, (–40°C to 125°C unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	C _L = 30 pF or 50 pF		UNIT
				MIN	MAX	
t _{pd}	A	Y	1.8 V ± 0.15 V	3.8	13	ns
			2.5 V ± 0.2 V	2	8	
			3.3 V ± 0.3 V	1.8	6.5	
			5 V ± 0.5 V	1.2	6	

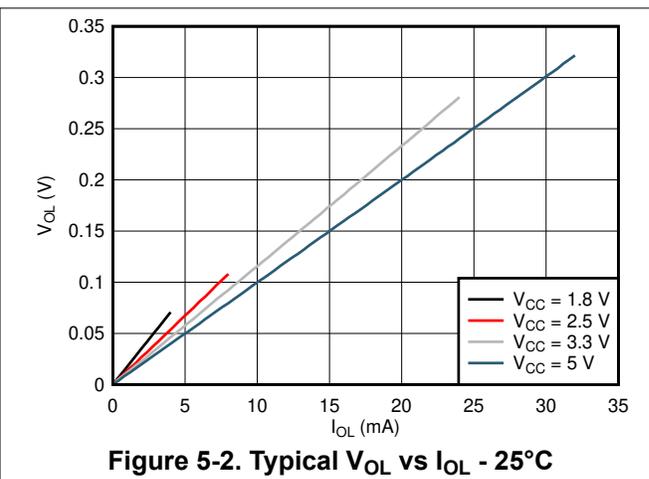
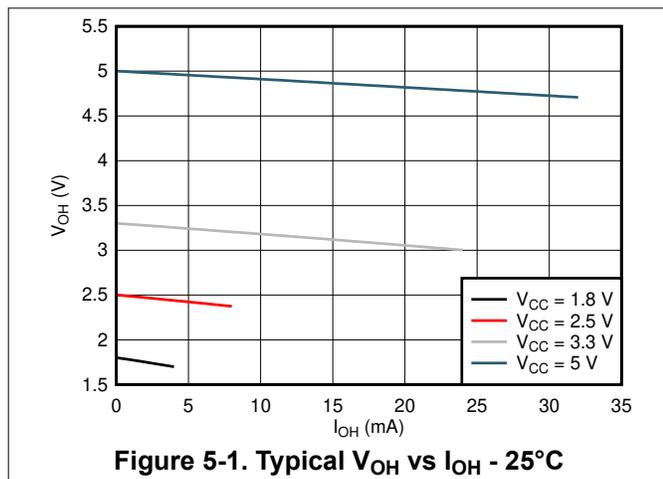
5.8 Operating Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd} Power dissipation capacitance	f = 10 MHz	1.8 V	20	pF
		2.5 V	21	
		3.3 V	22	
		5 V	25	

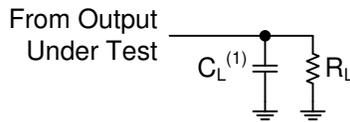
5.9 Typical Characteristics

T_A = 25°C



Parameter Measurement Information

- Input pulse is supplied by generator having the following characteristics: PRR \leq 10MHz. $Z_O = 50\Omega$.
- The outputs are measured one at a time, with one transition per measurement.

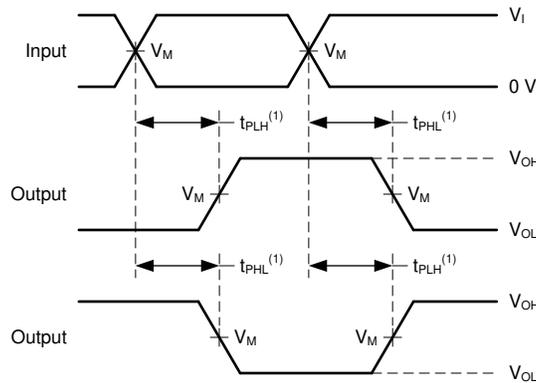


A. C_L includes probe and jig capacitance.

Figure 6-1. Load Circuit

Table 6-1. Parameter Measurement Conditions

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_D
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
					30 pF	1 k Ω	
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
					30 pF	500 Ω	
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
					50 pF	500 Ω	
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V
					50 pF	500 Ω	



A. The maximum value of t_{pd} is the worst case of t_{PLH} or t_{PHL}

Figure 6-2. Voltage Waveforms, Propagation Delay Times, Inverting and Non-Inverting Outputs

6 Detailed Description

6.1 Overview

The SN74LVC1G14 single Schmitt-trigger inverter is designed for 1.65 V to 5.5 V operation and performs the Boolean function $Y = \overline{A}$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

6.2 Functional Block Diagrams

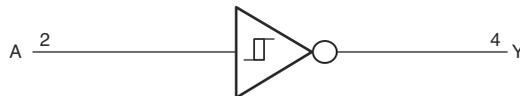


Figure 6-1. Logic Diagram (Positive Logic)
(DBV, DCK, DRL, DRY, DPW, and YZP Package)

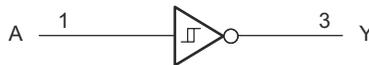


Figure 6-2. Logic Diagram (Positive Logic)
(YZV Package)

6.3 Feature Description

6.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#)

[Absolute Maximum Ratings](#) must be followed at all times.

6.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined in the [Electrical Characteristics](#), which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device.

6.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

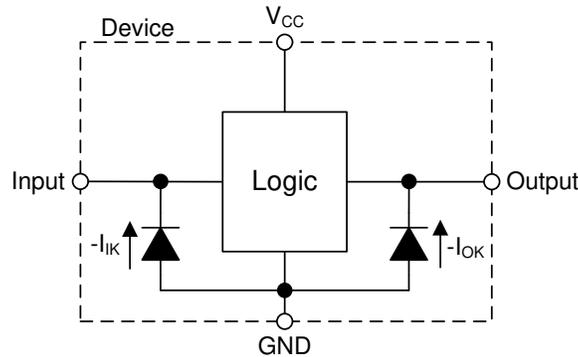


Figure 6-3. Electrical Placement of Clamping Diodes for Each Input and Output

6.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

6.3.5 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Absolute Maximum Ratings](#).

6.4 Device Functional Modes

[Table 6-1](#) lists the functional modes of the SN74LVC1G14 device.

Table 6-1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Mechanical input elements, such as push buttons or rotary knobs, offer simple ways to interact with electronic systems. Typically, these elements have recoil or bouncing, where the mechanical element makes and breaks contact multiple times during human interaction. This bouncing can cause one or more repeated signals to be passed, triggering multiple actions when only a single input was intended. One potential solution to mitigating these multiple inputs is by utilizing a Schmitt-trigger to create a debounce circuit. Figure 7-1 shows an example of this solution.

7.2 Typical Application

The input due to the push button switches multiple times, causing the output of a non Schmitt-trigger device to trigger multiple times, while the Schmitt-trigger input device with RC delay limits the output pulse to a single pulse desired by the user. The separated positive and negative input voltage threshold values, see Figure 7-2, prevent multiple triggers from occurring.

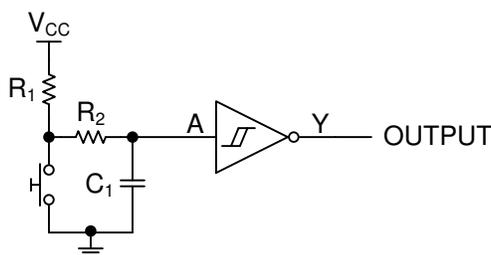


Figure 7-1. Push Button Debounce Circuit Schematic

7.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads so routing and load conditions should be considered to prevent ringing.

7.2.2 Detailed Design Procedure

- Recommended Input Conditions:
 - For specified high and low levels, see (V_{T+} and V_{T-}) in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the [Recommended Operating Conditions](#) table at any valid V_{CC} .
- Recommended Output Conditions:
 - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Absolute Maximum Ratings](#) table.

7.2.3 Application Curve

Figure 7-2 is created from the values given in the *Electrical Characteristics*. Linear interpolation shows the values between each given point.

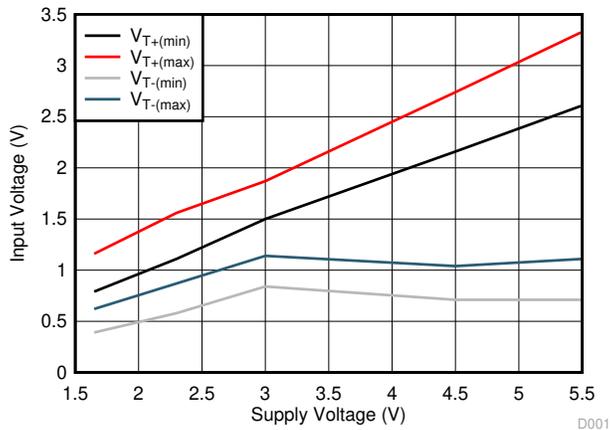


Figure 7-2. Interpolated Threshold Voltages vs. V_{CC}

7.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

7.4 Layout

7.4.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.

An example layout is given in Figure 7-3 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

7.4.2 Layout Example

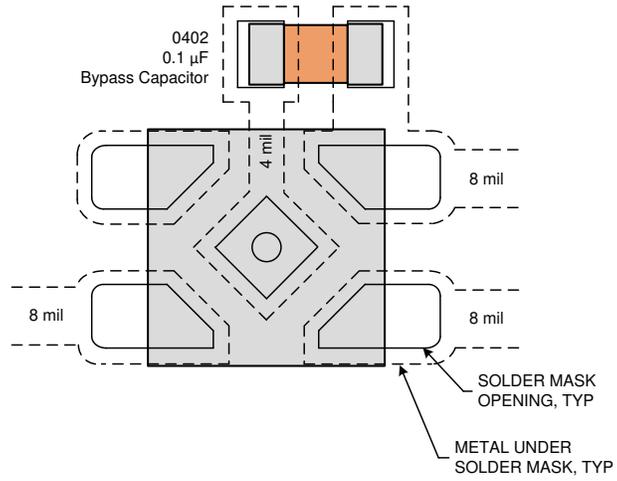


Figure 7-3. Example Layout With DPW (X2SON-5) Package

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Implications of Slow or Floating CMOS Inputs application note](#)

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

NanoFree™ and TI E2E™ are trademarks of Texas Instruments. All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Z (June 2025) to Revision AA (October 2025)	Page
• Changed Junction-to-ambient thermal resistance value for DCK package from: 276.1°C/W to: 371.0°C/W	6
• Changed Junction-to-case (top) thermal resistance value for DCK package from: 178.9°C/W to: 297.5°C/W..	6
• Changed Junction-to-board thermal resistance value for DCK package from: 70.9°C/W to: 258.6°C/W.....	6
• Changed Junction-to-top characterization value for DCK package from: 47.0°C/W to: 195.6°C/W.....	6
• Changed Junction-to-board characterization value for DCK package from: 69.3°C/W to: 256.2°C/W.....	6

Changes from Revision Y (November 2018) to Revision Z (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Changed <i>Device Information</i> table to <i>Package Information</i>	1
• Changed Junction-to-ambient thermal resistance value for DBV package from: 247.2°C/W to: 357.1°C/W	6
• Changed Junction-to-case (top) thermal resistance value for DBV package from: 154.5°C/W to: 263.7°C/W..	6
• Changed Junction-to-board thermal resistance value for DBV package from: 86.8°C/W to: 264.4°C/W.....	6
• Changed Junction-to-top characterization value for DBV package from: 58.0°C/W to: 195.6°C/W.....	6
• Changed Junction-to-board characterization value for DBV package from: 86.4°C/W to: 262.2°C/W.....	6

Changes from Revision X (August 2017) to Revision Y (November 2018)	Page
• Changed New package pinout added to Pin Functions table. Multiple Pin Functions tables condensed to one.....	3
• Changed T_j and T_{stg} lines switched for consistency with other devices.....	5
• Added differentiated ROC temperatures for DPW, YZP and YZV packages	6
• Changed format of Switching Characteristics tables to include columns for different C_L conditions	8
• Added temperature range to Conditions statement for Switching Characteristics tables	8
• Replaced PMI section with updated load circuit and relevant waveform figures. Collapsed parameter measurement values into one table.....	9

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G14DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C145, C14F, C14J, C14K, C14R) (C14H, C14S)
SN74LVC1G14DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C145, C14F, C14J, C14K, C14R) (C14H, C14S)
SN74LVC1G14DBVR.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(C145, C14F, C14J, C14K, C14R) (C14H, C14S)
SN74LVC1G14DBVRE4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F
SN74LVC1G14DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F
SN74LVC1G14DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F
SN74LVC1G14DBVRG4.B	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F
SN74LVC1G14DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C145, C14F, C14J, C14K, C14R) (C14H, C14S)
SN74LVC1G14DBVT.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(C145, C14F, C14J, C14K, C14R) (C14H, C14S)
SN74LVC1G14DBVTE4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F
SN74LVC1G14DBVTG4	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F
SN74LVC1G14DBVTG4.B	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14F
SN74LVC1G14DCKR	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CF5, CFF, CFJ, CFK, CFR, CFT) (CFH, CFS)
SN74LVC1G14DCKR.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CF5, CFF, CFJ, CFK, CFR, CFT) (CFH, CFS)
SN74LVC1G14DCKR.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CF5, CFF, CFJ, CFK, CFR, CFT) (CFH, CFS)
SN74LVC1G14DCKRE4	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC1G14DCKRG4.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS
SN74LVC1G14DCKRG4.B	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS
SN74LVC1G14DCKT	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(CF5, CFF, CFJ, CF K, CFR, CFT) (CFH, CFS)
SN74LVC1G14DCKT.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(CF5, CFF, CFJ, CF K, CFR, CFT) (CFH, CFS)
SN74LVC1G14DCKTE4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS
SN74LVC1G14DCKTG4	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS
SN74LVC1G14DCKTG4.B	Active	Production	SC70 (DCK) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF5 CFS
SN74LVC1G14DPWR	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9H
SN74LVC1G14DPWR.B	Active	Production	X2SON (DPW) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	9H
SN74LVC1G14DRLR	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CF7, CFR)
SN74LVC1G14DRLR.B	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CF7, CFR)
SN74LVC1G14DRLRG4	Active	Production	SOT-5X3 (DRL) 5	4000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(CF7, CFR)
SN74LVC1G14DRYR	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF
SN74LVC1G14DRYR.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF
SN74LVC1G14DRYRG4.B	Active	Production	SON (DRY) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF
SN74LVC1G14DSFR	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CF
SN74LVC1G14DSFR.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CF
SN74LVC1G14DSFRG4	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF
SN74LVC1G14DSFRG4.B	Active	Production	SON (DSF) 6	5000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CF
SN74LVC1G14YZPR	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CF7, CFN)
SN74LVC1G14YZPR.B	Active	Production	DSBGA (YZP) 5	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CF7, CFN)
SN74LVC1G14YZVR	Active	Production	DSBGA (YZV) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CF (7, N)
SN74LVC1G14YZVR.B	Active	Production	DSBGA (YZV) 4	3000 LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CF (7, N)

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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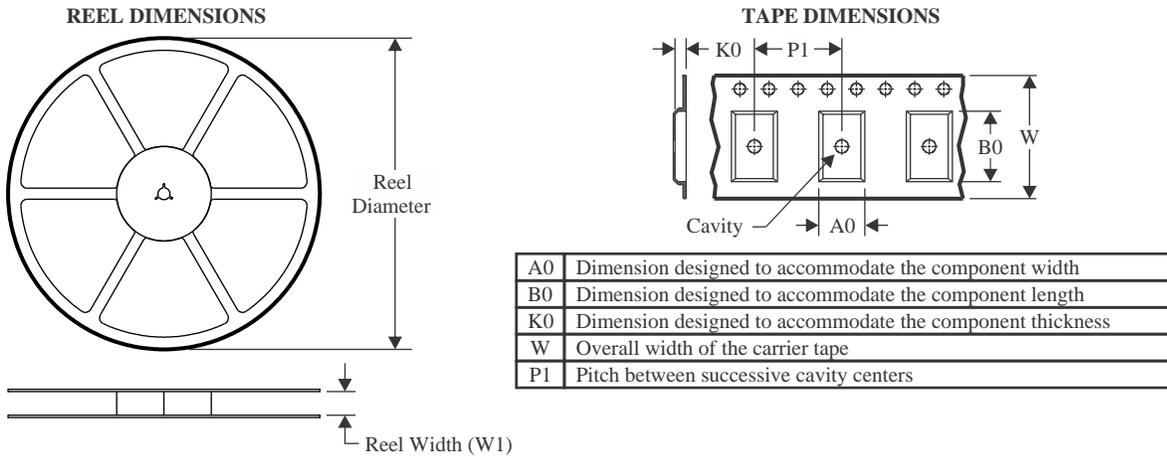
OTHER QUALIFIED VERSIONS OF SN74LVC1G14 :

- Automotive : [SN74LVC1G14-Q1](#)
- Enhanced Product : [SN74LVC1G14-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G14DBVR	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LVC1G14DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G14DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G14DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G14DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74LVC1G14DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G14DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G14DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G14DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G14DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G14DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G14DSFRG4	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G14YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G14YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

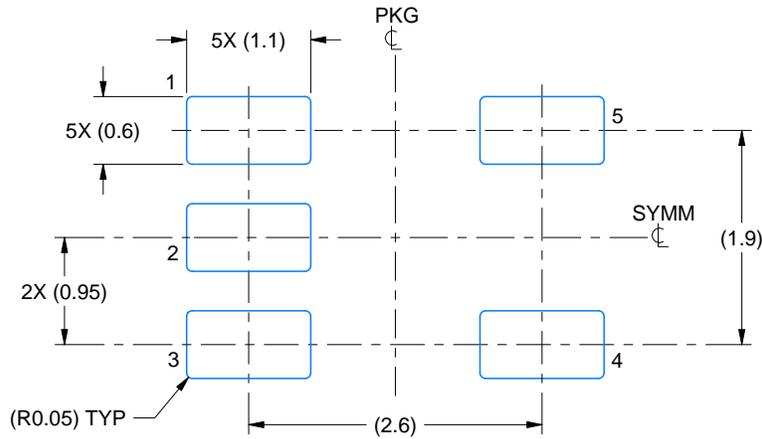
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G14DBVR	SOT-23	DBV	5	3000	208.0	191.0	35.0
SN74LVC1G14DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G14DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G14DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G14DCKR	SC70	DCK	5	3000	208.0	191.0	35.0
SN74LVC1G14DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G14DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G14DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G14DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G14DRYR	SON	DRY	6	5000	189.0	185.0	36.0
SN74LVC1G14DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G14DSFRG4	SON	DSF	6	5000	184.0	184.0	19.0
SN74LVC1G14YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G14YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRY 6

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

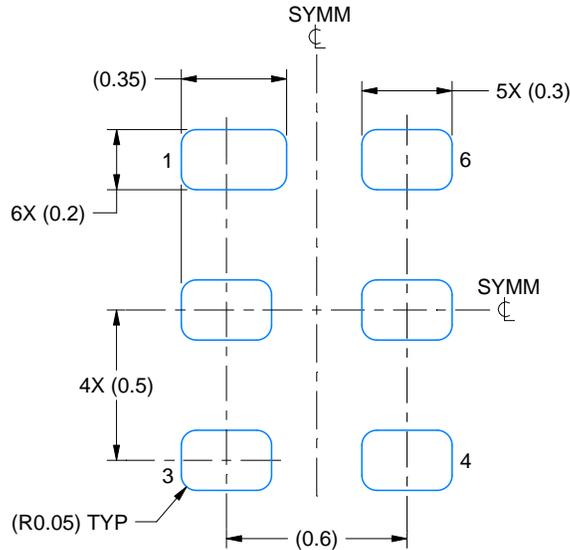
4207181/G

EXAMPLE BOARD LAYOUT

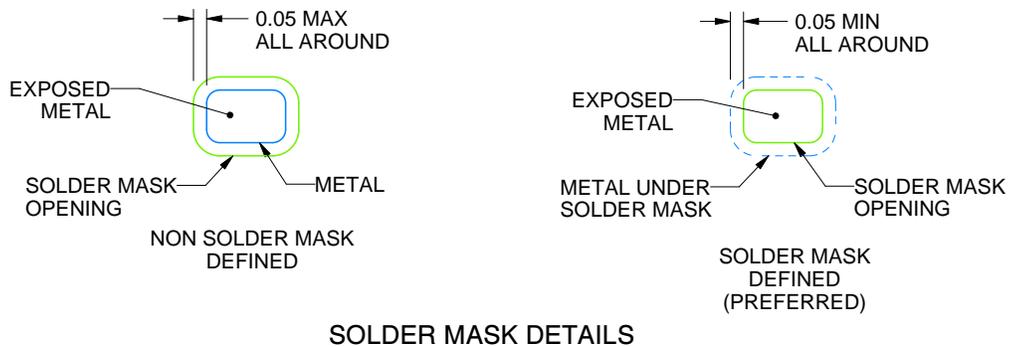
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

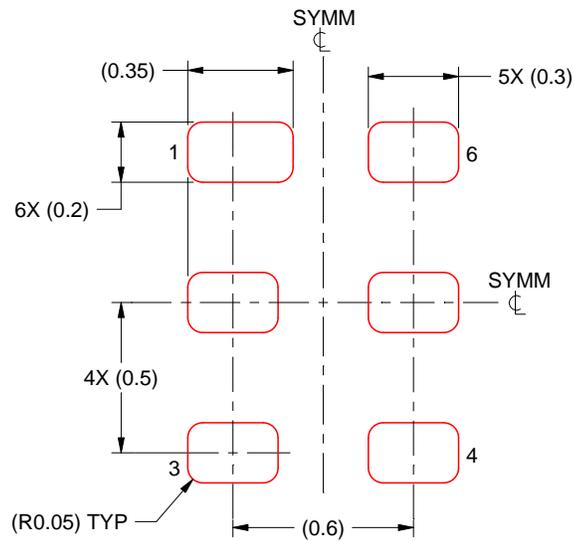
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

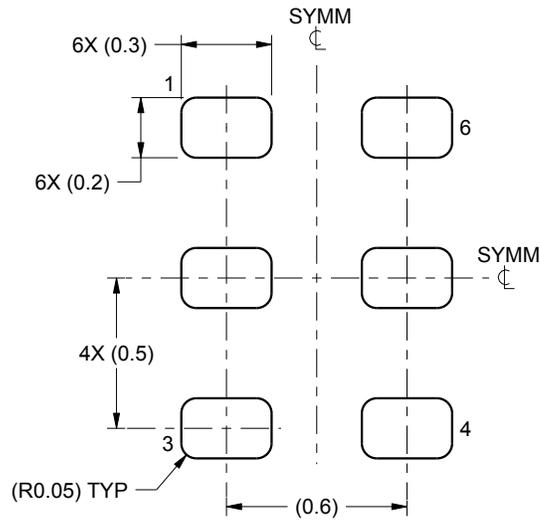
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

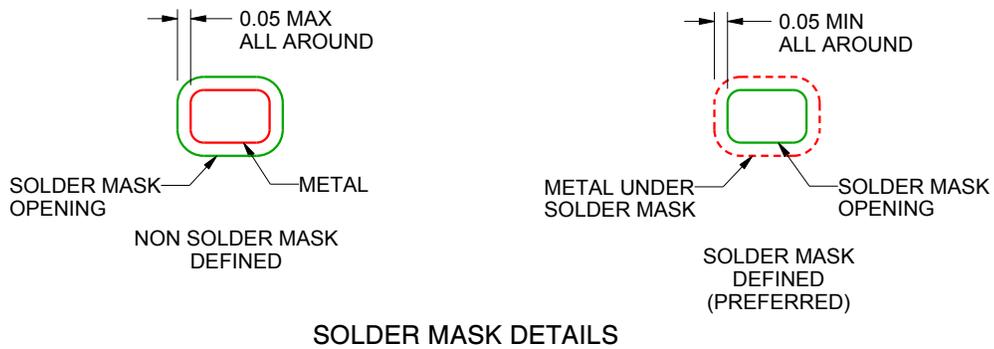
DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

4222207/B 02/2016

NOTES: (continued)

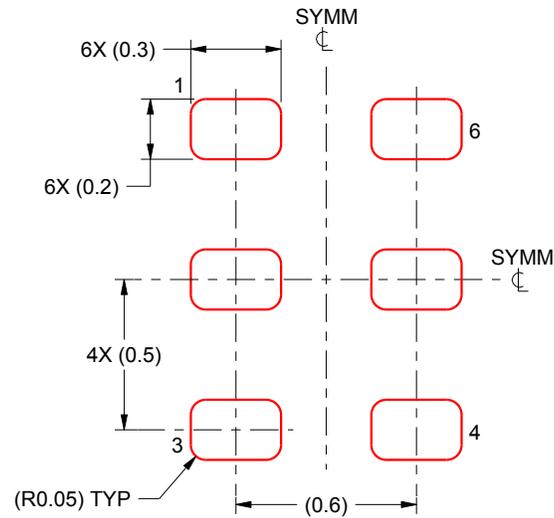
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

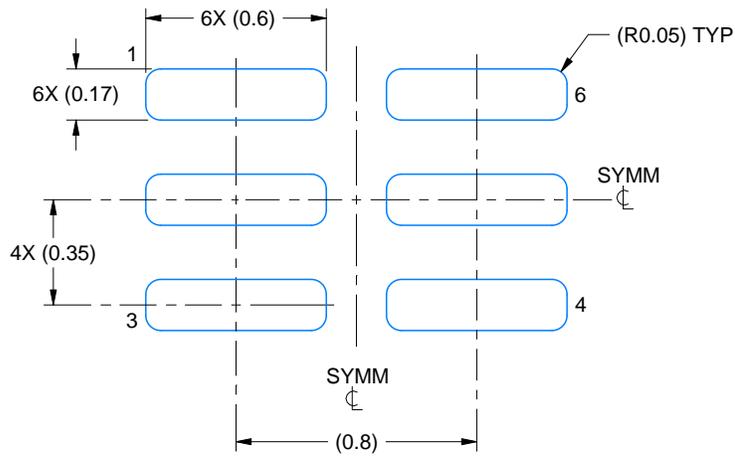
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

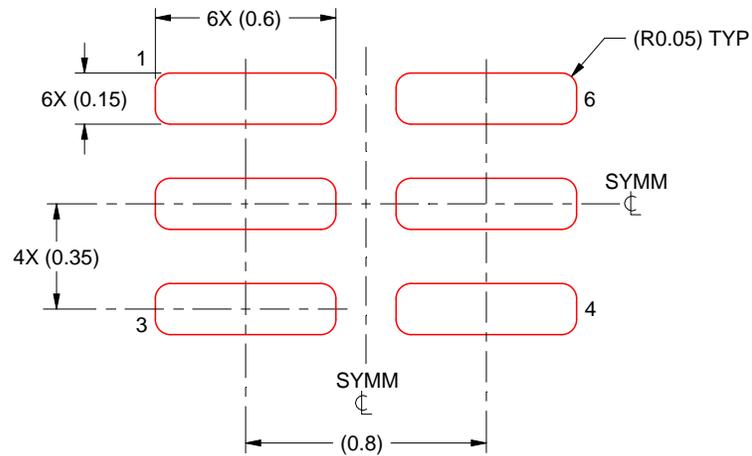
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

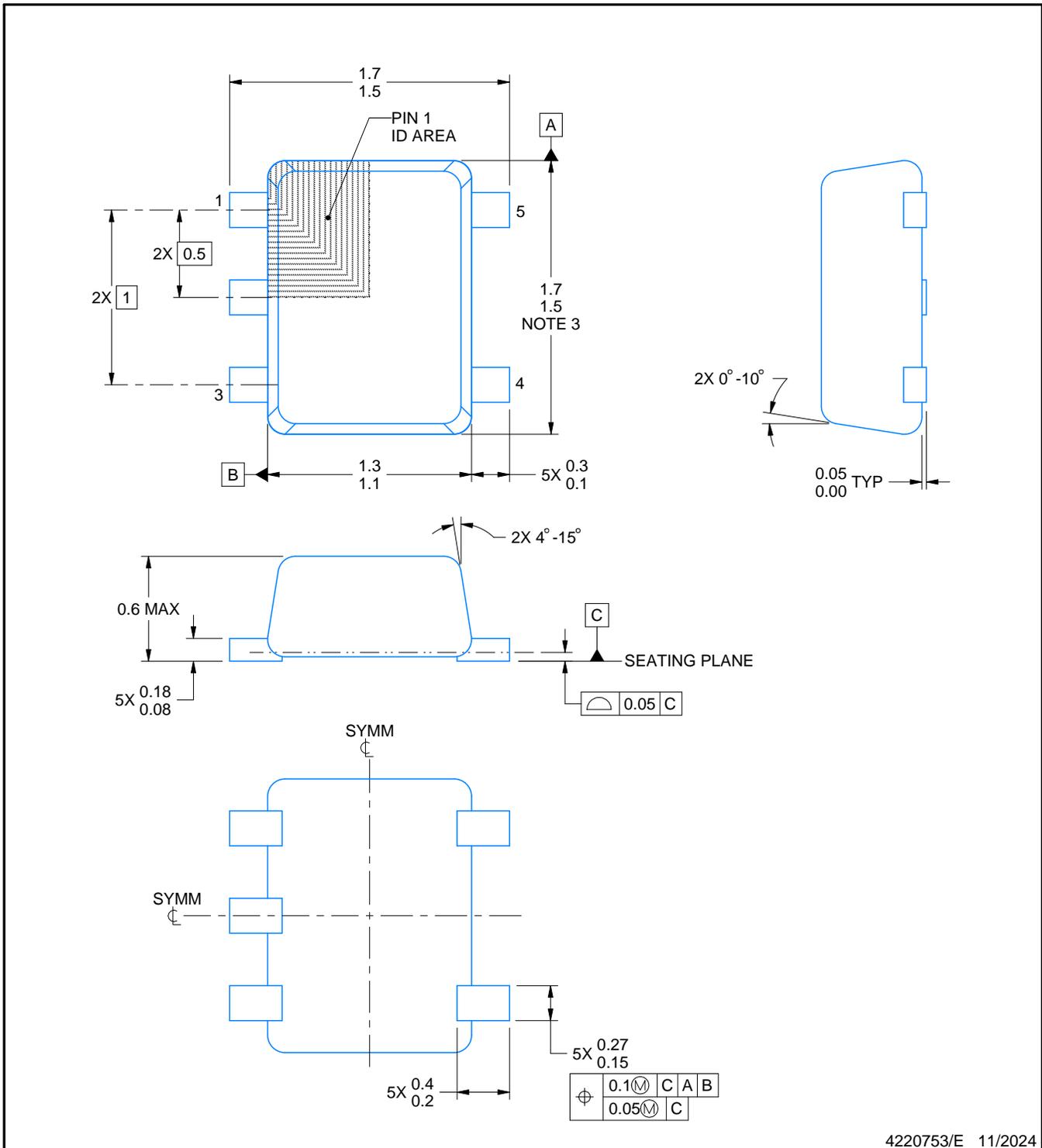
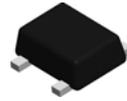


SOLDER PASTE EXAMPLE
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220753/E 11/2024

NOTES:

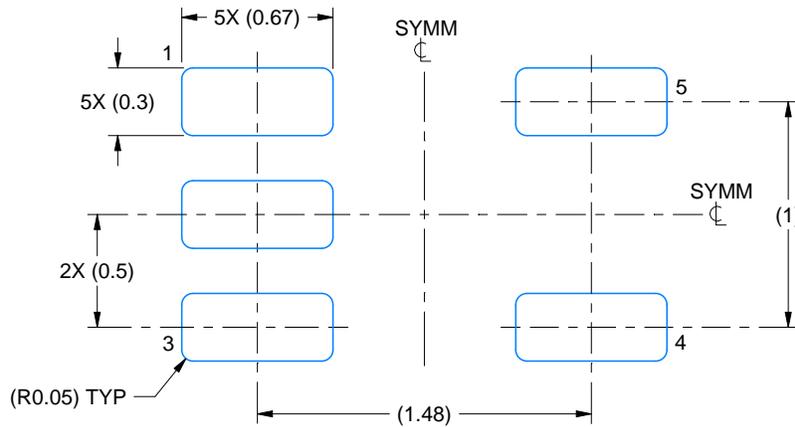
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

EXAMPLE BOARD LAYOUT

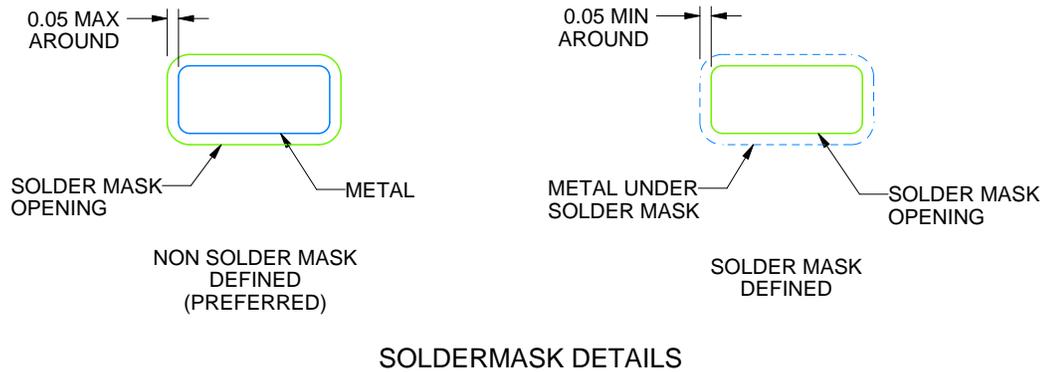
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4220753/E 11/2024

NOTES: (continued)

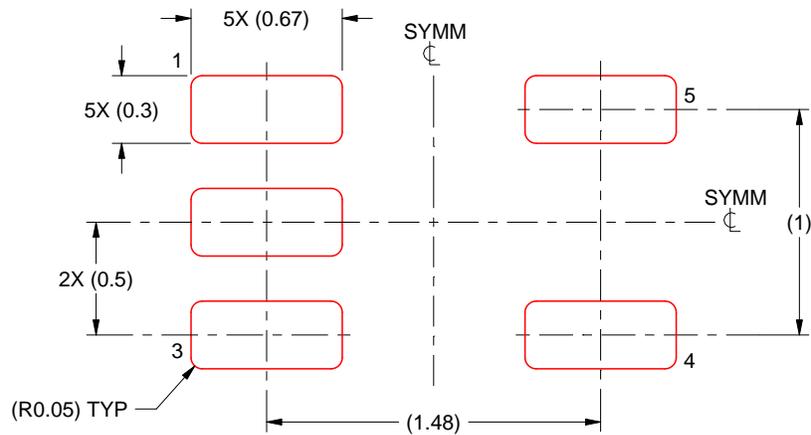
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4220753/E 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

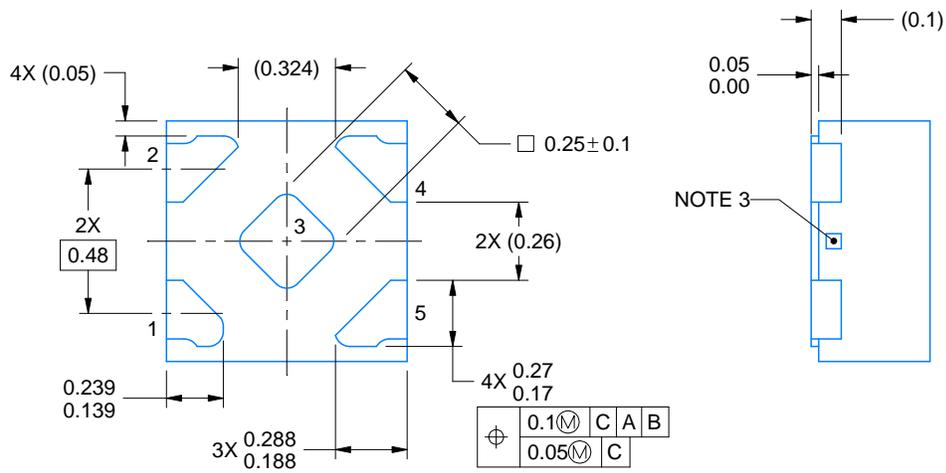
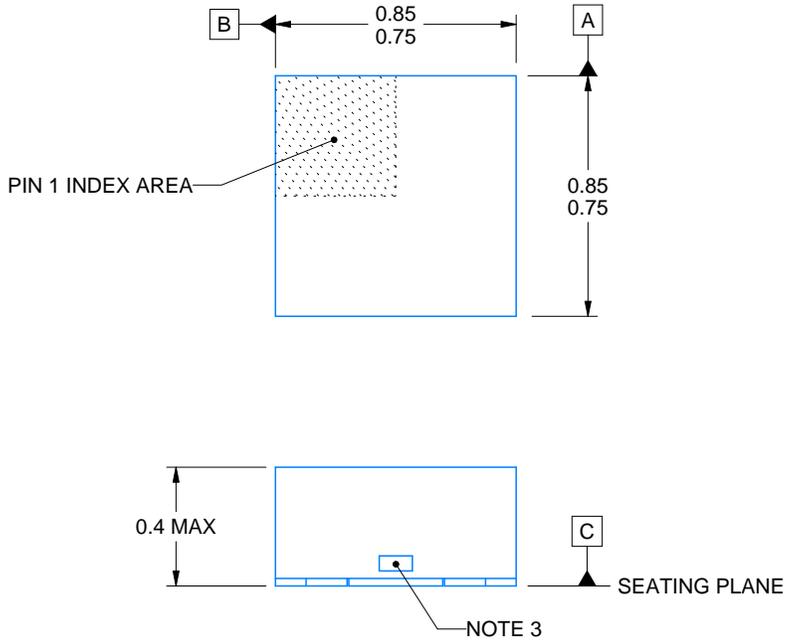
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

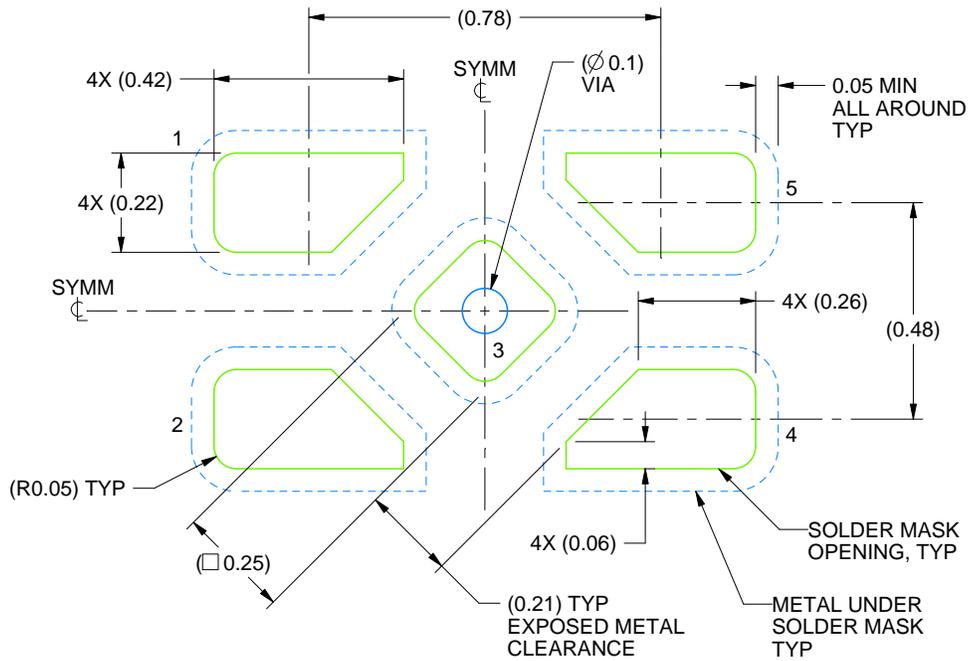
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

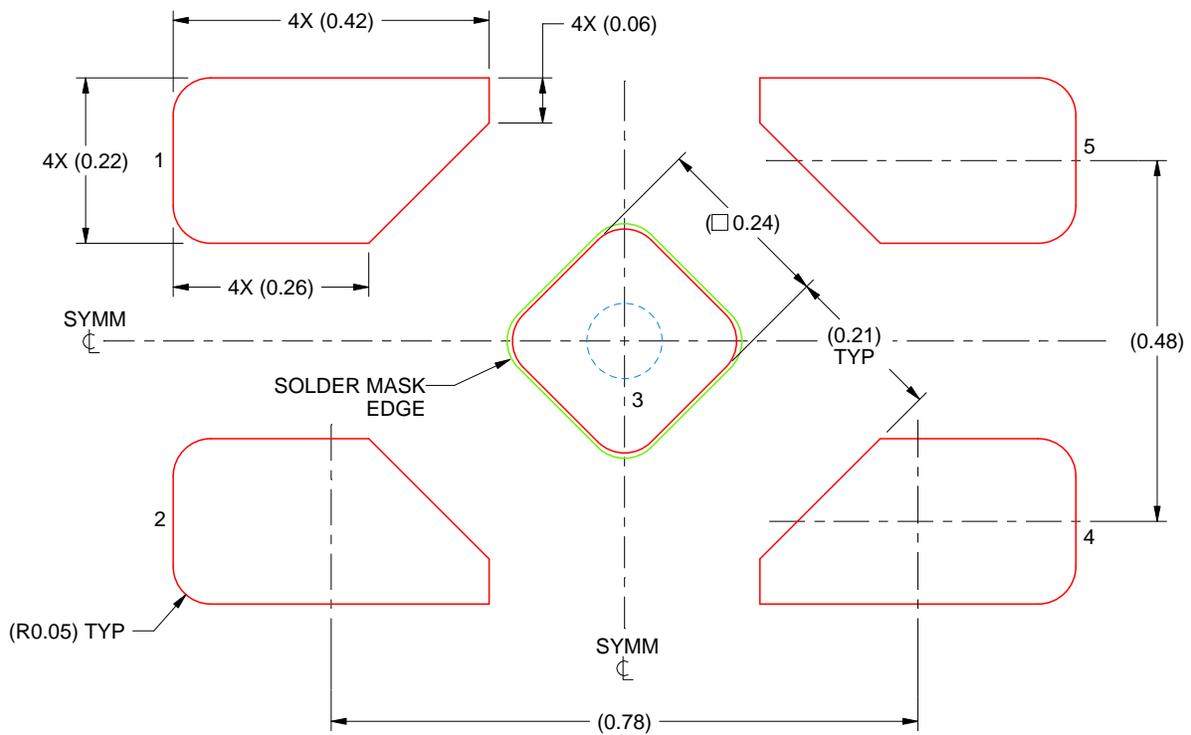
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

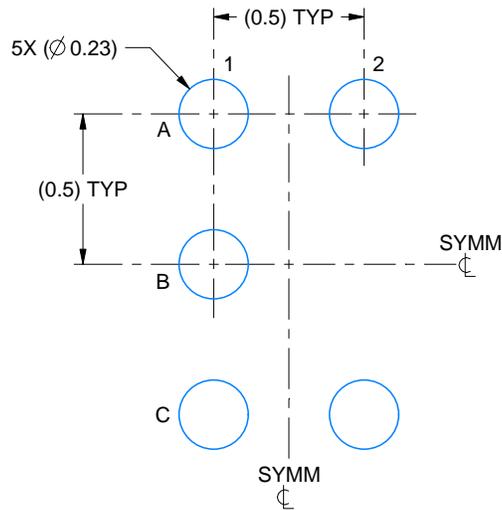
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

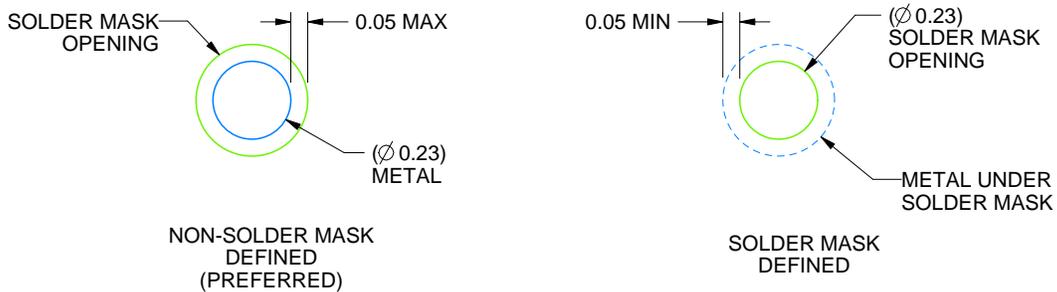
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

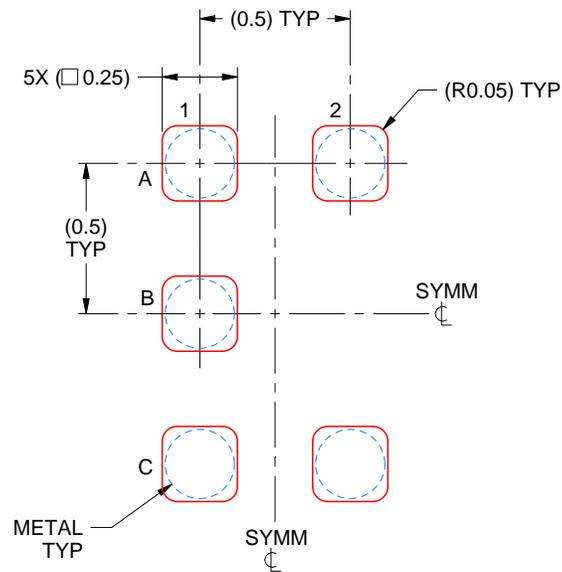
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

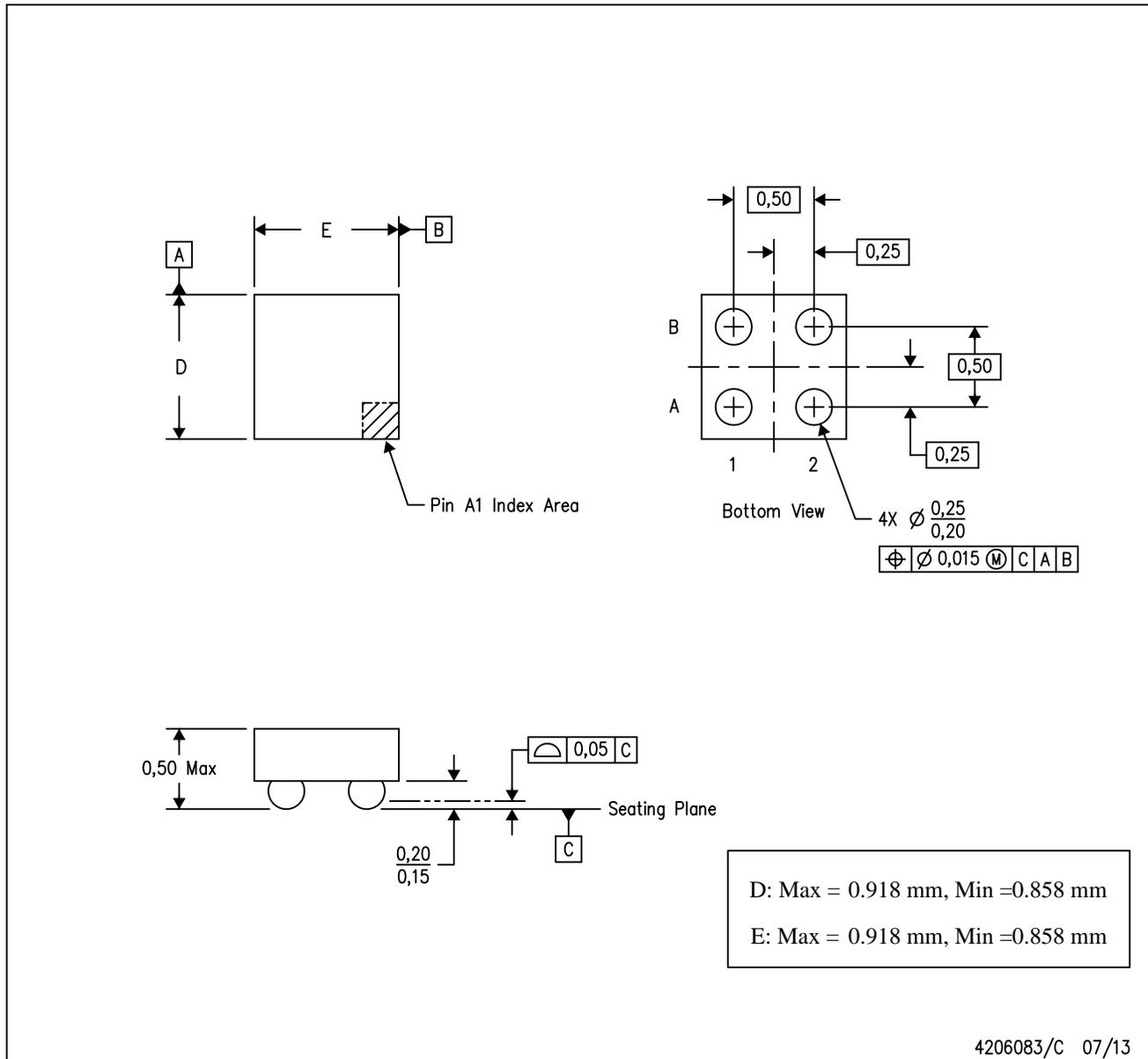
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

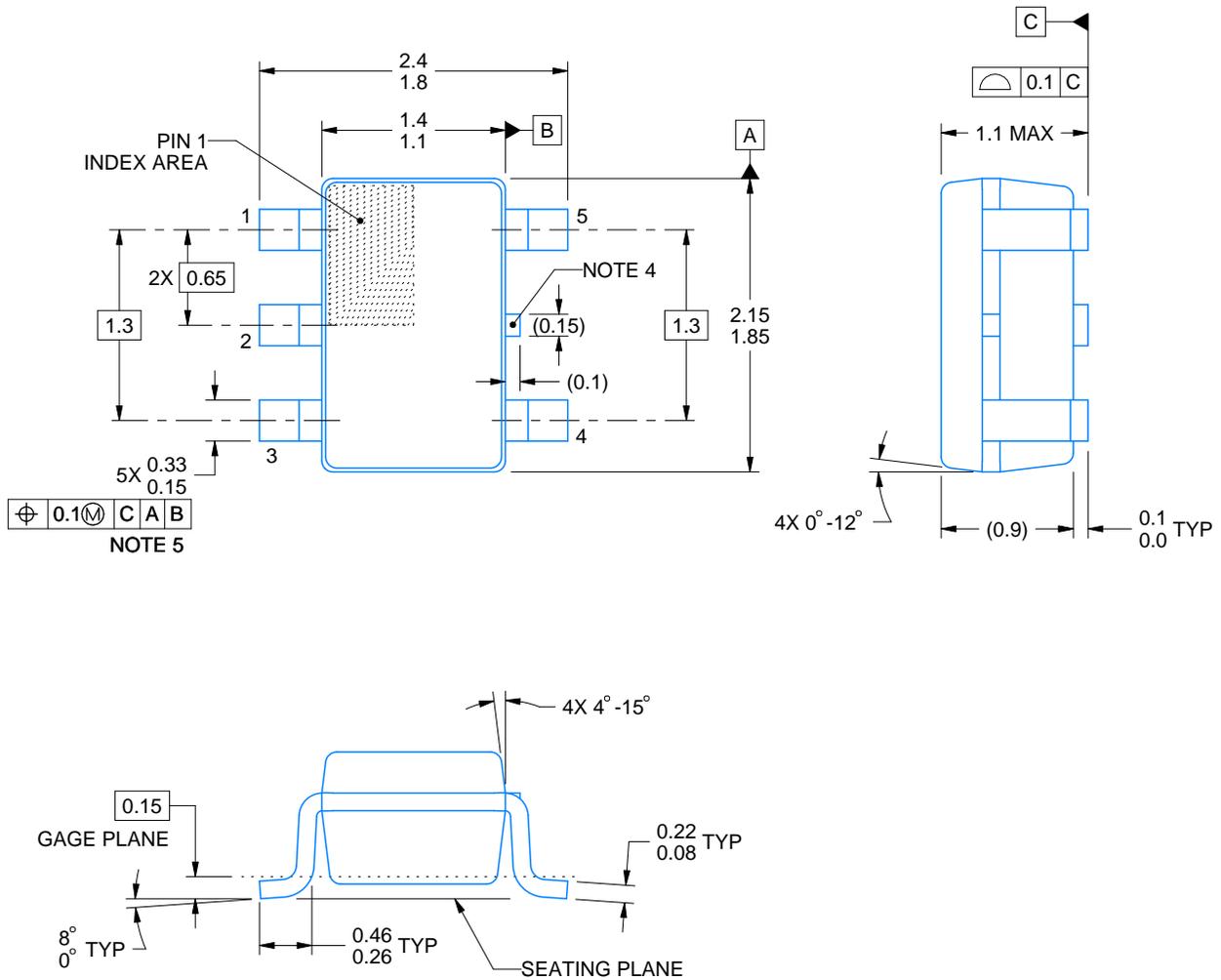
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

NOTES:

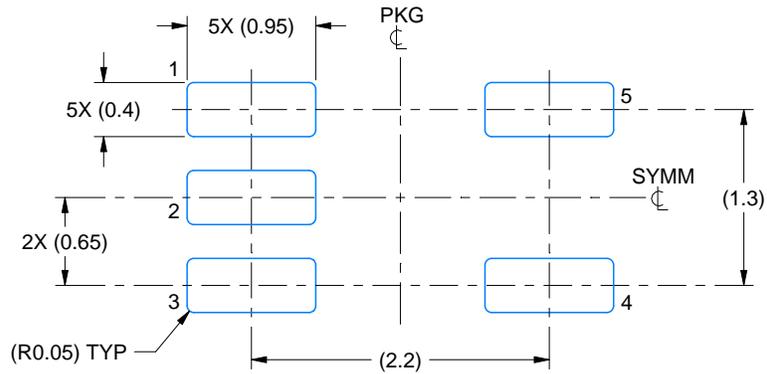
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

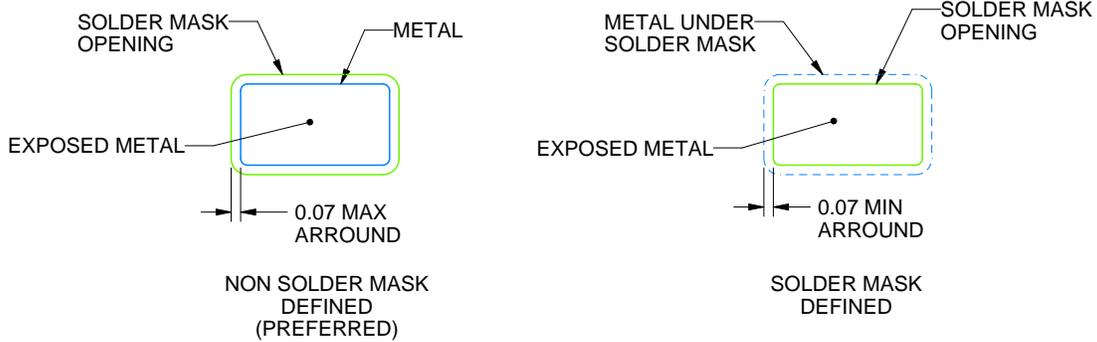
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

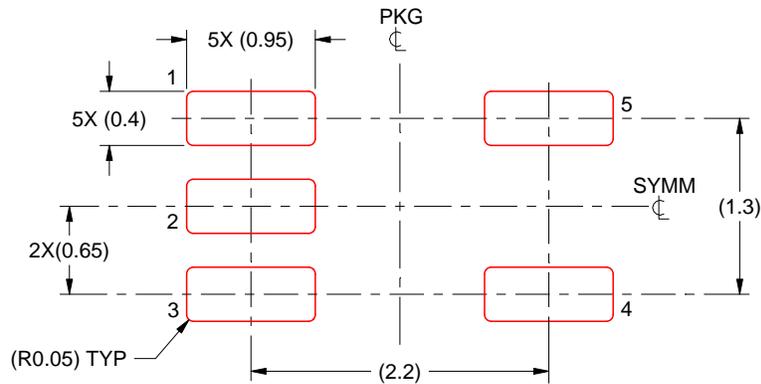
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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