

- Designed for Digital Data Transmission Over 50-Ω to 500-Ω Coaxial Cable, Strip Line, or Twisted Pair
- High Speed
 $t_{pd} = 20$ ns Maximum at $C_L = 15$ pF
- TTL Compatible With Single 5-V Supply
- 2.4-V Output at $I_{OH} = -75$ mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration
- Designed for Use With Triple Line Receivers SN55122, SN75122
- Designed to Be Interchangeable With Signetics N8T13

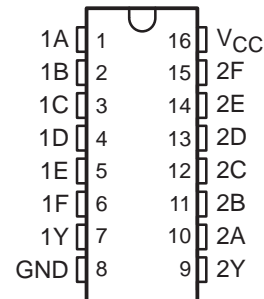
description

The SN55121 and SN75121 dual line drivers are designed for digital data transmission over lines having impedances from 50 to 500 Ω. They are also compatible with standard TTL logic and supply-voltage levels.

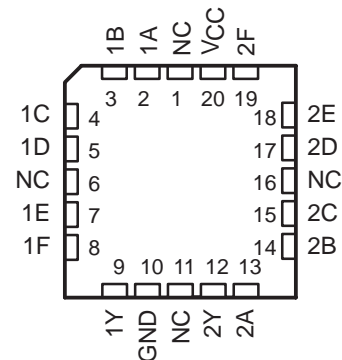
The low-impedance emitter-follower outputs of the SN55121 and SN75121 can drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 1.5 V. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN55121 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75121 is characterized for operation from 0°C to 70°C .

SN55121 . . . J PACKAGE
SN75121 . . . D OR N PACKAGE
(TOP VIEW)



SN55121 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

**THE SN75121 IS NOT
RECOMMENDED FOR NEW DESIGNS**



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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SN55121, SN75121 DUAL LINE DRIVERS

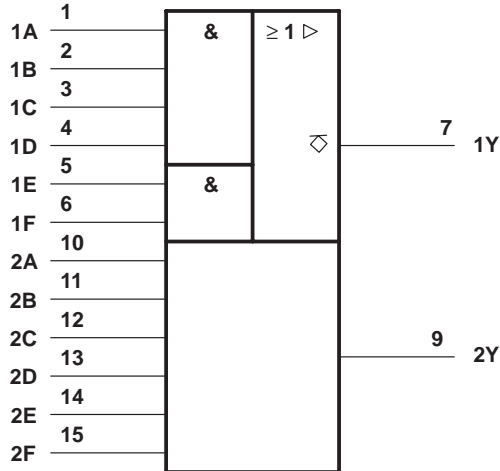
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FUNCTION TABLE

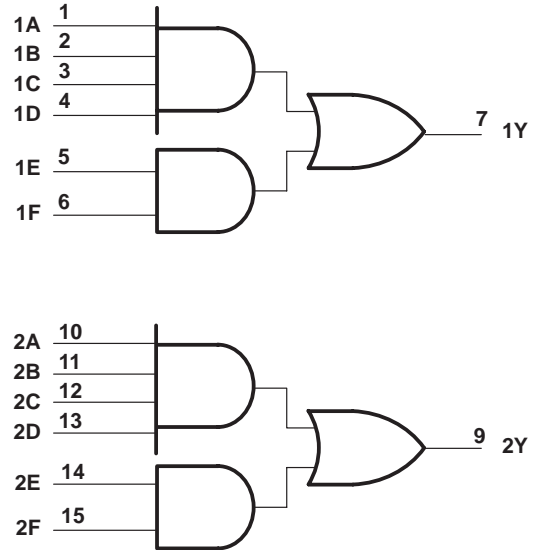
INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

H = high level, L = low level, X = irrelevant

logic symbol†

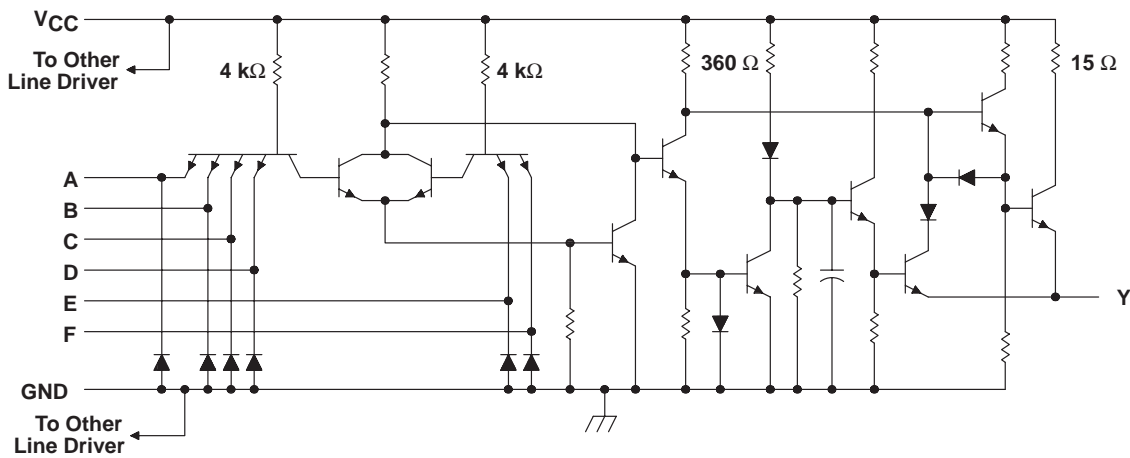


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

schematic (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	6 V
Input voltage	6 V
Output voltage	6 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to both ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—

‡ In the FK and J packages, SN55121 chips are either silver glass or alloy mounted.

recommended operating conditions

	SN55121			SN75121			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
High-level output current, I_{OH}			–75			–75	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{IK}	Input clamp voltage	$V_{CC} = 5\text{ V}$,	$I_I = -12\text{ mA}$		-1.5	V
$V_{(BR)}$	Breakdown voltage	$V_{CC} = 5\text{ V}$,	$I_I = 10\text{ mA}$	5.5		V
V_{OH}	High-level output voltage	$V_{IH} = 2\text{ V}$,	$I_{OH} = -75\text{ mA}$, See Note 2	2.4		V
I_{OH}	High-level output current	$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$,	$V_{IH} = 4.5\text{ V}$, See Note 2	-100	-250	mA
I_{OL}	Low-level output current	$V_{IL} = 0.8\text{ V}$,	$V_{OL} = 0.4\text{ V}$, See Note 2	-800		μA
$I_{O(off)}$	Off-state output current	$V_{CC} = 3\text{ V}$,	$V_O = 3\text{ V}$		500	μA
I_{IH}	High-level output current	$V_I = 4.5\text{ V}$			40	μA
I_{IL}	Low-level output current	$V_I = 0.4\text{ V}$		-0.1	-1.6	mA
I_{OS}	Short-circuit output current [†]	$V_{CC} = 5\text{ V}$,	$T_A = 25^\circ\text{C}$		-30	mA
I_{CCH}	Supply current, outputs high	$V_{CC} = 5.25\text{ V}$,	All inputs at 2 V, Outputs open		28	mA
I_{CCL}	Supply current, outputs low	$V_{CC} = 5.25\text{ V}$,	All inputs at 0.8 V, Outputs open		60	mA

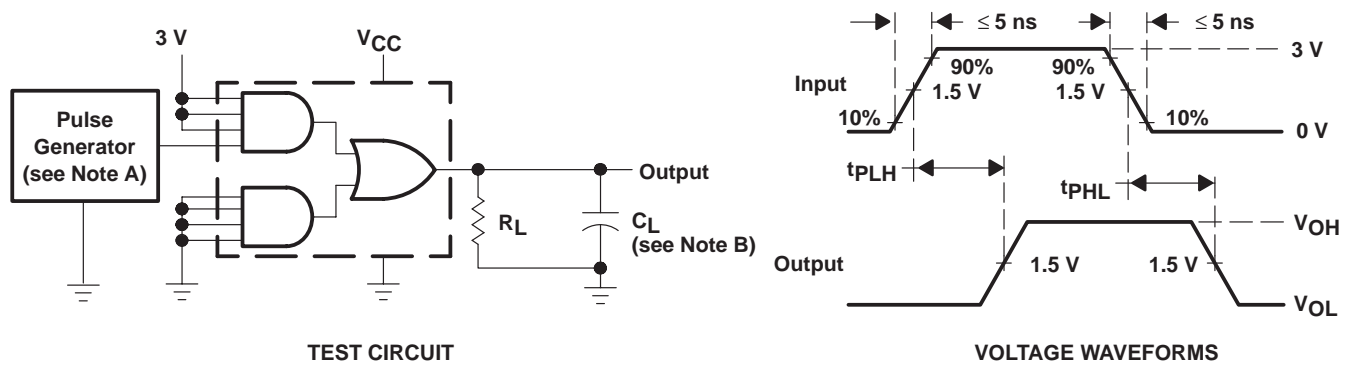
[†] Not more than one output should be shorted at a time.

NOTE 2: The output voltage and current limits are valid for any appropriate combination of high and low inputs specified by the function table for the desired output.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	$R_L = 37\ \Omega$, $C_L = 15\text{ pF}$, See Figure 1			11	20	ns
t_{PHL}	Propagation delay time, high-to-low level output				8	20	
t_{PLH}	Propagation delay time, low-to-high level output	$R_L = 37\ \Omega$, $C_L = 1000\text{ pF}$, See Figure 1			22	50	ns
t_{PHL}	Propagation delay time, high-to-low level output				20	50	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, $t_w = 200\text{ ns}$, duty cycle $\leq 50\%$, PRR $\leq 500\text{ kHz}$.
B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE

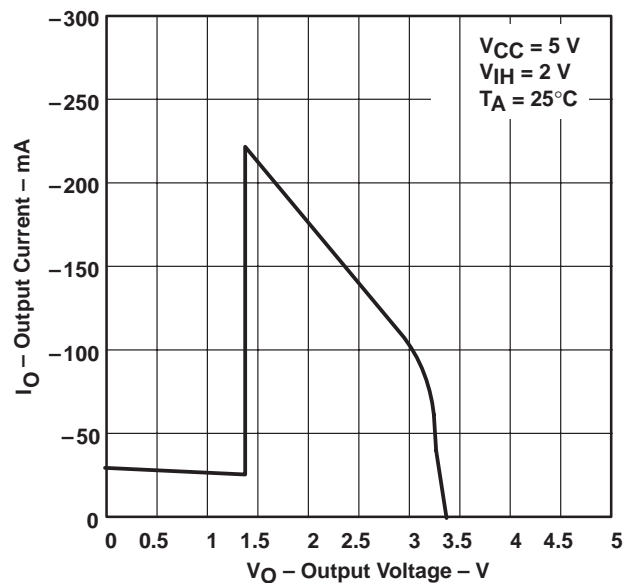


Figure 2

SN55121, SN75121 DUAL LINE DRIVERS

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APPLICATION INFORMATION

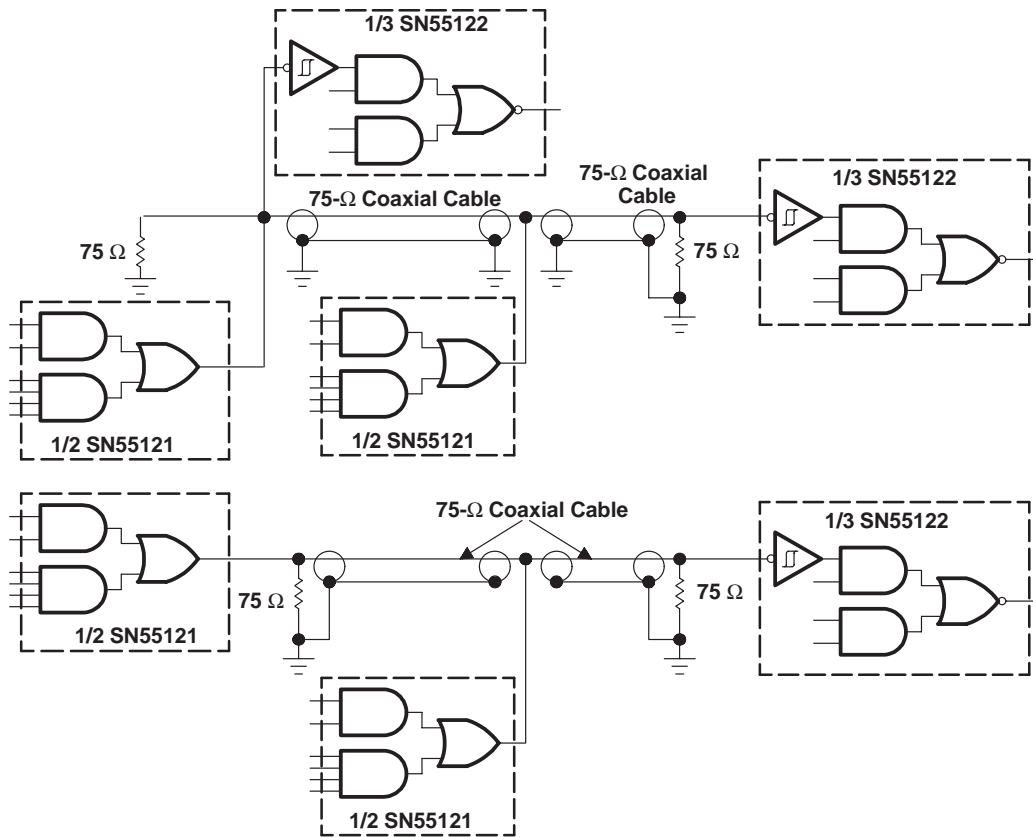


Figure 3. Single-Ended Party-Line Circuits

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75121N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75121N	Samples
SN75121NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75121	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75121NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75121NSR	SO	NS	16	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75121N	N	PDIP	16	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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