TEXAS INSTRUMENTS

SN75174
SLLS039C – OCTOBER 1980 – REVISED APRIL 2024

SN75174 Quadruple Differential Line Driver

1 Features

- Meets or exceeds the requirements of ANSI standards EIA/TIA-422-B and RS-485 and ITU recommendation V.11.
- Designed for multipoint transmission on long bus lines in noisy environments
- 3-state outputs
- Common-mode output voltage range of –7V to 12V
- Active-high enable
- Thermal shutdown protection
- Positive- and negative-current limiting
- Operates from single 5V supply
- Low power requirements
- Functionally interchangeable with MC3487

2 Applications

- Chemical and gas sensors
- Field transmitters: temperature sensors and pressure sensors
- Motor drives: brushless DC and brushed DC
- Temperature sensors and controllers using modbus

3 Description

The SN75174 is a monolithic quadruple differential line driver with 3-state outputs. It is designed to meet

the requirements of ANSI Standards EIA/TIA-422-B and RS-485 and ITU Recommendation V.11. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabaud. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75174 is characterized for operation from 0°C to 70°C.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
SN75174	N (PDIP, 16)	19.3mm × 9.4mm
	DW (SOIC, 20)	12.8mm × 10.3mm

(1) For more information, see Section 11.
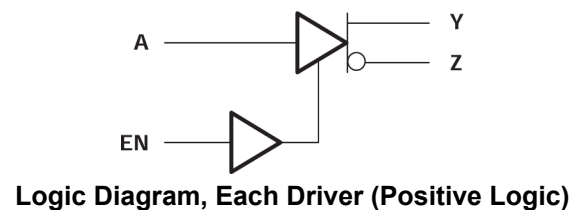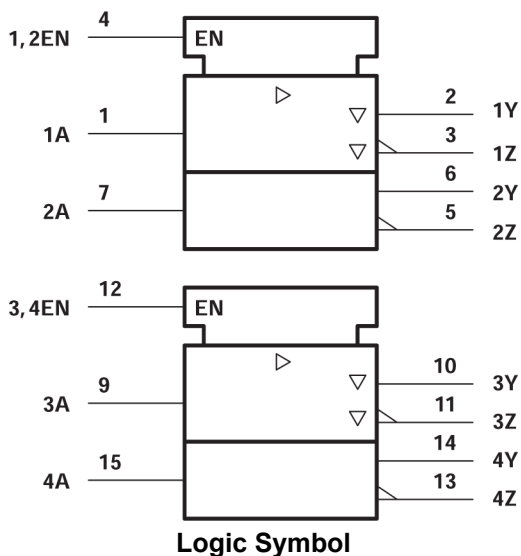(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Logic Symbol

Logic Diagram, Each Driver (Positive Logic)

Table of Contents

Product Folder Links: *SN75174*

4 Pin Configuration and Functions

```
          ___
    1A  1 |   U  16 | V_CC
    1Y  2 |        15 | 4A
    1Z  3 |        14 | 4Y
 1,2EN  4 |        13 | 4Z
    2Z  5 |        12 | 3,4EN
    2Y  6 |        11 | 3Z
    2A  7 |        10 | 3Y
   GND  8 |         9 | 3A
```

Figure 4-1. N Package (Top View)

```
          ___
    1A  1 |   U  20 | V_CC
    1Y  2 |        19 | 4A
    NC  3 |        18 | 4Y
    1Z  4 |        17 | NC
 1,2EN  5 |        16 | 4Z
    2Z  6 |        15 | 3,4EN
    NC  7 |        14 | 3Z
    2Y  8 |        13 | NC
    2A  9 |        12 | 3Y
   GND 10 |        11 | 3A
```

Figure 4-2. DW Package (Top View)

Product Folder Links: SN75174

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC} (see [2])	Supply voltage	-0.3	7	V
V_O	Output voltage range	−10	15	V
V_I	Input voltage	-0.3	5.5	V
P_D	Continuous total dissipation	See *Dissipation Rating* table		
T_A	Operating free-air temperature range	0	70	°C
T_{Lead}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C
T_{stg}	Storage temperature range	−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

5.2 Dissipation Rating

PACKAGE	$T_A \leq 25$°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	$T_A = 70$°C POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW
N	1150 mW	9.2 mW/°C	736 mW

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Common-mode output voltage, V_{OC}	−7		12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

Product Folder Links: *SN75174*

5.4 Thermal Information

THERMAL METRIC[1]		N (PDIP)	DW	UNIT
		16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [1]	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	$V_{IH} = 2V$, $I_{OH} = -33$mA	$V_{IL} = 0.8V$,		3.7		V
V_{OL}	Low-level output voltage	$V_{IH} = 2V$, $I_{OL} = 33$mA	$V_{IL} = 0.8V$,		1.1		V
V_O	Output voltage	$I_O = 0$		0		6	V
$|V_{OD1}|$	Differential output voltage	$I_O = 0$		1.5	6	6	V
$|V_{OD2}|$	Differential output voltage	$R_L = 100Ω$,	See Figure 6-1	1/2 V_{OD1} or 2 [2]			V
		$R_L = 54Ω$,	See Figure 6-1	1.5	2.5	5	V
V_{OD3}	Differential output voltage	See [5]		1.5		5	V
$Δ|V_{OD}|$	Change in magnitude of differential output voltage[3]					±0.2	V
V_{OC}	Common-mode output voltage[4]	$R_L = 54Ω$ or $100Ω$,	See Figure 6-1	-1		3	V
$Δ|V_{OC}|$	Change in magnitude of common-mode output voltage[3]					±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7V$ to 12V			±100	µA
I_{OZ}	High-impedance-state output current	$V_O = -7V$ to 12V				±100	µA
I_{IH}	High-level input current	$V_I = 2.7V$				20	µA
I_{IL}	Low-level input current	$V_I = 0.5V$				±360	µA
I_{OS}	Short-circuit output current	$V_O = ±7V$				±180	
		$V_O = V_{CC}$				180	mA
		$V_O = 12V$				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

(1)   All typical values are at $V_{CC} = 5V$ and $T_A = 25°C$.
(2)   The minimum V_{OD2} with a 100Ω load is either 1/2 V_{OD1} or 2V, whichever is greater.
(3) $Δ|V_{OD}|$ and $Δ|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4)   In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5)   See EIA Standard RS-485.

5.6 Switching Characteristics

$V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$R_L = 54Ω$,	See Figure 6-2		45	65	ns
$t_{t(OD)}$	Differential-output transition time				80	120	ns
t_{PZH}	Output enable time to high level	$R_L = 110Ω$,	See Figure 6-3		80	120	ns
t_{PZL}	Output enable time to low level	$R_L = 110Ω$,	See Figure 6-4		55	80	ns
t_{PHZ}	Output disable time from high level	$R_L = 110Ω$,	See Figure 6-3		75	115	ns
t_{PLZ}	Output disable time from low level	$R_L = 110Ω$,	See Figure 6-3		18	30	ns

5.7 Symbol Equivalents

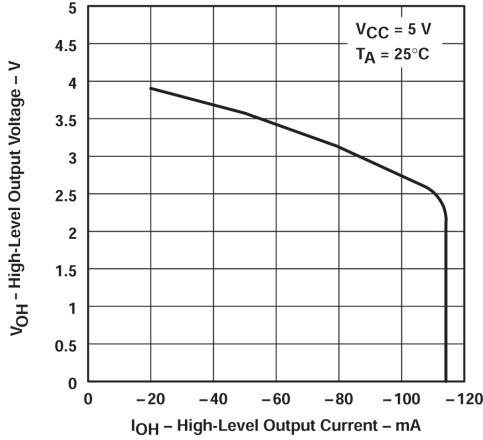| DATA SHEET PARAMETER	EIA/TIA-422-B	RS-485
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$|V_{OD1}|$	V_o	V_o
$|V_{OD2}|$	V_t (R_L = 100 Ω)	V_t (R_L = 54 Ω)
$|V_{OD3}|$		V_t (Test Termination Measurement 2)
$\Delta|V_{OD}|$	$||V_t| - |\overline{V}_t||$	$||V_t| - |\overline{V}_t||$
V_{OC}	$|V_{os}|$	$|V_{os}|$
$\Delta|V_{OC}|$	$|V_{os} - \overline{V}_{os}|$	$|V_{os} - \overline{V}_{os}|$
I_{OS}	$|I_{sa}|, |I_{sb}|$	
I_O	$|I_{xa}|, |I_{xb}|$	I_{ia}, I_{ib}

5.8 Typical Characteristics

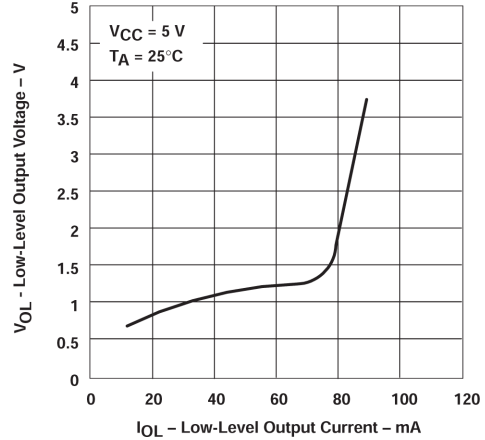**Figure 5-1. High-level Output Voltage vs High-level Output Current**

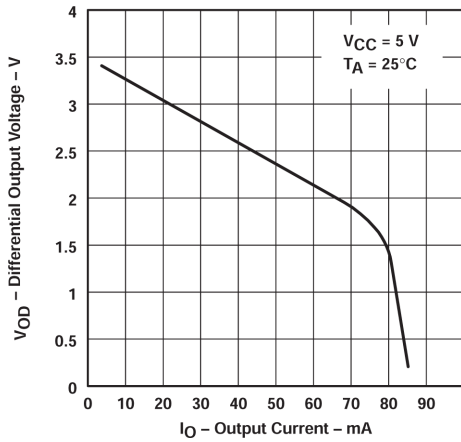**Figure 5-2. Low-level Output Voltage vs Low-level Output Current**

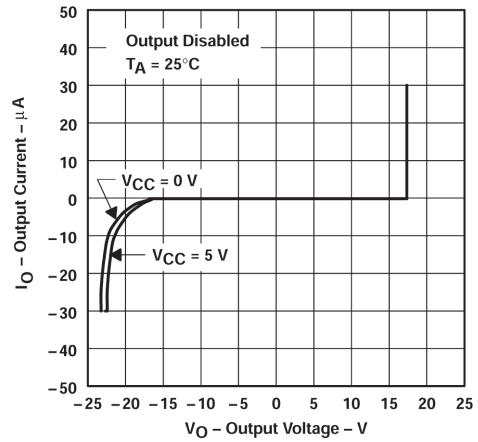**Figure 5-3. Differential Output Voltage vs Output Current**
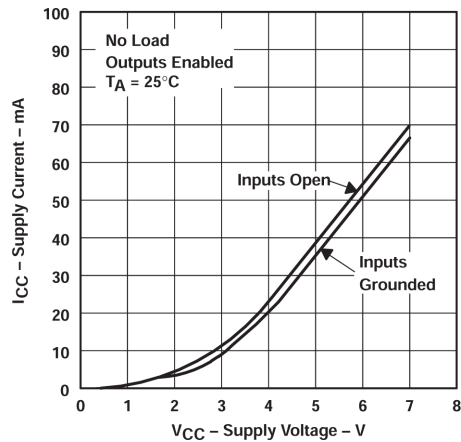

Figure 5-4. Output Current vs Output Voltage

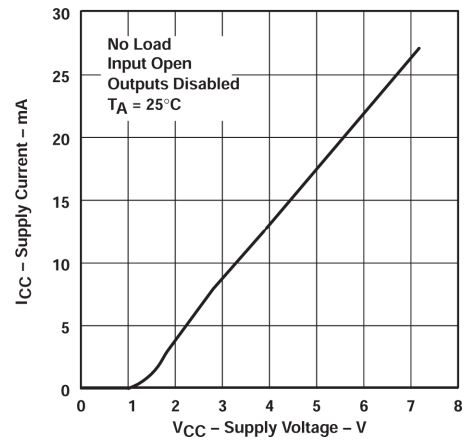**Figure 5-5. Supply Current vs Supply Voltage**

Figure 5-6. Supply Current vs Supply Voltage

6 Parameter Measurement Information
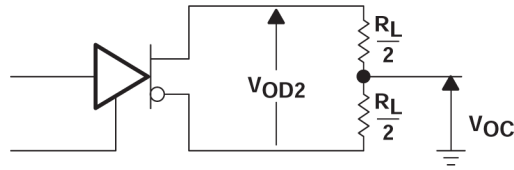
Figure 6-1. Differential and Common-Mode Output Voltages

TEST CIRCUIT
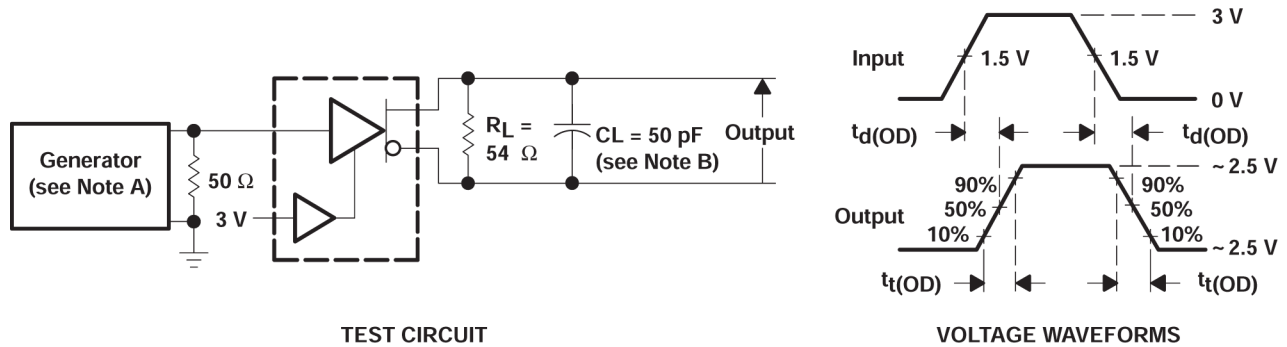
VOLTAGE WAVEFORMS

A.   The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5ns$, $t_f \leq 5$ ns, PRR ≤ 1MHz, duty cycle = 50%, $Z_O = 50Ω$.

B. C_L includes probe and stray capacitance.

Figure 6-2. Differential-Output Test Circuit and Voltage Waveforms
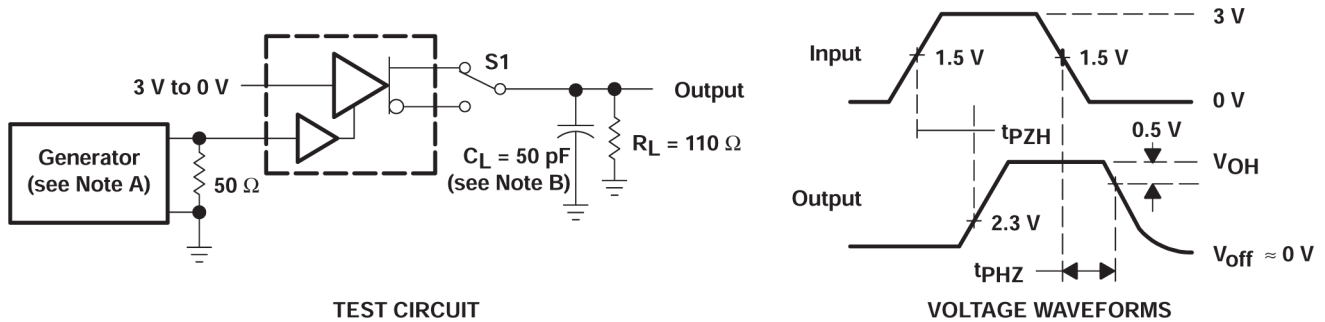
TEST CIRCUIT
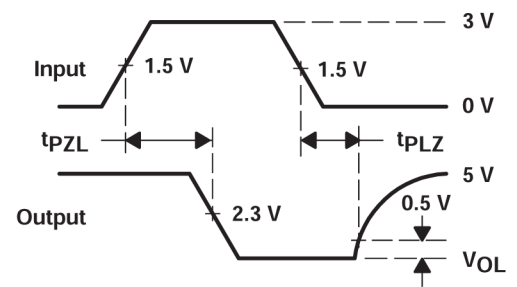
VOLTAGE WAVEFORMS

A.   The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle = 50%, $t_r \leq 10ns$, $t_f \leq 10ns$, $Z_O = 50Ω$.

B. C_L includes probe and stray capacitance.

Figure 6-3. Test Circuit and Voltage Waveforms

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle = 50%, t_r ≤ 5ns, t_f ≤ 5ns, Z_O = 50Ω.

B. C_L includes probe and stray capacitance.

Figure 6-4. Test Circuit and Voltage Waveforms

Product Folder Links: *SN75174*

7 Detailed Description

7.1 Device Functional Modes

Table 7-1. Function Table (Each Driver)

INPUT[1]	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1)   H = TTL high level, X = irrelevant, L = TTL low level, Z = high impedance (off)
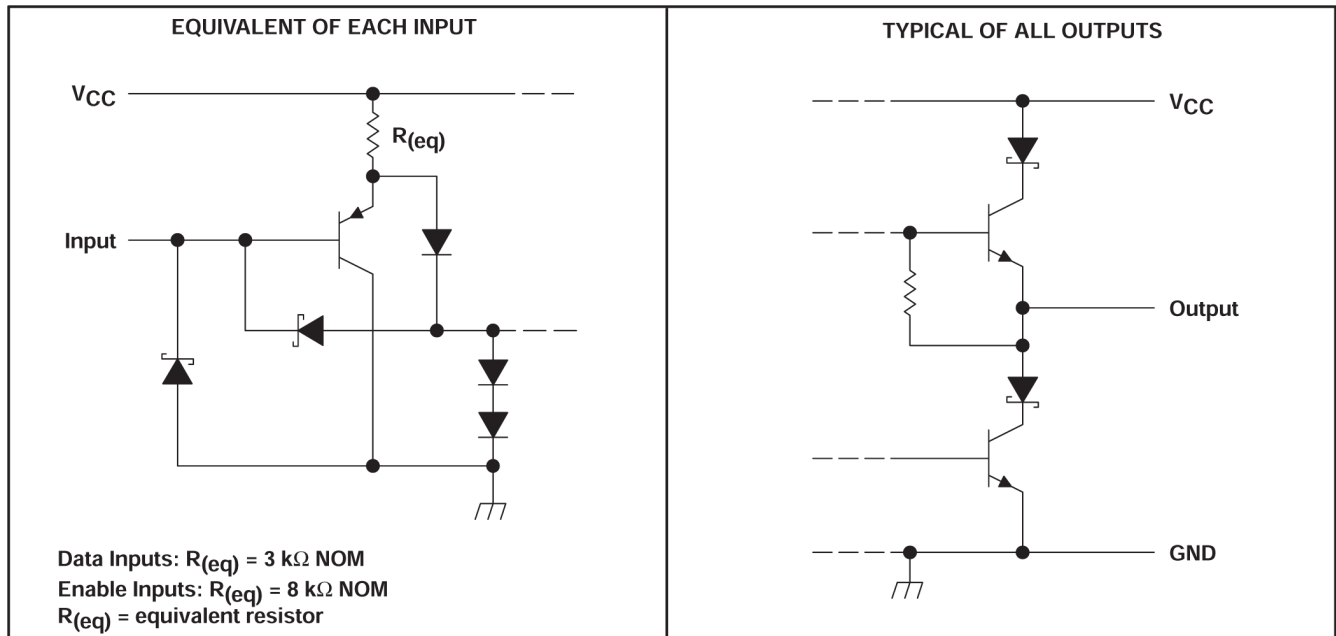
Figure 7-1. Schematics of Inputs and Outputs

Product Folder Links: SN75174

8 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information
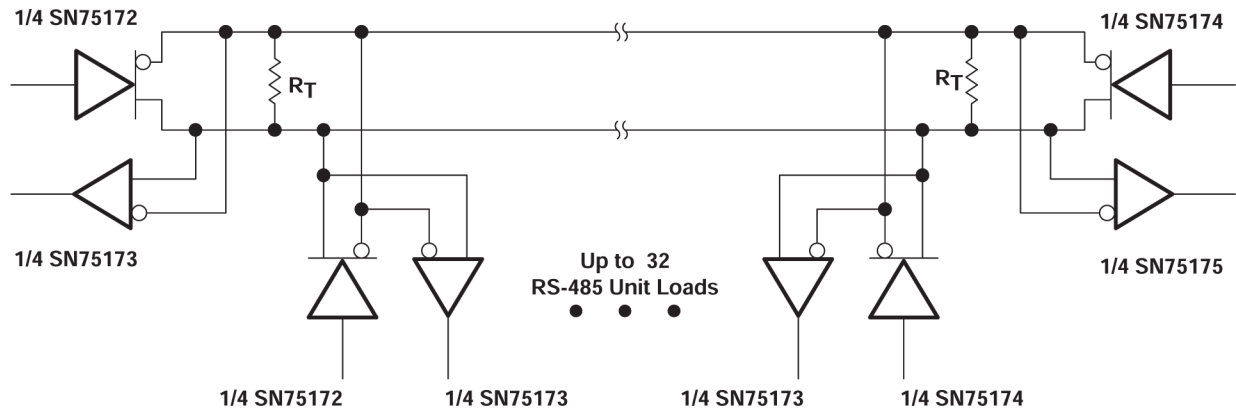
A.   The line length should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 8-1. Typical Application Circuit

Product Folder Links: *SN75174*

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75174DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	SN75174	
SN75174DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75174	Samples
SN75174DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75174	Samples
SN75174DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75174	Samples
SN75174N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75174N	Samples
SN75174NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75174N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75174DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75174DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75174DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75174DWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75174N	N	PDIP	16	25	506	13.97	11230	4.32
SN75174NE4	N	PDIP	16	25	506	13.97	11230	4.32

N (R−PDIP−T**) PLASTIC DUAL−IN−LINE PACKAGE
16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60) / 0.240 (6,10)

0.070 (1,78) / 0.045 (1,14)

0.045 (1,14) / 0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53) / 0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option

0.325 (8,26) / 0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20X (0.6)

20

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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