SN75ALS174 Quadruple Differential Line Driver

1 Features

- Meets or exceeds the requirements of ANSI EIA/TIA-422-B and RS-485
- High-speed advanced low-power Schottky circuitry
- Designed for up to 20Mbit/s operation in both serial and parallel applications
- Designed for multipoint transmission on long bus lines in noisy environments
- Low supply current requirements 55mA max
- Wide positive and negative input/output bus voltage ranges
- Driver output capacity: 60mA
- Thermal-shutdown protection
- Driver positive- and negative-current limiting

2 Applications

- Motor drives
- Factory automation and control

3 Description

The SN75ALS174 is a quadruple line driver with tri-state differential outputs. It is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485. This device is optimized for balanced multipoint bus transmission at rates of up to 20Mbit/s.

Each driver features wide positive and negative common-mode output voltage ranges that make them suitable for party-line applications in noisy environments.

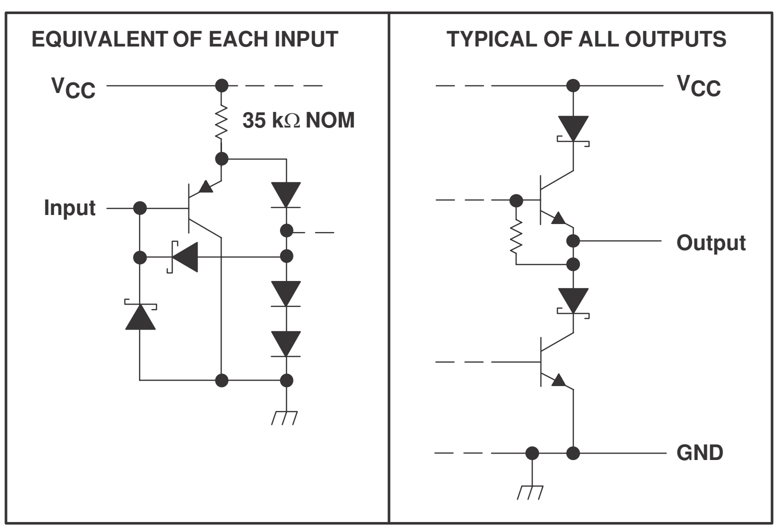
The SN75ALS174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C.

The SN75ALS174 is characterized for operation from 0°C to 70°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN75ALS174	SOIC (DW, 20)	12.8mm × 10.3mm

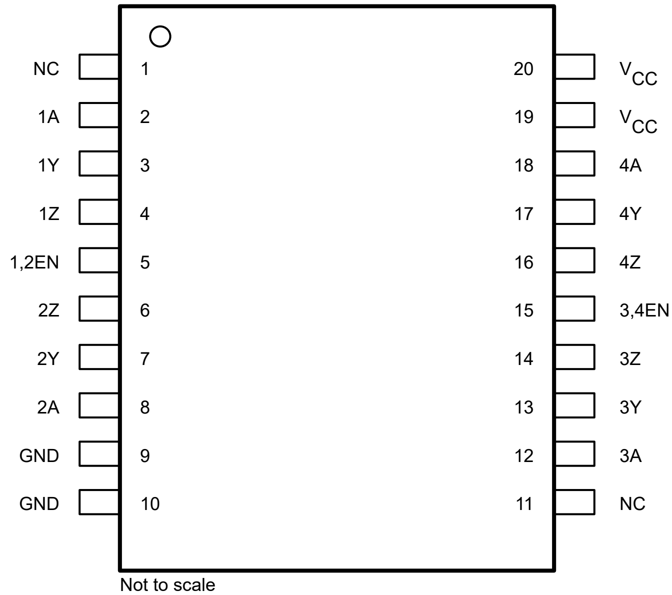
(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Schematics of Inputs and Outputs

Table of Contents

4 Pin Configuration and Functions



DW (SOIC) Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
V_{CC}	19, 20	VCC	5V supply. These pins are not connected together internally, so power must be applied to both
GND	9, 10	GND	Device ground
NC	1, 11	NC	Internally not connected
1A	2	I	Driver data input
1Y	3	O	Bus output, Y (Complementary to Z)
1Z	4	O	Bus output, Z (Complementary to Y)
1,2EN	5	I	Driver enable, active high
2Z	6	O	Bus output, Z (Complementary to Y)
2Y	7	O	Bus output, Y (Complementary to Z)
2A	8	I	Driver data input
3A	12	I	Driver data input
3Y	13	O	Bus output, Y (Complementary to Z)
3Z	14	O	Bus output, Z (Complementary to Y)
3,4EN	15	I	Driver enable, active high
4Z	16	O	Bus output, Z (Complementary to Y)
4Y	17	O	Bus output, Y (Complementary to Z)
4A	18	I	Driver data input

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply voltage, V_{CC} [(2)]		7	V
Input voltage, V_I		7	V
Output voltage range, V_O	–9	14	V
Continuous total dissipation	See the *Dissipation Rating* table		
Storage temperature, T_{stg}	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network GND.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	596 mW

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OC}	Common-mode output voltage			12	V
				–7	V
I_{OH}	High-level output current			–60	mA
I_{OL}	Low-level output current			60	mA
T_A	Operating free-air temperature	0		70	°C

5.4 Thermal Information

THERMAL METRIC[(1)]		DW (SOIC)	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	8.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0		1.5		6	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω	See Note Figure 6-1	1/2 V_{OD1} or 2(2)			V
		R_L = 54 Ω		1.5	2.5	5	V
$\lvert V_{OD3}\rvert$	Differential output voltage	See (5)		1.5		5	V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage(3)	R_L = 54 Ω or 100 Ω	See Figure 6-1			±0.2	V
V_{OC}	Common-mode output voltage(4)	R_L = 54 Ω or 100 Ω	See Figure 6-1			3	V
						–1	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage(3)	R_L = 54 Ω or 100 Ω	See Figure 6-1			±0.2	V
I_O	Output current with power off	V_{CC} = 0, V_O = –7 V to 12 V				±100	μA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				–100	μA
I_{OS}	Short-circuit output current	V_O = –7 V to 12 V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		36	55	mA
			Outputs disabled		16	30	mA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
(3) $\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(5) See EIA Standard RS-485, Figures 3-5, Test Termination Measurement 2.

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), C_L = 50 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, See Figure 6-2	9	15	22	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 6-3	30	45	70	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 6-4	25	40	65	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 6-3	10	20	35	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 6-4	10	30	45	ns

6 Parameter Measurement Information

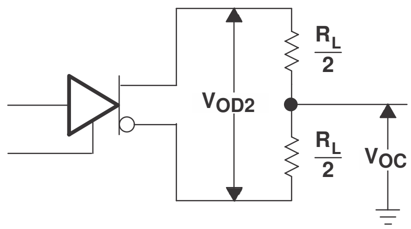
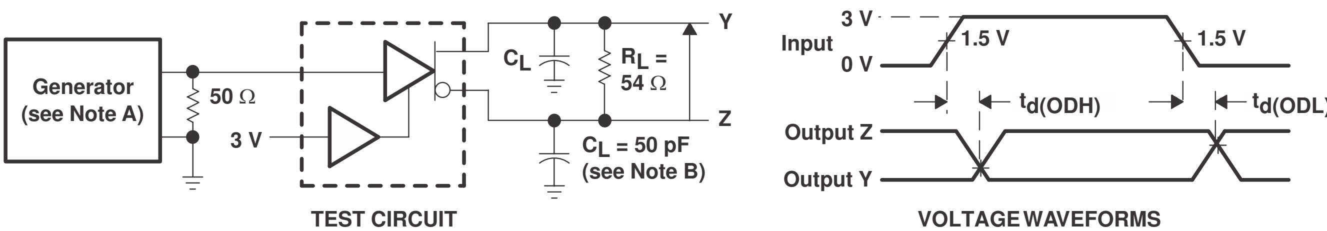
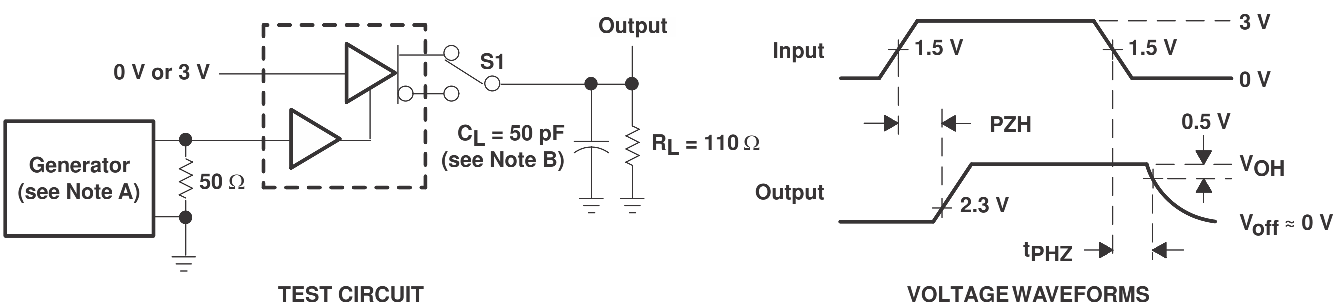


Figure 6-1. Differential and Common-Mode Output Voltages



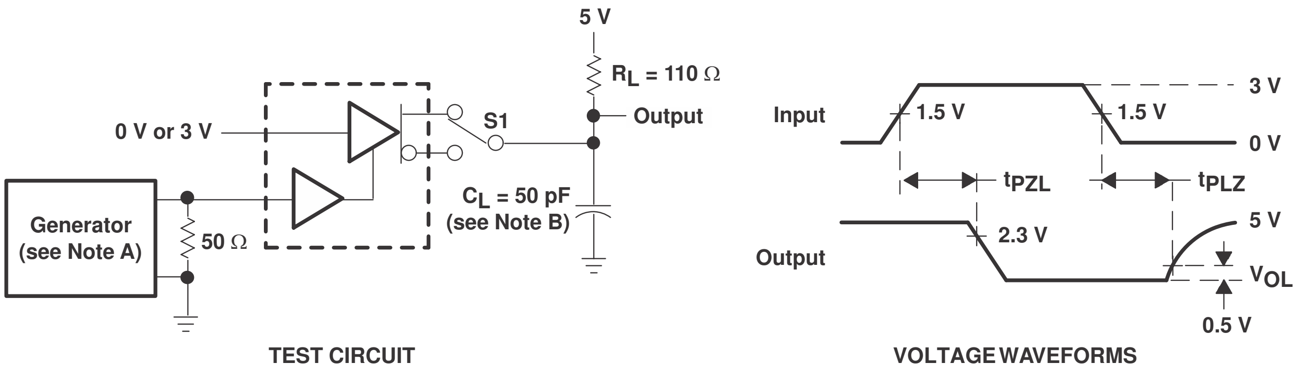
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, t_f 5ns, t_r 5ns.
B. C_L includes probe and stray capacitance.

Figure 6-2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, t_f 5ns, t_r 5ns.
B. C_L includes probe and stray capacitance.

Figure 6-3. Test Circuit and Voltage Waveforms, t_{PZH} and t_{PHZ}



A. The input pulse is supplied by a generator having the following characteristics: PRR = 1MHz, Z_O = 50Ω, duty cycle = 50%, t_f 10ns, t_r 10ns.
B. C_L includes probe and stray capacitance.

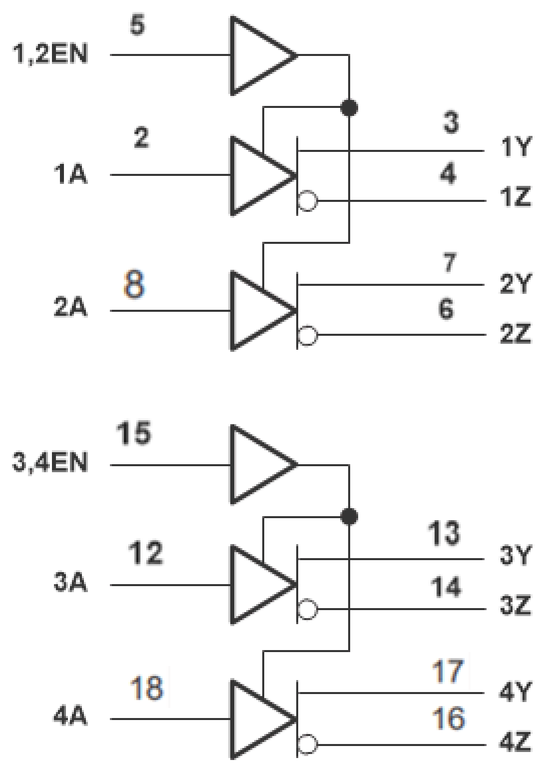
Figure 6-4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}

7 Detailed Description

7.1 Overview

The SN75ALS174 is a quadruple line driver with tristate differential outputs. the device is designed to meet the requirements of ANSI Standards EIA/TIA-422-B and RS-485. This device is optimized for balanced multipoint bus transmission at rates of up to 20Mbit/s

7.2 Functional Block Diagram



7.3 Feature Description

Each driver features wide positive and negative common-mode output voltage ranges that make them suitable for party-line applications in noisy environments. The SN75ALS174 provides positive- and negativecurrent limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C

7.4 Device Functional Modes

Table 7-1. Function Table (each driver)

INPUT A[(1)]	ENABLES	OUTPUTS[(2)]	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant.
(2) Z = high impedance (off)

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.2 Typical Application

When designing a system that uses drivers, receivers, and transceivers that comply with RS-422 or RS-485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because RS-422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, RS-485 requires termination at both ends of the cable. Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, ac termination, and multipoint termination

Figure 8-1. Typical RS-485 or RS-422 Application with Terminated Reciever.

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.2 Detailed Design Procedure

8.2.2.1 Data Rate and Bus Length

There is an inverse relationship between data rate and cable length, which means the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable length. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

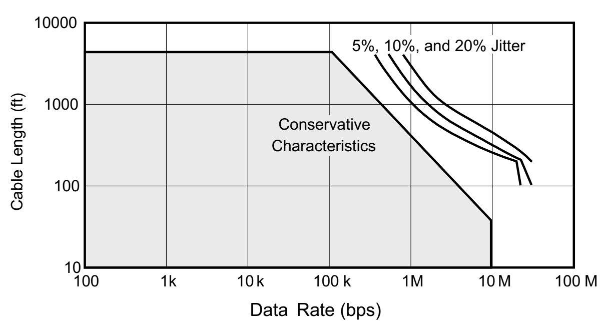


Figure 8-2. Cable Length vs Data Rate Characteristic

8.2.2.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections of varying phase as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

8.2.2.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ.

8.3 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply should be decoupled with a 100 nF ceramic capacitor located as close to the supply pins as possible. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes

8 Device and Documentation Support

8.1 Documentation Support

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2023) to Revision A (April 2024) — **Page**

- Changed the *Thermal Information* table.......... 4
- Changed Note A in Figure 6-4 6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75ALS174DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174
SN75ALS174DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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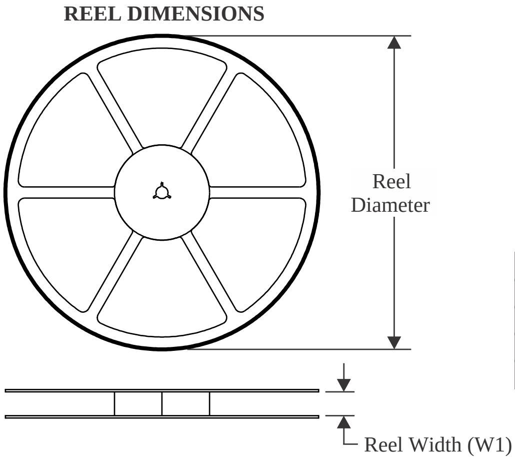
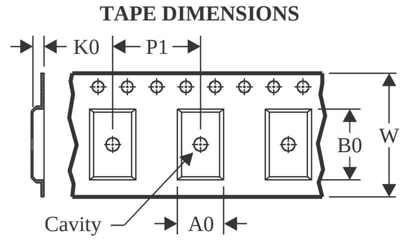
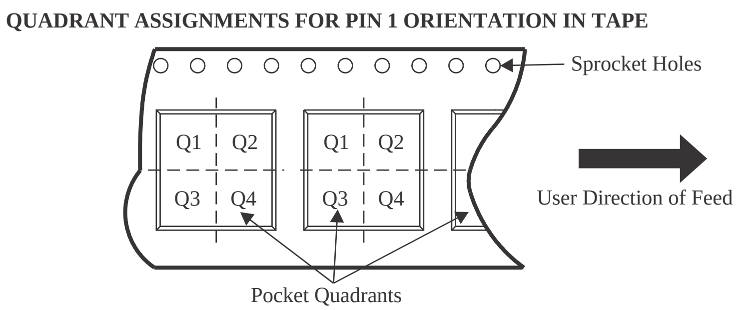
TAPE AND REEL INFORMATION





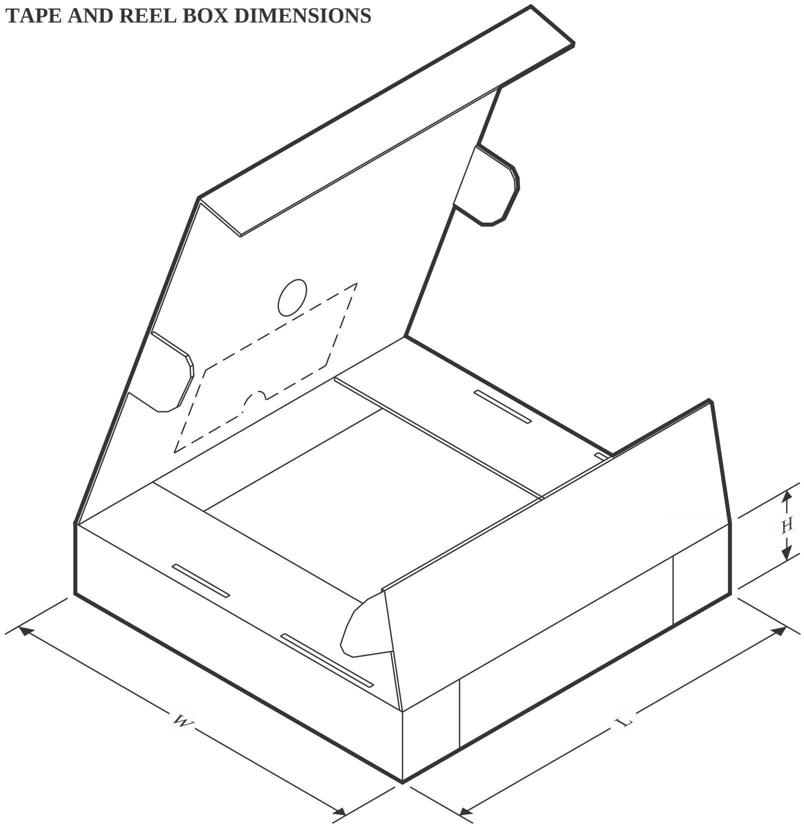
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

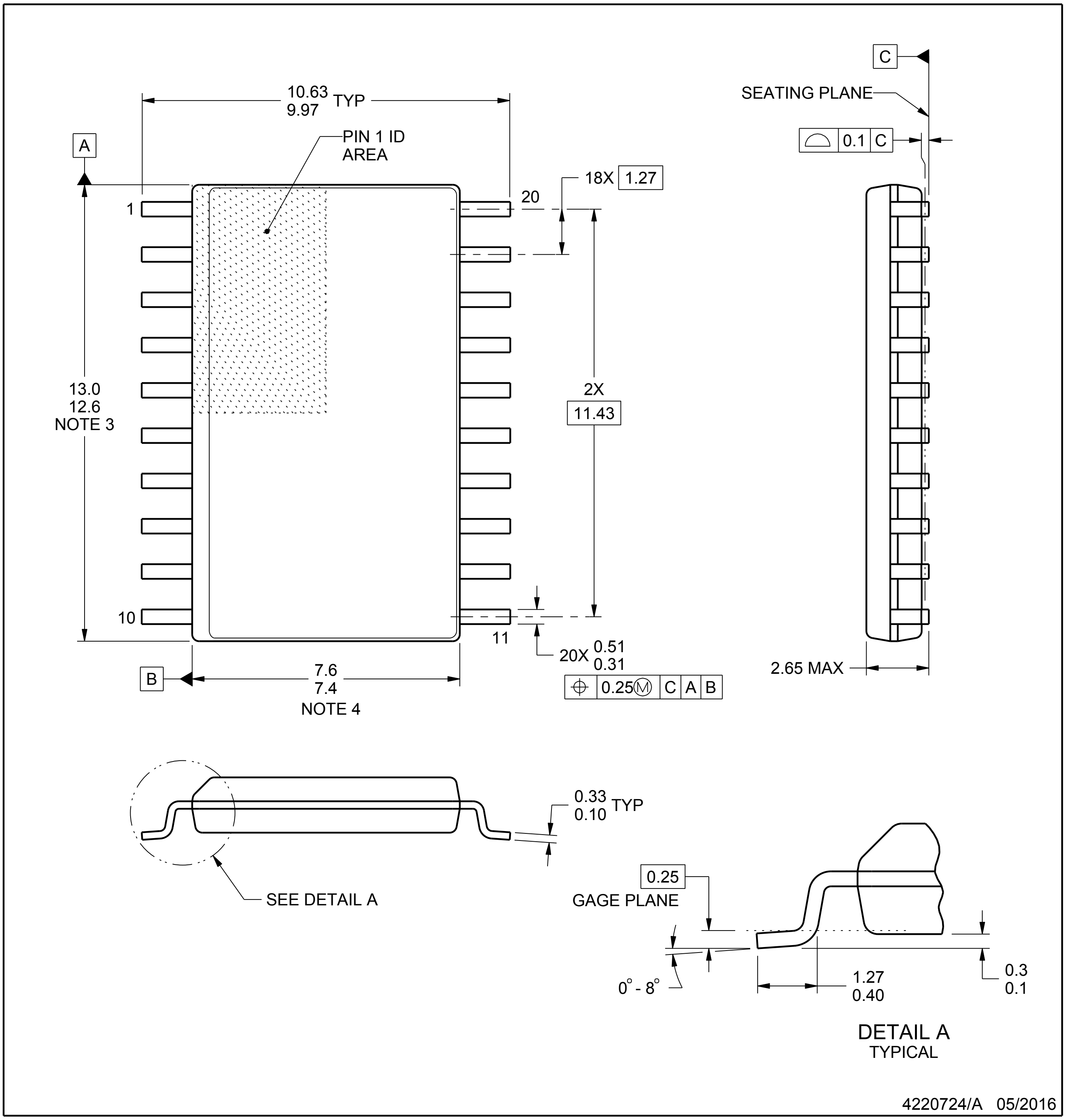
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS174DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75ALS174DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



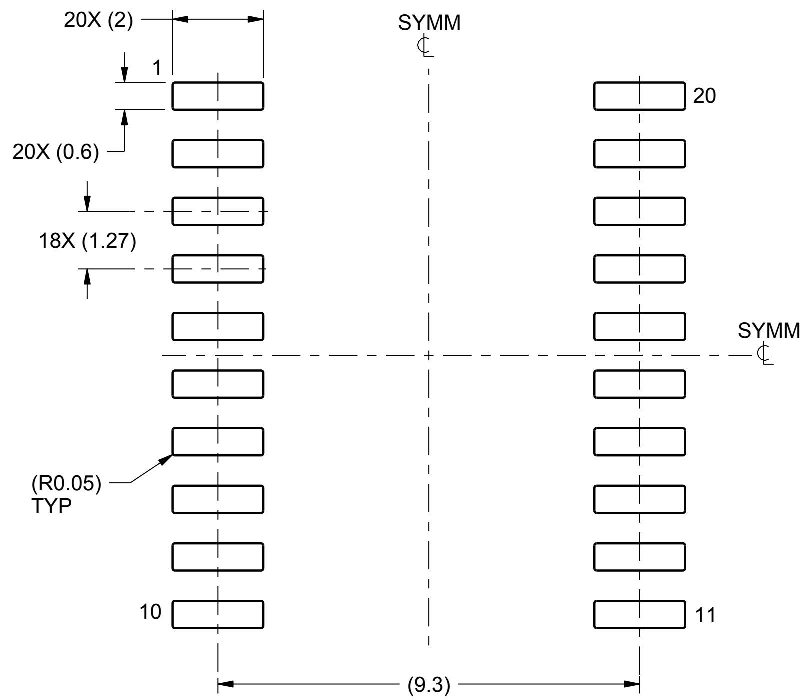
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS174DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN75ALS174DWR	SOIC	DW	20	2000	356.0	356.0	45.0

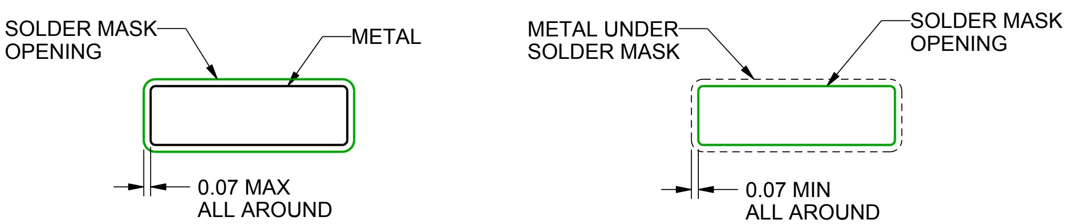


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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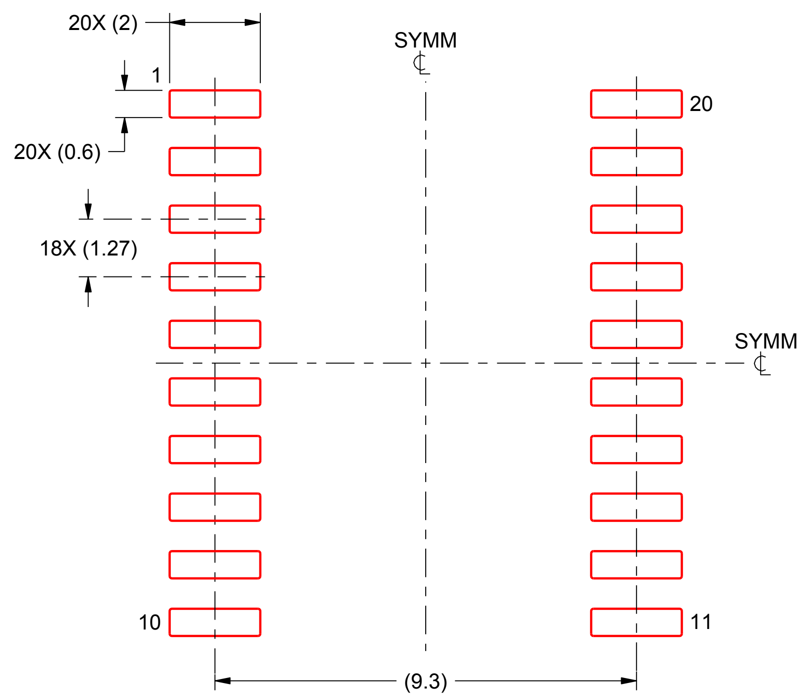
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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