HIGH-VOLTAGE, HIGH SLEW RATE, WIDEBAND FET-INPUT OPERATIONAL AMPLIFIER

Check for Samples: THS4631

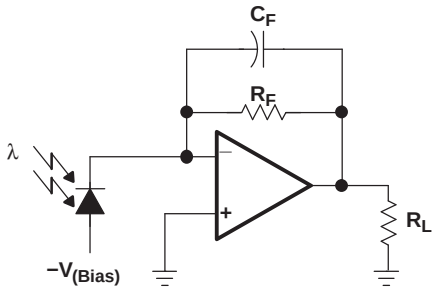
FEATURES

- **High Bandwidth:**
  - **325 MHz in Unity Gain**
  - **210 MHz Gain Bandwidth Product**
- **High Slew Rate:**
  - **900 V/µs (G = 2)**
  - **1000 V/µs (G = 5)**
- **Low Distortion of –76 dB, SFDR at 5 MHz**
- **Maximum Input Bias Current: 100 pA**
- **Input Voltage Noise: 7 nV/√Hz**
- **Maximum Input Offset Voltage: 500 µV at 25°C**
- **Low Offset Drift: 2.5 µV/°C**
- **Input Impedance: 10^9 || 3.9 pF**
- **Wide Supply Range: ± 5 V to ± 15 V**
- **High Output Current: 95 mA**

APPLICATIONS

- **Wideband Photodiode Amplifier**
- **High-Speed Transimpedance Gain Stage**
- **Test and Measurement Systems**
- **Current-DAC Output Buffer**
- **Active Filtering**
- **High-Speed Signal Integrator**
- **High-Impedance Buffer**

Photodiode Circuit



DESCRIPTION

The THS4631 is a high-speed, FET-input operational amplifier designed for applications requiring wideband operation, high-input impedance, and high-power supply voltages. By providing a 210-MHz gain bandwidth product, ±15-V supply operation, and 100-pA input bias current, the THS4631 is capable of simultaneous wideband transimpedance gain and large output signal swing. The fast 1000 V/µs slew rate allows for fast settling times and good harmonic distortion at high frequencies. Low current and voltage noise allow amplification of extremely low-level input signals while still maintaining a large signal-to-noise ratio.

The characteristics of the THS4631 make it ideally suited for use as a wideband photodiode amplifier. Photodiode output current is a prime candidate for transimpedance amplification as shown below. Other potential applications include test and measurement systems requiring high-input impedance, ADC and DAC buffering, high-speed integration, and active filtering.

The THS4631 is offered in an 8-pin SOIC (D), and the 8-pin SOIC (DDA) and MSOP (DGN) with PowerPAD™ package.

Related FET Input Amplifier Products

DEVICE	V_S (V)	GBWP (MHz)	SLEW RATE (V/µS)	VOLTAGE NOISE (nV/√Hz)	MINIMUM GAIN
OPA656	±5	230	290	7	1
OPA657	±5	1600	700	4.8	7
OPA627	±15	16	55	4.5	1
THS4601	±15	180	100	5.4	1

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNITS
V_S	Supply voltage, V_{S-} to V_{S+}		33 V
V_I	Input voltage		$\pm V_S$
I_O (2)	Output current		150 mA
	Continuous power dissipation		See Dissipation Rating Table
T_J	Maximum junction temperature(2)		150°C
T_A	Operating free-air temperature, continues operation, long-term reliability(2)		125°C
T_{stg}	Storage temperature range		–65°C to 150°C
	ESD ratings:	HBM	1000 V
		CDM	1500 V
		MM	100 V

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)	POWER RATING(1) (T_J =125°C)	
			$T_A \le 25$°C	$T_A = 85$°C
D (8)(2)	38.3	95	1.1 W	0.47 W
DDA (8)	9.2	45.8	2.3 W	0.98 W
DGN (8)	4.7	58.4	2.14 W	1.11 W

(1) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.
(2) This data was taken using the JEDEC standard High-K test PCB.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNITS
V_S	Supply Voltage	Dual Supply	±5	±15	V
		Single Supply	10	30	
T_A	Operating free-air temperature		-40	85	°C

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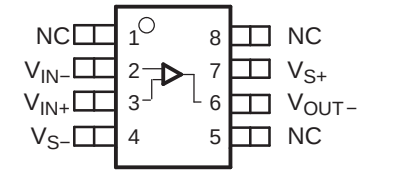
PACKAGE / ORDERING INFORMATION

PACKAGE DEVICES(1)	PACKAGE TYPE SOIC – 8	TRANSPORT MEDIA, QUANTITY
THS4631D	SOIC – 8	Rails, 75
THS4631DR		Tape and Reel, 2500
THS4631DDA	SOIC-PP – 8(2)	Rails, 75
THS4631DDAR		Tape and Reel, 2500
THS4631DGN	MSOP-PP – 8(2)	Rails, 100
THS4631DGNR		Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) PowerPad™ is electrically isolated from all other pins. Connection of the PowerPAD to the PCB ground plane is recommended because the ground plane is typically the largest copper area on a PCB. However, connection of the PowerPAD to V_{S-} up to V_{S+} is allowed if desired.

PIN ASSIGNMENTS

THS4631
TOP VIEW **D, DDA, AND DGN**



NC = No Internal Connection

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ELECTRICAL CHARACTERISTICS

V_S = ±15 V, R_F = 499 Ω, R_L = 1 kΩ, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/ MAX
AC PERFORMANCE								
Small signal bandwidth, -3 dB	G = 1, R_F = 0 Ω, V_O = 200 mV_{PP}		325				MHz	
	G = 2, R_F = 499 Ω, V_O = 200 mV_{PP}		105					
	G = 5, R_F = 499 Ω, V_O = 200 mV_{PP}		55					
	G = 10, R_F = 499 Ω, V_O = 200 mV_{PP}		25					
Gain bandwidth product	G > 20		210				MHz	
0.1 dB bandwidth flatness	G = 2, R_F = 499 Ω, C_F = 8.2 pF		38				MHz	
Large-signal bandwidth	G = 2, R_F = 499 Ω, V_O = 2 V_{PP}		105				MHz	
Slew rate	G = 2, R_F = 499 Ω, V_O = 2-V step		550				V/µs	
	G = 2, R_F = 499 Ω, V_O = 10-V step		900					
	G = 5, R_F = 499 Ω, V_O = 10-V step		1000					
Rise and fall time	2-V step		5				ns	
Settling time	0.1%, G = -1, V_O = 2-V step, C_F = 4.7 pF		40				ns	
	0.01%, G = -1, V_O = 2-V step, C_F = 4.7 pF		190					
HARMONIC DISTORTION								
Second harmonic distortion	G = 2, V_O = 2 V_{PP}, f = 5 MHz	R_L = 100 Ω	-65				dBc	
		R_L = 1 k Ω	-76					
Third harmonic distortion		R_L = 100 Ω	-62				dBc	
		R_L = 1 kΩ	-94					
Input voltage noise	f > 10 kHz		7				nV/√Hz	
Input current noise	f > 10 kHz		20				fA/√Hz	
DC PERFORMANCE								
Open-loop gain	R_L = 1 kΩ		80	70	65	65	dB	Min
Input offset voltage(1)	V_{CM} = 0 V		260	500	1600	2000	µV	Max
Average offset voltage drift(1)		25°C to 85°C	±2.5	±10	±12	±12	µV/°C	Max
Input bias current	V_{CM} = 0 V		50	100	1500	2000	pA	Max
Input offset current			25	100	700	1000	pA	Max
INPUT CHARACTERISTICS								
Common-mode input range			-13 to 12	-12.5 to 11.5	-12 to 11	-9 to 11	V	Min
Common-mode rejection ratio	V_{CM} = 10 V		95	86	80	80	dB	Min
Differential input resistance			10^9 || 3.9				Ω || pF	
Common-mode input resistance			10^9 || 3.9				Ω || pF	
OUTPUT CHARACTERISTICS								
Output voltage swing	R_L = 100 Ω		±11	±10	±9.5	±9.5	V	Min
	R_L = 1 kΩ		±13.5	±13	±12.8	±12.8		
Static output current (sourcing)	R_L = 20 Ω		98	90	85	80	mA	Min
Static output current (sinking)	R_L = 20 Ω		95	85	80	80	mA	Min
Closed loop output impedance	G = 1, f = 1 MHz		0.1				Ω	
POWER SUPPLY								
Specified operating voltage			±15	±16.5	±16.5	±16.5	V	Max
			±5	±4	±4	±4	V	Min
Maximum quiescent current			11.5	13	14	14	mA	Max
Minimum quiescent current			11.5	10	9	9	mA	Min
Power supply rejection (PSRR +)	V_{S+} = 15.5 V to 14.5 V, $V_{S–}$ = 15 V		95	85	80	80	dB	Min
Power supply rejection (PSRR –)	V_{S+} = 15 V, $V_{S–}$ = -15.5 V to -14..5 V		95	85	80	80	dB	Min

(1) Input offset voltage is 100% tested at 25°C. It is specified by characterization and simulation over the listed temperature range.

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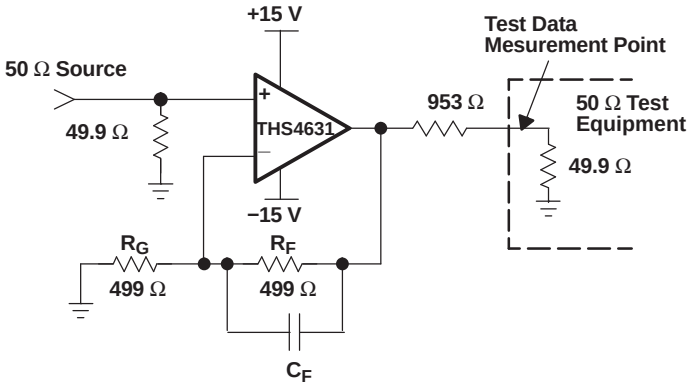
TYPICAL CHARACTERISTICS (±15 V GRAPHS)

T_A = 25°C, G = 2, R_F = 499 Ω, R_L = 1 kΩ, Unless otherwise noted.



SMALL SIGNAL FREQUENCY RESPONSE

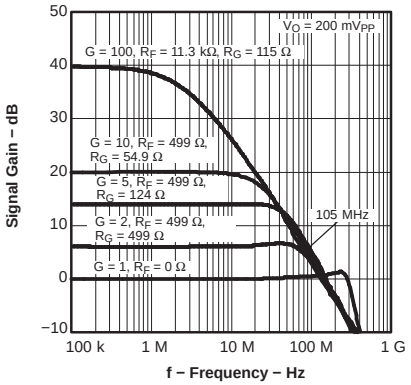


Figure 1.

SMALL SIGNAL FREQUENCY RESPONSE

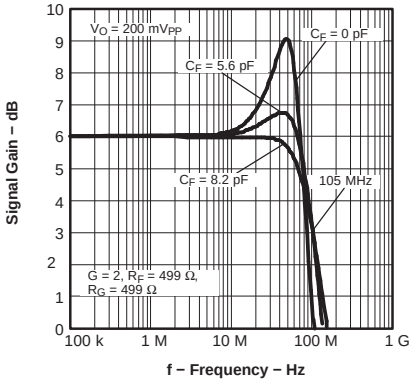


Figure 2.

0.1-dB FLATNESS

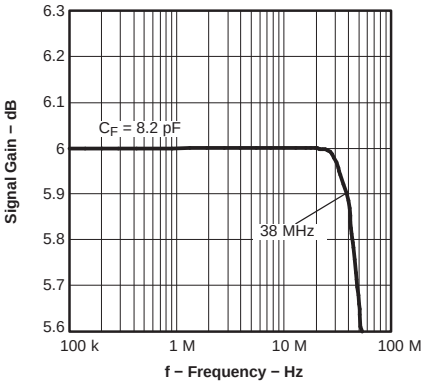


Figure 3.

SMALL SIGNAL FREQUENCY RESPONSE

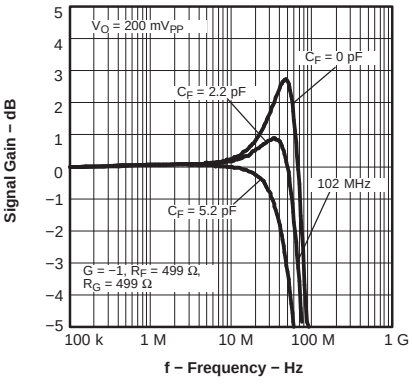


Figure 4.

LARGE SIGNAL FREQUENCY RESPONSE

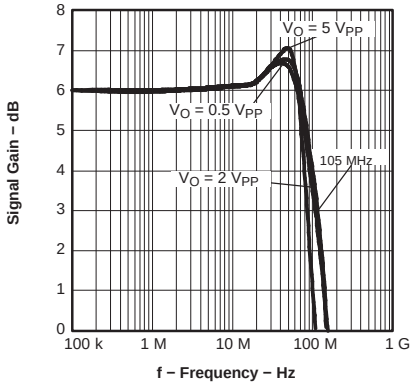


Figure 5.

FREQUENCY RESPONSE vs CAPACiTIVE LOAD

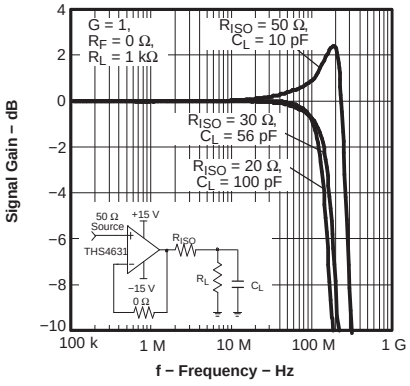


Figure 6.

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TYPICAL CHARACTERISTICS (±15 V GRAPHS) (continued)

T_A = 25°C, G = 2, R_F = 499 Ω, R_L = 1 kΩ, Unless otherwise noted.

SECOND ORDER HARMONIC DISTORTION vs FREQUENCY

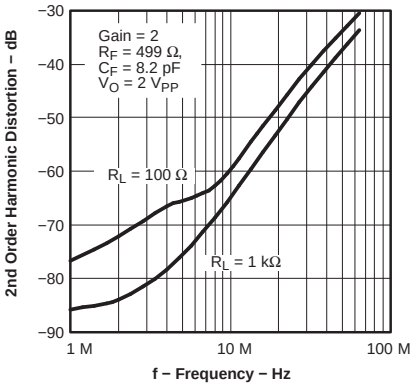

Figure 7.

THIRD ORDER HARMONIC DISTORTION vs FREQUENCY

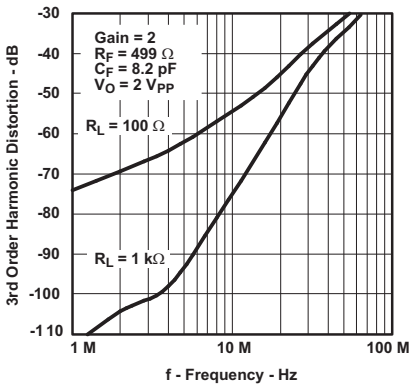

Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

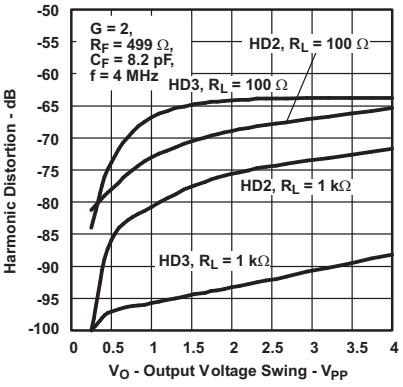

Figure 9.

SLEW RATE vs OUTPUT VOLTAGE

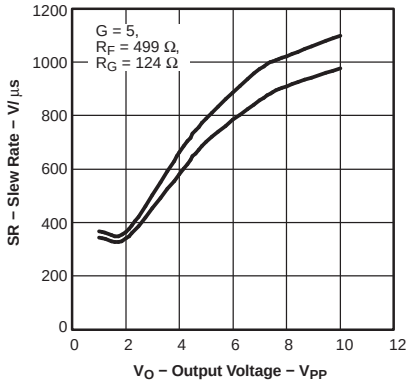

Figure 10.

OPEN-LOOP GAIN vs TEMPERATURE

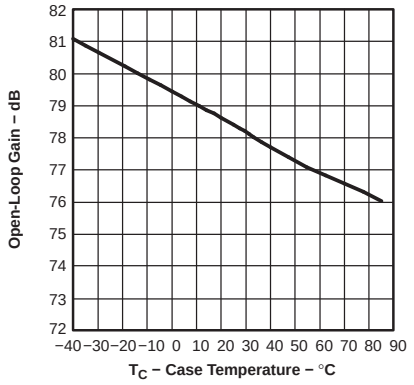

Figure 11.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

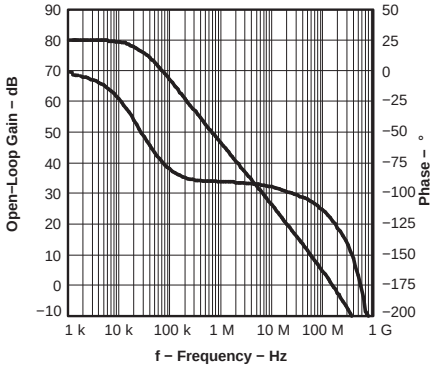

Figure 12.

INPUT VOLTAGE vs FREQUENCY

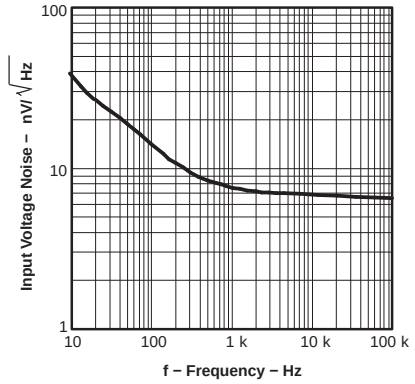

Figure 13.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

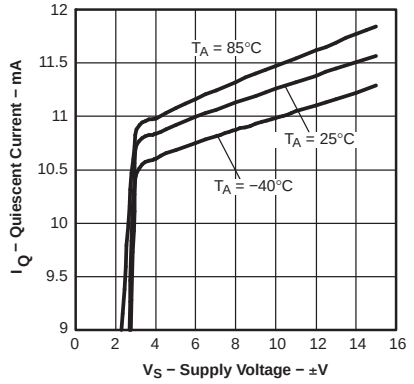

Figure 14.

INPUT BIAS CURRENT vs TEMPERATURE

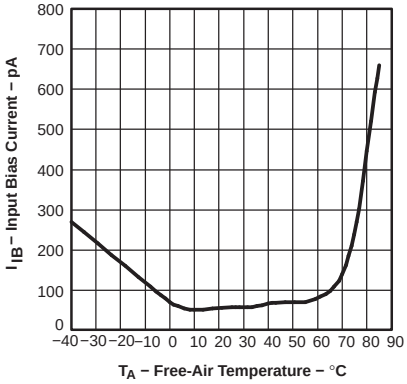

Figure 15.

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TYPICAL CHARACTERISTICS (±15 V GRAPHS) (continued)

T_A = 25°C, G = 2, R_F = 499 Ω, R_L = 1 kΩ, Unless otherwise noted.

INPUT OFFSET CURRENT vs TEMPERATURE

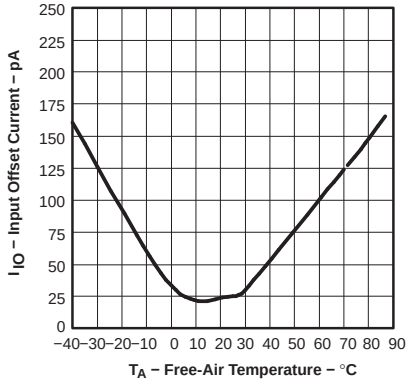

Figure 16.

INPUT OFFSET VOLTAGE vs TEMPERATURE

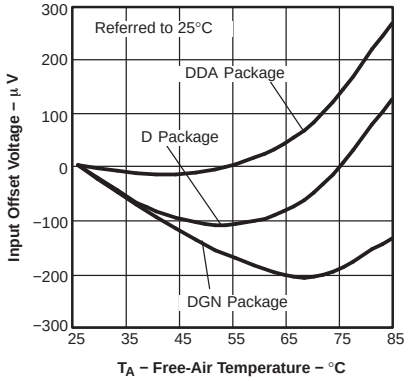

Figure 17.

OUTPUT VOLTAGE vs TEMPERATURE

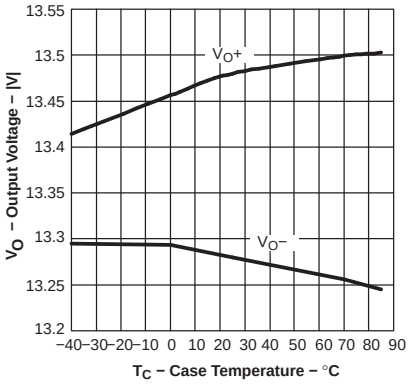

Figure 18.

STATIC OUTPUT DRIVE CURRENT vs TEMPERATURE

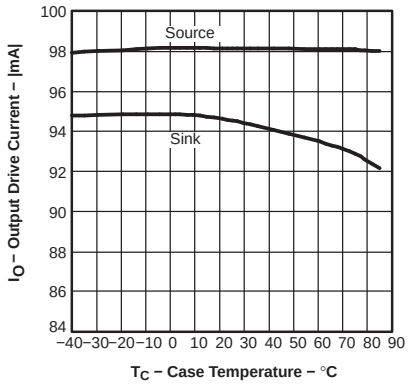

Figure 19.

SMALL SIGNAL TRANSIENT RESPONSE

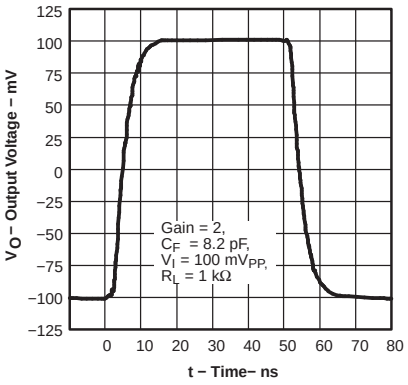

Figure 20.

LARGE SIGNAL TRANSIENT RESPONSE

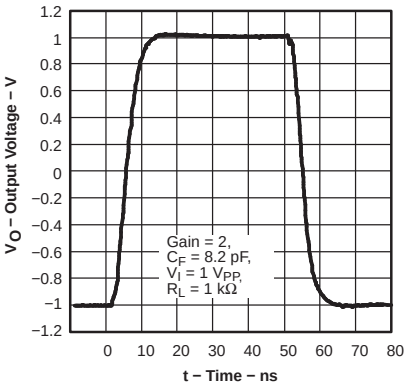

Figure 21.

LARGE SIGNAL TRANSIENT RESPONSE

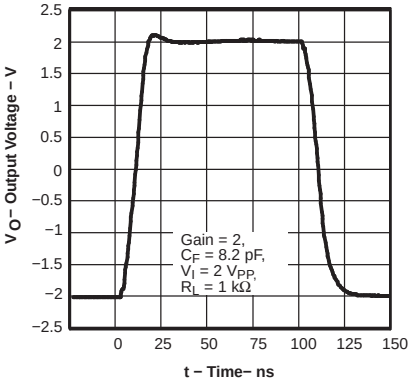

Figure 22.

LARGE SIGNAL TRANSIENT RESPONSE

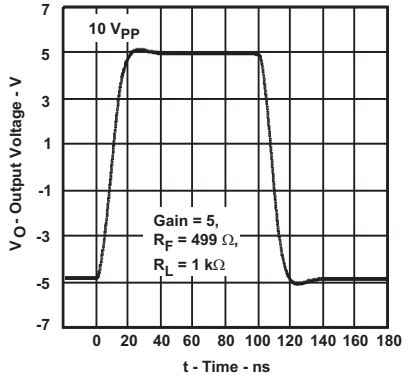

Figure 23.

LARGE SIGNAL TRANSIENT RESPONSE

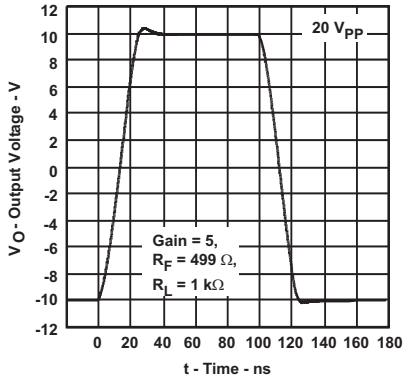

Figure 24.

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TYPICAL CHARACTERISTICS (±15 V GRAPHS) (continued)

T_A = 25°C, G = 2, R_F = 499 Ω, R_L = 1 kΩ, Unless otherwise noted.

SETTLING TIME

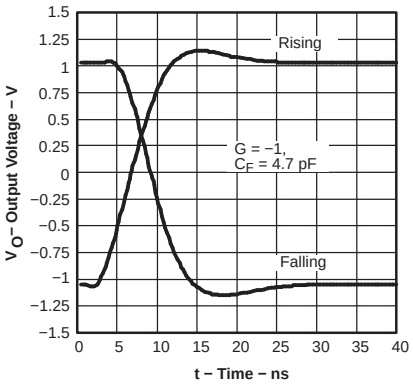

Figure 25.

SETTLING TIME

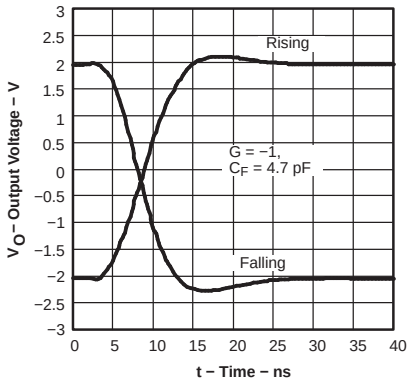

Figure 26.

OVERDRIVE RECOVERY

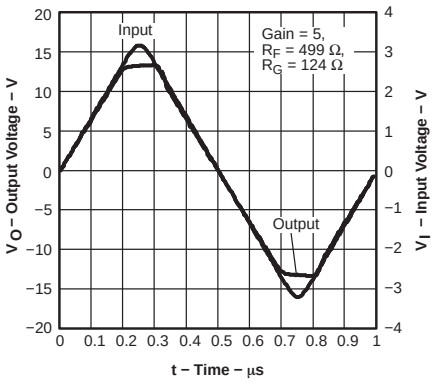

Figure 27.

OVERDRIVE RECOVERY

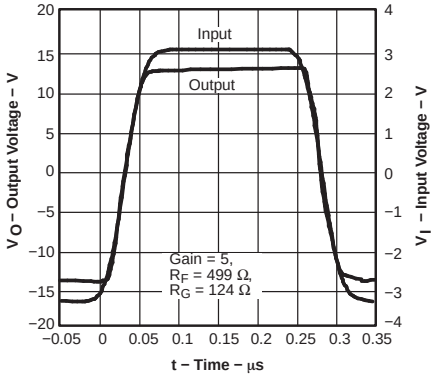

Figure 28.

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

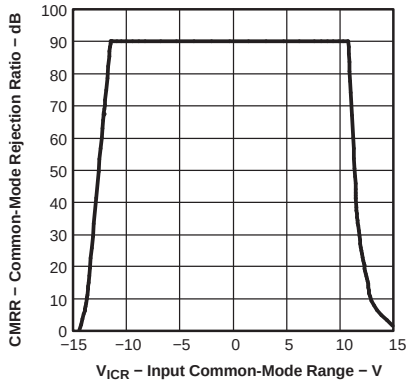

Figure 29.

REJECTION RATIO vs FREQUENCY

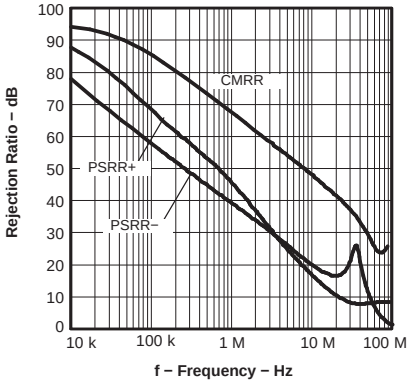

Figure 30.

OUTPUT IMPEDANCE vs FREQUENCY

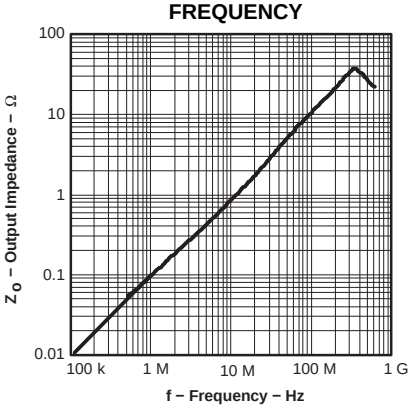

Figure 31.

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APPLICATION INFORMATION

INTRODUCTION

The THS4631 is a high-speed, FET-input operational amplifier. The combination of: high gain bandwidth product of 210 MHz, high slew rate of 1000 V/µs, and trimmed dc precision makes the device an excellent design option for a wide variety of applications, including test and measurement, optical monitoring, transimpedance gain circuits, and high-impedance buffers. The applications section of the data sheet discusses these particular applications in addition to general information about the device and its features

TRANSIMPEDANCE FUNDAMENTALS

FET-input amplifiers are often used in transimpedance applications because of their extremely high input impedance. A transimpedance block accepts a current as an input and converts this current to a voltage at the output. The high-input impedance associated with FET-input amplifiers minimizes errors in this process caused by the input bias currents, IIB, of the amplifier.

DESIGNING THE TRANSIMPEDANCE CIRCUIT

Typically, design of a transimpedance circuit is driven by the characteristics of the current source that provides the input to the gain block. A photodiode is the most common example of a capacitive current source that interfaces with a transimpedance gain block. Continuing with the photodiode example, the system designer traditionally chooses a photodiode based on two opposing criteria: speed and sensitivity. Faster photodiodes cause a need for faster gain stages, and more sensitive photodiodes require higher gains in order to develop appreciable signal levels at the output of the gain stage.

These parameters affect the design of the transimpedance circuit in a few ways. First, the speed of the photodiode signal determines the required bandwidth of the gain circuit. Second, the required gain, based on the sensitivity of the photodiode, limits the bandwidth of the circuit. Third, the larger capacitance associated with a more sensitive signal source also detracts from the achievable speed of the gain block. The dynamic range of the input signal also places requirements on the amplifier dynamic range. Knowledge of the source output current levels, coupled with a desired voltage swing on the output, dictates the value of the feedback resistor, RF. The transfer function from input to output is VOUT = $I_{IN}R_F$.

The large gain-bandwidth product of the THS4631 provides the capability for simultaneously achieving both high-transimpedance gain, wide bandwidth, high slw rate, and low noise. In addition, the high-power supply rails provide the potential for a very wide dynamic range at the output, allowing for the use of input sources which possess wide dynamic range. The combination of these characteristics makes the THS4631 a design option for systems that require transimpedance amplification of wideband, low-level input signals. A standard transimpedance circuit is shown in Figure 32.

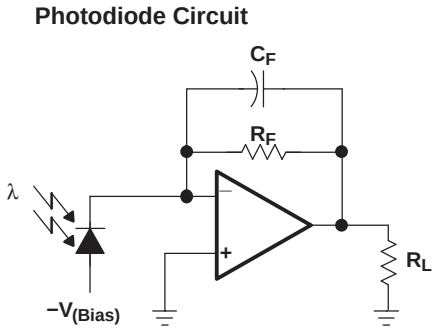

Figure 32. Wideband Photodiode Transimpedance Amplifier

As indicated, the current source typically sets the requirements for gain, speed, and dynamic range of the amplifier. For a given amplifier and source combination, achievable performance is dictated by the following parameters: the amplifier gain-bandwidth product, the amplifier input capacitance, the source capacitance, the transimpedance gain, the amplifier slew rate, and the amplifier output swing. From this information, the optimal performance of a transimpedance circuit using a given amplifier is determined. Optimal is defined here as providing the required transimpedance gain with a maximized flat frequency response.

For the circuit shown in Figure 32, all but one of the design parameters is known; the feedback capacitor (C_F) must be determined. Proper selection of the feedback capacitor prevents an unstable design, controls pulse response characteristics, provides maximized flat transimpedance bandwidth, and limits broadband integrated noise. The maximized flat frequency response results with CF calculated as shown in Equation 1, where CF is the feedback capacitor, R_F is the feedback resistor, CS is the total source capacitance (including amplifier input capacitance and parasitic capacitance at the inverting node), and GBP is the gain-bandwidth product of the amplifier in hertz.

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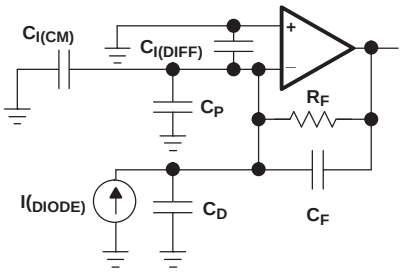
$$C_F = \frac{\frac{1}{\pi R_F GBP} + \sqrt{\left(\frac{1}{\pi R_F GBP}\right)^2 + \frac{4C_S}{\pi R_F GBP}}}{2} \quad (1)$$

Once the optimal feedback capacitor has been selected, the transimpedance bandwidth can be calculated with Equation 2.

$$F_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F (C_S + C_F)}} \quad (2)$$



$C_S = C_{I(CM)} + C_{I(DIFF)} + C_P + C_D$

A. The total source capacitance is the sum of several distinct capacitances.

Figure 33. Transimpedance Analysis Circuit

Where:

$C_{I(CM)}$ is the common-mode input capacitance.

$C_{I(DIFF)}$ is the differential input capacitance.

C_D is the diode capacitance.

C_P is the parasitic capacitance at the inverting node.

The feedback capacitor provides a pole in the noise gain of the circuit, counteracting the zero in the noise gain caused by the source capacitance. The pole is set such that the noise gain achieves a 20-dB per decade rate-of-closure with the open-loop gain response of the amplifier, resulting in a stable circuit. As indicated, the formula given provides the feedback capacitance for maximized flat bandwidth. Reduction in the value of the feedback capacitor can increase the signal bandwidth, but this occurs at the expense of peaking in the ac response.

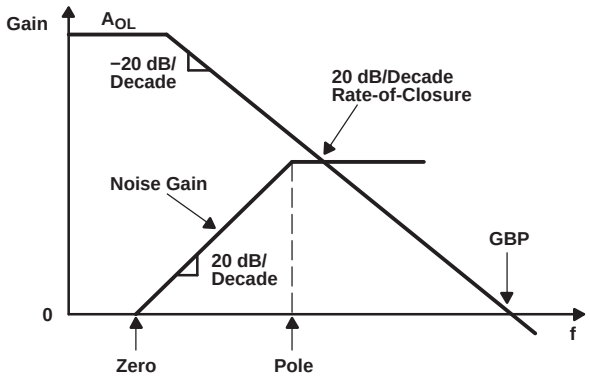


Figure 34. Transimpedance Circuit Bode Plot

The performance of the THS4631 has been measured for a variety of transimpedance gains with a variety of source capacitances. The achievable bandwidths of the various circuit configurations are summarized numerically in Table 1. The frequency responses are presented in Figure 35, Figure 36, and Figure 37.

Note that the feedback capacitances do not correspond exactly with the values predicted by the equation. They have been tuned to account for the parasitic capacitance of the feedback resistor (typically 0.2 pF for 0805 surface mount devices) as well as the additional capacitance associated with the PC board. The equation should be used as a starting point for the design, with final values for CF optimized in the laboratory.

Table 1. Transimpedance Performance Summary for Various Configurations

SOURCE CAPACITANCE (PF)	TRANS-IMPEDANCE GAIN (Ω)	FEEDBACK CAPACITANCE (PF)	-3 dB FREQUENCY (MHZ)
18	10 k	2	15.8
18	100 k	0.5	3
18	1 M	0	1.2
47	10 k	2.2	8.4
47	100 k	0.7	2.1
47	1 M	0.2	0.52
100	10 k	3	5.5
100	100 k	1	1.4
100	1 M	0.2	0.37

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Table 1. Transimpedance Performance Summary for Various Configurations (continued)

10-kΩ TRANSIMPEDANCE RESPONSES

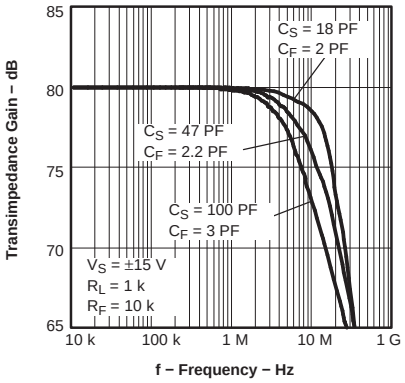


Figure 35.

100-kΩ TRANSIMPEDANCE RESPONSES

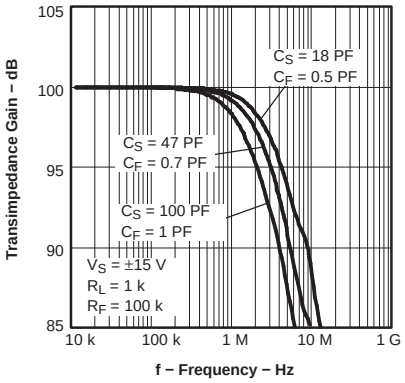


Figure 36.

1-MΩ TRANSIMPEDANCE RESPONSES

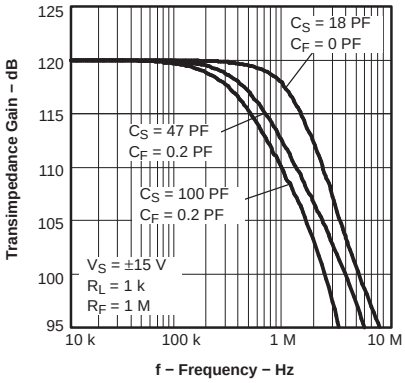
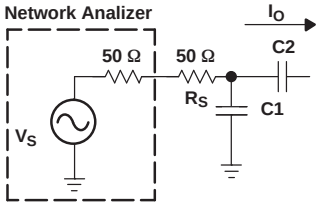


Figure 37.

MEASURING TRANSIMPEDANCE BANDWIDTH

While there is no substitute for measuring the performance of a particular circuit under the exact conditions that are used in the application, the complete system environment often makes measurements harder. For transimpedance circuits, it is difficult to measure the frequency response with traditional laboratory equipment because the circuit requires a current as an input rather than a voltage. Also, the capacitance of the current source has a direct effect on the frequency response. A simple interface circuit can be used to emulate a capacitive current source with a network analyzer. With this circuit, trans- impedance bandwidth measurements are simplified, making amplifier evaluation easier and faster.



$$\frac{I_O}{V_S}(s) = \frac{1}{2R_S\left(1 + \frac{C1}{C2}\right)}$$

(Above the Pole Frequency)

A. The interface network creates a capacitive, constant current source from a network analyzer and properly terminates the network analyzer at high frequencies.

Figure 38. Emulating a Capacitive Current Source With a Network Analyzer

The transconductance transfer function of the interface circuit is:

$$\frac{I_O}{V_S}(s) = \frac{\frac{s}{2R_S\left(1+\frac{C1}{C2}\right)}}{s + \frac{1}{2R_S(C1+C2)}} \quad (3)$$

The transfer function contains a zero at dc and a pole at: $\frac{1}{2R_S(C1 + C2)}$. The transconductance is constant at: $\frac{1}{2R_S\left(1 + \frac{C1}{C2}\right)}$, above the pole frequency, providing a controllable ac-current source. This circuit also properly terminates the network analyzer with 50 Ω at high frequencies. The second requirement for this current source is to provide the desired output impedance, emulating the output impedance of a photodiode or other current source. The output impedance of this circuit is given by:

$$Z_O(s) = \frac{C1 + C2}{C1 \times C2}\left[\frac{s + \frac{1}{2R_S(C1+C2)}}{s\left(s + \frac{1}{2R_S C1}\right)}\right] \quad (4)$$

Assuming C1 >> C2, the equation reduces to: $Z_O \approx \frac{1}{sC2}$, giving the appearance of a capacitive source at a higher frequency.

Capacitor values should be chosen to satisfy two requirements. First, C2 represents the anticipated capacitance of the true source. Second C1 is chosen

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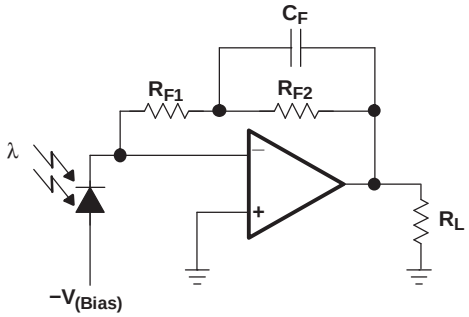
such that the corner frequency of the transconductance network is much less than the transimpedance bandwidth of the circuit. Choosing this corner frequency properly leads to more accurate measurements of the transimpedance bandwidth. If the interface circuit corner frequency is too close to the bandwidth of the circuit, determining the power level in the flatband is difficult. A decade or more of flat bandwidth provides a good basis for determining the proper transimpedance bandwidth.

ALTERNATIVE TRANSIMPEDANCE CONFIGURATIONS

Other transimpedance configurations are possible. Three possibilities are shown below.

The first configuration is a slight modification of the basic transimpedance circuit. By splitting the feedback resistor, the feedback capacitor value becomes more manageable and easier to control. This type of compensation scheme is useful when the feedback capacitor required in the basic configuration becomes so small that the parasitic effects of the board and components begin to dominate the total feedback capacitance. By reducing the resistance across the capacitor, the capacitor value can be increased. This mitigates the dominance of the parasitic effects.

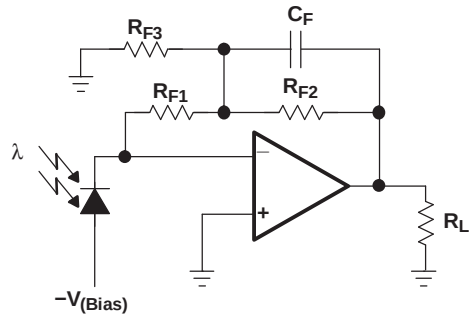


A. Splitting the feedback resistor enables use of a larger, more manageable feedback capacitor.

Figure 39. Alternative Transimpedance Configuration 1

The second configuration uses a resistive T-network to achieve high transimpedance gains using relatively small resistor values. This topology can be useful when the desired transimpedance gain exceeds the value of available resistors. The transimpedance gain is given by Equation 5.

$$R_{EQ} = R_{F1}\left(1 + \frac{R_{F2}}{R_{F3}}\right) \quad (5)$$

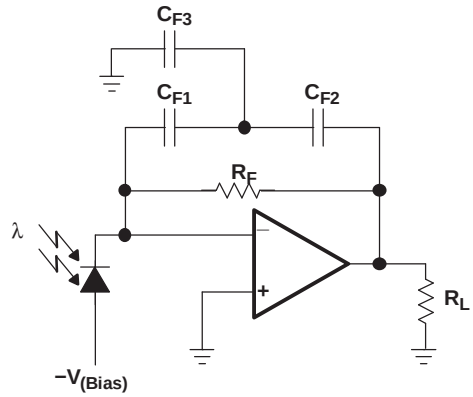


A. A resistive T-network enables high transimpedance gain with reasonable resistor values.

Figure 40. Alternative Transimpedance Configuration 2

The third configuration uses a capacitive T-network to achieve fine control of the compensation capacitance. The capacitor CF3 can be used to tune the total effective feedback capacitance to a fine degree. This circuit behaves the same as the basic transimpedance configuration, with the effective CF given by Equation 6.

$$\frac{1}{C_{FEQ}} = \frac{1}{C_{F1}}\left(1 + \frac{C_{F3}}{C_{F2}}\right) \quad (6)$$



A. A capacitive T-network enables fine control of the effective feedback capacitance using relatively large capacitor values.

Figure 41. Alternative Transimpedance Configuration 3

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SUMMARY OF KEY DECISIONS IN TRANSIMPEDANCE DESIGN

The following is a simplified process for basic transimpedance circuit design. This process gives a start to the design process, though it does ignore some aspects that may be critical to the circuit.

STEP 1: Determine the capacitance of the source.

STEP 2: Calculate the total source capacitance, including the amplifier input capacitance, $C_{I(CM)}$ and $C_{I(DIFF)}$.

STEP 3: Determine the magnitude of the possible current output from the source, including the minimum signal current anticipated and maximum signal current anticipated.

STEP 4: Choose a feedback resistor value such that the input current levels create the desired output signal voltages, and ensure that the output voltages can accommodate the dynamic range of the input signal.

STEP 5: Calculate the optimum feedback capacitance using Equation 1.

STEP 6: Calculate the bandwidth given the resulting component values.

STEP 7: Evaluate the circuit to determine if all design goals are satisfied.

SELECTION OF FEEDBACK RESISTORS

Feedback resistor selection can have a significant effect on the performance of the THS4631 in a given application, especially in configurations with low closed-loop gain. If the amplifier is configured for unity gain, the output should be directly connected to the inverting input. Any resistance between these two points interacts with the input capacitance of the amplifier and causes an additional pole in the frequency response. For nonunity gain configurations, low resistances are desirable for flat frequency response. However, care must be taken not to load the amplifier too heavily with the feedback network if large output signals are expected. In most cases, a trade off is made between the frequency response characteristics and the loading of the amplifier. For a gain of 2, a 499-Ωfeedback resistor is a suitable operating point from both perspectives. If resistor values are chosen too large, the THS4631 is subject to oscillation problems. For example, an inverting amplifier configuration with a 5-kΩ gain resistor and a 5-kΩ feedback resistor develops an oscillation due to the interaction of the large resistors with the input capacitance. In low gain configurations, avoid feedback resistors this large or anticipate using an external compensation scheme to stabilize the circuit. Using a simple capacitor in parallel with the feedback resistor makes the amplifier more stable as shown in the *Typical Characteristics* graphs.

NOISE ANALYSIS

High slew rate, unity gain stable, voltage-feedback operational amplifiers usually achieve their slew rate at the expense of a higher input noise voltage. The 7 nV/√Hz input voltage noise for the THS4631 is, however, much lower than comparable amplifiers while achieving high slew rates. The input-referred voltage noise, and the input-referred current noise term, combine to give low output noise under a wide variety of operating conditions. Figure 42 shows the amplifier noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or fA/√Hz.

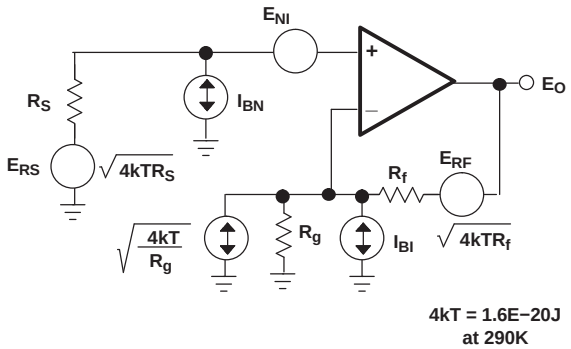

Figure 42. Noise Analysis Model

The total output noise voltage can be computed as the square root of all square output noise voltage contributors. Equation 7 shows the general form for the output noise voltage using the terms shown in Figure 42.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_f\right)^2 + 4kTR_fNG} \quad (7)$$

Dividing this expression by the noise gain [NG = (1+ R_f/R_g)] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 8:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_f}{NG}\right)^2 + \frac{4kTR_f}{NG}} \quad (8)$$

Using high resistor values can dominate the total equivalent input-referred noise. Using a 3-kΩ source-resistance (R_S) value adds a voltage noise term of approximately 7 nV/√Hz. This is equivalent to the amplifier voltage noise term. Using higher resistor

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values dominate the noise of the system. Although the THS4631 JFET input stage is ideal for high-source impedance because of the low-bias currents, the system noise and bandwidth is limited by a high-source (R_S) impedance.

SLEW RATE PERFORMANCE WITH VARYING INPUT STEP AMPLITUDE AND RISE/FALL TIME

Some FET input amplifiers exhibit the peculiar behavior of having a larger slew rate when presented with smaller input voltage steps and slower edge rates due to a change in bias conditions in the input stage of the amplifier under these circumstances. This phenomena is most commonly seen when FET input amplifiers are used as voltage followers. As this behavior is typically undesirable, the THS4631 has been designed to avoid these issues. Larger amplitudes lead to higher slew rates, as would be anticipated, and fast edges do not degrade the slew rate of the device. The high slew rate of the THS4631 allows improved SFDR and THD performance, especially noticeable above 5 MHz.

PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with high frequency amplifier-like devices in the THS4631 requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (< 0.25”) from the power supply pins to high frequency 0.1-µF and 100-pF de-coupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the de-coupling capacitors. The power supply connections should always be de-coupled with these capacitors. Larger (6.8 µF or more) tantalum de-coupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
- Careful selection and placement of external components preserve the high frequency performance of the THS4631. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PC board trace length as short as possible. Never use wirebound type resistors in a high frequency application. Since the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an RS since the THS4631 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an RS are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS4631 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace

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impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity or a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

- Socketing a high-speed part like the THS4631 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates a troublesome parasitic network which makes it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4631 part directly onto the board.

PowerPAD DESIGN CONSIDERATIONS

The THS4631 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 43 (a) and Figure 43 (b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 43 (c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the mechanical methods of heatsinking.

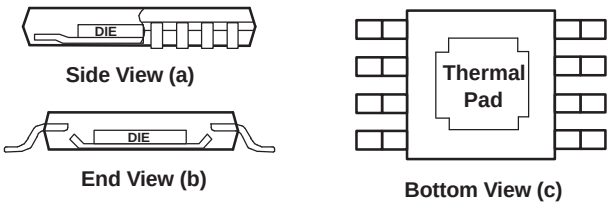

Figure 43. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

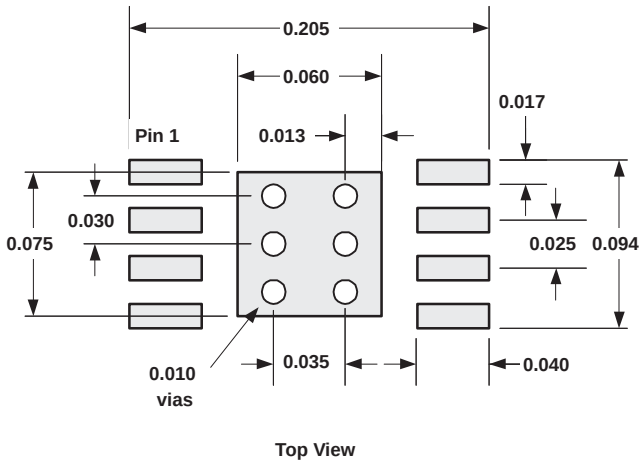

Figure 44. DGN PowerPAD PCB Etch and Via Pattern

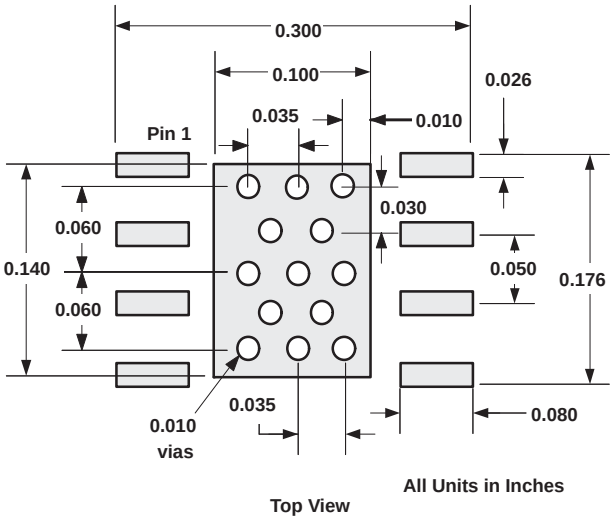

Figure 45. DDA PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. PCB with a top side etch pattern is shown in Figure 44 and Figure 45. There should be etch for the leads and for the thermal pad.
2. Place the recommended number of holes in the area of the thermal pad. These holes should be 10 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS4631 IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be

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soldered so that wicking is not a problem.

4. Connect all holes to the internal ground plane. Although the PowerPAD is electrically isolated from all pins and the active circuitry, connection to the ground plane is recommended. This is due to the fact that ground planes on most PCBs are typically the targets copper area. Offering the best thermal path heat to flow out of the device.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS4631 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its via holes exposed. The bottom-side solder mask should cover the via holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

To maintain maximum output capabilities, the THS4631 does not incorporate automatic thermal shutoff protection. The designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150°C is exceeded. For best performance, design for a maximum junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade. The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using Equation 9.

$$P_{D\,max} = \frac{T_{max} - T_A}{\theta_{JA}} \quad (9)$$

where:

P_{Dmax} is the maximum power dissipation in the amplifier (W).

T_{max} is the absolute maximum junction temperature (°C).

T_A is the ambient temperature (°C).

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).

θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

NOTE:

For systems where heat dissipation is more critical, the THS4631 is offered in an 8-pin MSOP with PowerPAD package and an 8-pin SOIC with PowerPAD package with better thermal performance. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in Figure 46 for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note number SLMA002. Figure 46 also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.

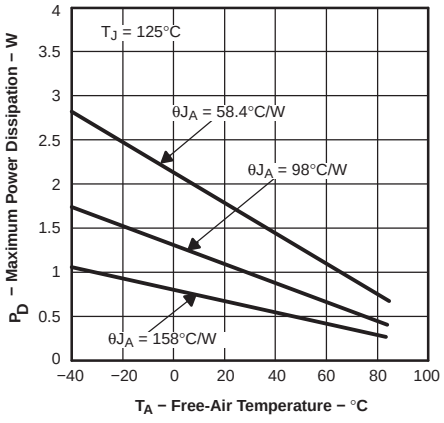

Figure 46. Maximum Power Dissipation vs. Ambient Temperature

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Results are with no air flow and PCB size = 3" x 3 "

θ_{JA} = 58.4°C/W for the 8-pin MSOP with PowerPAD (DGN).

θ_{JA} = 98°C/W for the 8-pin SOIC high-K test PCB (D).

θ_{JA} = 158°C/W for the 8-pin MSOP with PowerPAD, without solder.

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem

DESIGN TOOLS EVALUATION FIXTURE, SPICE MODELS, AND APPLICATIONS SUPPORT

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal an evaluation board has been developed for the THS4631 operational amplifier. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative. The board layers are provided in Figure 47, Figure 48, and Figure 49. The bill of materials for the evaluation board is provided in Table 2.

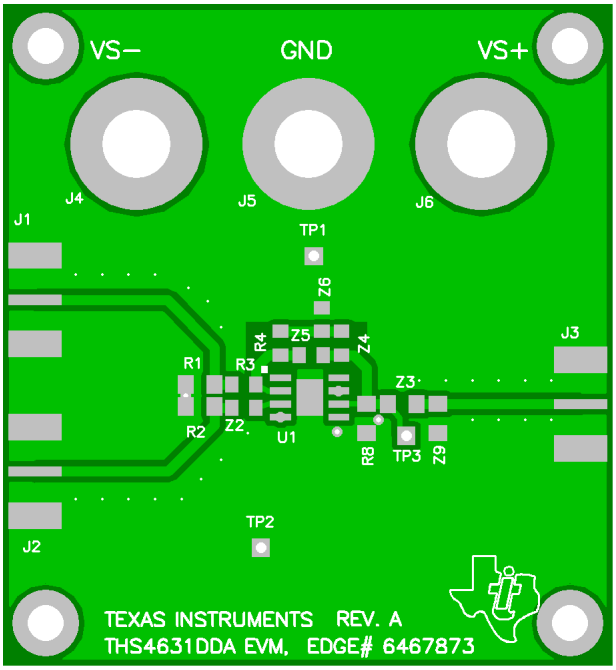

Figure 47. EVM Top Layer

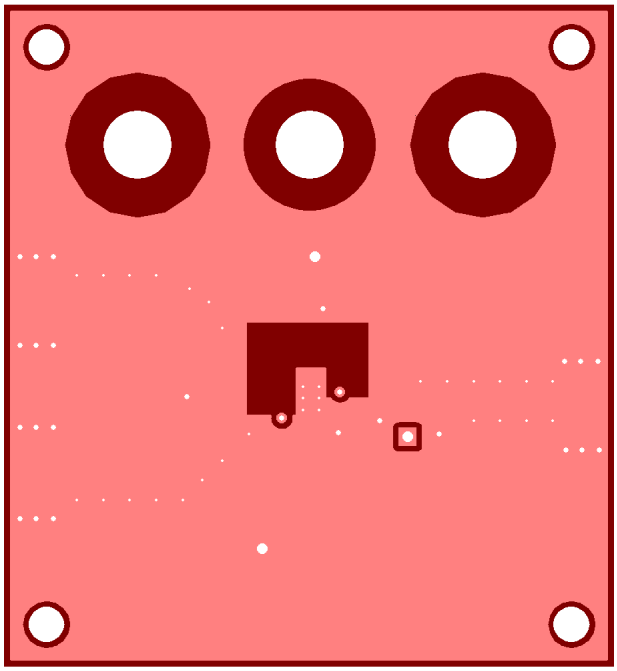

Figure 48. EVM Layers 2 and 3, Ground

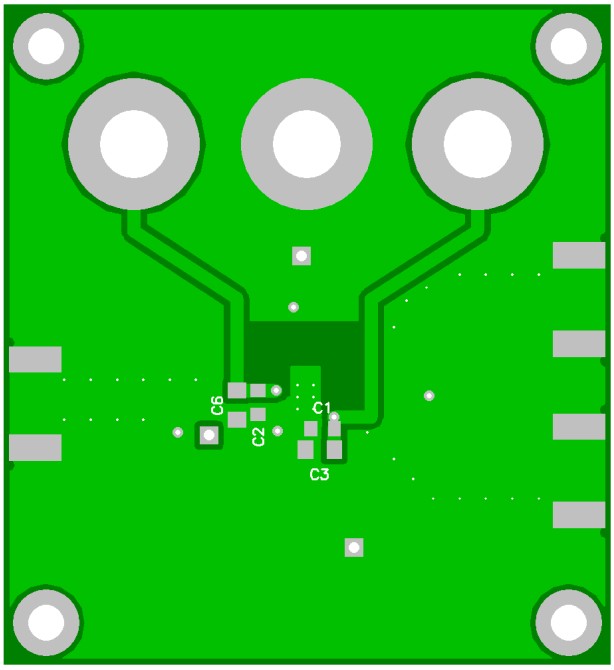

Figure 49. EVM Bottom Layer

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BILL OF MATERIALS

Table 2. THS4631DDA EVM

ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QUANTITY	MANUFACTURER'S PART NUMBER(1)
1	CAP, 2.2 µF, CERAMIC, X5R, 25 V	1206	C3, C6	2	(AVX) 12063D225KAT2A
4	CAP, 0.1µF, CERAMIC, X7R, 50 V	0805	C1, C2	2	(AVX) 08055C104KAT2A
	OPEN	0805	R4, Z4, Z6	3	
6	RESISTOR, 0 OHM, 1/8 W	0805	Z2	1	(KOA) RK73Z2ATTD
7	RESISTOR, 499 OHM, 1/8 W, 1%	0805	R3, Z5	2	(KOA) RK73H2ATTD4990F
8	OPEN	1206	R8, Z9	2	
9	RESISTOR, 0 OHM, 1/4 W	1206	R1	1	(KOA) RK73Z2BLTD
10	RESISTOR, 49.9 OHM, 1/4 W, 1%	1206	R2	1	(KOA) RK73H2BLTD49R9F
11	RESISTOR, 953 OHM, 1/4 W, 1%	1206	Z3	1	(KOA) RK73H2BLTD9530F
13	CONNECTOR, SMA PCB JACK		J1, J2, J3	3	(JOHNSON) 142-0701-801
14	JACK, BANANA RECEPTANCE, 0.25" DIA. HOLE		J4, J5, J6	3	(SPC) 813
15	TEST POINT, BLACK		TP1, TP2	2	(KEYSTONE) 5001
	TEST POINT, RED		TP3	1	(KEYSTONE) 5000
16	STANDOFF, 4-40 HEX, 0.625" LENGTH			4	(KEYSTONE) 1808
17	SCREW, PHILLIPS, 4-40, .250"			4	SHR-0440-016-SN
18	IC, THS4631		U1	1	(TI) THS4631DDA
19	BOARD, PRINTED CIRCUIT			1	(TI) EDGE # 6467873 Rev.A

(1) The manufacturer's part numbers are used for test purposes only.

EVM

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF-amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4631 is available through either the Texas Instruments web site (www.ti.com). These models help in predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

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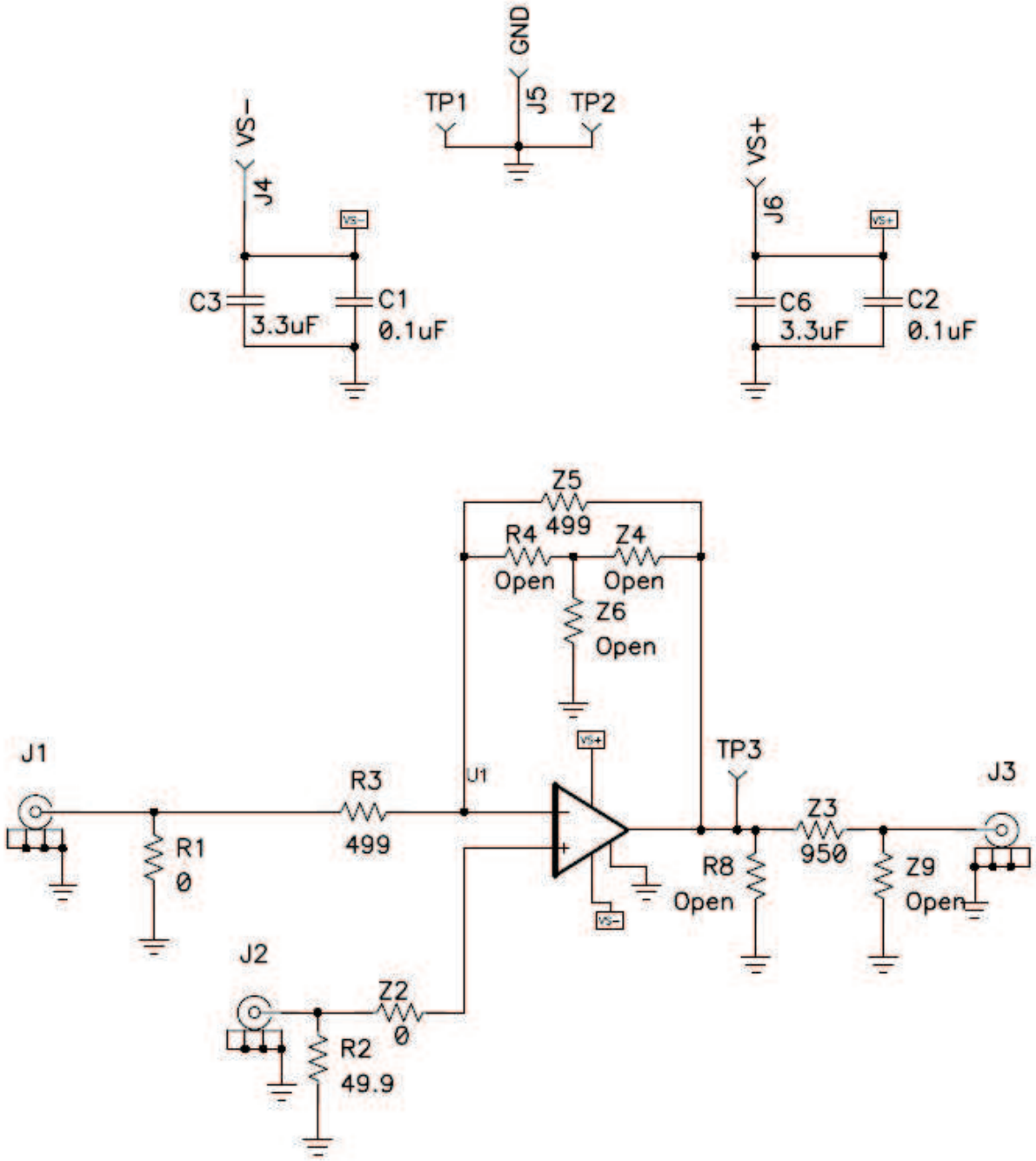

Figure 50. THS4631 EVM Schematic

ADDITIONAL REFERENCE MATERIAL

- *PowerPAD Made Easy*, application brief (SLMA004)
- *PowerPAD Thermally Enhanced Package*, technical brief (SLMA002)
- *Noise Analysis of FET Transimpedance Amplifiers*, application bulletin, Texas Instruments Literature Number SBOA060.
- *Tame Photodiodes With Op Amp Bootstrap*, application bulletin, Texas Instruments Literature Number SBBA002.
- *Designing Photodiode Amplifier Circuits With OPA128*, application bulletin, Texas Instruments Literature Number SBOA061.
- *Photodiode Monitoring With Op Amps*, application bulletin, Texas Instruments Literature Number SBOA035.
- *Comparison of Noise Performance Between a FET Transimpedance Amplifier and a Switched Integrator*, Application Bulletin, Texas Instruments Literature Number SBOA034.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input and output voltage ranges as specified in the table provided below.

Input Range, V_{S+} to V_{S-}	**10 V to 30 V**
Input Range, V_I	10 V to 30 V NOT TO EXCEED VS+ or VS–
Output Range, V_O	10 V to 30 V NOT TO EXCEED VS+ or VS–

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Consult the product data sheet or EVM user's guide (if user's guide is available) prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 50°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the material provided. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments Post Office Box 655303 Dallas, Texas 75265

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REVISION HISTORY

Changes from Original (December 2004) to Revision A **Page**

- Changed the Related FET Input Amplifier Products table 1
- Changed the Differential input resistance value From: 10^9 || 6.5 To: 10^9 || 3.9 4
- Changed the Common-mode input resistance value From: 10^9 || 6.5 To: 10^9 || 3.9 4
- Changed Figure 8 - From: R_L = 499Ω To R_F = 499Ω 6
- Changed Figure 9 - From: R_L = 499Ω To R_F = 499Ω 6
- Added Figure 23 7
- Added Figure 24 7
- Added Figure 50 19

Changes from Revision A (March 2005) to Revision B **Page**

- Changed the T_{stg} value in the Absolute Maximum Ratings table From: 65°C to 150°C To: –65°C to 150°C 2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4631D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	4631	
THS4631DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	4631	Samples
THS4631DGN	OBSOLETE	HVSSOP	DGN	8		TBD	Call TI	Call TI	-40 to 85	ADK	
THS4631DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ADK	Samples
THS4631DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4631	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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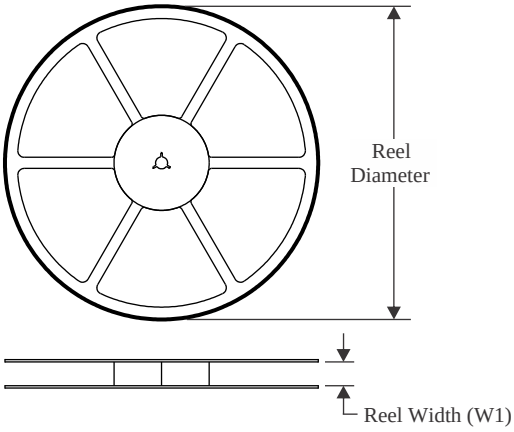
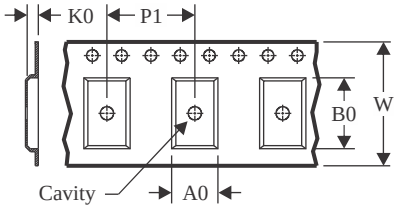
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

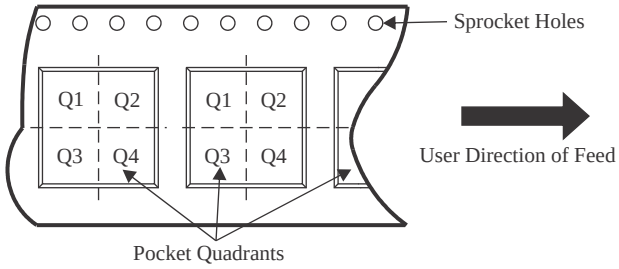


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

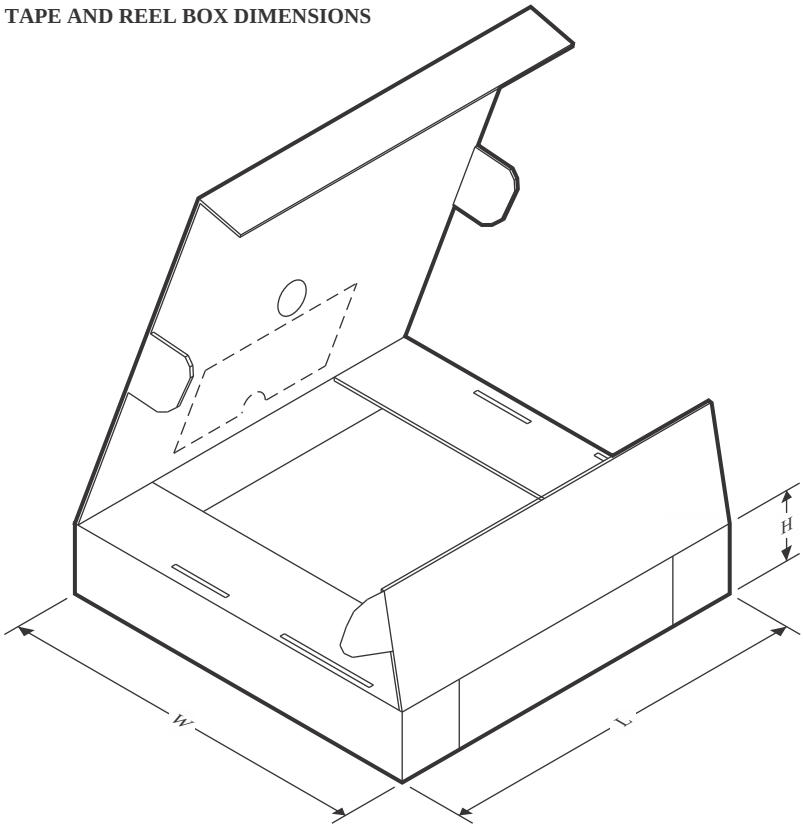
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4631DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4631DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4631DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

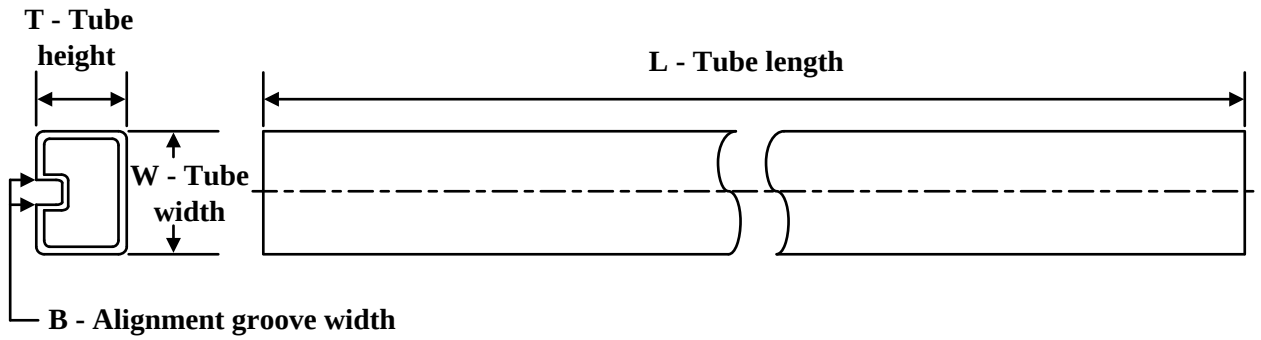
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4631DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
THS4631DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4631DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4631DDA	DDA	HSOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

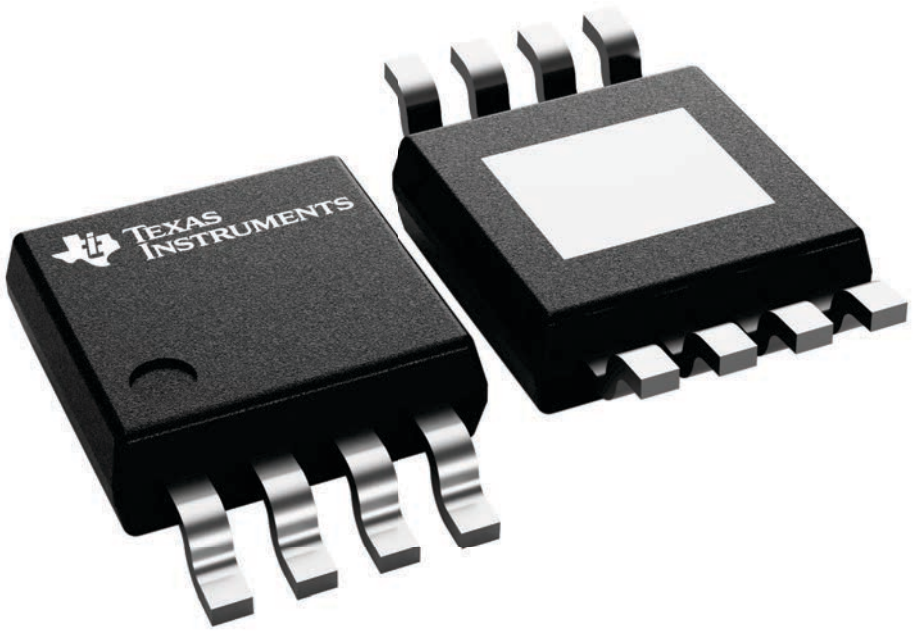
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

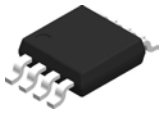
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/B

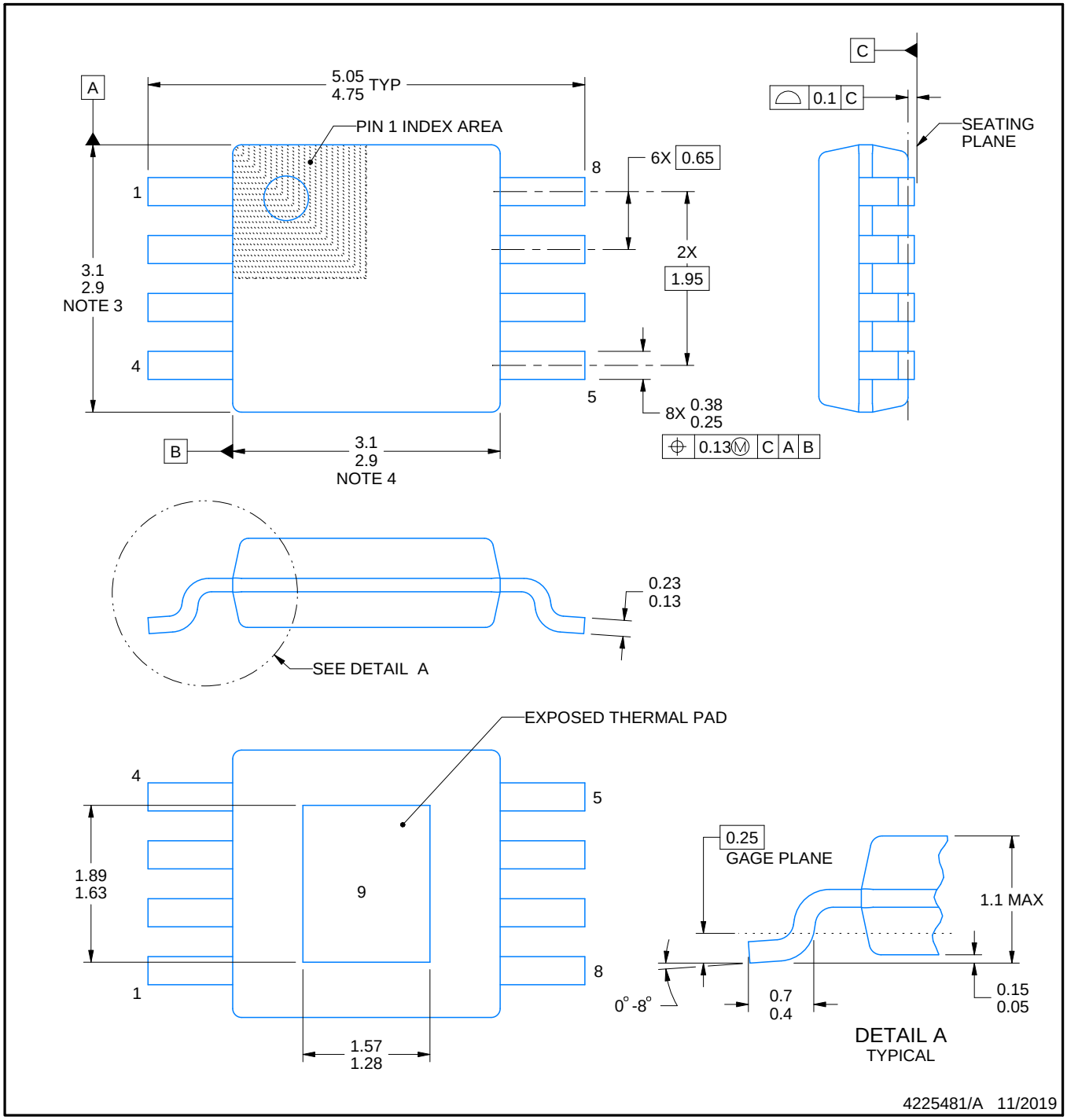
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

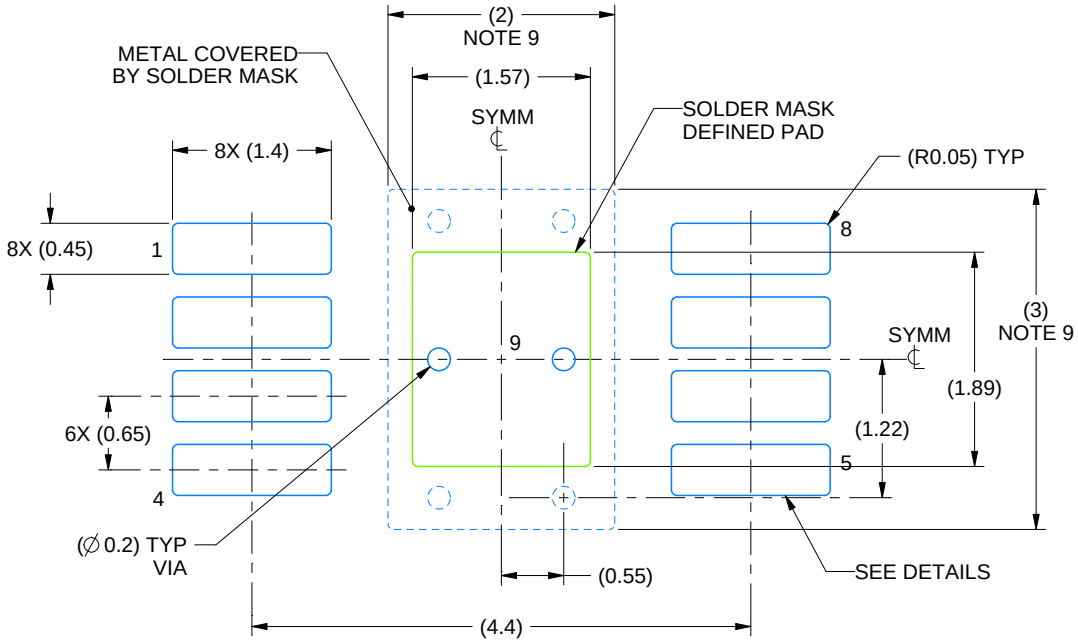
SMALL OUTLINE PACKAGE



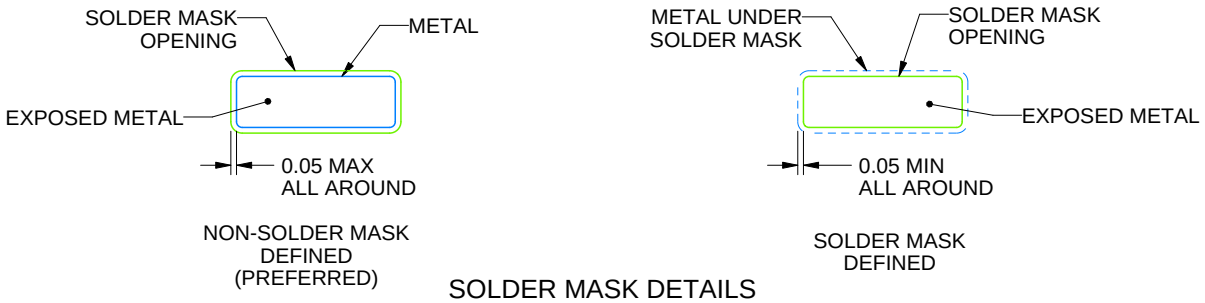
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

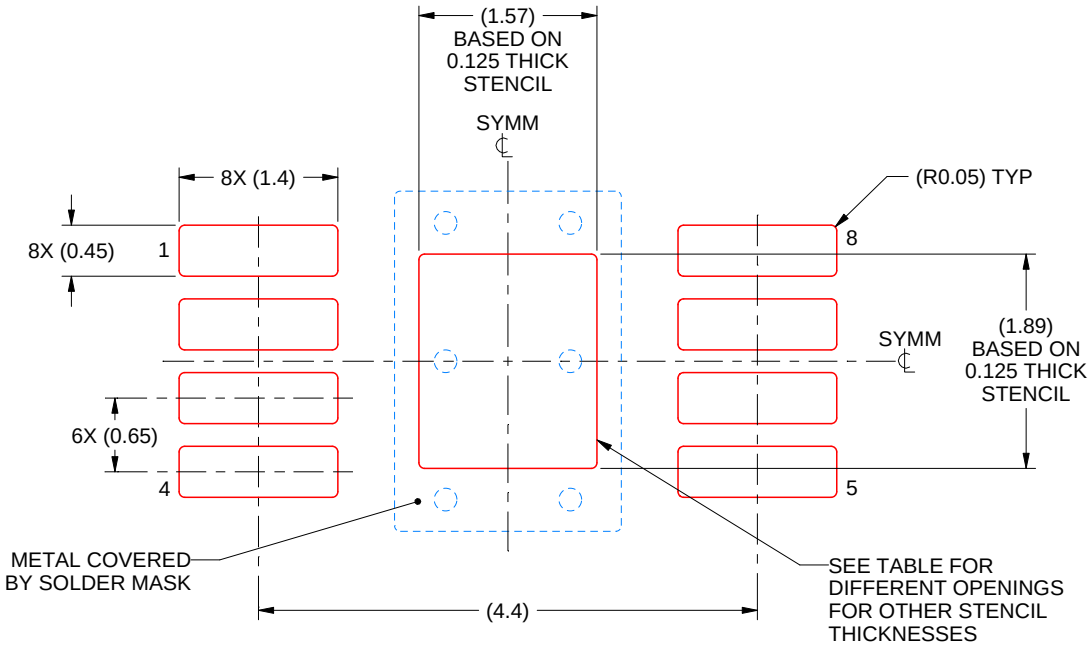


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

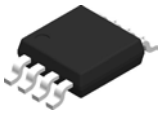
4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

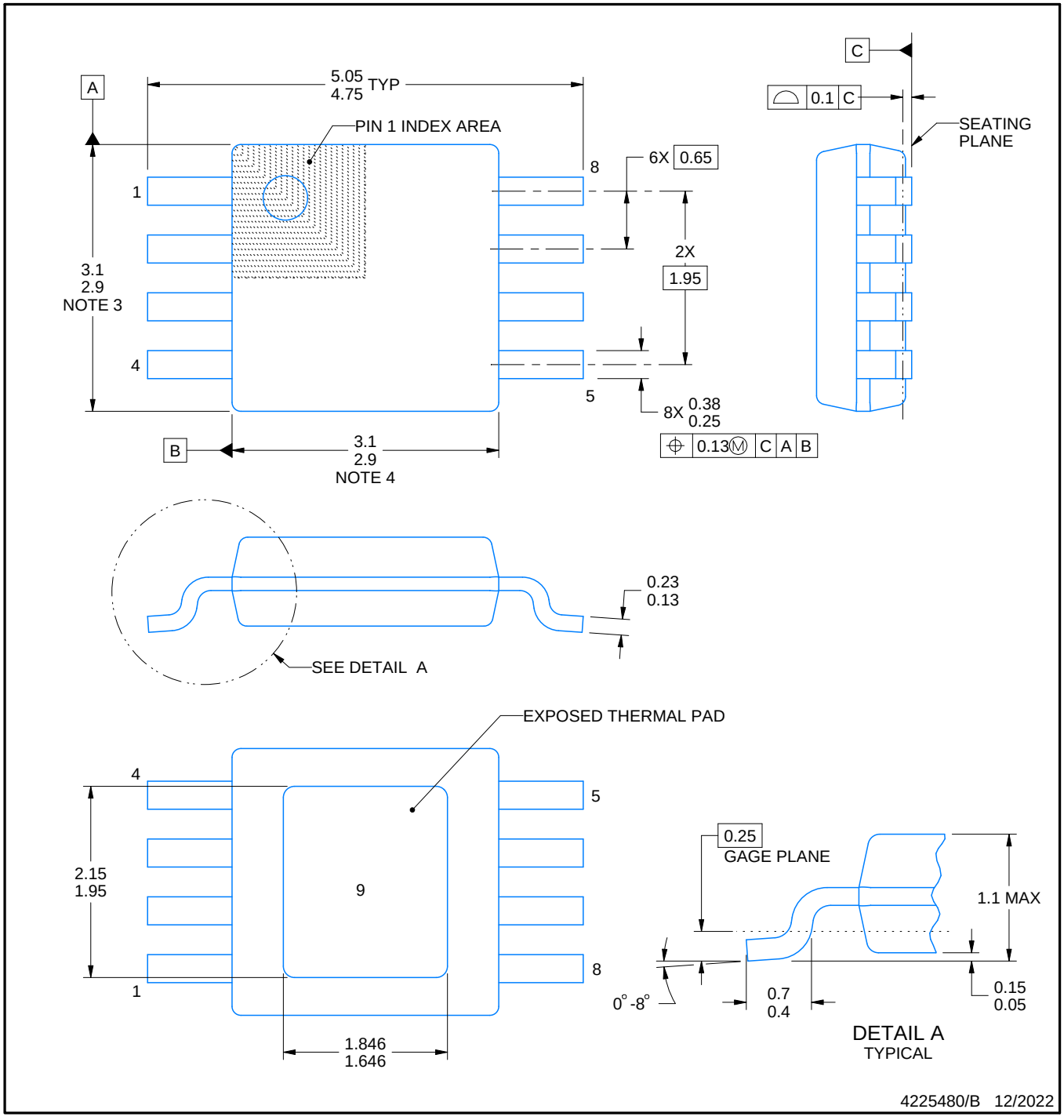
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

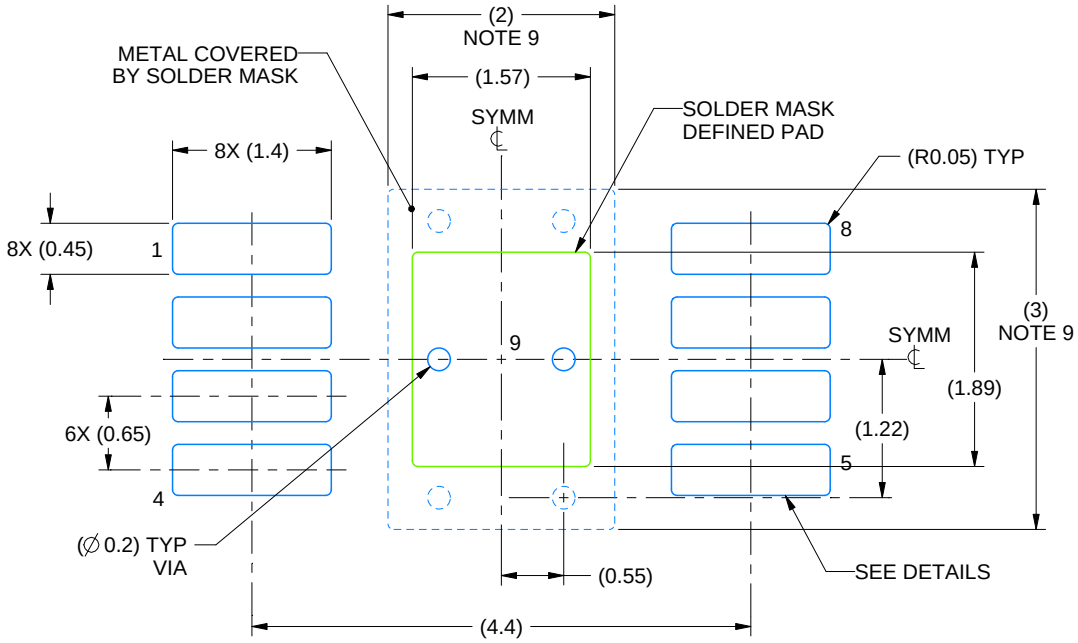
SMALL OUTLINE PACKAGE



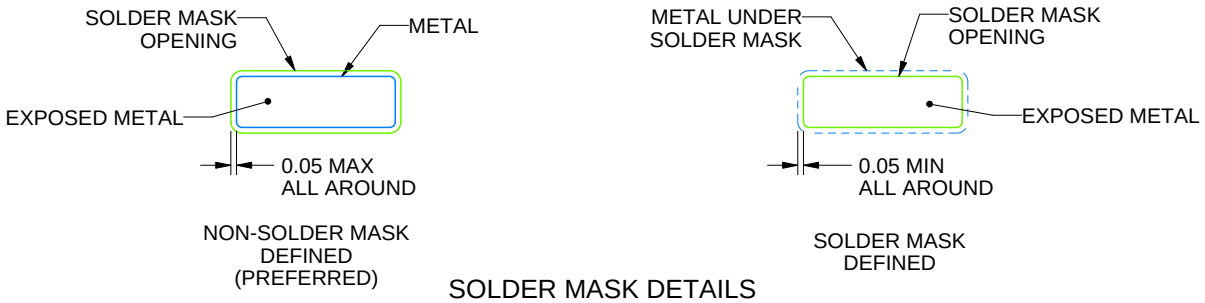
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

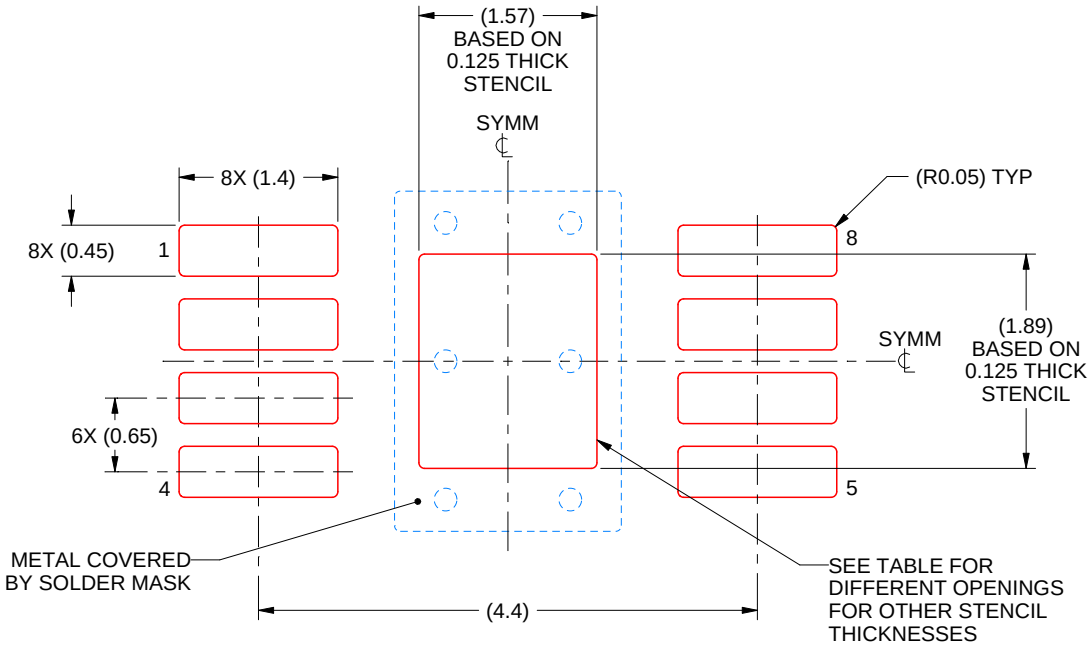


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

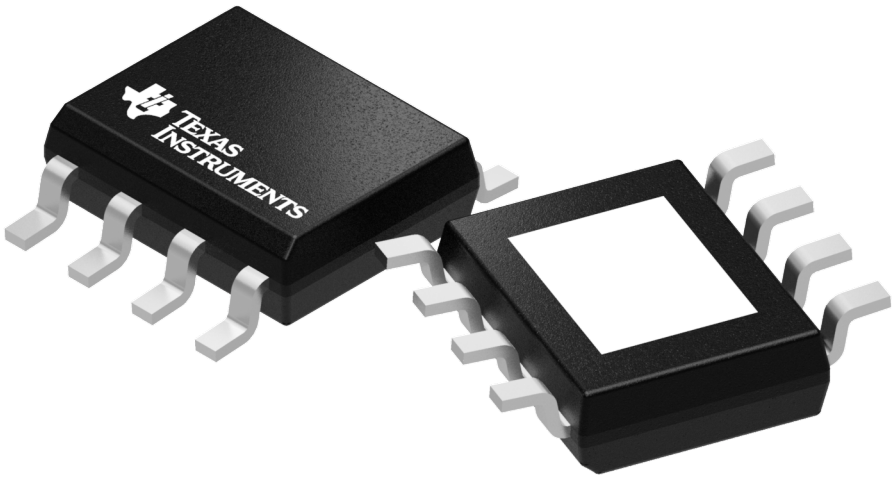
4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



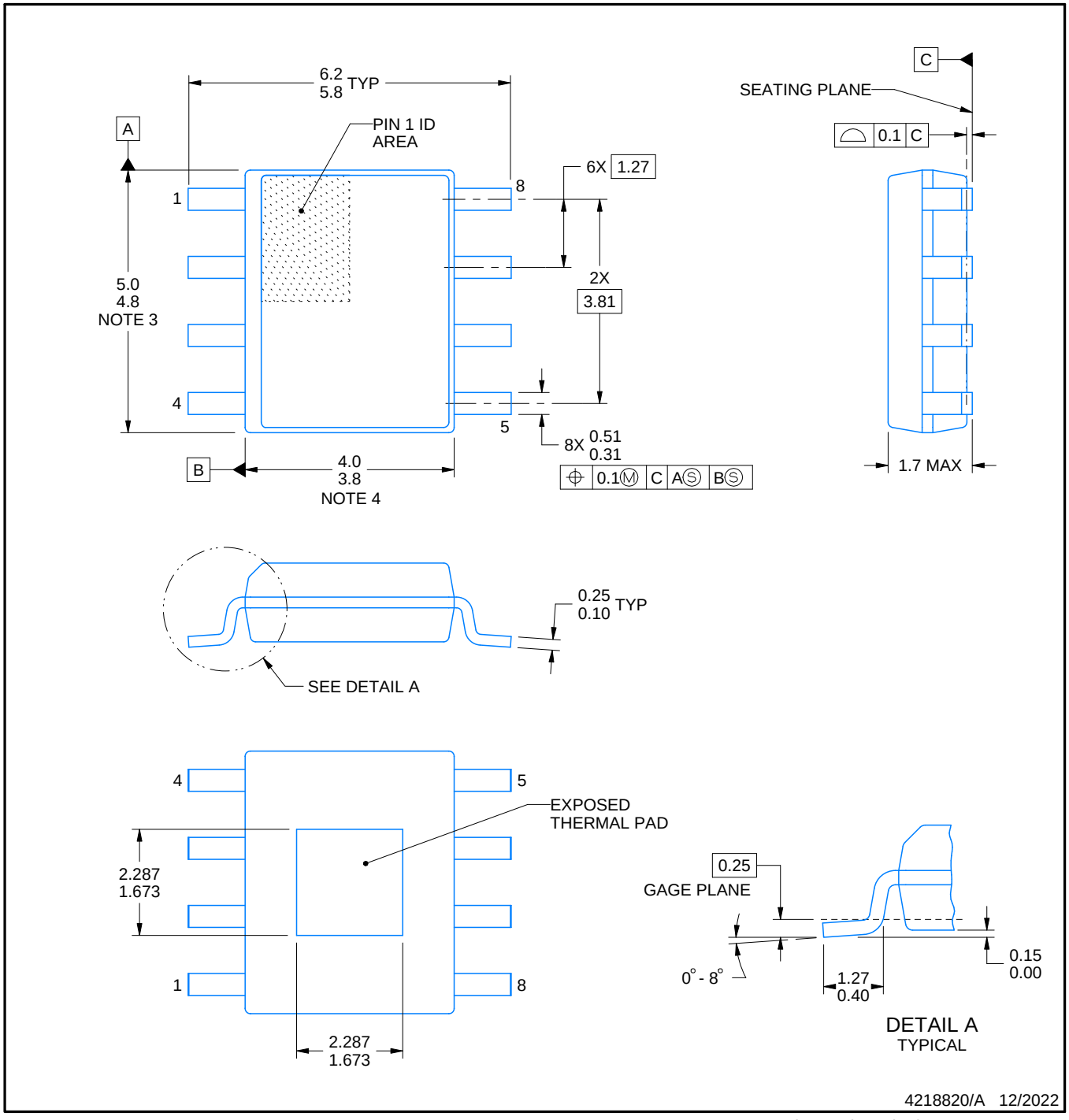
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008D

PowerPAD™ SOIC - 1.7 mm max height

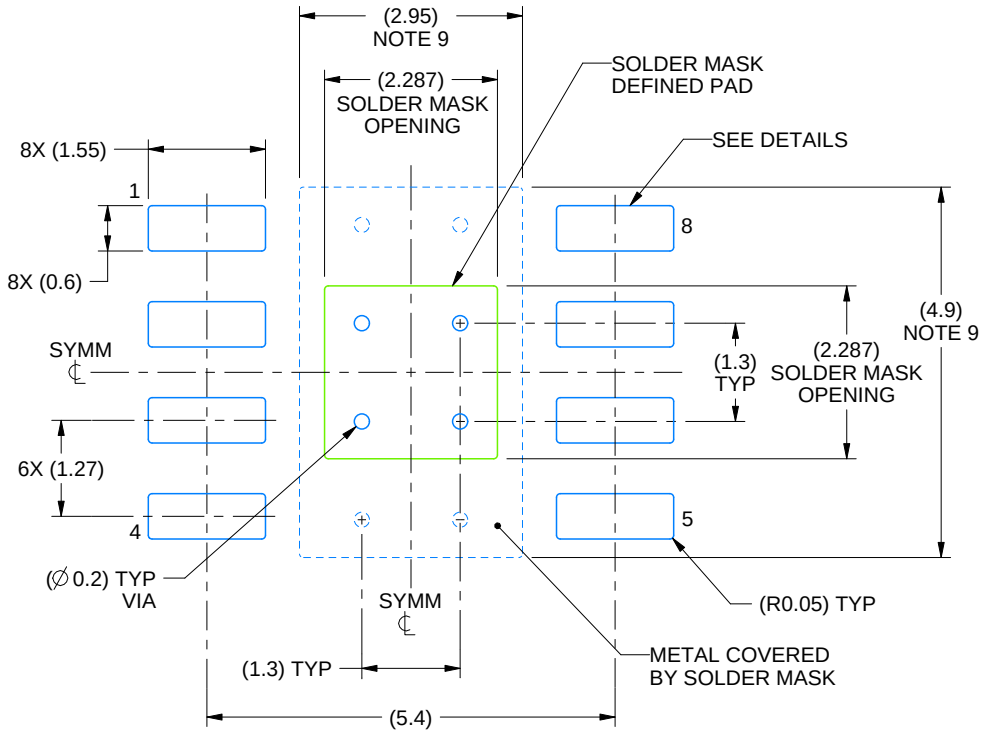
PLASTIC SMALL OUTLINE



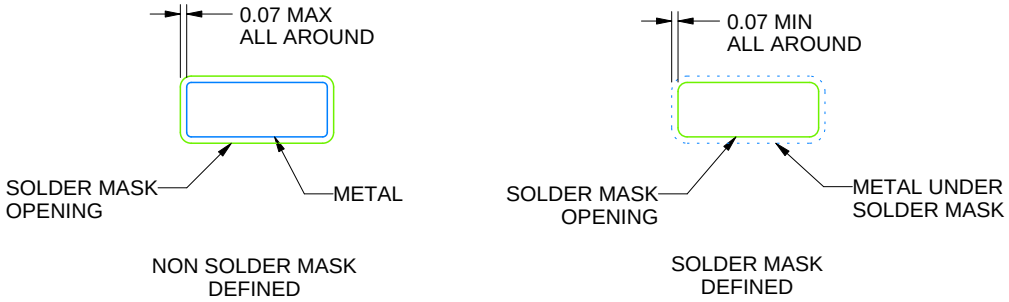
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

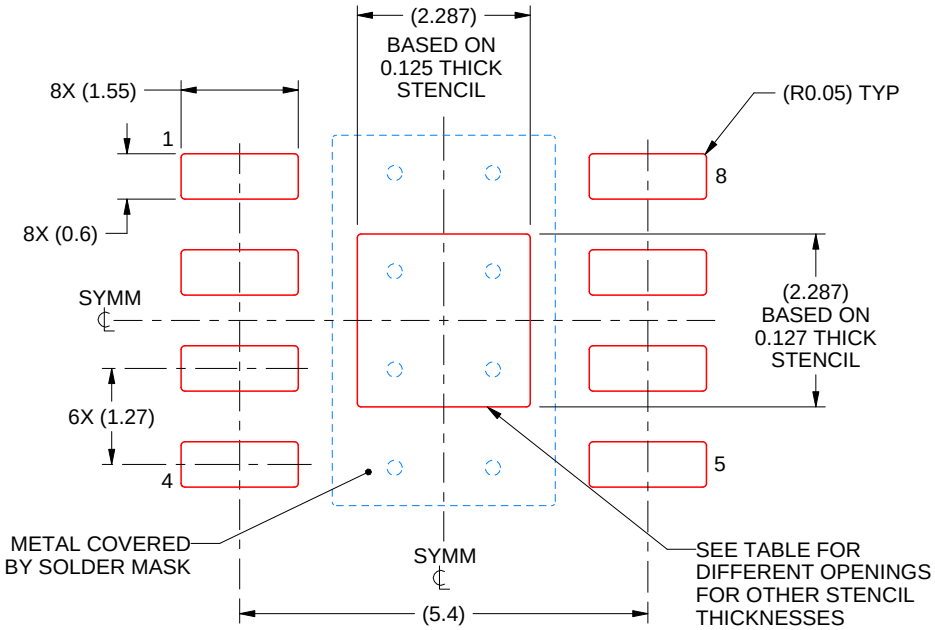


SOLDER MASK DETAILS

4218820/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.557 X 2.557
0.125	2.287 X 2.287 (SHOWN)
0.150	2.088 X 2.088
0.175	1.933 X 1.933

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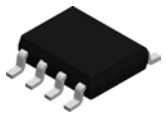
NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

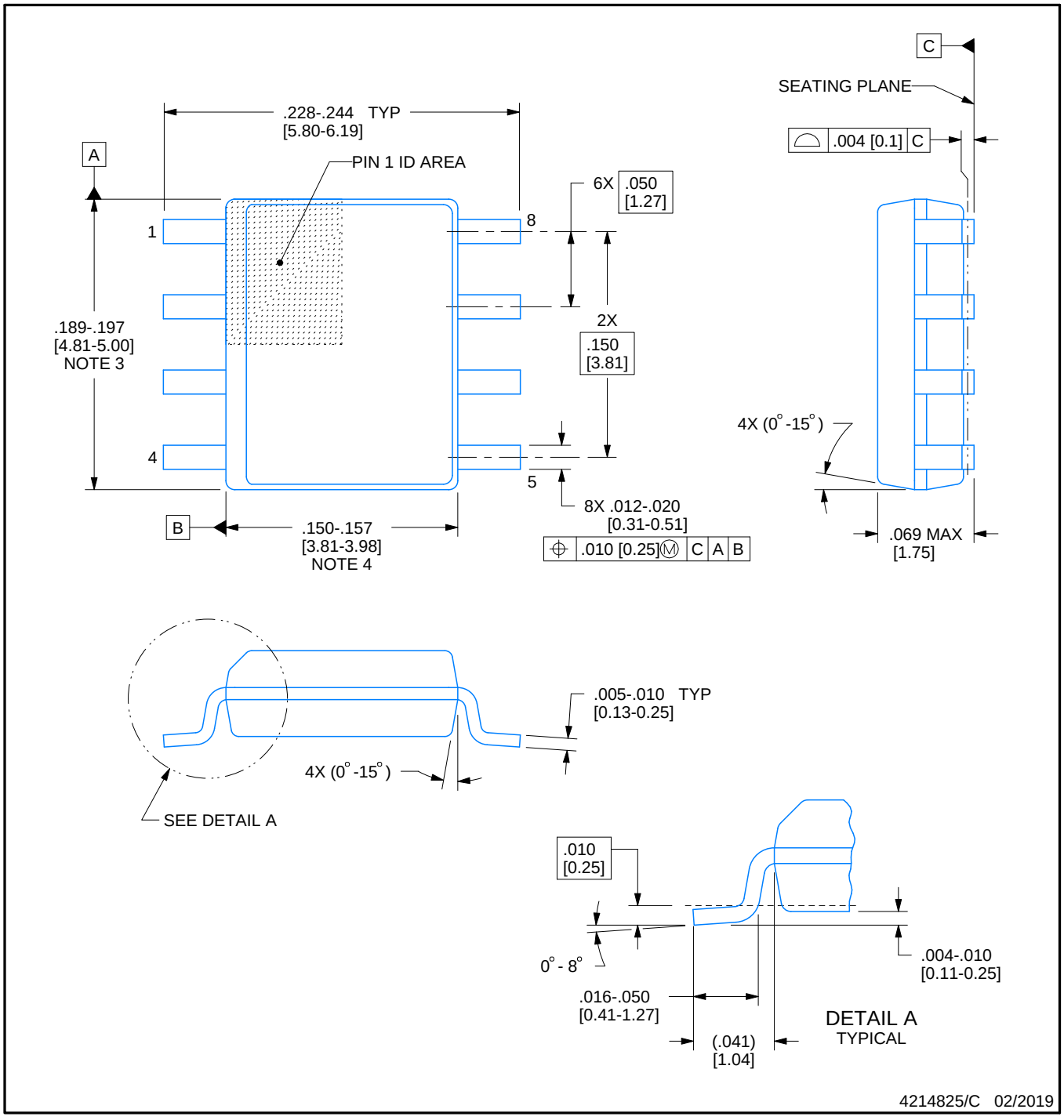


PACKAGE OUTLINE

D0008A

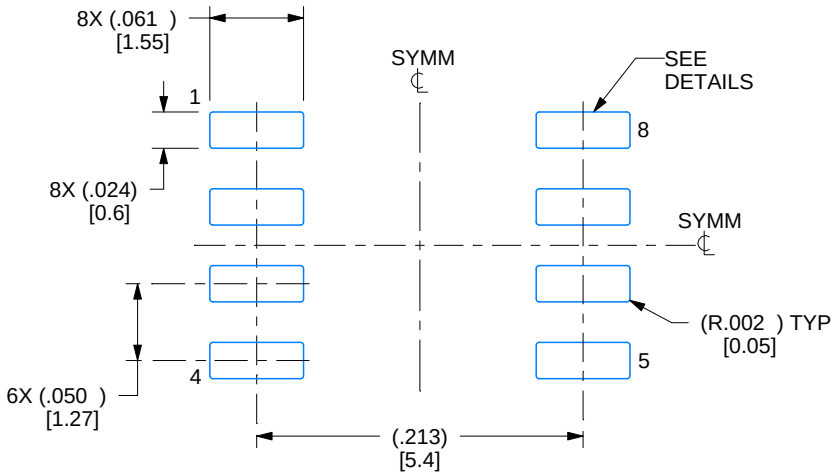
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

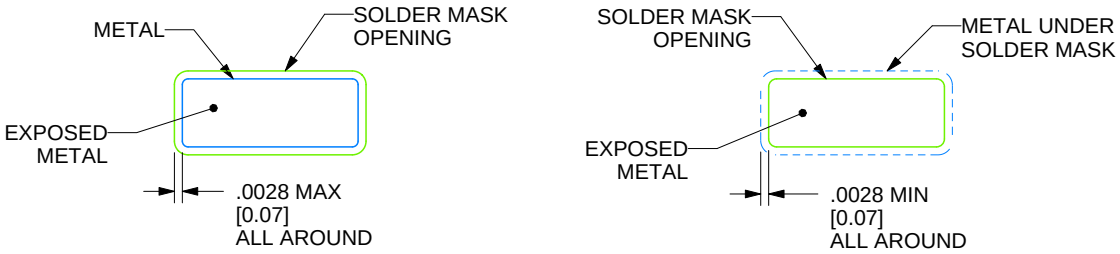


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

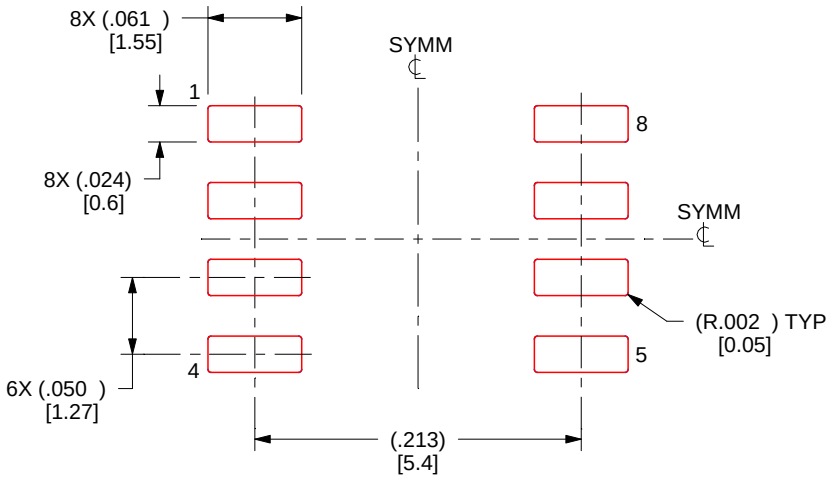
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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