TLC08x-Q1 Wide-Bandwidth High-Output-Drive Single-Supply Operational Amplifiers

1 Features

- Wide Bandwidth: 10 MHz
- High-Output Drive
  - I_{OH}: 57 mA at V_{DD} –1.5 V
  - I_{OL}: 55 mA at 0.5 V
- High Slew Rate
  - SR+: 16 V/μs
  - SR−: 19 V/μs
- Wide Supply Range: 4.5 V to 16 V
- Supply Current: 1.9 mA per Channel
- Low Input Noise Voltage: 8.5 nV/√Hz
- Input Offset Voltage: 60 μV
- Ultra-Small 8-Pin MSOP-PowerPAD Package for TLC082-Q1

2 Applications

- Automotive
- Blind Spot Detection
- Engine Control Units
- Electric Mirrors
- HVAC
- Steering
- Collision Warnings
- Telematics
- Clusters
- Audio
- Industrial
- Instrumentations

3 Description

The TLC08x-Q1 is the first general purpose operational amplifier to highlight TI's BiCMOS technology. The BiMOS family concept is simple: provide an upgrade path for BiFET users who are moving away from dual-supply to single-supply systems and demand higher AC and DC performance. With performance rated from 4.5 V to 16 V across an automotive temperature range (–40°C to 125°C), BiMOS suits a wide range of audio, automotive, industrial, and instrumentation applications.

Developed in TI's patented LBC3 BiCMOS process, the BiMOS amplifiers combine a very high input impedance, low-noise CMOS front end with a high-drive bipolar output stage, thus providing the optimum performance features of both. AC performance improvements over the TL08x-Q1 BiFET predecessors include a bandwidth of 10 MHz and voltage noise of 8.5 nV/√Hz. These features enable the TLC08x-Q1 devices to be suitable for ADAS (such as short-range radar) and body in automotive. The TLC082-Q1 is also suitable in infotainment and cluster as a pre amp in car audio applications.

DC improvements include an ensured V_{ICR} that includes ground, a factor of four reduction in input offset voltage down to 1.5 mV (maximum), and a power-supply rejection improvement of greater than 40 dB to 130 dB. Added to this list of impressive features is the ability to drive ±50-mA loads comfortably from an ultrasmall-footprint MSOP PowerPAD™ package, which positions the TLC08x-Q1 as the ideal high-performance, general-purpose operational amplifier family.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC082-Q1	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm
TLC084-Q1	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Operational Amplifier

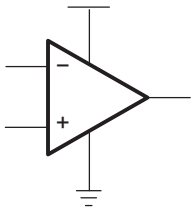


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2016) to Revision E — **Page**

- Changed y-axis label from Phase Margin to Gain Margin for the *Gain Margin vs Load Capacitance* graph ... 11

Changes from Revision C (January 2016) to Revision D — **Page**

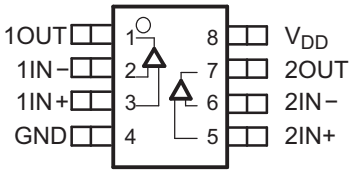
- Deleted the *Maximum Power Dissipation vs Free-Air Temperature* graph ... 25
- Added the *Receiving Notification of Documentation Updates* section ... 27

Changes from Revision B (May 2011) to Revision C — **Page**

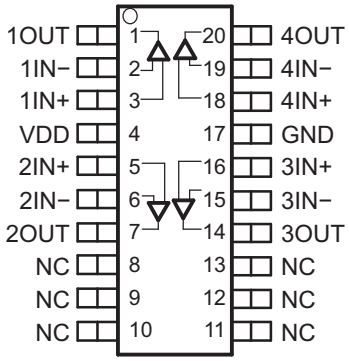
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Ultralow-Power Shutdown Mode bullet from *Features* ... 1
- Deleted Typical Pin Indicators image from *Pin Configuration and Functions* ... 3
- Deleted VIH and VIL rows in *Recommended Operating Conditions* ... 4
- Deleted Shutdown Forward and Reverse Isolation vs Frequency graphs (formerly Figures 38 and 39) from *Typical Characteristics* ... 14

5 Pin Configuration and Functions

DGN Package
8-Pin MSOP With PowerPAD
Top View



PWP Package
20-Pin HTSSOP
Top View



NC − No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	TLC082-Q1	TLC084-Q1		
1IN+	3	3	I	Noninverting input, Channel 1
1IN–	2	2	I	Inverting input, Channel 1
1OUT	1	1	O	Output, Channel 1
2IN+	5	5	I	Noninverting input, Channel 2
2IN–	6	6	I	Inverting input, Channel 2
2OUT	7	7	O	Output, Channel 2
3IN+	—	16	I	Noninverting input, Channel 3
3IN–	—	15	I	Inverting input, Channel 3
3OUT	—	14	O	Output, Channel 3
4IN+	—	18	I	Noninverting input, Channel 4
4IN–	—	19	I	Inverting input, Channel 4
4OUT	—	20	O	Output, Channel 4
GND	4	17	—	Negative (lowest) power supply
NC	—	8 to13	—	Non-connect
VDD	8	4	I	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage(2)	–0.3	17	V
V_{ID}	Differential input voltage		$\pm V_{DD}$	V
	Continuous total power dissipation	See *Thermal Information*		
T_J	Operating junction temperature	–40	125	°C
T_A	Operating ambient temperature	–40	125	°C
$T_{J(max)}$	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 4, 5, and 8)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{DD}	Supply voltage	Single supply	4.5	16	V
		Split supply	±2.25	±8	
V_{ICR}	Common-mode input voltage		GND	V_{DD} – 2	V
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLC082-Q1 DGN (MSOP-PowerPAD) 8-PIN	TLC084-Q1 PWP (HTSSOP) 20-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.1	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.2	46.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35.3	22.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.1	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	35.9	26.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.9	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_{DD} = 5 V

V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J(1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		390	1900	μV
				Full range			3300	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω				1.2		μV/°C
I_{IO}	Input offset current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		1.9	50	pA
				Full range			700	
I_{IB}	Input bias current	V_{DD} = 5 V, V_{IC} = 2.5 V, V_O = 2.5 V, R_S = 50 Ω		25°C		3	50	pA
				Full range			700	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω		25°C	0 to 3	0 to 3.5		V
				Full range	0 to 3	0 to 3.5		
V_{OH}	High-level output voltage	V_{IC} = 2.5 V	I_{OH} = –1 mA	25°C	4.1	4.3		V
				Full range	3.9			
			I_{OH} = –20 mA	25°C	3.7	4		
				Full range	3.5			
			I_{OH} = –35 mA	25°C	3.4	3.8		
				Full range	3.2			
			I_{OH} = –50 mA	25°C	3.2	3.6		
				Full range	3			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V	I_{OL} = 1 mA	25°C		0.18	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.39	
				Full range			0.45	
			I_{OL} = 35 mA	25°C		0.43	0.55	
				Full range			0.7	
			I_{OL} = 50 mA	25°C		0.45	0.63	
				Full range			0.7	
I_{OS}	Short-circuit output current	Sourcing		25°C		100		mA
		Sinking				100		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail				55		
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ		25°C	100	120		dB
				Full range	100			
$r_{j(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		22.9		pF
Z_O	Closed-loop output impedance	f = 10 kHz, A_V = 10		25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 3 V, R_S = 50 Ω		25°C	70	110		dB
				Full range	70			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.5 V to 16 V, V_{IC} = V_{DD}/2, No load		25°C	80	100		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 2.5 V, No load		25°C		1.8	2.5	mA
				Full range			3.5	

(1) Full range is –40°C to 125°C.

6.6 Electrical Characteristics: V_{DD} = 12 V

V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω		25°C		390	1900	μV
				Full range			3300	
α_{VIO}	Temperature coefficient of input offset voltage	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω				1.2		μV/°C
I_{IO}	Input offset current	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω		25°C		1.5	50	pA
				Full range			700	
I_{IB}	Input bias current	V_{DD} = 12 V, V_{IC} = 6 V, V_O = 6 V, R_S = 50 Ω		25°C		3	50	pA
				Full range			700	
V_{ICR}	Common-mode input voltage	R_S = 50 Ω		25°C	0 to 10	0 to 10.5		V
				Full range	0 to 10	0 to 10.5		
V_{OH}	High-level output voltage	V_{IC} = 6 V	I_{OH} = –1 mA	25°C	11.1	11.2		V
				Full range	11			
			I_{OH} = –20 mA	25°C	10.8	11		
				Full range	10.7			
			I_{OH} = –35 mA	25°C	10.6	10.7		
				Full range	10.3			
			I_{OH} = –50 mA	25°C	10.3	10.5		
				Full range	10.1			
V_{OL}	Low-level output voltage	V_{IC} = 6 V	I_{OL} = 1 mA	25°C		0.17	0.25	V
				Full range			0.35	
			I_{OL} = 20 mA	25°C		0.35	0.45	
				Full range			0.55	
			I_{OL} = 35 mA	25°C		0.4	0.52	
				Full range			0.6	
			I_{OL} = 50 mA	25°C		0.45	0.6	
				Full range			0.7	
I_{OS}	Short-circuit output current	Sourcing		25°C		150		mA
		Sinking				150		
I_O	Output current	V_{OH} = 1.5 V from positive rail		25°C		57		mA
		V_{OL} = 0.5 V from negative rail				55		
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)}$ = 8 V, R_L = 10 kΩ		25°C	110	130		dB
				Full range	110			
$r_{j(d)}$	Differential input resistance			25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 10 kHz		25°C		21.6		pF
Z_O	Closed-loop output impedance	f = 10 kHz, A_V = 10		25°C		0.25		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 10 V, R_S = 50 Ω		25°C	80	110		dB
				Full range	80			
k_{SVR}	Supply voltage rejection ratio (ΔV_{DD} / ΔV_{IO})	V_{DD} = 4.5 V to 16 V, V_{IC} = V_{DD} / 2, No load		25°C	80	100		dB
				Full range	80			
I_{DD}	Supply current (per channel)	V_O = 7.5 V, No load		25°C		1.9	2.9	mA
				Full range			3.5	

(1) Full range is –40°C to 125°C.

6.7 Operating Characteristics: V_{DD} = 5 V

V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J(1)	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 50 pF, R_L = 10 kΩ		25°C	10	16		V/μs
				Full range	9			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 0.8 V, C_L = 50 pF, R_L = 10 kΩ		25°C	11	19		V/μs
				Full range	8.5			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		12		nV/√Hz
		f = 1 kHz				8.5		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 3 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002%		—
			A_V = 10			0.012%		
			A_V = 100			0.085%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ		25°C		10		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.18		μs
			0.01%			0.39		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.18		
			0.01%			0.39		
φ_m	Phase margin	R_L = 10 kΩ	C_L = 50 pF	25°C		32		°
			C_L = 0 pF			40		
	Gain margin	R_L = 10 kΩ	C_L = 50 pF	25°C		2.2		dB
			C_L = 0 pF			3.3		

(1) Full range is –40°C to 125°C.

6.8 Operating Characteristics: V_{DD} = 12 V

V_{DD} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J(1)	MIN	TYP	MAX	UNIT
SR+	Positive slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 50 pF, R_L = 10 kΩ		25°C	10	16		V/μs
				Full range	9.5			
SR–	Negative slew rate at unity gain	$V_{O(PP)}$ = 2 V, C_L = 50 pF, R_L = 10 kΩ		25°C	12.5	19		V/μs
				Full range	10			
V_n	Equivalent input noise voltage	f = 100 Hz		25°C		14		nV/√Hz
		f = 1 kHz				8.5		
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		fA/√Hz
THD+N	Total harmonic distortion plus noise	$V_{O(PP)}$ = 8 V, R_L = 10 kΩ and 250 Ω, f = 1 kHz	A_V = 1	25°C		0.002%		—
			A_V = 10			0.005%		
			A_V = 100			0.022%		
	Gain-bandwidth product	f = 10 kHz, R_L = 10 kΩ		25°C		10		MHz
t_s	Settling time	$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 10 pF, R_L = 10 kΩ	0.1%	25°C		0.17		μs
			0.01%			0.22		
		$V_{(STEP)PP}$ = 1 V, A_V = –1, C_L = 47 pF, R_L = 10 kΩ	0.1%			0.17		
			0.01%			0.29		
φ_m	Phase margin	R_L = 10 kΩ	C_L = 50 pF	25°C		37		deg
			C_L = 0 pF			42		
	Gain margin	R_L = 10 kΩ	C_L = 50 pF	25°C		3.1		dB
			C_L = 0 pF			4		

(1) Full range is –40°C to 125°C.

6.9 Typical Characteristics

Table 1. Table of Graphs

GRAPH NAME			FIGURE NO.
V_{IO}	Input offset voltage	vs Common-mode input voltage	Figure 1, Figure 2
I_{IO}	Input offset current	vs Free-air temperature	Figure 3
I_{IB}	Input bias current	vs Free-air temperature	Figure 4
V_{OH}	High-level output voltage	vs High-level output current	Figure 5, Figure 7
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 6, Figure 8
Z_O	Output impedance	vs Frequency	Figure 9
I_{DD}	Supply current	vs Supply voltage	Figure 10
PSRR	Power supply rejection ratio	vs Frequency	Figure 11
CMRR	Common-mode rejection ratio	vs Frequency	Figure 12
V_n	Equivalent input noise voltage	vs Frequency	Figure 13
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	Figure 14, Figure 15
	Crosstalk	vs Frequency	Figure 16
	Differential voltage gain and Phase	vs Frequency	Figure 17, Figure 18
φ_m	Phase margin	vs Load capacitance	Figure 19, Figure 20
	Gain margin	vs Load capacitance	Figure 21, Figure 22
	Gain-bandwidth product	vs Supply voltage	Figure 23
SR	Slew rate	vs Supply voltage	Figure 24
		vs Free-air temperature	Figure 25, Figure 26
THD+N	Total harmonic distortion plus noise	vs Frequency	Figure 27, Figure 28
		vs Peak-to-peak output voltage	Figure 29, Figure 30
	Large-signal follower pulse response		Figure 31, Figure 32
	Small-signal follower pulse response		Figure 33
	Large-signal inverting pulse response		Figure 34, Figure 34
	Small-signal inverting pulse response		Figure 36

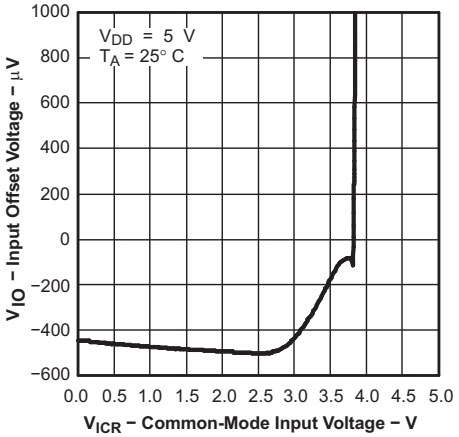


Figure 1. Input Offset Voltage vs Common-Mode Input Voltage

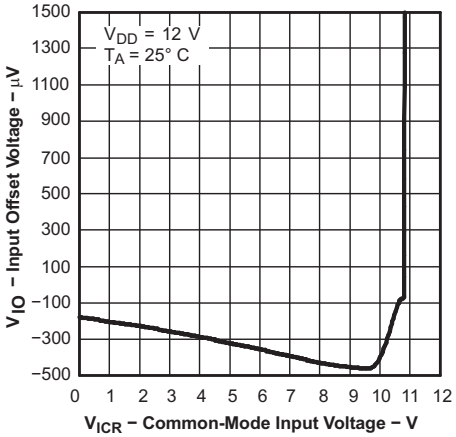


Figure 2. Input Offset Voltage vs Common-Mode Input Voltage

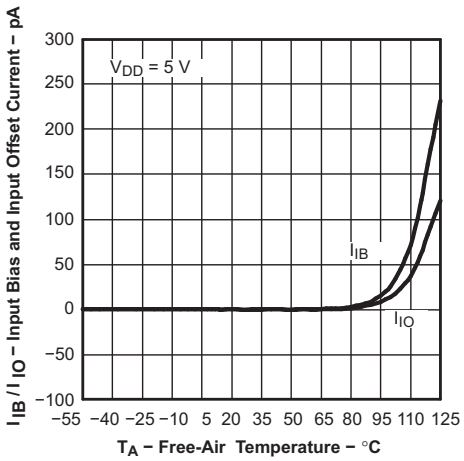


Figure 3. Input Bias Current and Input Offset Current vs Free-Air Temperature

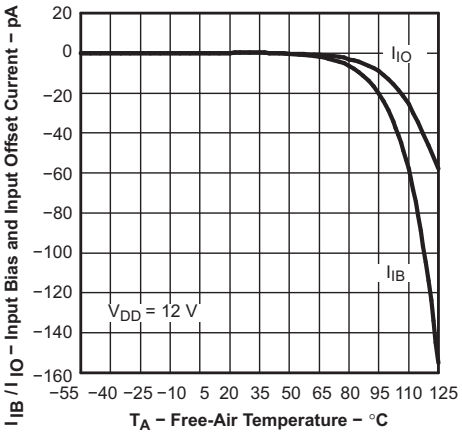


Figure 4. Input Bias Current and Input Offset Current vs Free-Air Temperature

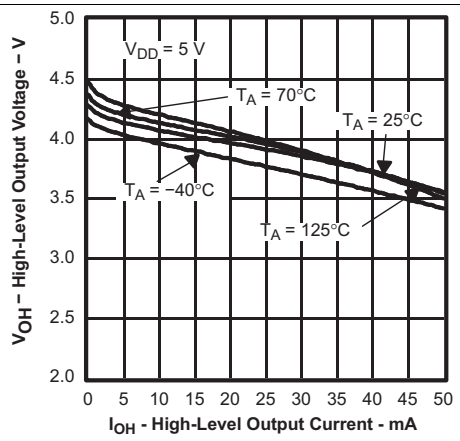


Figure 5. High-Level Output Voltage vs High-Level Output Current

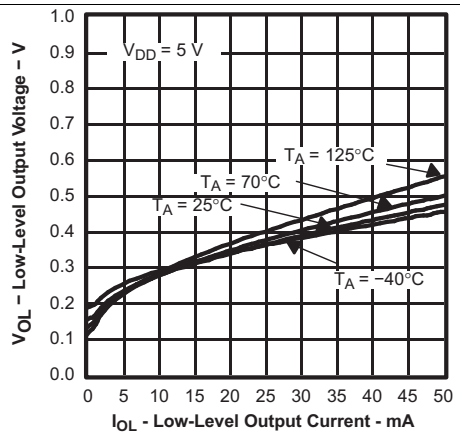


Figure 6. Low-Level Output Voltage vs Low-Level Output Current

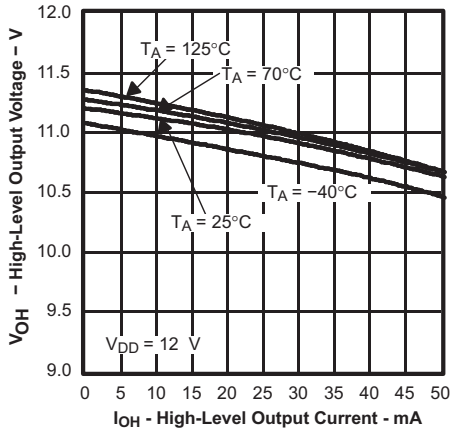


Figure 7. High-Level Output Voltage vs High-Level Output Current

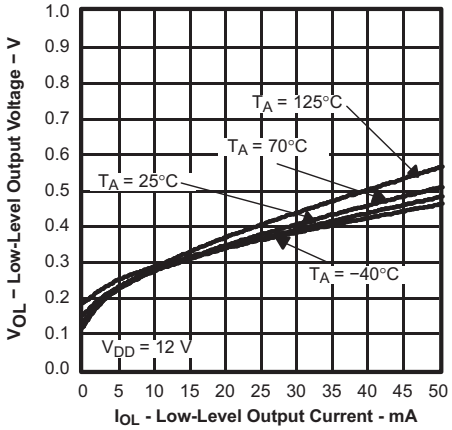


Figure 8. Low-Level Output Voltage vs Low-Level Output Current

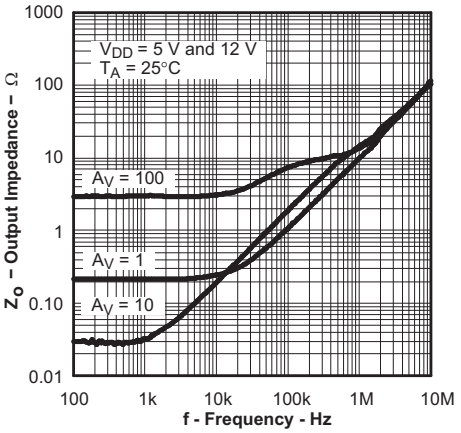


Figure 9. Output Impedance vs Frequency

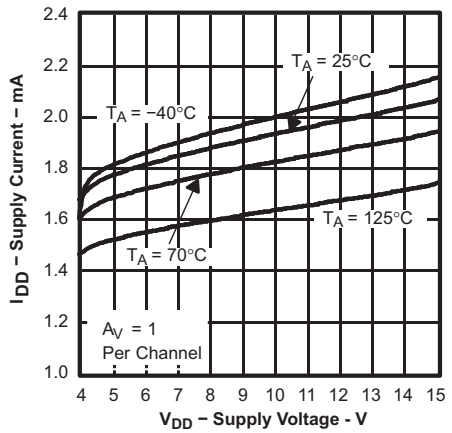


Figure 10. Supply Current vs Supply Voltage

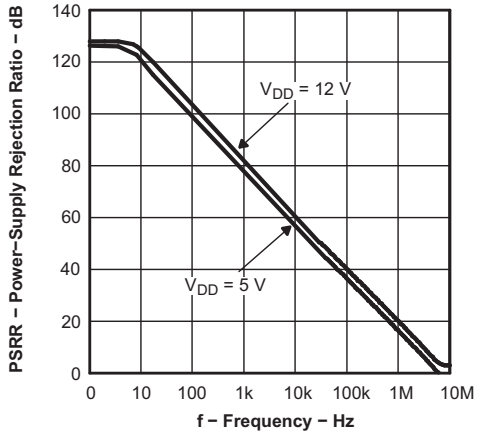


Figure 11. Power-Supply Rejection Ratio vs Frequency

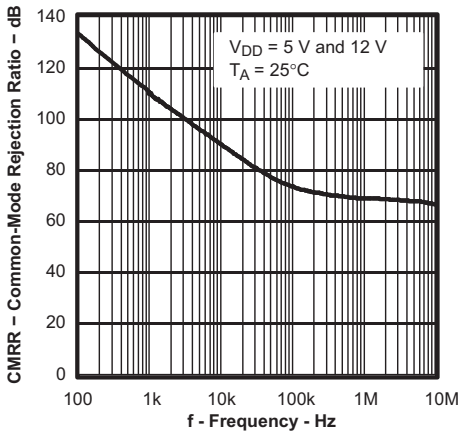


Figure 12. Common-Mode Rejection Ration vs Frequency

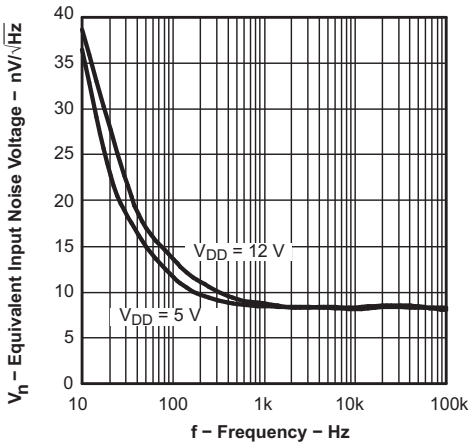


Figure 13. Equivalent Input Noise Voltage vs Frequency

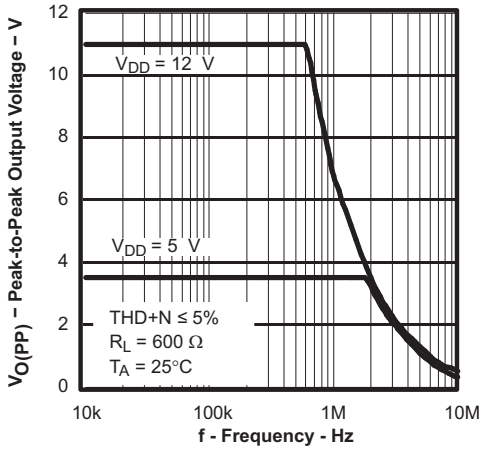


Figure 14. Peak-to-Peak Output Voltage vs Frequency

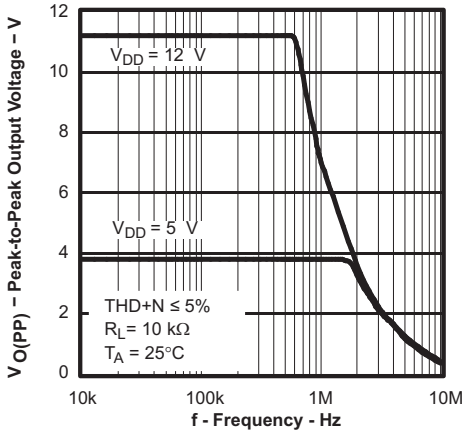


Figure 15. Peak-to-Peak Output Voltage vs Frequency

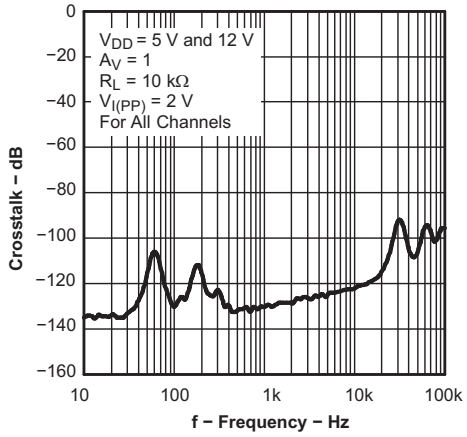


Figure 16. Crosstalk vs Frequency

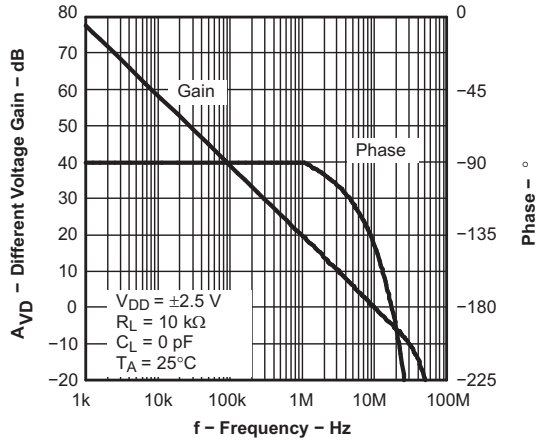


Figure 17. Differential Voltage Gain and Phase vs Frequency

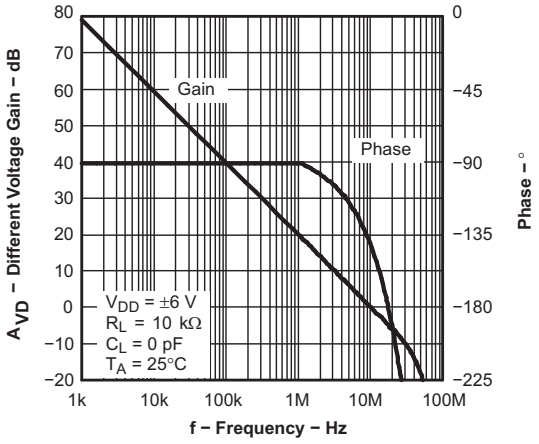


Figure 18. Differential Voltage Gain and Phase vs Frequency

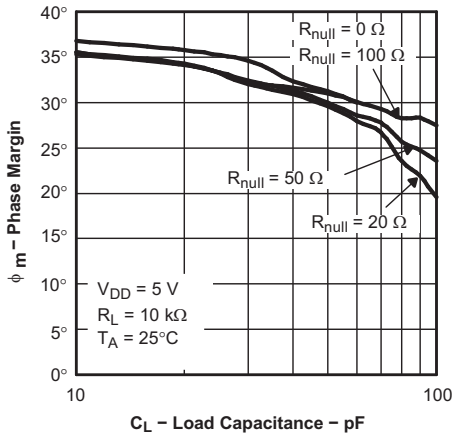


Figure 19. Phase Margin vs Load Capacitance

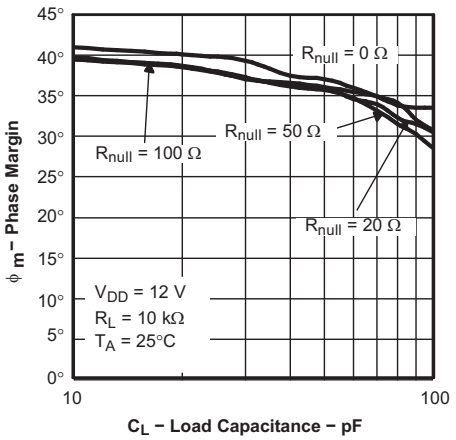


Figure 20. Phase Margin vs Load Capacitance

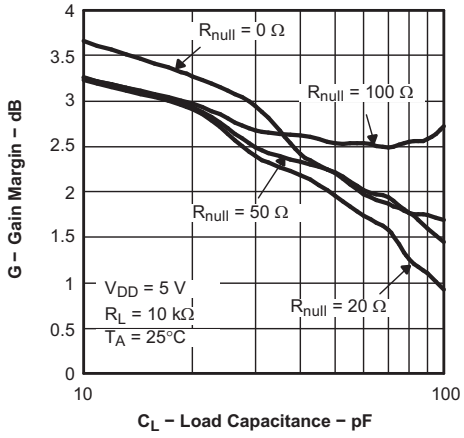


Figure 21. Gain Margin vs Load Capacitance

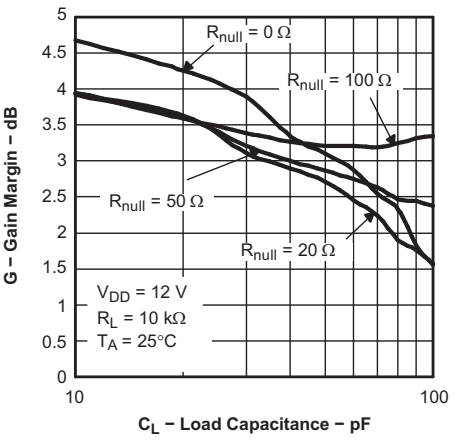


Figure 22. Gain Margin vs Load Capacitance

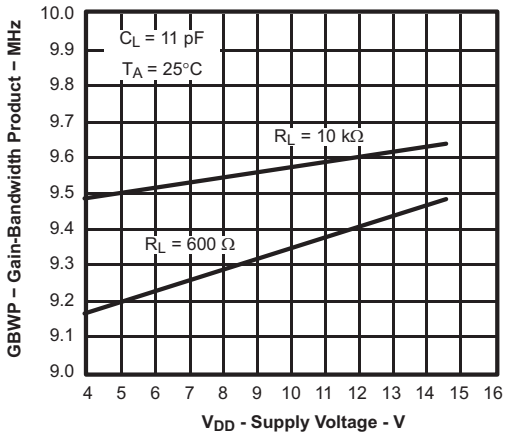


Figure 23. Gain-Bandwidth Product vs Supply Voltage

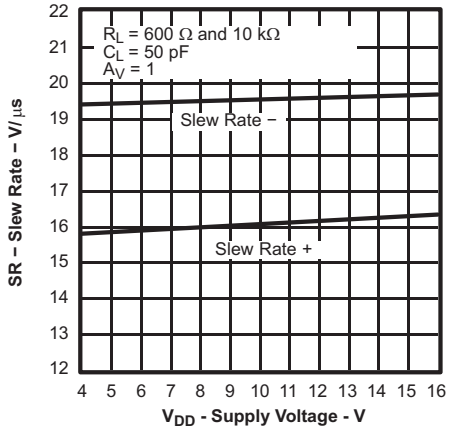


Figure 24. Slew Rate vs Supply Voltage

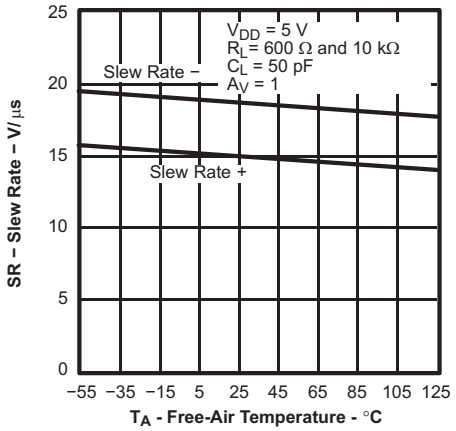


Figure 25. Slew Rate vs Free-Air Temperature

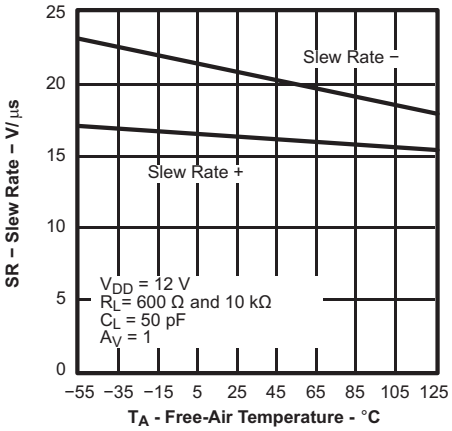


Figure 26. Slew Rate vs Free-Air Temperature

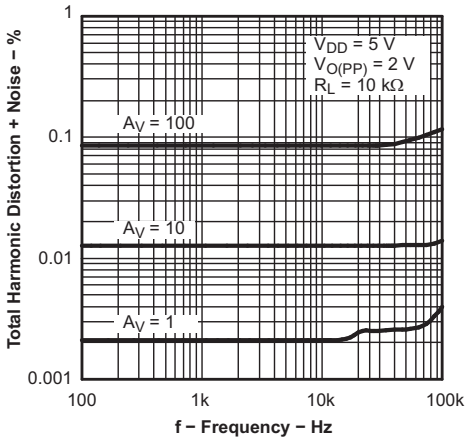


Figure 27. Total Harmonic Distortion + Noise vs Frequency

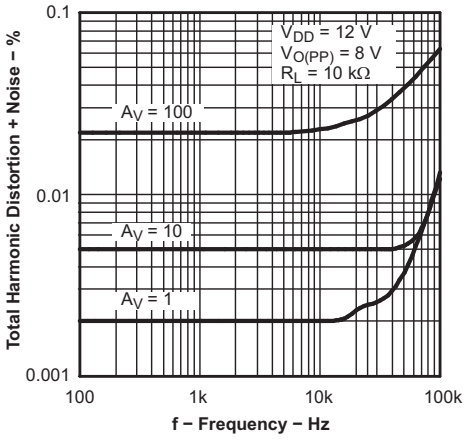


Figure 28. Total Harmonic Distortion + Noise Frequency

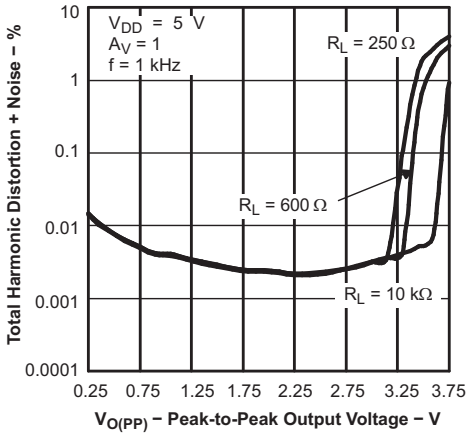


Figure 29. Total Harmonic Distortion Plus Peak-to-Peak Output Voltage

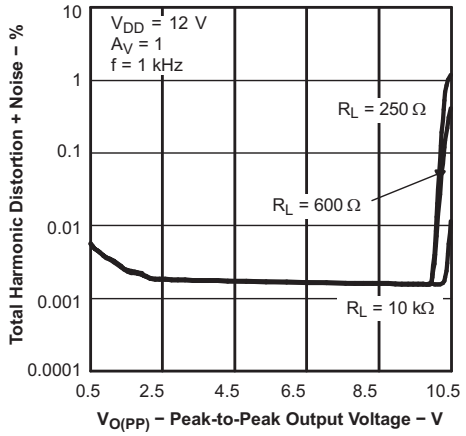


Figure 30. Total Harmonic Distortion Plus Peak-to-Peak Output Voltage

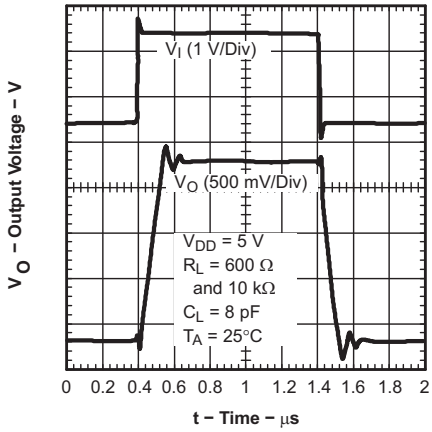


Figure 31. Large-Signal Follower Pulse Response

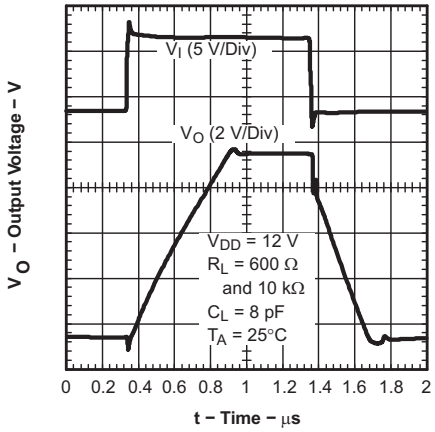


Figure 32. Large-Signal Follower Pulse Response

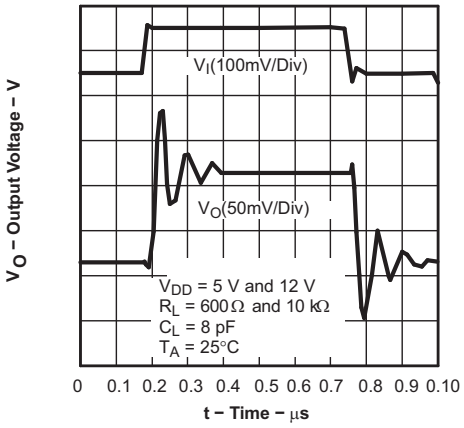


Figure 33. Small-Signal Follower Pulse Response

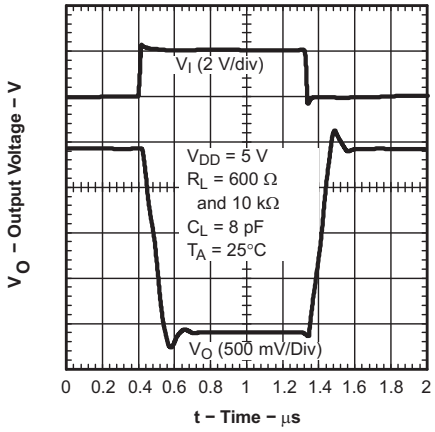


Figure 34. Large-Signal Follower Pulse Response

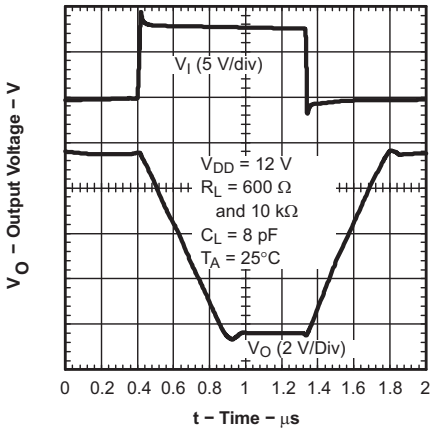


Figure 35. Large-Signal Inverting Pulse Response

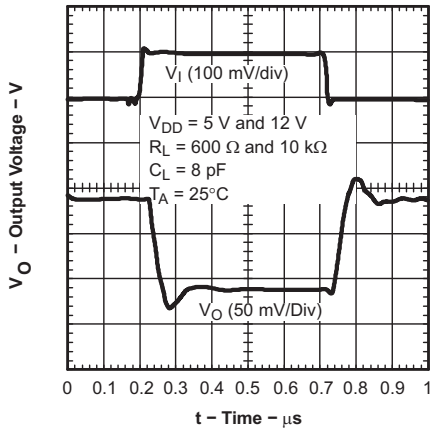


Figure 36. Small-Signal Inverting Pulse Response

7 Parameter Measurement Information

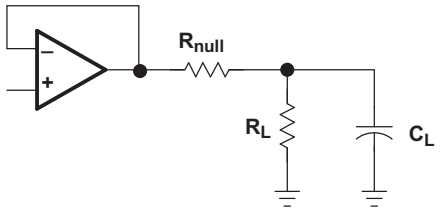


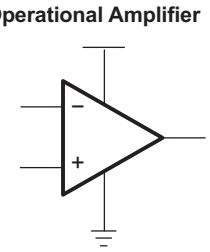
Figure 37. Voltage Follower Circuit

8 Detailed Description

8.1 Overview

The TLC08x-Q1 BiCMOS amplifiers provide an upgrade path for BiFET users who are moving away from dual-supply to single-supply systems and demand higher AC and DC performance. With performance rated from 4.5 V to 16 V across an automotive temperature range (–40°C to 125°C), BiMOS suits a wide range of audio, automotive, industrial, and instrumentation applications. BiCMOS amplifiers combine a very high input low-noise CMOS front end drive bipolar output stage, thus providing the optimum performance features of both. AC performance include a bandwidth of 10 MHz and voltage noise of 8.5 nV/$\sqrt{\text{Hz}}$.

8.2 Functional Block Diagram



8.3 Feature Description

The TLC08x-Q1 family features 10-MHz bandwidth and voltage noise of 8.5 nV/$\sqrt{\text{Hz}}$ with performance rated from 4.5 V to 16 V across an automotive temperature range (–40°C to 125°C). BiMOS suits a wide range of audio, automotive, industrial, and instrumentation applications.

8.4 Device Functional Modes

The TLC08x-Q1 family of devices is powered on when the supply is connected. The device can operate with single or dual supply, depending on the application. The device is in its full performance once the supply is above the recommended value.

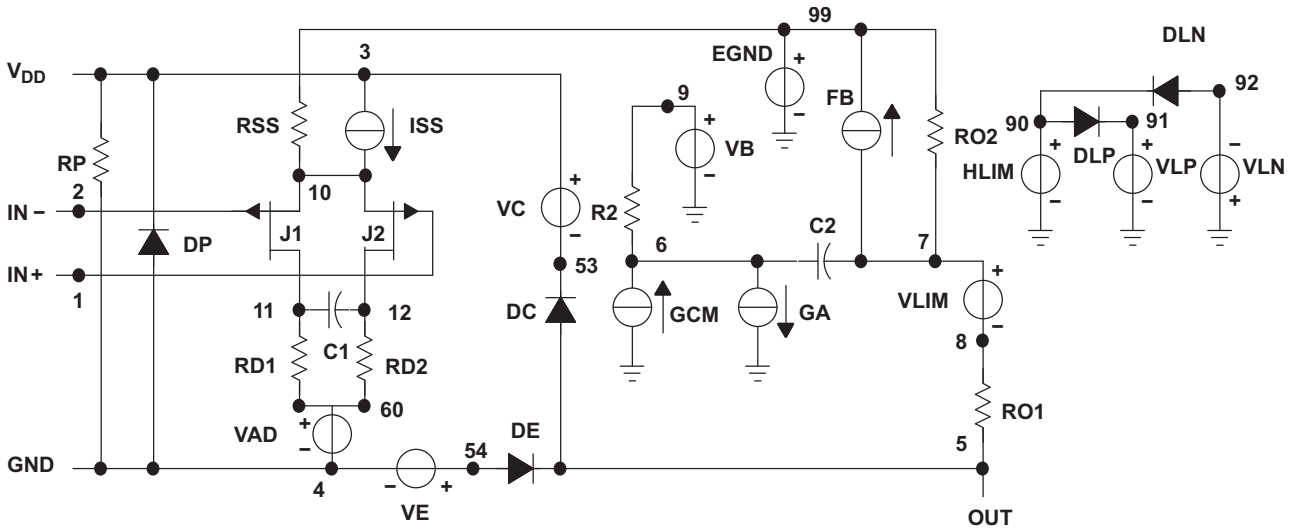
8.5 Programming

8.5.1 Macromodel Information

Derivation of the provided macromodel information was by use of Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel (1) and subcircuit in Figure 38 are generated using the TLC08x-Q1 typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

(1) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, *Macromodeling of Integrated Circuit Operational Amplifiers*, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).




```
*DEVICE=TLC08X_5V,OPAMP, PJF, INT

* TLC08X_5V − 5V operational amplifier "macromodel" subcir
cuit
* created using Parts release 8.0 on 12/16/99 at 14:03
* Parts is a MicroSim product.
*
* connections:          | non-inverting input
*                       | | inverting input
*                       | | | positive power supply
*                       | | | | negative power supply
*                       | | | | | output
*                       | | | | |
.subckt TLC08X_5V  1 2 3 4 5
*
 c1     11  12 4.6015E−12
 c2     6   7  8.0000E−12
 css    10  99 986.29E−15
 dc     5   53 dy
 de     54  5  dy
 dlp    90  91 dx
 dln    92  90 dx
 dp     4   3  dx
 egnd   99  0  poly(2) (3,0) (4,0) 0 .5 .5
 fb     7   99 poly(5) vb vc ve vlp vln 0 13.984E6 −1E3 1E3
               14E6 −14E6
 ga     6   0  11  12 402.12E−6
 gcm    0   6  10  99 1.5735E−6
 ioff   0   6  dc  1.212E−6
 iss    3   10 dc  130.40E−6
 hlim   90  0  vlim 1K
 j1     11  2  10  jx1
 j2     12  1  10  jx2
 r2     6   9      100.00E3
 rd1    4   11     2.4868E3
 rd2    4   12     2.4868E3
 ro1    8   5  10
 ro2    7   99 10
 rp     3   4      2.8249E3
 rss    10  99     1.5337E6
 vb     9   0  dc  0
 vc     3   53 dc  1.5537
 ve     54  4  dc  .84373
 vlim   7   8  dc  0
 vlp    91  0  dc  117.60
 vln    0   92 dc  117.60
.model  dx  D(Is=800.00E−18)
.model  dy  D(Is=800.00E−18 Rs=1m Cjo=10p)
.model  jx1 PJF(Is=80.000E−15 Beta=1.2401E−3  Vto=−1)
.model  jx2 PJF(Is=80.000E−15 Beta=1.2401E−3  Vto=−1)
.ends
```

Figure 38. Boyle Macromodel and Subcircuit

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLC08x-Q1 devices features wide supply voltage range, high-output current drive in the order of 60 mA, low input offset voltage, a high unity gain bandwidth 10 MHz and high slew of 16 V/µS. These features make the device suitable in amplifying high-frequency and slew rate signals.

9.2 Typical Applications

9.2.1 TLC08x-Q1 Single-Supply Typical Application

Some applications require amplification of low amplitude and relatively high-frequency input signal. The sine wave maximum slew rate is at zero crossing. The amplified signal distorts if the minimum slew rate is not met. Operational amplifier slew rate must be higher than $2 \times \pi \times F \times V$, where F is the input signal frequency and V is the output signal amplitude. TLC08x-Q1 Slew rate of 16 V/µS is capable of delivering an output signal of 2-V peak and 1-MHz frequency with no distortion. See Figure 45 for an application curve that shows the results of Figure 39.

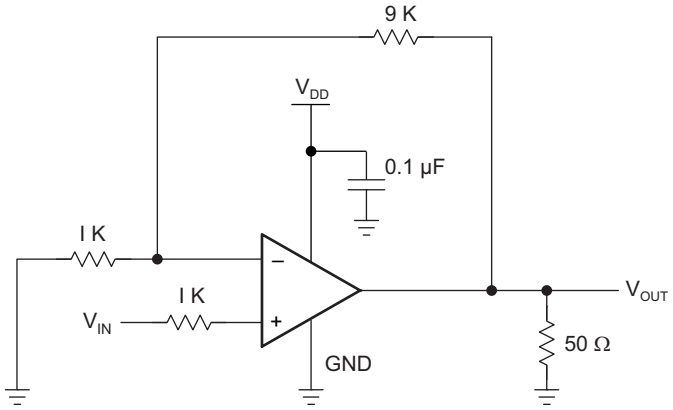


Figure 39. TLC08x-Q1 Typical Application

9.2.1.1 Design Requirements

Use the following parameters for this design example:

- Noninverting configuration with gain of 10 or 20 dB
- Single supply minimum: 4.5 V
- Single supply maximum: 16 V
- Output common mode minimum should be higher than output level V_{OL}
- Output common mode maximum should be lower than output level V_{OH}
- Unity gain bandwidth: 10 MHz
- Output load current lower than 60 mA
- Maximum input signal frequency below 1 MHz for less than –3-dB attenuation at 1 MHz

Typical Applications (continued)

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, TI recommends placing a resistor in series (R_{NULL}) with the output of the amplifier, as shown in Figure 40. A minimum value of 20 Ω should work well for most applications.

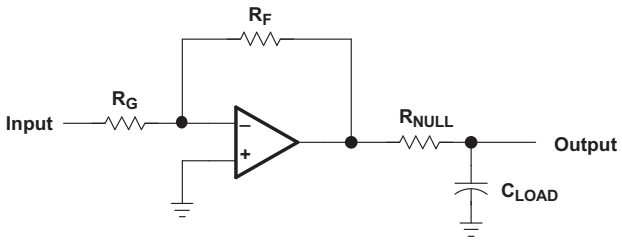
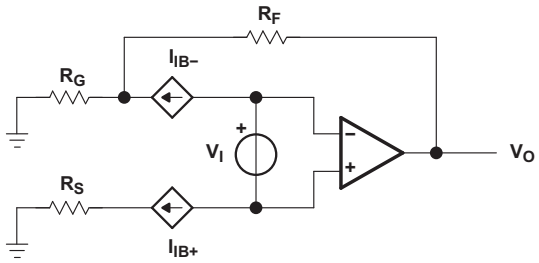


Figure 40. Driving a Capacitive Load

9.2.1.2.2 Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The schematic and formula in Figure 41 can be used to calculate the output offset voltage.



$$V_{OO} = V_{IO}\left(1+\left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\,R_S\left(1+\left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\,R_F$$

Figure 41. Output Offset Voltage Model

9.2.1.2.3 High-Speed CMOS Input Amplifiers

The TLC08x-Q1 is a family of high-speed low-noise CMOS input operational amplifiers that has an input capacitance on the order of 20 pF. Any resistor used in the feedback path adds a pole in the transfer function equivalent to the input capacitance multiplied by the combination of source resistance and feedback resistance. For example, a gain of –10, a source resistance of 1 kΩ, and a feedback resistance of 10 kΩ add an additional pole at approximately 8 MHz. This is more apparent with CMOS amplifiers than bipolar amplifiers due to their greater input capacitance.

This is of little consequence on slower CMOS amplifiers, as this pole normally occurs at frequencies above their unity-gain bandwidth. However, the TLC08x-Q1 with its 10-MHz bandwidth means that this pole normally occurs at frequencies where there is on the order of 5-dB gain left and the phase shift adds considerably.

The effect of this pole is the strongest with large feedback resistances at small closed-loop gains. As the feedback resistance is increased, the gain peaking increases at a lower frequency and the 180° phase-shift crossover point also moves down in frequency, decreasing the phase margin.

For the TLC08x-Q1, the maximum feedback resistor recommended is 5 kΩ; larger resistances can be used but a capacitor in parallel with the feedback resistor is recommended to counter the effects of the input capacitance pole.

Typical Applications (continued)

The TLC08x-Q1 with a 1-V step response has an 80% overshoot with a natural frequency of 3.5 MHz when configured as a unity gain buffer and with a 10-kΩ feedback resistor. By adding a 10-pF capacitor in parallel with the feedback resistor, the overshoot is reduced to 40% and eliminates the natural frequency, resulting in a much faster settling time (see Figure 42). The 10-pF capacitor was chosen for convenience only.

Load capacitance had little effect on these measurements due to the excellent output drive capability of the TLC08x-Q1.

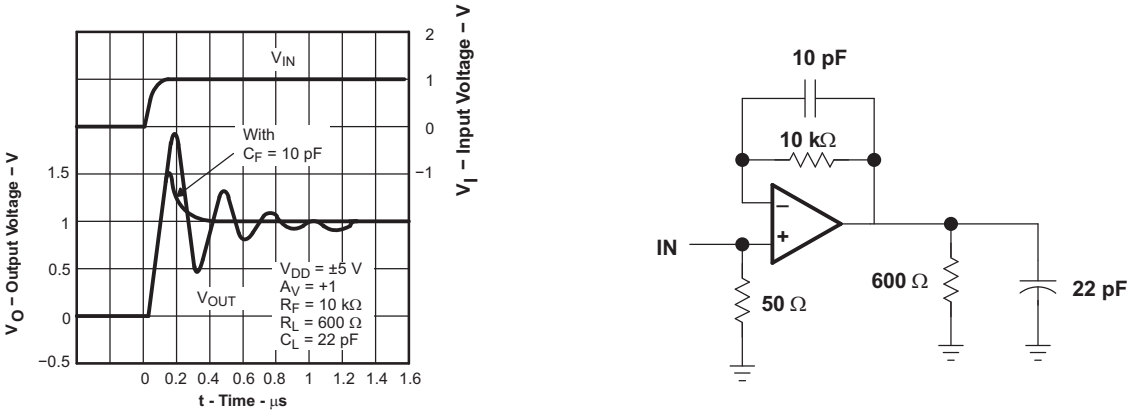
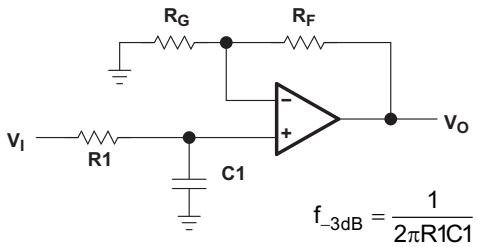


Figure 42. 1-V Step Response

9.2.1.2.4 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 43).



$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 43. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple-pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

Typical Applications (continued)

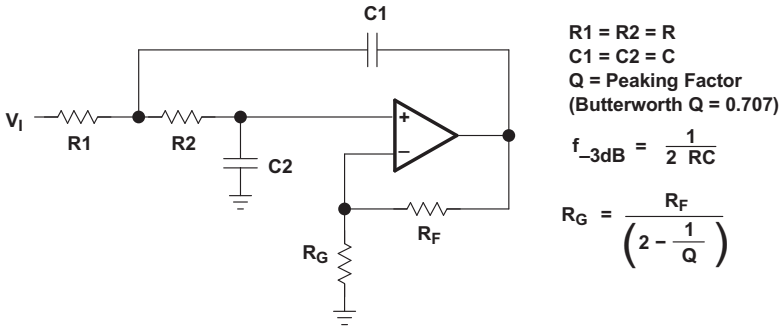
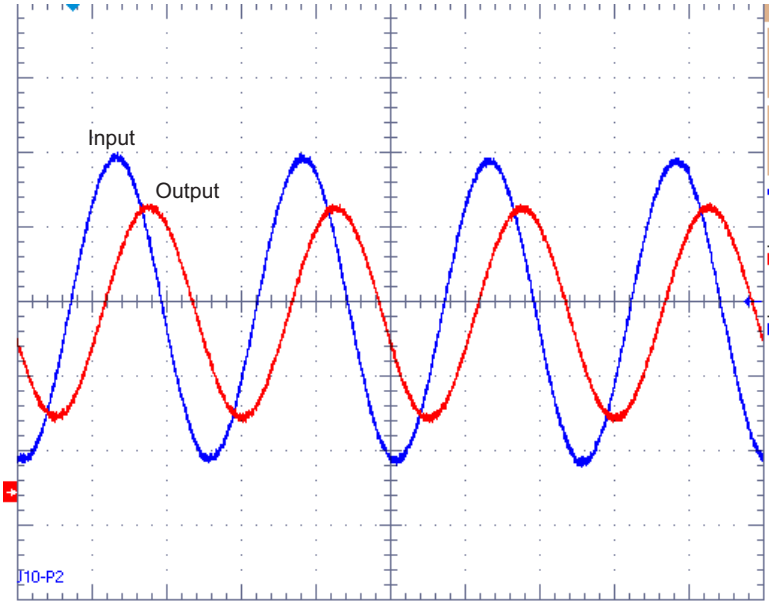


Figure 44. 2-Pole Low-Pass Sallen-Key Filter

9.2.1.3 Application Curve



Gain Vout / Vin = 1.471 V / 0.2 V = 7.335

Gain(db) = 20 Log (7.335) = 17.33 dB
and is 2.7 dB below 10 dB

Figure 45. Single Supply Application at 1-MHz Input Signal

Typical Applications (continued)

9.2.2 Dual-Supply Typical Application

The dual-supply application has a gain of 10 and a bandwidth of 1 MHz.

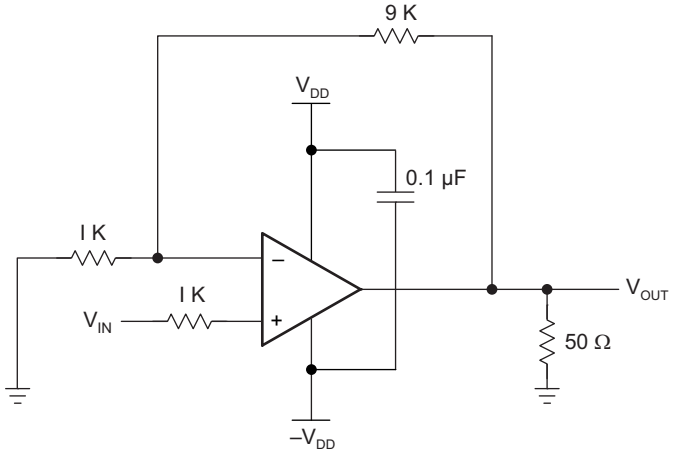


Figure 46. Dual Supply Typical Application Schematic

9.2.2.1 Design Requirements

Use the following parameters for this design example:

- Noninverting configuration with gain of 10 or 20 dB
- Dual supply minimum: ±2.25 V
- Dual supply maximum: ±8 V
- Output common mode minimum should be higher than output level V_{OL}
- Output common mode maximum should be lower than output level V_{OH}
- Unity gain bandwidth: 10 MHz
- Maximum input signal frequency is 1 MHz for less than 3-dB attenuation at 1 MHz
- Output load current lower than 60 mA

9.2.2.2 Detailed Design Procedure

For this example, see *Detailed Design Procedure* in *TLC08x-Q1 Single-Supply Typical Application*.

Typical Applications (continued)

9.2.2.3 Application Curve

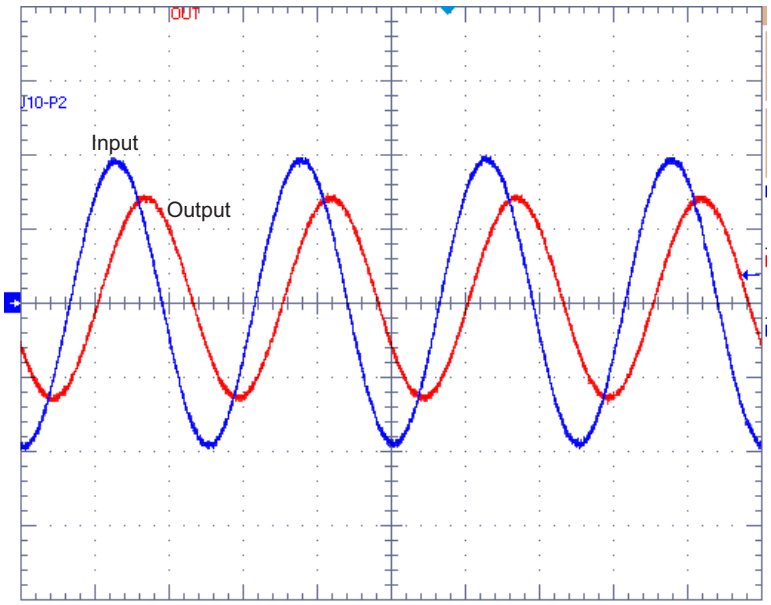


Figure 47. Dual Supply Application at 1-MHz Input Signal

10 Power Supply Recommendations

The TLC08x-Q1 operational amplifier is specified for use on a single supply from 4.5 V to 16 V (or a dual supply from over a temperature range of −40°C to 125°C. The device continues to function below this range, but performance is not specified. Place bypass capacitors close to the power supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

To achieve the levels of high performance of the TLC08x-Q1, follow proper printed-circuit board (PCB) design techniques. A general set of guidelines is given in the following.

Ground planes TI highly recommends using a ground plane on the board to provide all components with a low-inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.

Proper power-supply decoupling Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

Sockets Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the PCB is the best implementation.

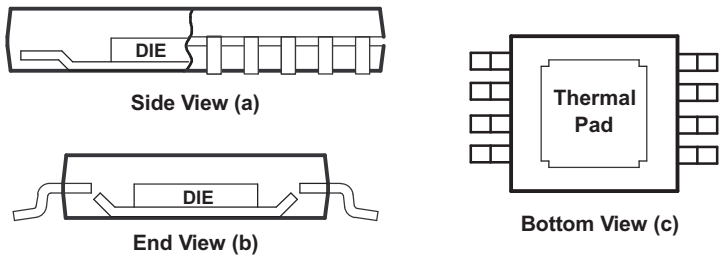
Layout Guidelines (continued)

Short trace runs and compact part placements Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps minimize stray capacitance at the input of the amplifier.

Surface-mount passive components TI recommends using surface-mount passive components for high-performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more-compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, TI recommends keeping the lead lengths as short as possible.

11.1.1 General PowerPAD™ Design Considerations

The TLC08x-Q1 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 48(a) and Figure 48(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 48(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.



NOTE A: The thermal pad is electrically isolated from all terminals in the package.

Figure 48. Views of Thermally-Enhanced DGN Package

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

NOTE

Soldering the thermal pad to the PCB is always required, even with applications that have low power dissipation.

This soldering provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB. Although there are many ways to properly heatsink the PowerPAD package, the following steps list the recommended approach.

The thermal pad must be connected to the most-negative supply voltage (GND pin potential) of the device.

1. Prepare the PCB with a top-side etch pattern (see the landing patterns at the end of this data sheet). There should be etch for the leads, as well as etch for the thermal pad.
2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLC08x-Q1 device. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal-pad area to be soldered, so that wicking is not a problem.
4. Connect all holes to the internal plane that is at the same potential as the ground pin of the device.

Layout Guidelines (continued)

5. When connecting these holes to this internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high-thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLC08x-Q1 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal-pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal-pad area. This prevents solder from being pulled away from the thermal-pad area during the reflow process.
7. Apply solder paste to the exposed thermal-pad area and all of the IC terminals.
8. With these preparatory steps in place, the TLC08x-Q1 IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

For a given $R_{\theta JA}$, use Equation 1 to calculate the maximum power dissipation.

$$P_D = \left(\frac{T_{MAX} - T_A}{R_{\theta JA}} \right) \quad (1)$$

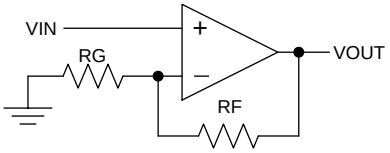
Where:

P_D = Maximum power dissipation of TLC08x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$
$R_{\theta JC}$ = Thermal coefficient from junction to case
$R_{\theta CA}$ = Thermal coefficient from case to ambient air (°C/W)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (class A-B), most of the heat dissipation is at low-output voltages with high-output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the thermal pad. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, $R_{\theta JA}$ decreases and the heat dissipation capability increases. The currents and voltages shown in *Typical Characteristics* are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

11.2 Layout Example



(Schematic Representation)

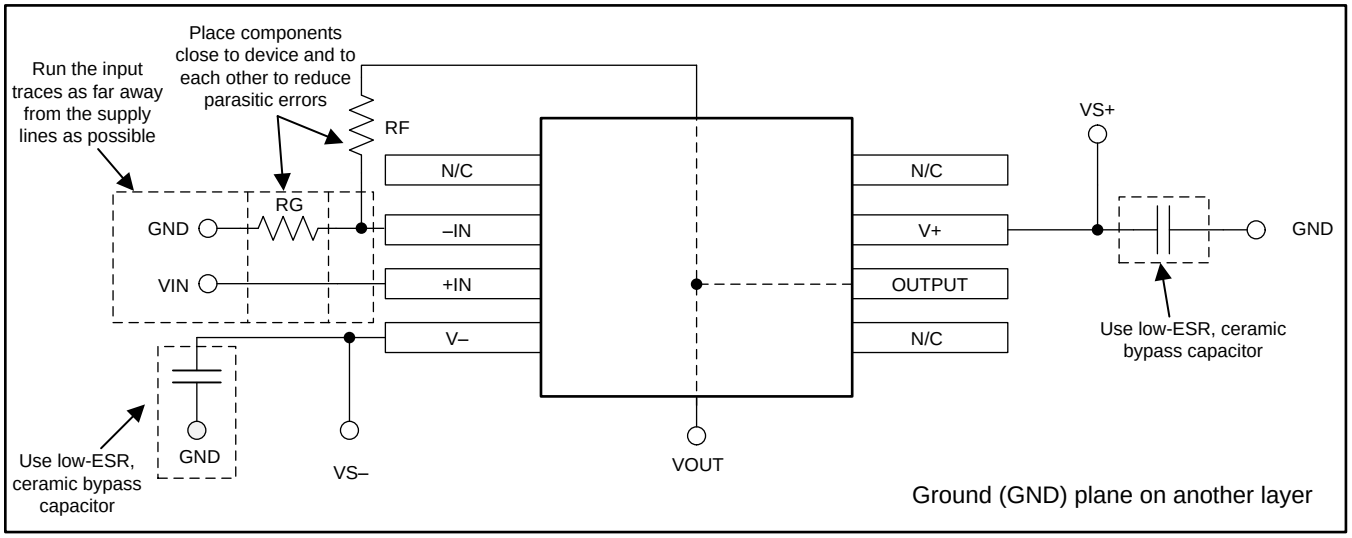


Figure 49. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

TLC081 EMI Immunity Performance (SBOT011)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLC082-Q1	Click here	Click here	Click here	Click here	Click here
TLC084-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentsation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
Parts, PSpice are trademarks of MicroSim Corporation.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC082QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	QXO	Samples
TLC084QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC084Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLC082-Q1, TLC084-Q1 :

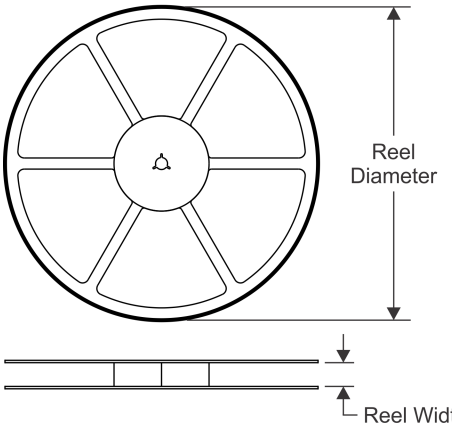
- Catalog: TLC082, TLC084

NOTE: Qualified Version Definitions:

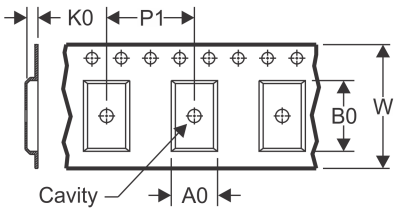
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

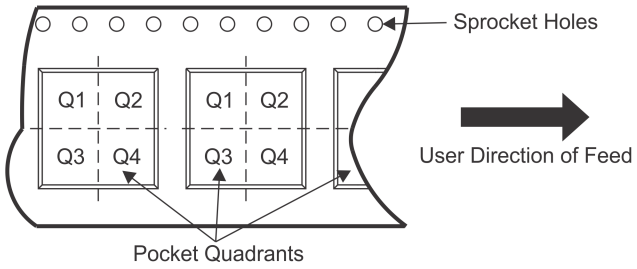


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

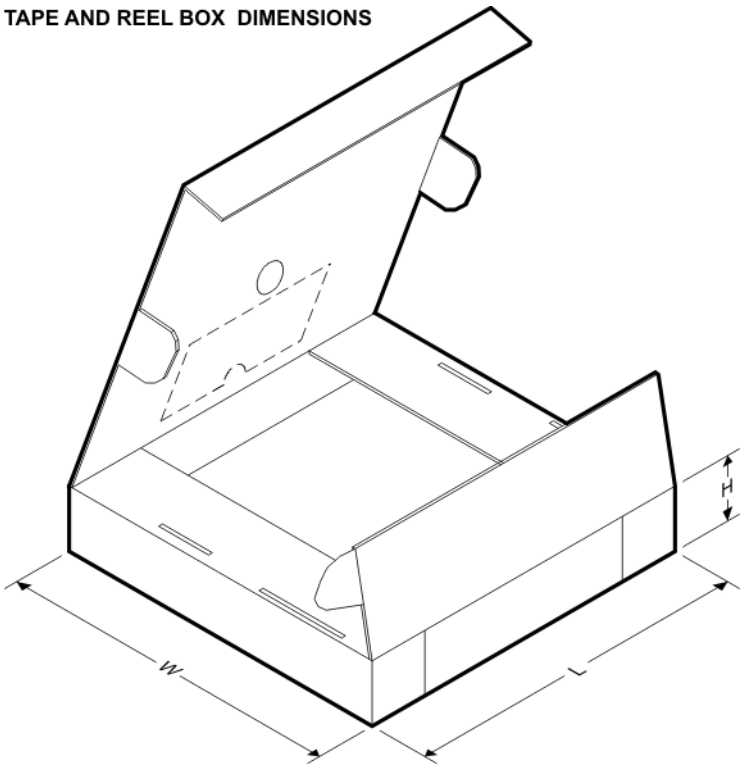
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC082QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC082QDGNRQ1	HVSSOP	DGN	8	2500	346.0	346.0	29.0

GENERIC PACKAGE VIEW

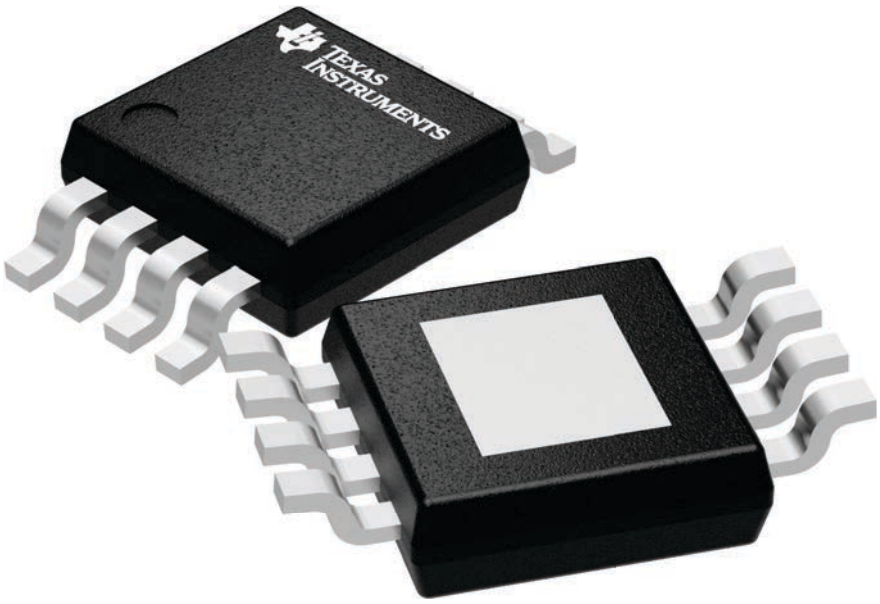
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

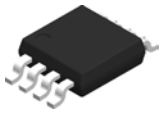
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

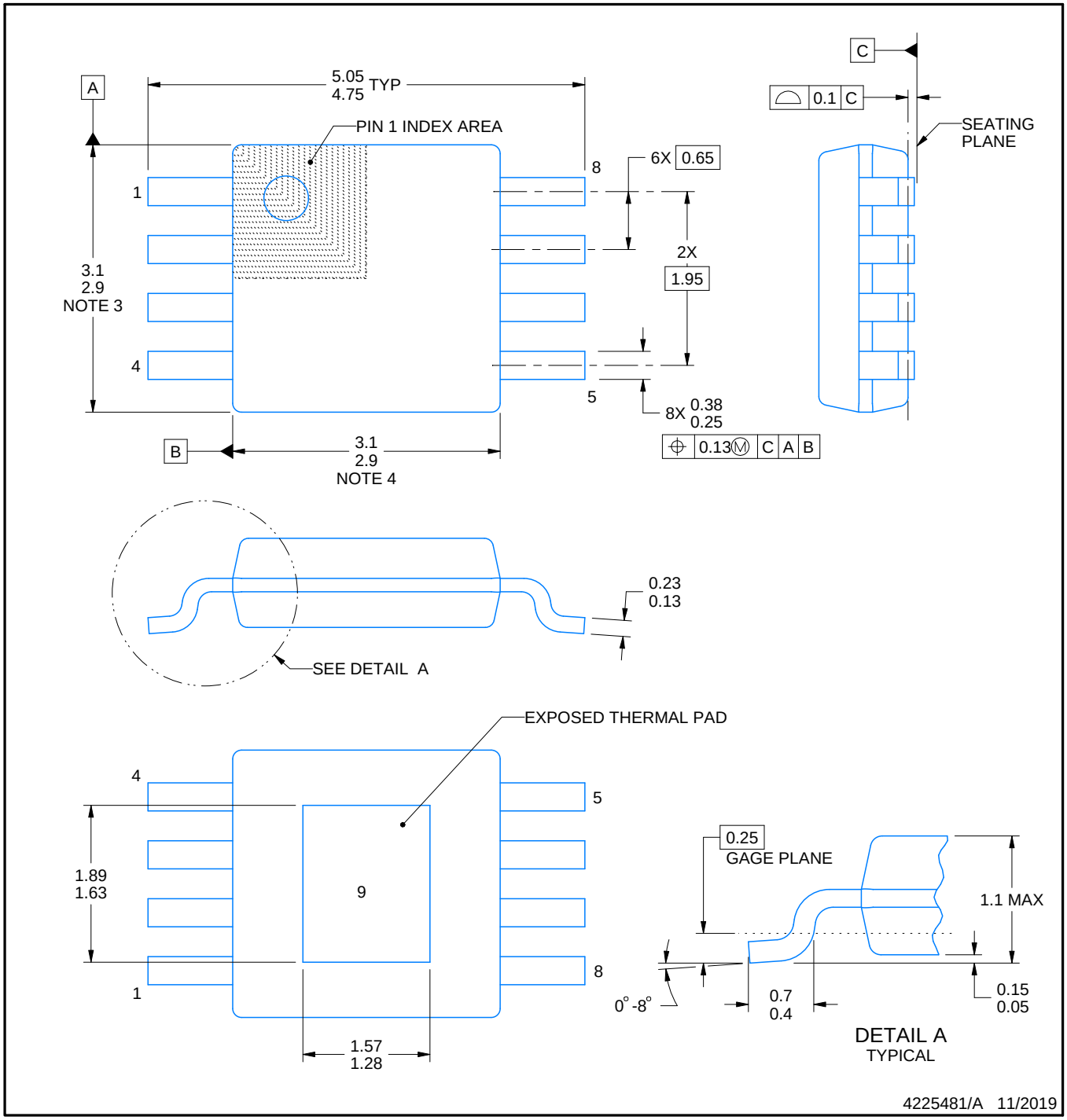
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

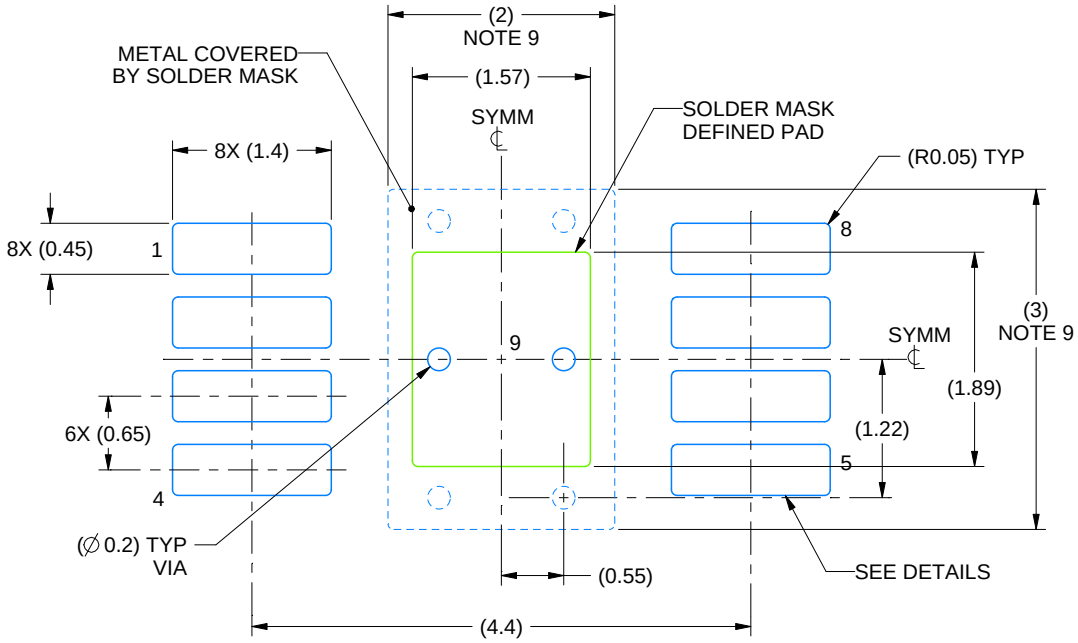
SMALL OUTLINE PACKAGE



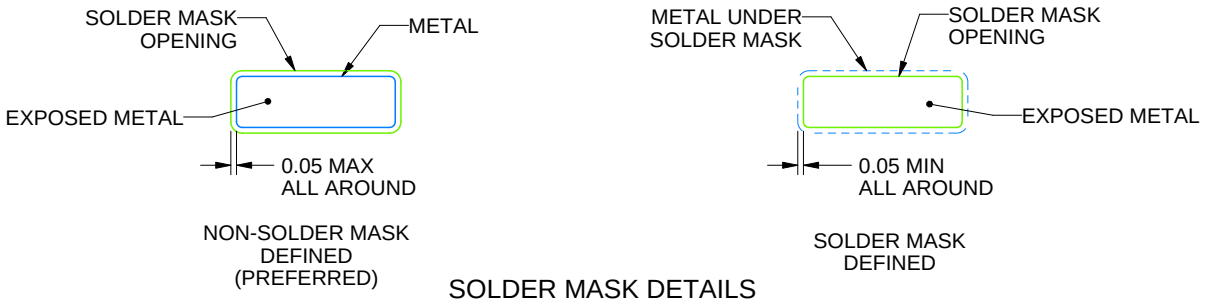
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

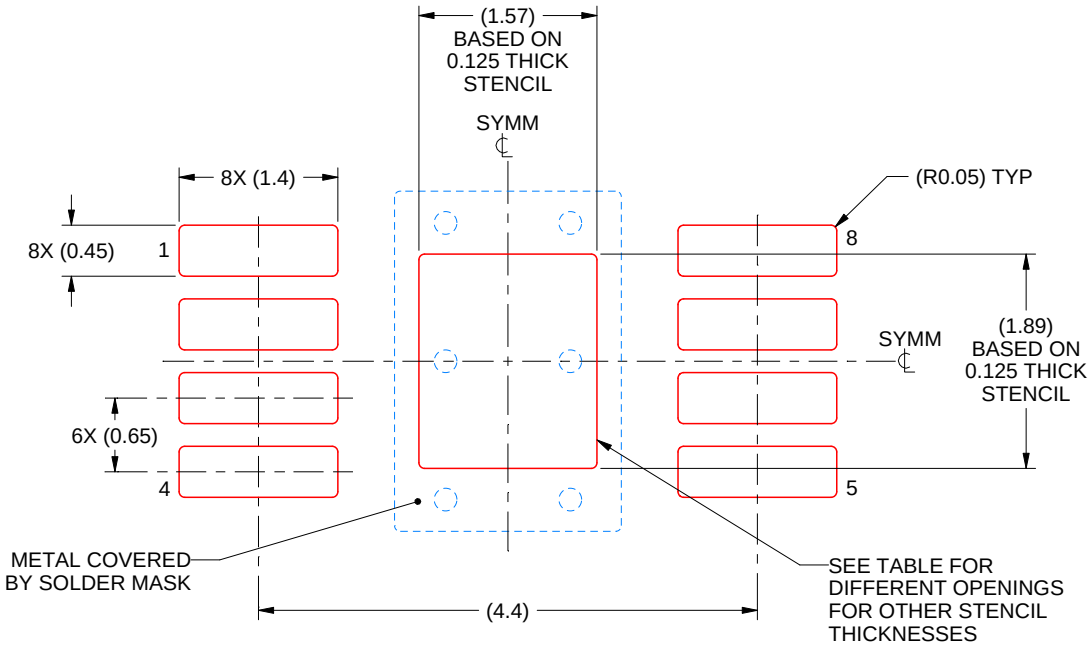


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

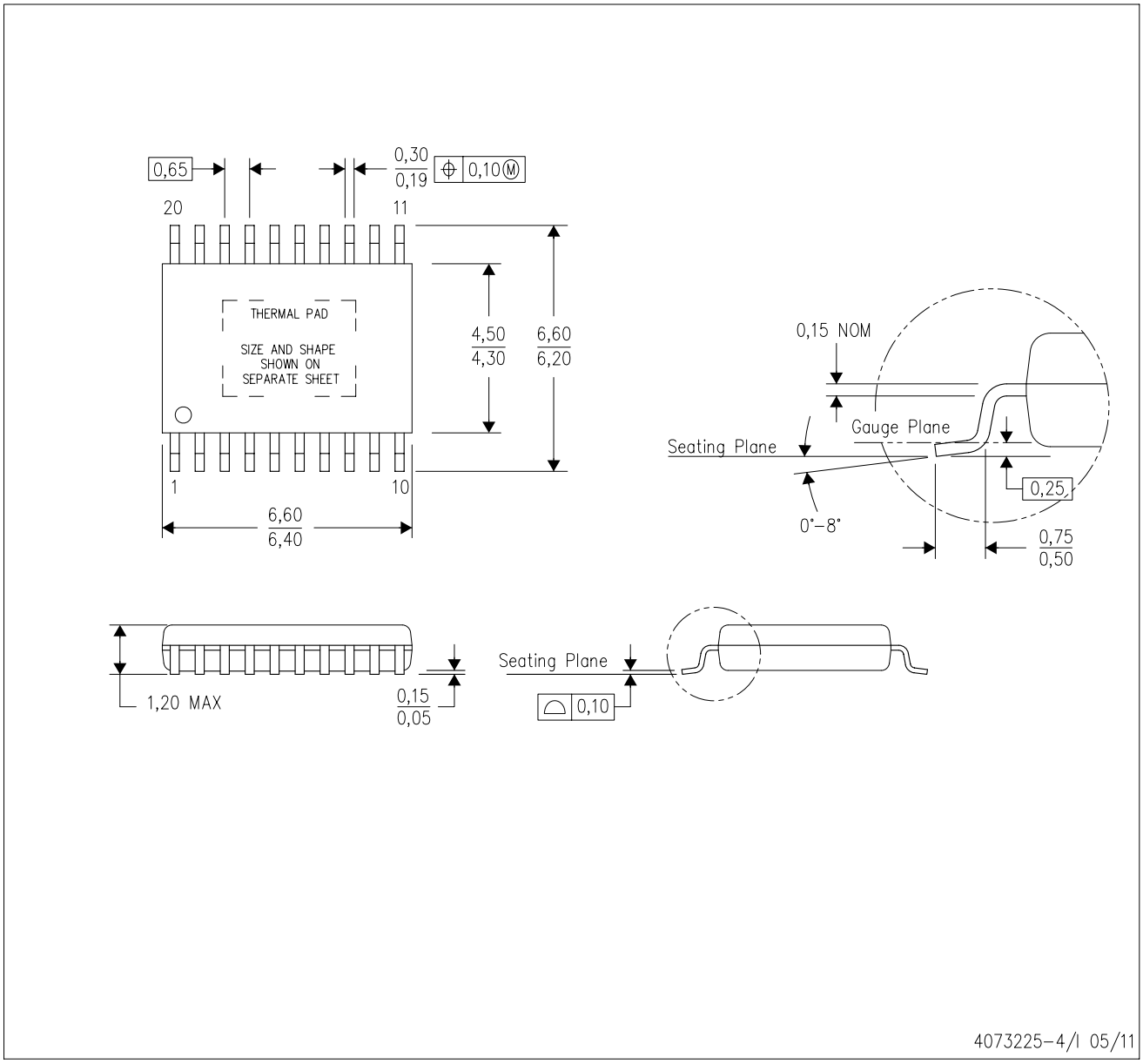
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

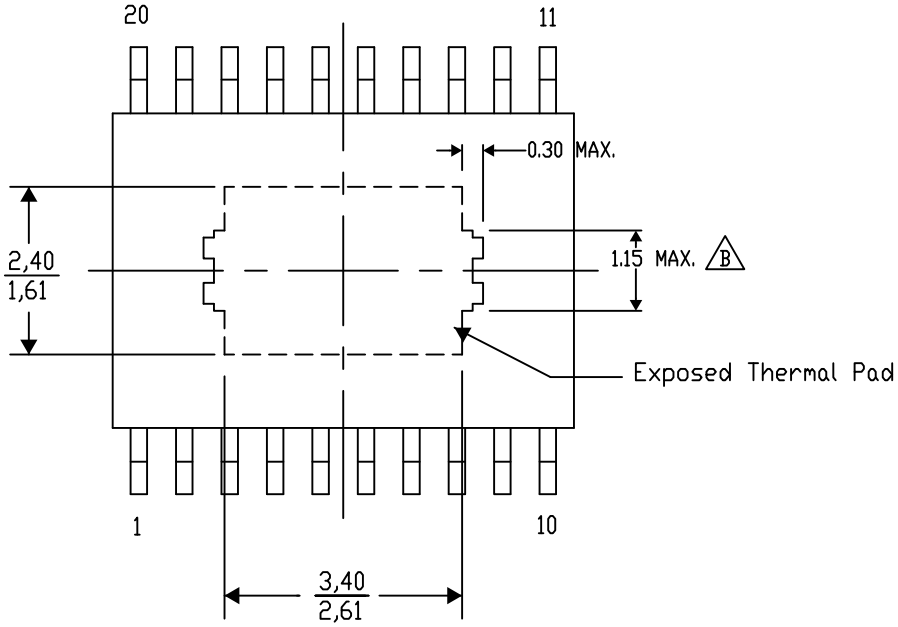
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

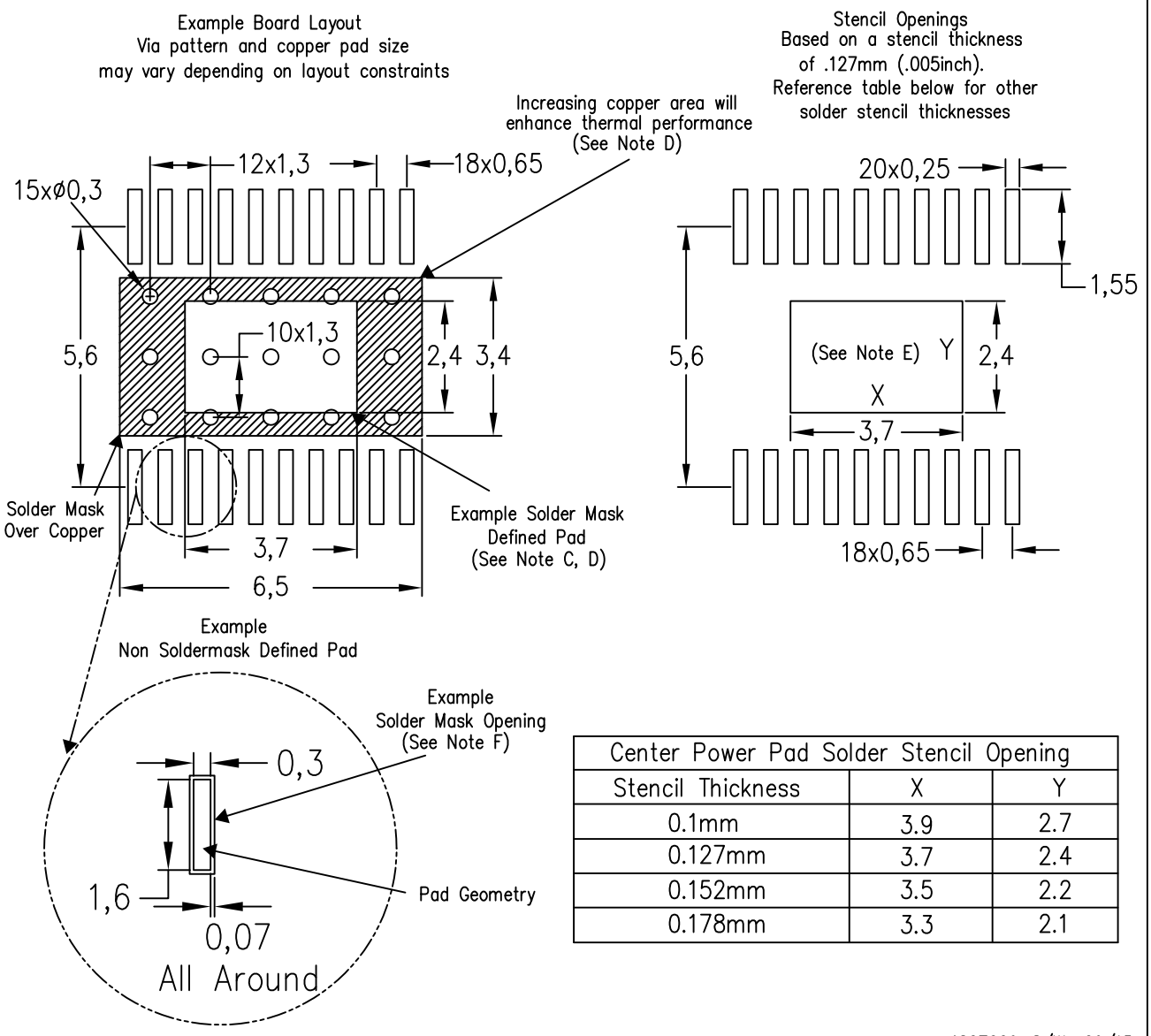
4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–8/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265