

TLC6C5724-Q1 Automotive 24-Channel, Full Diagnostics, Constant-Current RGB LED Driver

1 Features

- AEC-Q100 Qualified for Automotive Applications
 - Device Temperature Grade 1: -40°C to 125°C , T_A
- 24 Constant-Current-Sink Output Channels
 - 50-mA Maximum Output Current
 - 8-V Maximum Output Voltage
 - 3 Output Groups: OUTRn, OUTGn, OUTBn
- Output Current Adjustment
 - 7-Bit Dot Correction for Each Channel
 - 8-Bit Intensity Control for Each Group
- Integrated PWM Grayscale Generator
 - PWM Dimming for Each Individual Channel
 - Adjustable Global Grayscale Mode: 12-Bit, 10-Bit, 8-Bit
- Protection and Diagnostics
 - LED-Open Detection, LED-Short Detection, Output Short-to-GND Detection
 - Adjacent-Pin Short Detection
 - Pre-Thermal Warning, Thermal Shutdown
 - IREF Resistor Open- and Short-Detection and -Protection
 - Negate Bit Toggle for GCLK Error Detect and LOD_LSD Register Error Check
 - LOD_LSD Circuit Self-Test
- Programmable Output Slew Rate
- Output Channel Group Delay
- Serial Data Interface

2 Applications

- Automotive Cluster
- Automotive Local Dimming Display
- Automotive Faceplate
- Automotive HVAC Control Panel
- Automotive Center Stack Display
- Automotive Interior and RGB Ambient Lighting
- Automotive Shift-by-Wire and Gear Shifter

3 Description

There are automotive applications for indicators and for LCD local-dimming backlighting. For these applications, more persons think multi-channel constant-current LED drivers are necessary. The requirement is to get the same intensity and color temperature of LEDs. For system-level safety, it is necessary that the LED drivers can sense faults.

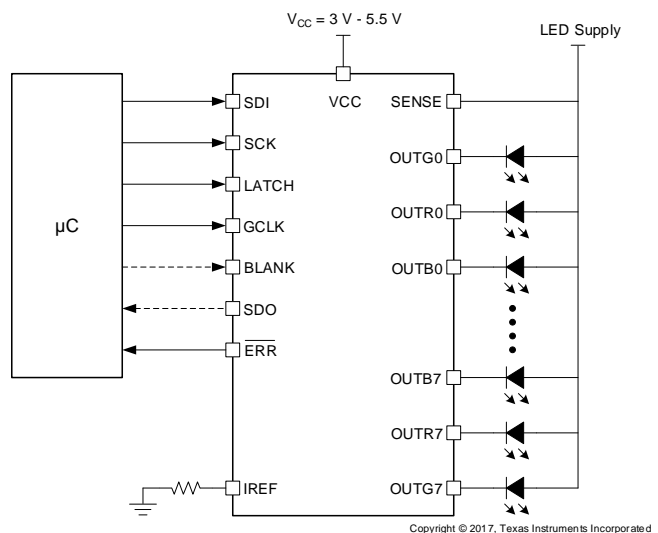
The TLC6C5724-Q1 device is an automotive 24-channel constant-current RGB LED driver that can do tests on the LEDs. The TLC6C5724-Q1 device supplies a maximum of 50-mA output current set by an external resistor. The device has a 7-bit dot correction with two ranges for each output. The device also has an 8-bit intensity control for the outputs of each color group. A 12-, 10-, or 8-bit grayscale control adjusts the intensity of each output. The device has circuits that sense faults in the system, including LED faults, adjacent-pin short faults, reference-resistor faults, and more. A slew rate control has 2 positions for adjustment to get the largest decrease in system noise. There is an interval between the changes of output level from one LED group to a different one. This interval helps to decrease the starting electrical current. The SDI and SDO pins let more than one device be connected in series for control through one serial interface.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC6C5724-Q1	HTSSOP (38)	6.20 mm x 12.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

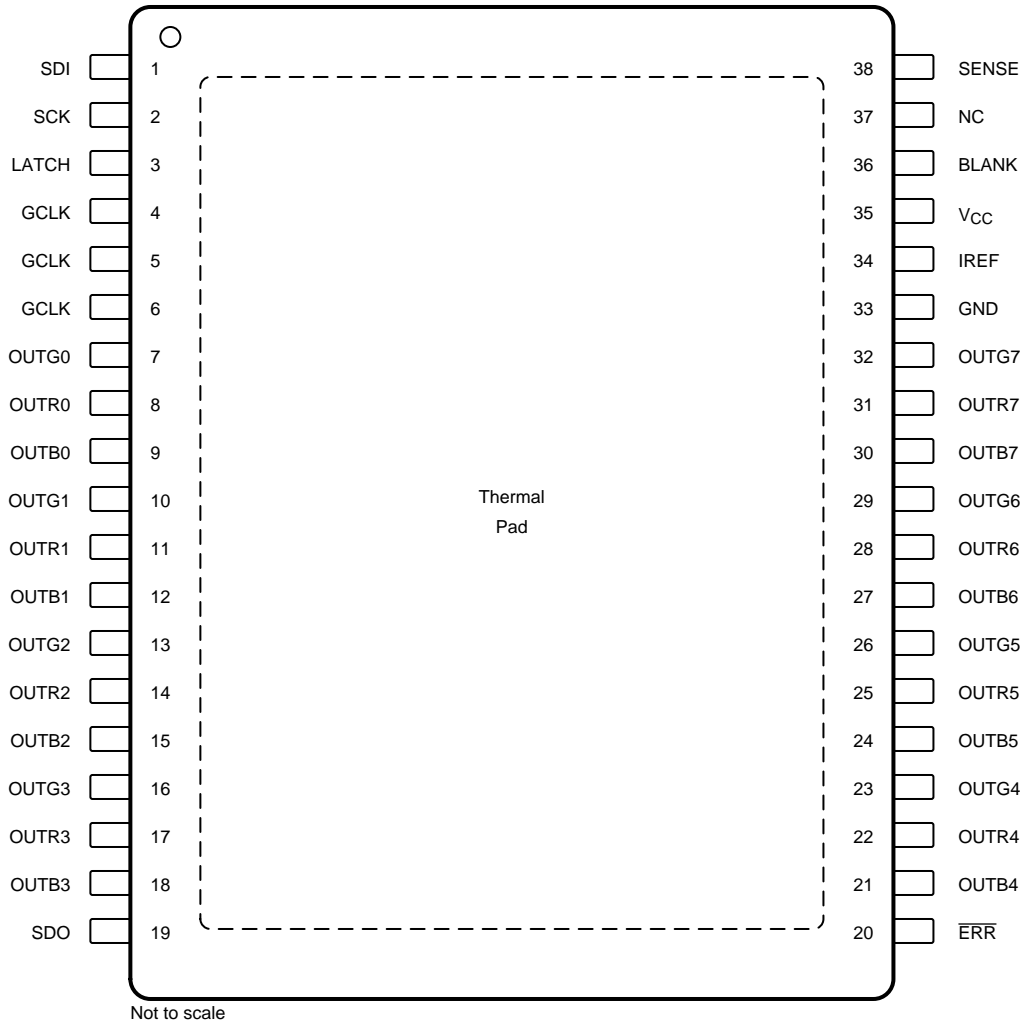
Changes from Original (December 2017) to Revision A	Page
• Changed the title of the data sheet	1
• Changed items in the <i>Features</i> list	1
• Changed the I section	1
• Changed the text of the <i>Description</i> section	1
• Changed the descriptions for the GCLK, OUTBx, OUTGx, OUTRx, SENSE, and Thermal pad rows of the <i>Pin Functions</i> table	4
• Deleted a sentence and added a paragraph at the end of the <i>Grayscale Configuration</i> section	24
• Changed the section title from <i>Display Timing Reset</i> to <i>PWM Auto Repeat</i> and changed the text	25
• Changed the section title from <i>Auto Display Repeat</i> to <i>PWM Timing Reset</i> and changed the text	26
• Deleted "and PWM" from section title "LED and PWM Diagnostics"	26
• Changed Table 1	26
• Changed the text following Table 1	26
• Changed the Table 2 column headers	26
• Changed the Table 3 table headers and the text following the table	26
• Changed "two kinds" to "two sets" in the sentence immediately following Table 3	26
• Changed the text preceding Table 6	27
• Added a table note to Table 6	28
• Deleted the first sentence following Table 6	28
• Changed the text and deleted two tables in the <i>Adjacent-Pin-Short Check</i> section	28
• Added text and two tables following Table 8	29
• Changed the text of the <i>IREF Short and IREF Open Detection</i> section	29
• Changed the contents of the OUTUT column in Table 11	29
• Changed the text in the <i>Pre-Thermal Warning Flag</i> section	29
• Changed the text in the <i>Thermal Error Flag</i> section	30
• Changed the text and deleted a diagram in the <i>Negate Bit Toggle</i> section	30

Revision History (continued)

• Changed the text and deleted a diagram in the LOD_LSD Self-Test section	30
• Changed the text in the ERROR Clear section	31
• Changed the text in the Global Reset section	31
• Changed the LED supply voltage from 7 V to 8 V in the Power Up section	32
• Added the TEF register, where the overtemperature fault is latched	32
• Added a sentence to paragraph 2 of the Register Write and Read section, changed "data" to "288-bit data", and changed "last SCK rising edge" to "288th SCK rising edge"	32
• Changed "data" to "288-bit data" in the FC-BC-DC Write section	33
• Changed "sink current" to "APS current" and added "APS detection time" to the definition for bits 200 and 199, respectively	33
• Deleted two equations preceding Table 16	35
• Changed the titles of Table 16 , Table 17 , and Table 18	35
• Added Equation 5 to calculate duty cycle	36
• Changed "OUTB0" to "OUTG0" for bits 167–156 in Table 19	36
• Changed the last sentence of the Special Command Function section	37
• Changed the wording and deleted three figures in the Register Maps section	39
• Changed bit numbers 287 and 286 to 277 and 276 in Figure 28	39
• Changed "Output slew rate" to "Output slew-rate time" for bit 203	43
• Changed the text in the Typical Application section	49
• Added a sentence and a figure to the Detailed Design Procedure section	50
• Added the Application Curves section to the data sheet	50
• Changed the LED supply voltage from 7 V to 8 V and added a sentence to the Power Supply Recommendations section	51
• Added positioning information for the IREF resistor to the Layout Guidelines section	51

5 Pin Configuration and Functions

DAP PowerPAD™ Package
38-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BLANK	36	I	Blank all outputs. BLANK low forces all channels off. Grayscale counter resets, grayscale PWM timing controller is initialized. BLANK high starts grayscale PWM timing controller, channels are controlled by PWM timing controller.
$\overline{\text{ERR}}$	20	O	Open-drain error feedback
GCLK	4, 5, 6	I	Clock input for grayscale PWM counter. The three pins are internally connected together.
GND	33	—	Power ground
IREF	34	I	Reference-current pin for setting the full-scale output current
LATCH	3	I	Latch-enable input pin
NC	37	—	No internal connection
OUTB0–OUTB7	9, 12, 15, 18, 21, 24, 27, 30	O	Constant-current outputs for color group B
OUTG0–OUTG7	7, 10, 13, 16, 23, 26, 29, 32	O	Constant-current outputs for color group G

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUTR0–OUTR7	8, 11, 14, 17, 22, 25, 28, 31	O	Constant-current outputs for color group R
SCK	2	I	Data-shift clock-input pin
SDI	1	I	Serial data-in pin
SDO	19	O	Serial data-out pin
SENSE	38	I	Connect to LED supply for LED diagnostics
V _{CC}	35	I	Power supply pin
Thermal pad	—	—	Connect to ground to improve thermal performance

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	V _{CC}	-0.3	6	V
	SENSE	-0.3	8	
	BLANK, GCLK, LATCH, SCK, SDI	-0.3	V _{CC} + 0.3	
Output voltage	ERR, IREF, SDO	-0.3	V _{CC} + 0.3	V
	OUTR0–OUTR7, OUTG0–OUTG7, OUTB0–OUTB7	-0.3	8	
Output current	OUTR0–OUTR7, OUTG0–OUTG7, OUTB0–OUTB7	0	50	mA
Operating junction temperature, T _J		-40	150	°C
Storage temperature, T _{stg}		-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V	
		Charged-device model (CDM), per AEC Q100-011	All pins		±500
			Corner pins (1, 19, 20, and 38)		±750

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Device supply voltage	3		5.5	V
V _{SENSE}	LED supply voltage			8	V
V _O	Output voltage			8	V
V _{IL}	Input logic-low voltage	BLANK, GCLK, LATCH, SCK, SDI	0	0.3 V _{CC}	V
V _{IH}	Input logic-high voltage	BLANK, GCLK, LATCH, SCK, SDI	0.7 V _{CC}	V _{CC}	V
I _{OH}	High-level output source current	SDO		1	mA
I _{OL}	Low-level input sink current	SDO		1	mA
		ERR		5	
I _O	Constant output sink current	OUTR0–OUTR7, OUTG0–OUTG7, OUTB0–OUTB7	2	50	mA
T _A	Operating ambient temperature		-40	125	°C
T _J	Operating junction temperature		-40	150	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLC6C5724-Q1	UNIT
		DAP (HTSSOP)	
		38 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	39.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	31.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	18	°C/W

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		TLC6C5724-Q1	UNIT
		DAP (HTSSOP)	
		38 PINS	
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2	°C/W

6.5 Electrical Characteristics

$V_{CC} = 3\text{ V to }5.5\text{ V}$, $T_J = -40^\circ\text{C to }150^\circ\text{C}$, $V_{SENSE} = 5\text{ V}$, $GS = \text{FFFh}$, $BC = \text{FFh}$, $DC = 7\text{Fh}$ with upperDCrange (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES					
I_{CC}	Supply current	SDI, SCK, LATCH = L, BLANK = L, GCLK = L, $V_{OUT} = 1\text{ V}$, $I_{OUT} = 2\text{ mA}$	4.2	5.5	mA
		SDI, SCK, LATCH = L, BLANK = L, GCLK = L, $V_{OUT} = 1\text{ V}$, $I_{OUT} = 20\text{ mA}$	7.7	9	
		SDI, SCK, LATCH = L, BLANK = H, GCLK = 8 MHz, $V_{OUT} = 1\text{ V}$, $I_{OUT} = 20\text{ mA}$, auto-repeat on	8.3	10	
		SDI, SCK, LATCH = L, BLANK = H, GCLK = 8 MHz, $V_{OUT} = 1\text{ V}$, $I_{OUT} = 50\text{ mA}$, auto-repeat on	13.5	16	
LOGIC INPUTS (SDI, SCK, LATCH, GCLK, BLANK)					
I_{lkq}	Input leakage current	At SDI, SCK, LATCH, with $V_I = V_{CC}$; or at SDI, SCK, LATCH, BLANK, GCLK, with $V_I = \text{GND}$		-1	1 μA
R_{pd}	Pull down resistance at BLANK, GCLK	250	500	750	k Ω
CONTROL OUTPUTS (IREF, $\overline{\text{ERR}}$, SDO)					
V_{IREF}	IREF voltage	$R_{IREF} = 0.96\text{ k}\Omega$	1.17	1.2	1.23 V
V_{OH}	High-level output voltage	At SDO, $I_{OH} = -1\text{ mA}$	$V_{CC} - 0.4$		V_{CC} V
V_{OL}	Low-level output voltage	At SDO, $I_{OL} = 1\text{ mA}$			0.4 V
V_{ERR}	$\overline{\text{ERR}}$ pin open-drain voltage drop	$I_{ERR} = 4\text{ mA}$			0.1 V_{CC} V
I_{LKG_ERR}	$\overline{\text{ERR}}$ pin leakage current	$V_{ERR} = 5\text{ V}$			1 μA
OUTPUT STAGE					
$V_{(OUT,min)}$	Minimum output voltage	$V_{CC} = 3.6\text{ V}$, $I_{OUT} = 50\text{ mA}$			0.67 V
		$V_{CC} = 3\text{ V}$, $I_{OUT} = 50\text{ mA}$			0.7 V
$K_{(OUT)}$	Ratio of output current to IREF current, $K = I_{(OUTx)} / I_{(IREF)}$			40	mA/mA
$I_{lkq(OUT)}$	Output leakage current	BLANK = L, $V_{OUT} = 7\text{ V}$, $V_{SENSE} = 7\text{ V}$		0.1	μA
CHANNEL ACCURACY					
$I_{(OUT)}$	Constant output current	$V_{OUT} = 1\text{ V}$, $R_{IREF} = 24\text{ k}\Omega$	1.86	2	2.14 mA
		$V_{OUT} = 1\text{ V}$, $R_{IREF} = 0.96\text{ k}\Omega$	46.5	50	53.5 mA
		$V_{OUT} = 1\text{ V}$, R_{IREF} open or short	7	10	13 mA

Electrical Characteristics (continued)

$V_{CC} = 3\text{ V to }5.5\text{ V}$, $T_J = -40^\circ\text{C to }150^\circ\text{C}$, $V_{SENSE} = 5\text{ V}$, $GS = \text{FFFh}$, $BC = \text{FFh}$, $DC = 7\text{Fh}$ with upperDCrange (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$\Delta I_{(\text{Ch-Ch})}$ (1)	Current accuracy (channel-to-channel in same color group)	$V_{OUT} = 1\text{ V}$, $I_{OUT} = 50\text{ mA}$	-4%	4%		
		$V_{OUT} = 1\text{ V}$, $I_{OUT} = 2\text{ mA}$	-4%	4%		
$\Delta I_{(\text{Dev-Dev})}$ (2)	Current accuracy (device-to-device)	$V_{OUT} = 1\text{ V}$, $I_{OUT} = 50\text{ mA}$	-4%	4%		
		$V_{OUT} = 1\text{ V}$, $I_{OUT} = 2\text{ mA}$	-4%	4%		
$\Delta I_{(\text{Ch-Ideal})}$ (3)	Current accuracy (channel-to-ideal output)	$V_{OUT} = 1\text{ V}$, $I_{OUT} = 50\text{ mA}$	-7%	7%		
		$V_{OUT} = 1\text{ V}$, $I_{OUT} = 2\text{ mA}$	-7%	7%		
$\Delta I_{(\text{OUT-VCC})}$ (4)	Line regulation	$V_{OUT} = 1\text{ V}$, $V_{CC} = 3\text{ V to }5.5\text{ V}$, $I_{OUT} = 50\text{ mA}$	-0.7	0.7	%V	
		$V_{OUT} = 1\text{ V}$, $V_{CC} = 3\text{ V to }5.5\text{ V}$, $I_{OUT} = 2\text{ mA}$	-0.7	0.7		
$\Delta I_{(\text{OUT-VOUT})}$ (5)	Load regulation	$V_{OUT} = 1\text{ V to }3\text{ V}$, $I_{OUT} = 50\text{ mA}$	-0.7	0.7	%V	
		$V_{OUT} = 1\text{ V to }3\text{ V}$, $I_{OUT} = 2\text{ mA}$	-0.7	0.7		
PROTECTION CIRCUITS						
V_{LOD1}	LED open-circuit detection low threshold	$LOD_VOLTAGE = 0b$	0.275	0.3	0.32	V
V_{LOD2}	LED open-circuit detection high threshold	$LOD_VOLTAGE = 1b$	0.48	0.5	0.52	V
V_{LSD1}	LED short-circuit detection high threshold	$LSD_VOLTAGE = 0b$	$V_{SENSE} - 0.4$	$V_{SENSE} - 0.3$	$V_{SENSE} - 0.2$	V
V_{LSD2}	LED short-circuit detection low threshold	$LSD_VOLTAGE = 1b$	$V_{SENSE} - 0.8$	$V_{SENSE} - 0.7$	$V_{SENSE} - 0.6$	V
I_{IREF_OC}	IREF resistor open-circuit detection threshold	$V_{CC} = 5\text{ V}$	8	10	12	μA
I_{IREF_OCHYS}	IREF resistor open-circuit detection threshold hysteresis	$V_{CC} = 5\text{ V}$		5		μA

(1) Channel to channel accuracy in the same color group is calculated by the formula below. (X = color group; i, j = 0 to 7)

$$\Delta I_{(\text{Ch-Ch})} = \left(\frac{8 \times I_{OUTXi} - \sum_{j=0}^7 I_{OUTXj}}{\sum_{j=0}^7 I_{OUTXj}} - 1 \right) \times 100\%$$

(2) Device to device accuracy is calculated by the formula below.

$$\Delta I_{(\text{Dev-Dev})} = \left(\frac{\sum_{i=0}^7 (I_{OUTRi} + I_{OUTGi} + I_{OUTBi}) - I_{OUT,ideal}}{24 I_{OUT,ideal}} \right) \times 100\%$$

$$I_{OUT,ideal} = \frac{V_{IREF}}{R_{IREF}} \times K_{(OUT)}$$

(3) Channel to ideal accuracy is calculated by the formula below.

$$\Delta I_{(\text{Ch-Ideal})} = \left(\frac{I_{OUTXi} - I_{OUT,ideal}}{I_{OUT,ideal}} - 1 \right) \times 100\%$$

(4) Line regulation accuracy is calculated by the formula below.

$$\Delta I_{(\text{OUT-VCC})} = \left(\frac{I_{(\text{OUTXi}, VCC=5.5V)} - I_{(\text{OUTXi}, VCC=3V)}}{I_{(\text{OUTXi}, VCC=3V)}} \right) \times \frac{100}{5.5 - 3} \% / V$$

(5) Load regulation accuracy is calculated by the formula below.

$$\Delta I_{(\text{OUT-VOUT})} = \left(\frac{I_{(\text{OUTXi}, VOUT=3V)} - I_{(\text{OUTXi}, VOUT=1V)}}{I_{(\text{OUTXi}, VOUT=1V)}} \right) \times \frac{100}{3 - 1} \% / V$$

Electrical Characteristics (continued)

$V_{CC} = 3\text{ V to }5.5\text{ V}$, $T_J = -40^\circ\text{C to }150^\circ\text{C}$, $V_{SENSE} = 5\text{ V}$, $GS = \text{FFFh}$, $BC = \text{FFh}$, $DC = \text{7Fh}$ with upperDCrange (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I_{REF_SC}	IREF resistor short-circuit-detection threshold	$V_{CC} = 5\text{ V}$	2	2.7	3.2	mA
$I_{REF_SCHY_S}$	IREF resistor short-circuit-detection threshold hysteresis	$V_{CC} = 5\text{ V}$	0.3			mA
T_{PTW}	Pre-thermal warning flag threshold	Junction temperature	125	135	145	$^\circ\text{C}$
T_{HYS_PTW}	Pre-thermal warning flag hysteresis	Junction temperature		10		$^\circ\text{C}$
T_{SD}	Thermal error flag threshold	Junction temperature	150	160	170	$^\circ\text{C}$
T_{HYS_TEF}	Thermal error flag hysteresis	Junction temperature		10		$^\circ\text{C}$

6.6 Timing Requirements

$V_{CC} = 3\text{ V to }5.5\text{ V}$, $T_J = -40^\circ\text{C to }150^\circ\text{C}$.

	MIN	NOM	MAX	UNIT
$f_{CLK(SCK)}$ SCK data-shift clock frequency			4	MHz
$f_{CLK(GCLK)}$ GCLK grayscale clock frequency			8	MHz
t_{WH0} SCK high pulse duration	60			ns
t_{WL0} SCK low pulse duration	60			ns
t_{WH1} LATCH high pulse duration	80			ns
t_{WL1} LATCH low pulse duration	80			ns
t_{WL2} BLANK pulse duration	80			ns
t_{WH3} GCLK high pulse duration	40			ns
t_{WL3} GCLK low pulse duration	40			ns
t_{SU0} SDI - SCK \uparrow setup time	55			ns
t_{SU1} BLANK \uparrow - GCLK \uparrow setup time	60			ns
t_{SU2} LATCH \uparrow - SCK \uparrow setup time	200			ns
t_{SU3} LATCH \uparrow for GS data - GCLK \uparrow when display timing reset mode is disabled, setup time	90			ns
t_{SU4} LATCH \uparrow for GS data - GCLK \uparrow when display timing reset mode is enabled, setup time	150			ns
t_{H0} SCK \uparrow - SDI hold time	55			ns
t_{H1} SCK \uparrow - LATCH \uparrow hold time	85			ns
t_{H2} SCK \uparrow - LATCH \downarrow hold time	55			ns
t_{RI0} SDI, SCK, LATCH rise time			50	ns
t_{RI1} GCLK rise time			30	ns
t_{FI0} SDI, SCK, LATCH fall time			50	ns
t_{FI1} GCLK fall time			30	ns

6.7 Switching Characteristics

over operating junction temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{ro0}	Rise time from 10% V_{SDO} to 90% V_{SDO}		60		ns	
t_{ro1}	Rise time from 10% V_{OUT} to 90% V_{OUT}	$I_{OUT} = 50\text{ mA}$, $SLEW_RATE = 0\text{b}$	200		ns	
t_{ro2}	Rise time from 10% V_{OUT} to 90% V_{OUT}	$I_{OUT} = 50\text{ mA}$, $SLEW_RATE = 1\text{b}$	60	100	140	ns

Switching Characteristics (continued)

over operating junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{fo0}	Fall time from 90% V_{SDO} to 10% V_{SDO}			30		ns
t_{fo1}	Fall time from 90% V_{OUT} to 10% V_{OUT}	$I_{OUT} = 50 \text{ mA}$, SLEW_RATE = 0b		200		ns
t_{fo2}	Fall time from 90% V_{OUT} to 10% V_{OUT}	$I_{OUT} = 50 \text{ mA}$, SLEW_RATE = 1b	30	80	130	ns
t_{pd0}	Propagation delay, SCK \uparrow to SDO		100	140	200	ns
t_{pd1}	Propagation delay, LATCH \uparrow to SDO		130	180	220	ns
t_{pd2}	Propagation delay, BLANK \downarrow to OUTR0, -G0, -B0, -R4, -G4, -B4 off		10	120	260	ns
t_{pd3}	Propagation delay, GCLK \uparrow to OUTR0, -G0, -B0, -R4, -G4, -B4 on		80	160	260	ns
t_{pd4}	Propagation delay, GCLK \uparrow to OUTR1, -G1, -B1, -R5, -G5, -B5 on		120	200	330	ns
t_{pd5}	Propagation delay, GCLK \uparrow to OUTR2, -G2, -B2, -R6, -G6, -B6 on		160	250	370	ns
t_{pd6}	Propagation delay, GCLK \uparrow to OUTR3, -G3, -B3, -R7, -G7, -B7 on		190	280	400	ns
t_{pd7}	Propagation delay, LATCH \uparrow to V_{OUT}	Changing by dot correction control (control data are 0Ch \rightarrow 72h or 72h \rightarrow 0Ch with upper DC range), BCR, -G, -B = FFh	10	80	120	ns
t_{pd8}	Propagation delay, LATCH \uparrow to V_{OUT}	Changing by global brightness control (control data are 19h \rightarrow E6h or E6h \rightarrow 19h with DCRn, -Gn, -Bn = 7Fh with upper DC range)	10	130	200	ns
t_{pd9}	Propagation delay, LATCH \uparrow to APS register and APS_FLAG change	SINK_CURRENT = 0b		5		ns
t_{pd10}	Propagation delay, LATCH \uparrow to APS register and APS_FLAG change	SINK_CURRENT = 1b		10		ns
t_{pd11}	Propagation delay, LATCH \uparrow to LOD_LSD_FLAG change	No failure in LOD-LSD detector circuit		24		ns

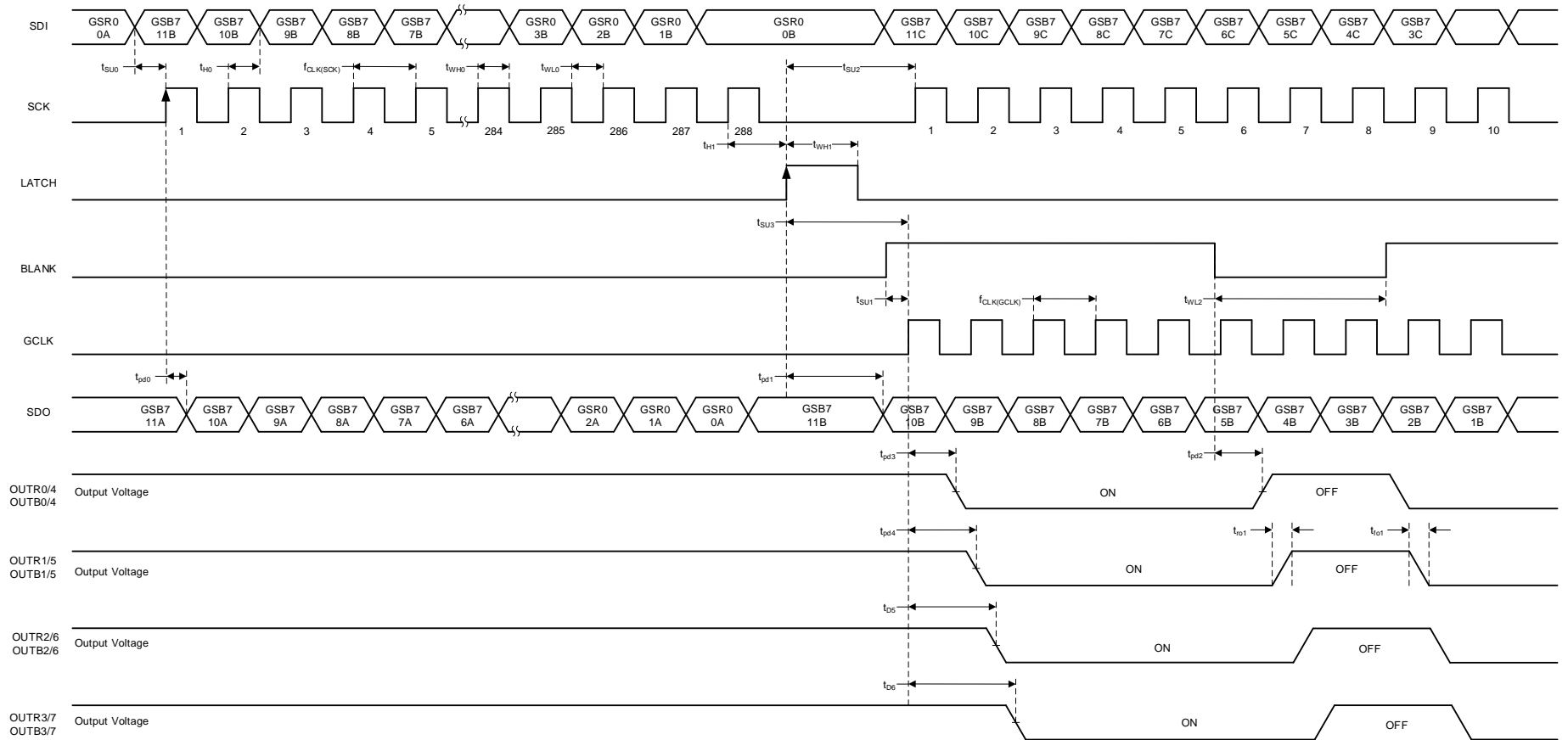
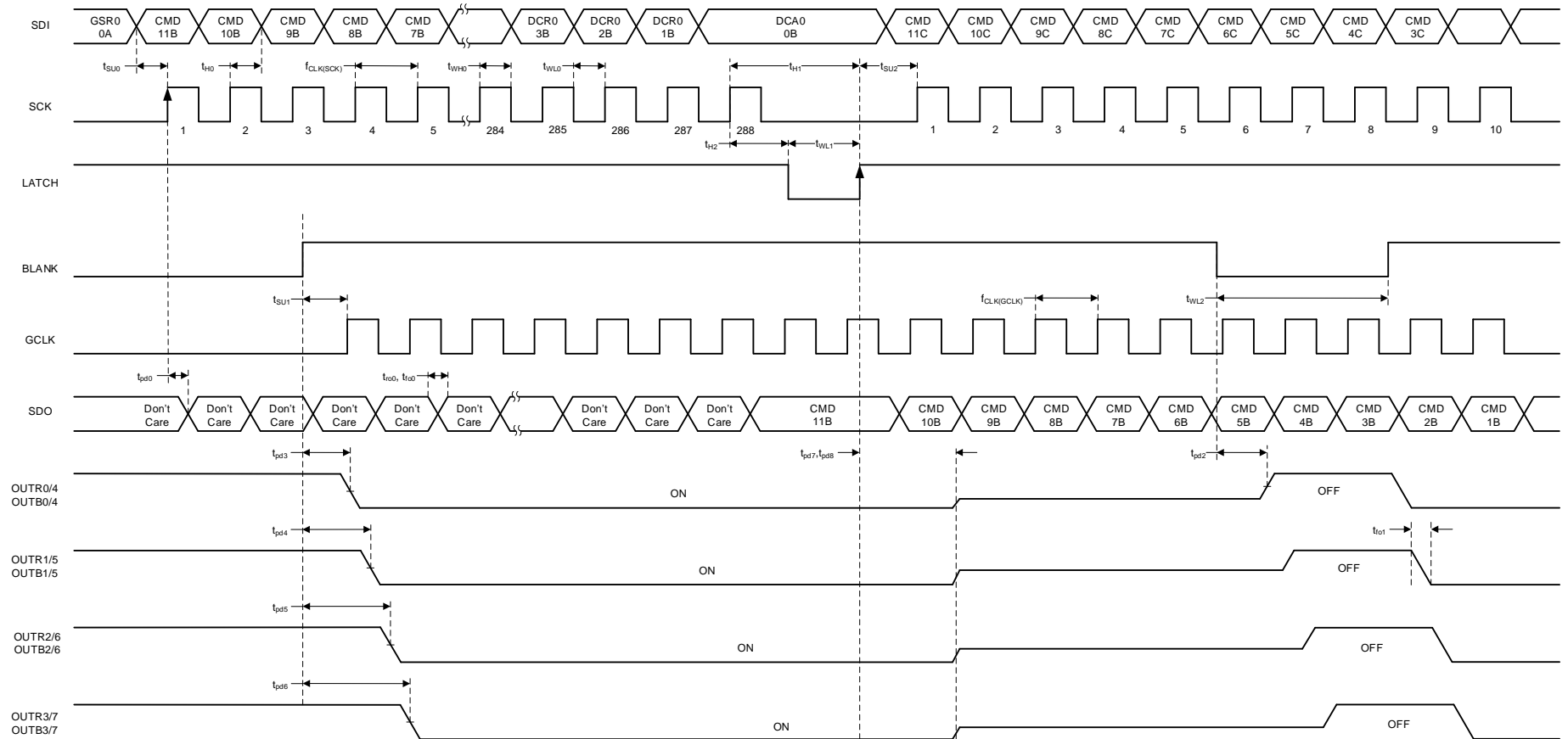


Figure 1. Grayscale (GS) Data Write

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Figure 2. Function Control, Brightness Control, and Dot Correction Data (FC-BC-DC) Write

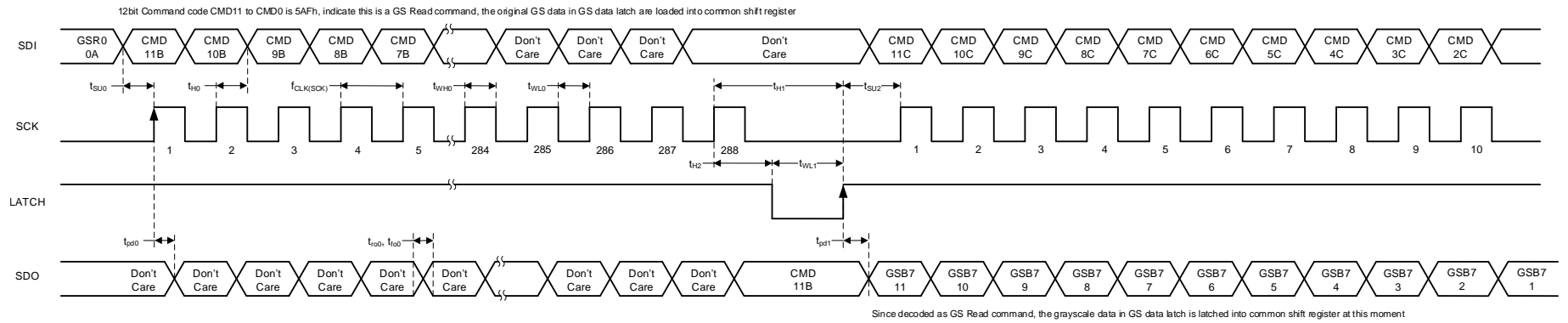


Figure 3. Grayscale (GS) Data Read

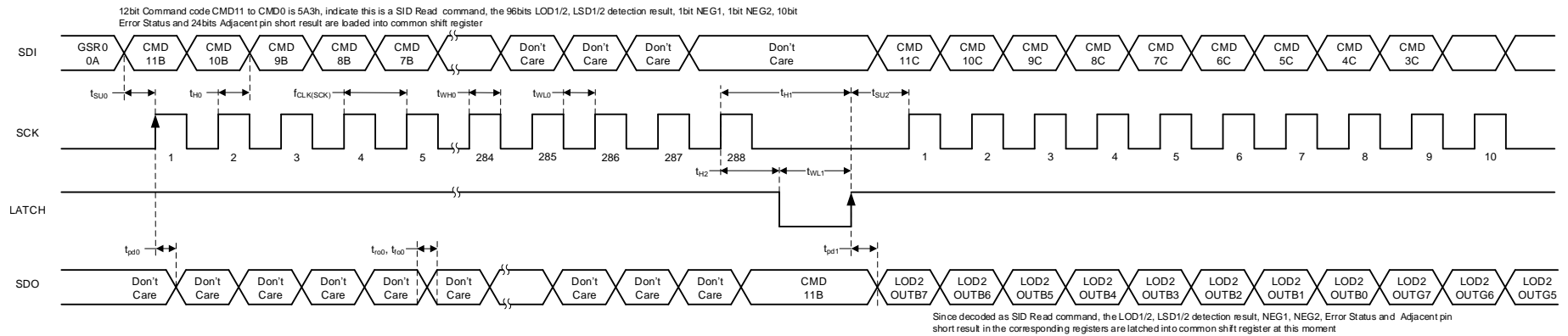


Figure 4. Status Information Data (SID) Read

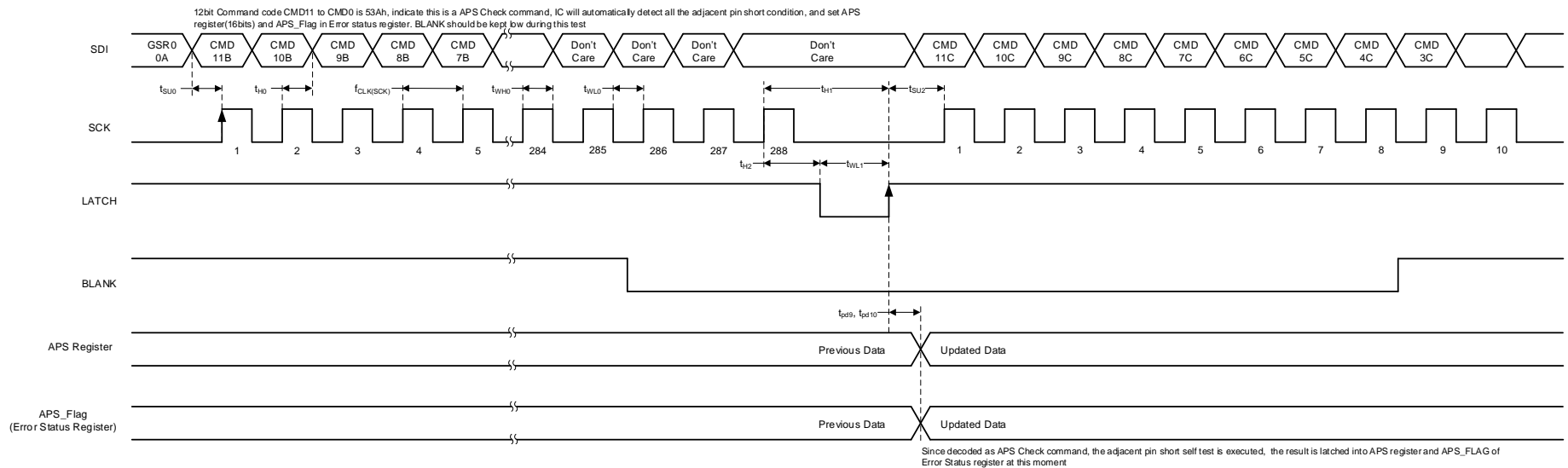


Figure 5. Adjacent-Pin-Short (APS) Check

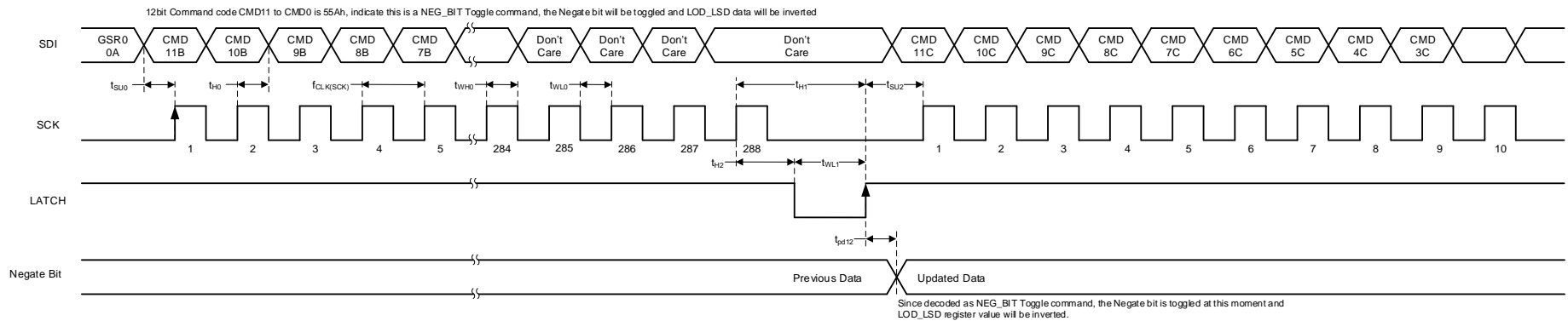


Figure 6. Negate Bit Toggle

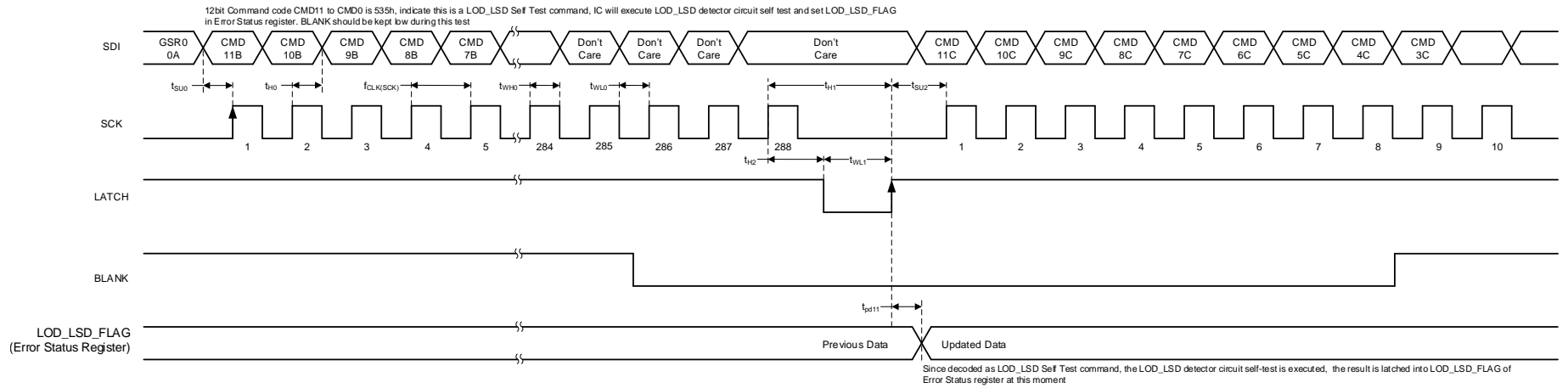


Figure 7. LOD_LSD Self-Test

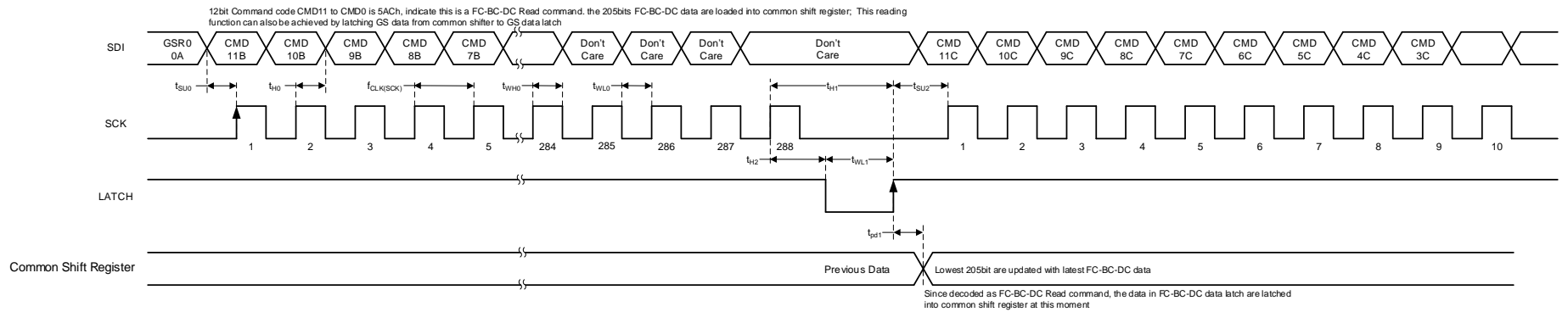


Figure 8. Function Control, Brightness Control, and Dot Correction Data (FC-BC-DC) Read

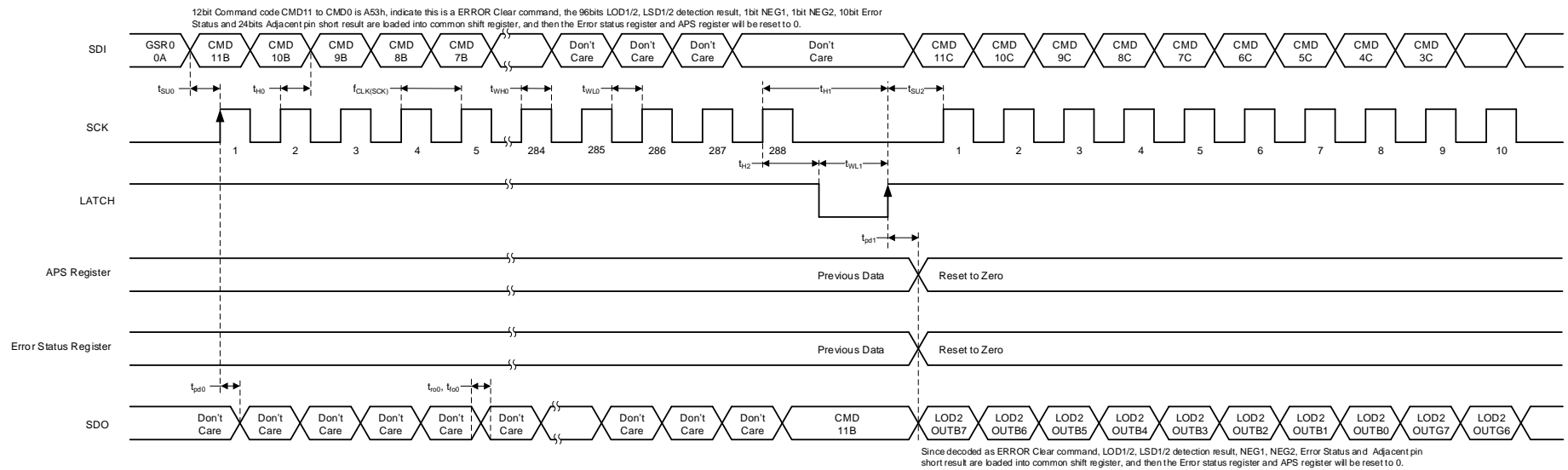


Figure 9. ERROR Clear

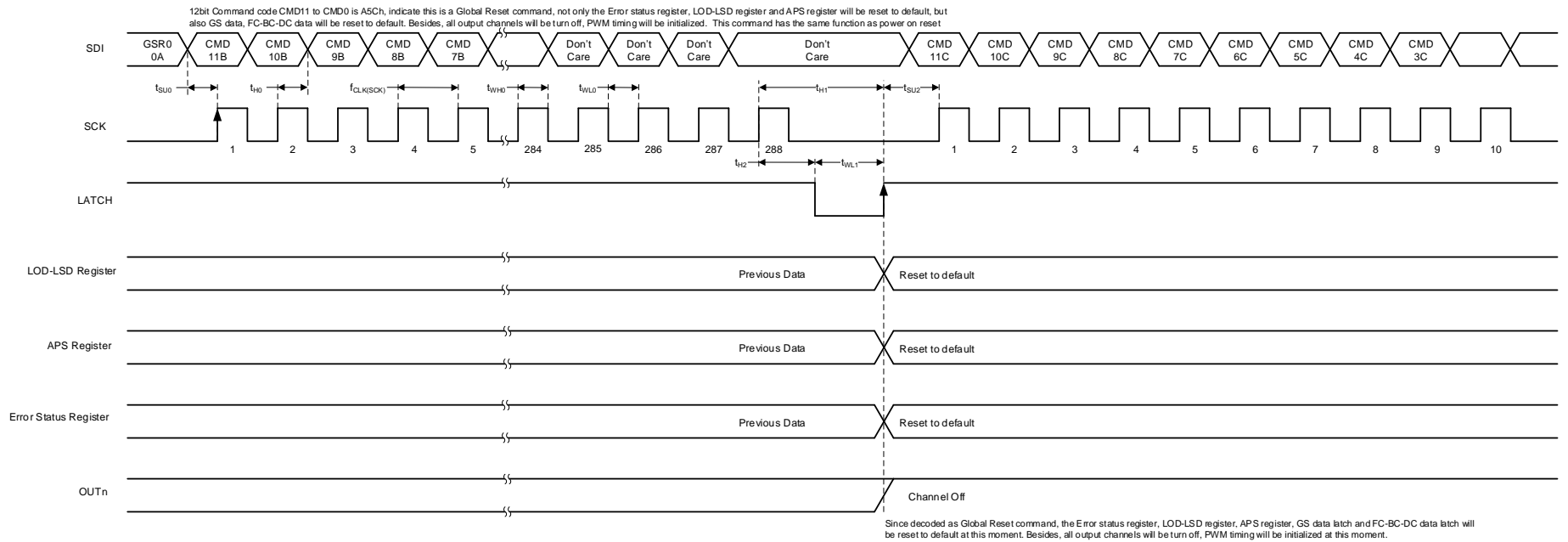
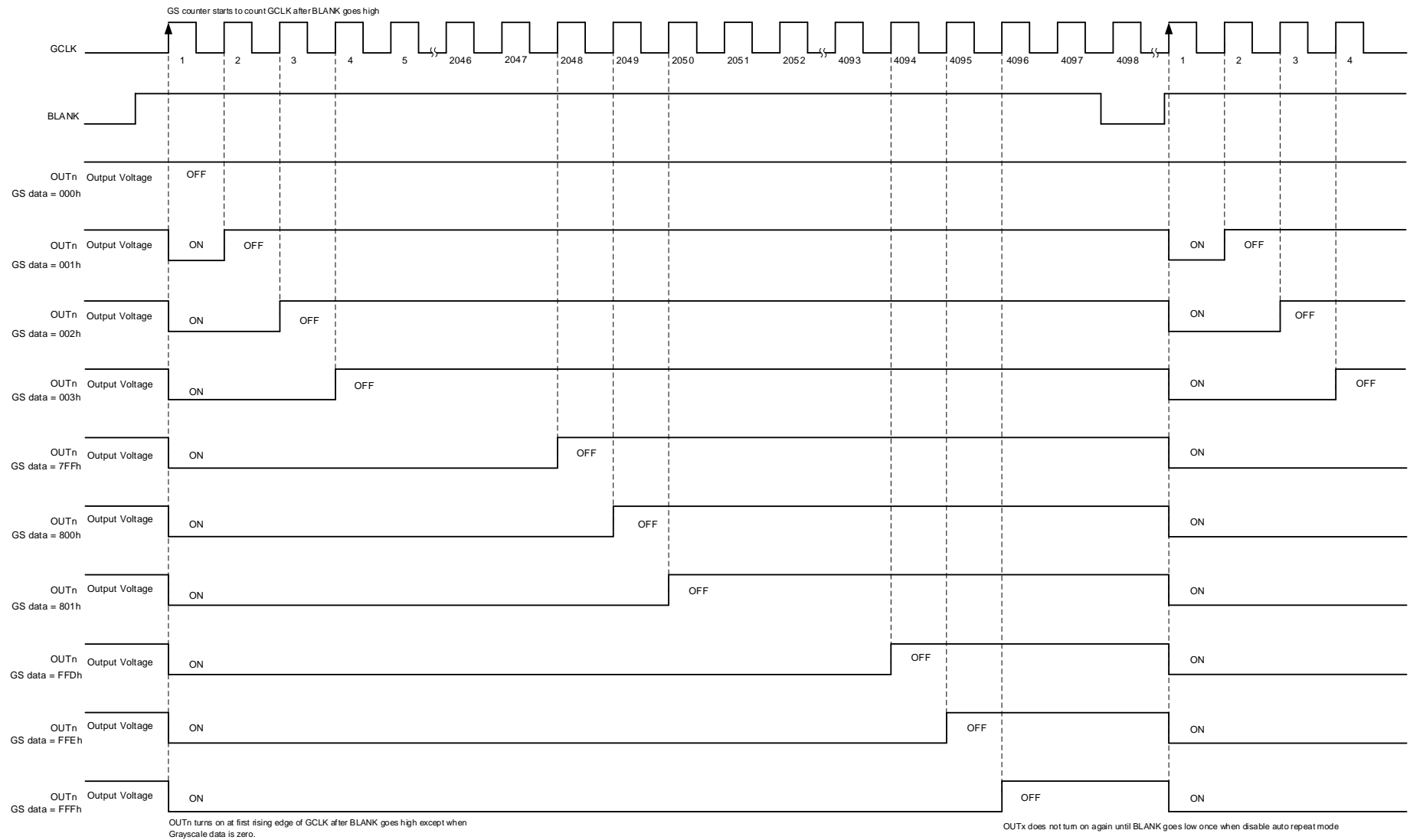


Figure 10. Global Reset



Note 1: The internal blank signal is generated when LATCH is input for GS data with display timing reset enable. Also the signal is generated at 4096 \times GCLK when auto repeat mode is enabled. BLANK can be connected to VCC when TIMING_RESET or AUTO_REPEAT is enabled.

Figure 11. 12-Bit Mode PWM Counter Without Auto-Repeat Mode

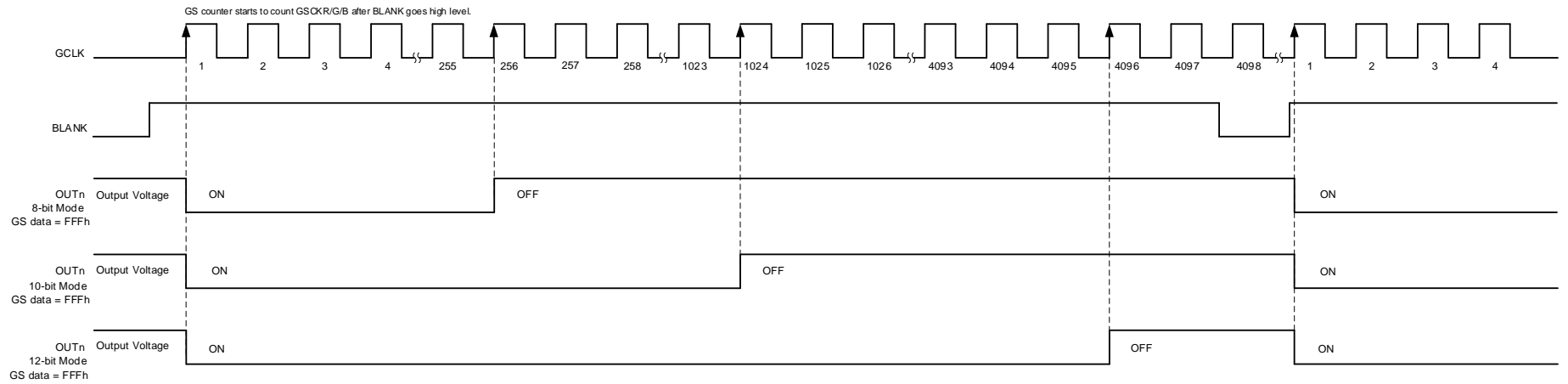


Figure 12. 8-, 10-, 12-Bit Mode PWM Counter Without Auto-Repeat Mode

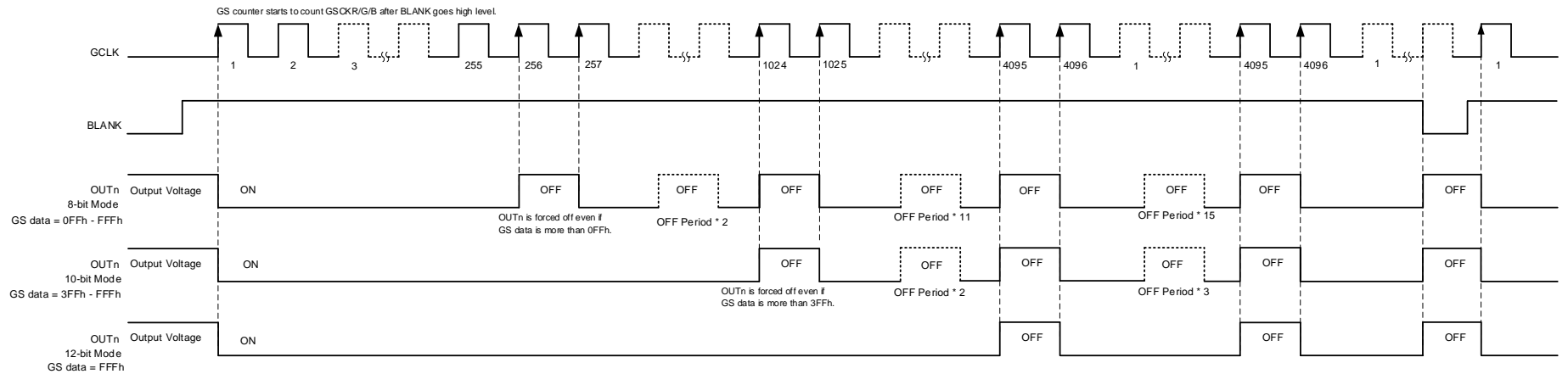


Figure 13. 8-, 10-, 12-Bit Mode PWM Counter With Auto-Repeat Mode

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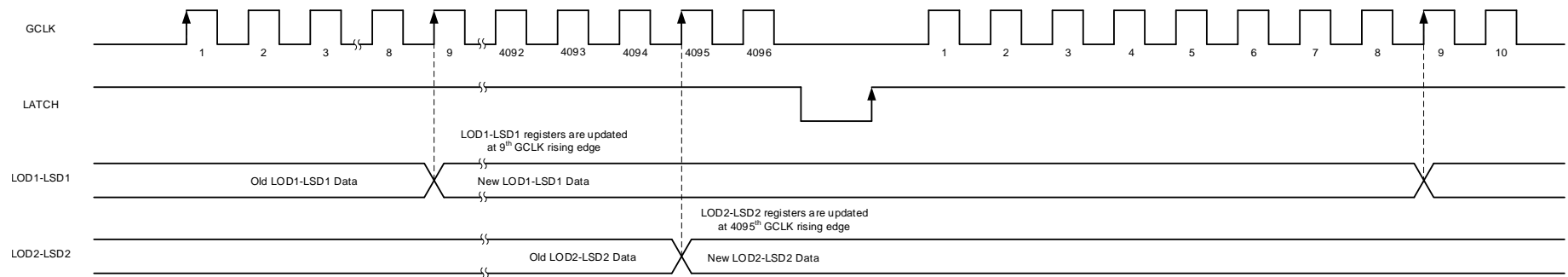
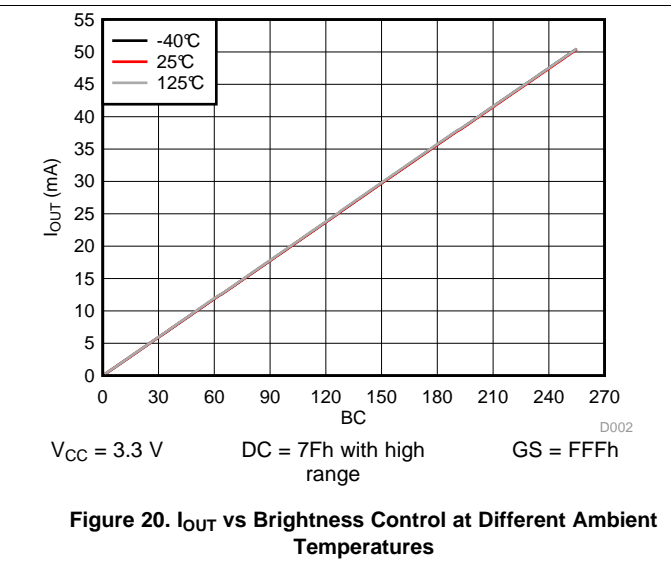
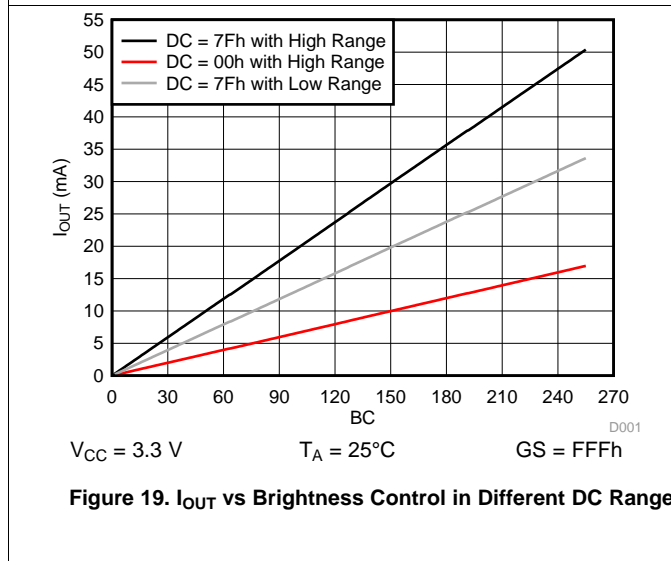
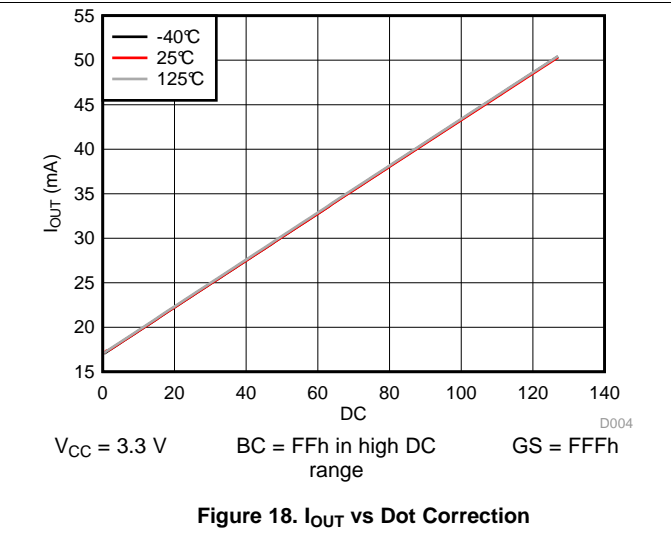
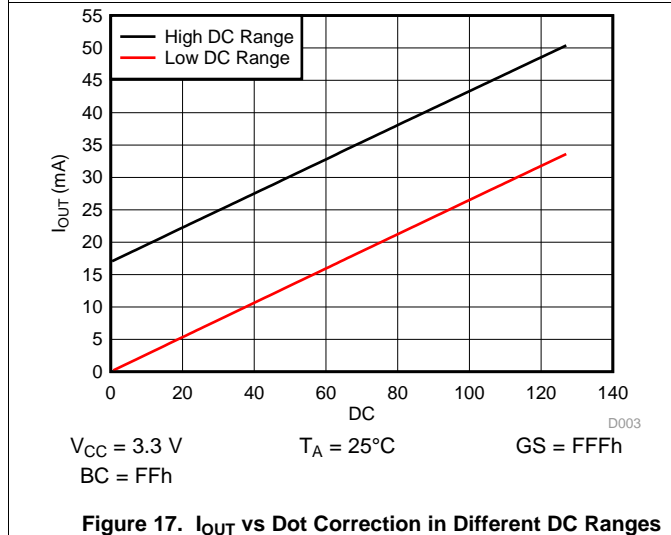
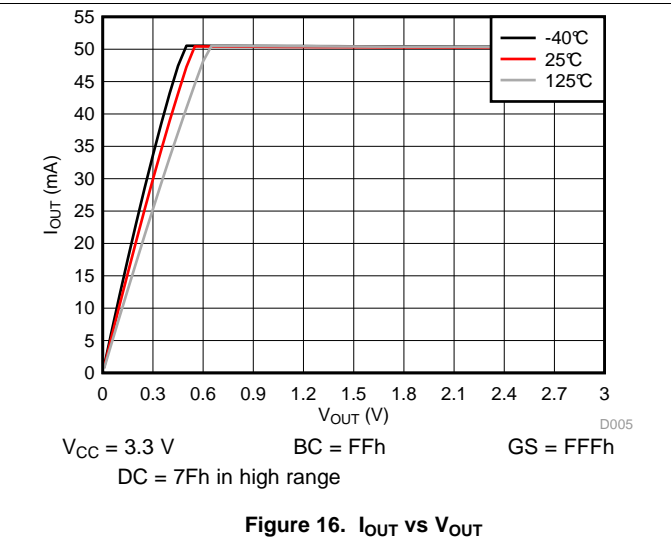
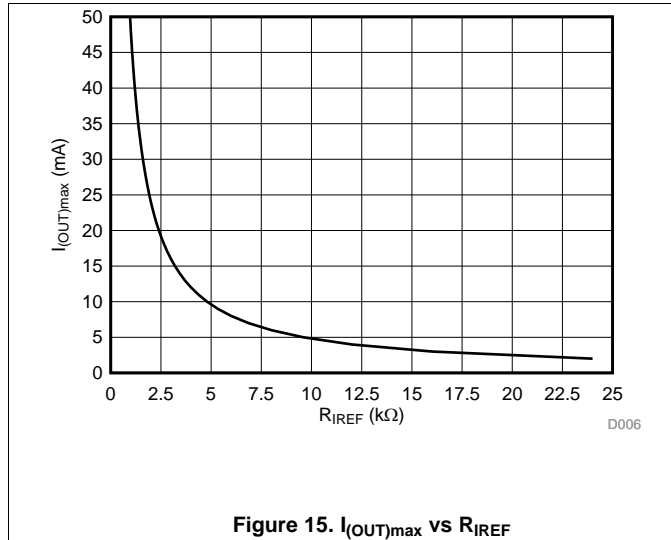


Figure 14. LOD-LSD Register Update Timing

6.8 Typical Characteristics



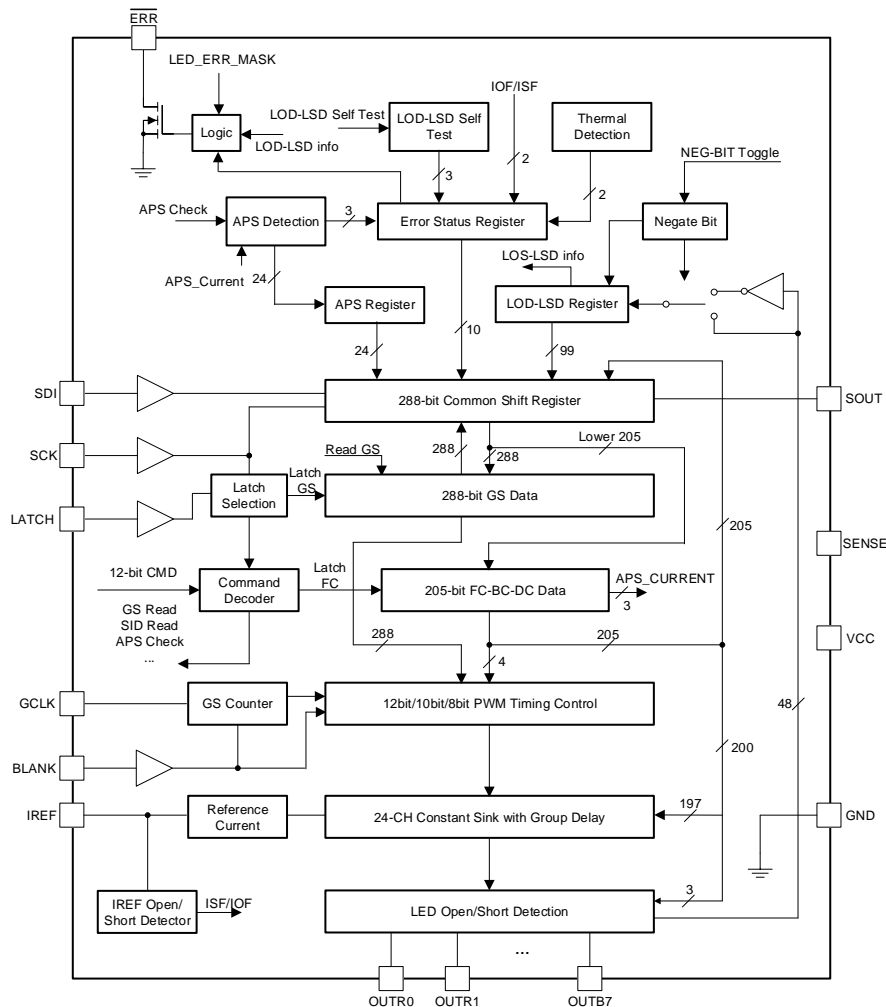
7 Detailed Description

7.1 Overview

In automotive indicator and local dimming backlighting applications, the demand for multi-channel constant-current LED drivers is increasing to achieve uniformity of LED brightness and color temperature. System-level safety considerations require fault-detection capability and device self-check features.

The TLC6C5724-Q1 device is an automotive 24-channel constant-current RGB LED driver with LED diagnostics. The TLC6C5724-Q1 device provides up to 50-mA output current set by an external resistor. The current can be adjusted by 7-bit dot correction with two subranges for individual output and an 8-bit brightness control for the outputs of each color group. The brightness can be adjusted individually for each channel through a 12-, 10-, or 8-bit grayscale control. Fault-detection circuits are available to detect system faults including LED faults, adjacent-pin short faults, reference-resistor faults, and more. Negate bit toggle and LOD-LSD self-test provide a device self-check function to improve system reliability. Configurable slew-rate control optimizes the noise generation of the system and improves the system EMC performance. Output -channel group delay helps to reduce inrush current to optimize the system design. The SDI and SDO pins allow more than one device to be connected in a daisy chain for control through one serial interface.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Maximum Constant-Sink-Current Setting

LED full-scale current can be programmed using an external resistor connected between the IREF pin and GND. The R_{IREF} resistor value is calculated with the following formula.

$$R_{IREF} = K \times \frac{V_{IREF}}{I_{(OUT)max}}$$

where

- V_{IREF} is the reference voltage
 - K is the IREF-current to output-current ratio
 - $I_{(OUT)max}$ is full-scale current for each output
- (1)

Figure 15 shows the reference resistor calculation curve.

7.3.2 Brightness Control and Dot Correction

The TLC6C5724-Q1 device implements an 8-bit group brightness control (BC) and 7-bit individual dot correction (DC) to calibrate the output current. The 24 output channels are divided into three groups: OUTRn, OUTGn, and OUTBn. Each group contains 8 output channels. There are two configurable ranges for the DC value of each group. One is the low DC range with output current from 0 to 66.7% $I_{(OUT)max}$. The other is the high DC range with output current from 33.3% $I_{(OUT)max}$ to 100% $I_{(OUT)max}$. The IREF resistor, BC, DC, and DC range together determine the channel output current, as shown in Figure 21. Equation 2 and Equation 3 are the detailed output current calculation formulas.

Equation 2 determines the output sink current for each color group when DC is in the high adjustment range.

$$I_{OUT} = \left(\frac{1}{3} \times I_{(OUT)max} + \frac{2}{3} \times I_{(OUT)max} \times \frac{DC}{127} \right) \times \frac{BC}{255}$$
(2)

Equation 3 determines the output sink current for each color group when DC is in the low adjustment range.

$$I_{OUT} = \frac{2}{3} \times I_{(OUT)max} \times \frac{DC}{127} \times \frac{BC}{255}$$
(3)

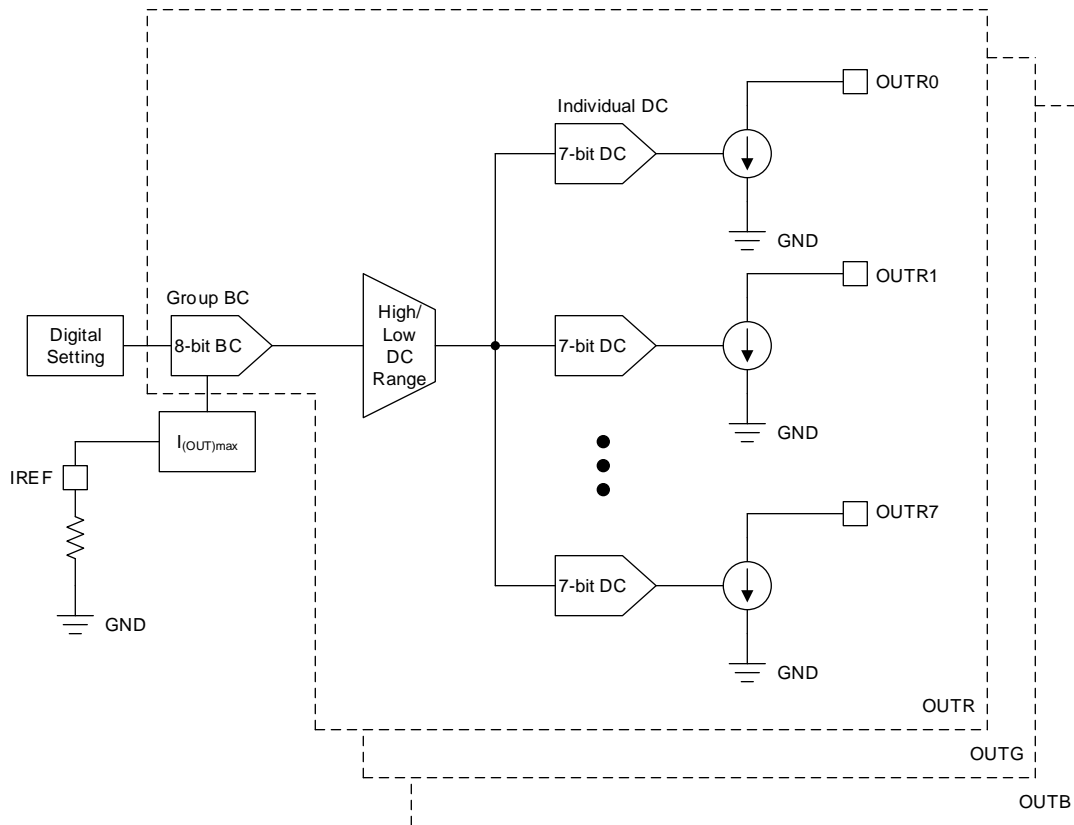
Feature Description (continued)


Figure 21. Brightness Control and Dot Correction Block Diagram

7.3.3 Grayscale Configuration

The TLC6C5724-Q1 device implements a grayscale configuration function to realize the individual PWM dimming function for the output channels. The grayscale has three global configuration modes, 12-bit, 10-bit and 8-bit. The GCLK input provides the clock source for the internal PWM generator. The GS counter counts the GCLK number and compares the number with the channel grayscale register value. The output channel turns off when the GS counter value reaches the grayscale register value. [Figure 22](#) shows the detailed block diagram of the PWM generator.

To restart a new PWM cycle, users can use two methods. One is to toggle the BLANK pin after the GS counter reaches the maximum count value, because BLANK low resets the GS counter and BLANK high restarts the GS counter. Another is to pull BLANK high and set the AUTO_REPEAT&TIMING_RESET register bit to 1. The PWM starts a new cycle automatically after the GS counter reaches the maximum count value.

Feature Description (continued)

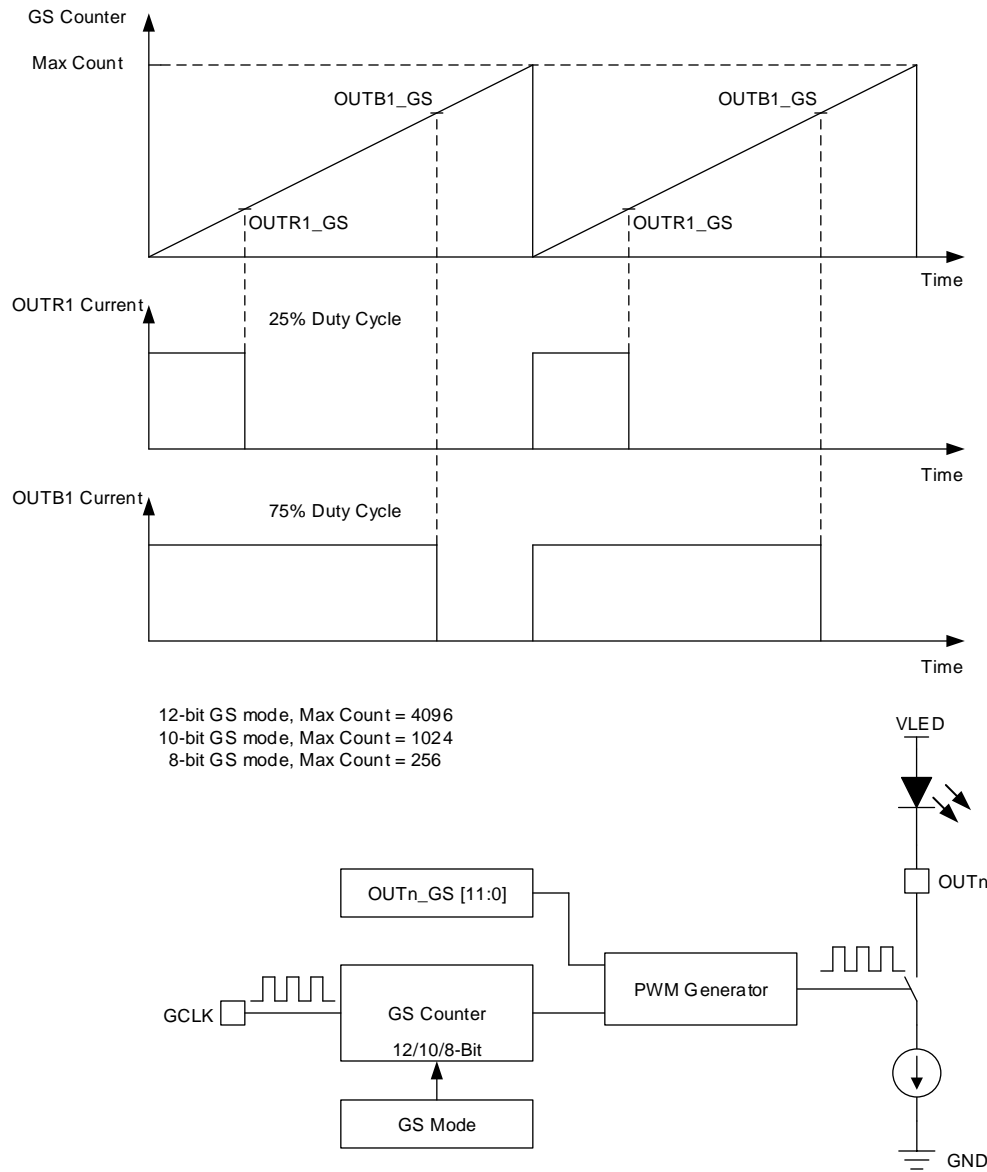


Figure 22. PWM Generator

7.3.3.1 PWM Auto Repeat

The PWM auto repeat function is configured by the AUTO_REPEAT bit. The AUTO_REPEAT bit is 0 by default, and the PWM auto repeat function is disabled under this condition. The PWM cycle only executes once, so users must toggle BLANK to restart a new PWM cycle. [Figure 11](#) and [Figure 12](#) show the PWM operation in this mode. When the AUTO_REPEAT bit is 1, the PWM auto repeat function is enabled. The PWM cycle automatically repeats as long as BLANK is high and GCLK is present, as shown in [Figure 13](#).

Feature Description (continued)

7.3.3.2 PWM Timing Reset

PWM timing reset function is configured by the TIMING_RESET bit. The PWM timing reset function can restart a PWM cycle with newly configured duty-cycle after a GS data write. The TIMING_RESET bit is 0 by default. The PWM timing reset function is disabled in this condition. The PWM duty cycle is not influenced by a GS data write. The newly configured PWM duty-cycle only is valid after the current PWM cycle finishes. When the TIMING_RESET bit is 1, the PWM timing reset function is enabled, and the PWM cycle restarts with the new PWM duty-cycle immediately after the GS data write.

7.3.4 Diagnostics

The TLC6C5724-Q1 device integrates a full LED diagnostics functionality, such as LED open detection (LOD), LED short detection (LSD), and output short-to-GND detection (OSD), which improves the system safety.

7.3.4.1 LED Diagnostics

An LOD-LSD detection circuit compares the output voltage with the LOD threshold and LSD threshold, and the output results show in [Table 1](#).

Table 1. LOD-LSD Detection

OUTPUT VOLTAGE CONDITION	DETECTOR OUTPUT BIT VALUE	
	LOD	LSD
$V_{OUTn} < LOD_VOLTAGE$	1	0
$LOD_VOLTAGE < V_{OUTn} < LSD_VOLTAGE$	0	0
$V_{OUTn} > LSD_VOLTAGE$	0	1

The LOD threshold can be configured by the LOD_VOLTAGE bit. The threshold is 0.3 V when LOD_VOLTAGE = 0, and the threshold is 0.5 V when LOD_VOLTAGE = 1.

Table 2. LOD Threshold

LOD_VOLTAGE BIT	LOD THRESHOLD
0 (Default)	0.3 V
1	0.5 V

LSD threshold is configured by the LSD_VOLTAGE bit. The threshold is $V_{VSENSE} - 0.3$ V when LSD_VOLTAGE = 0, and the threshold is $V_{SENSE} - 0.7$ V when LSD_VOLTAGE = 1.

Table 3. LSD Threshold

LSD_VOLTAGE BIT	LSD THRESHOLD
0 (Default)	$V_{SENSE} - 0.3$ V
1	$V_{SENSE} - 0.7$ V

There are two sets of LOD-LSD registers in the device. One is the LOD1-LSD1 registers, another is the LOD2-LSD2 registers. Each group of registers consists of 24 bits of LOD data and 24 bits of LSD data, corresponding to 24 channel outputs. The device updates the LOD1-LSD1 registers at the 9th GCLK rising edge. The device updates the LOD2-LSD2 registers the Nth GCLK rising edge. N is the maximum GCLK number in a PWM period minus 1, see [Table 4](#).

To detect all kinds of LED faults, the output channel should turn ON at the 9th GCLK rising edge, and turn OFF at the Nth GCLK rising edge.

The device integrates an internal pullup circuit for LED diagnostics, shown in [Figure 23](#). The circuit turns off during the channel on-state, but turns on to charge the output pin during the channel off-state. For an LED-short fault, both LSD1 and LSD2 are 1. For an LED-open fault, both LOD1 and LSD2 are 1. For an output short-to-GND fault, both LOD1 and LOD2 are 1. [Table 5](#) shows the details.

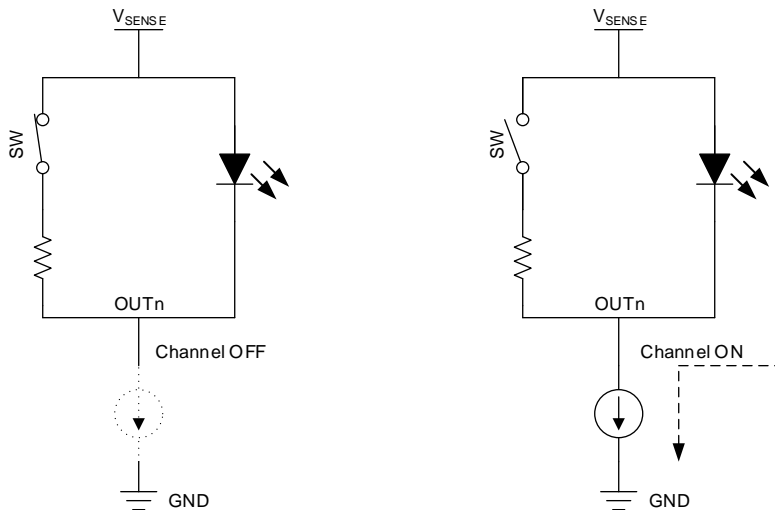


Figure 23. Internal Pullup Circuit

Table 4. LOD-LSD Register Latch Timing

GS COUNTER MODE	LOD1-LSD1	LOD2-LSD2
12-bit	9th GCLK rising edge	4095th GCLK rising edge
10-bit	9th GCLK rising edge	1023rd GCLK rising edge
8-bit	9th GCLK rising edge	255th GCLK rising edge

Table 5. LED Status Lookup Table

LED STATUS	LOD-LSD RESULT			
	LOD1-LSD1 UPDATED AT 9 th GCLK		LOD2-LSD2 UPDATED AT N th GCLK ⁽¹⁾	
LED Ok	LOD1	0	LOD2	0
	LSD1	0	LSD2	1
LED open	LOD1	1	LOD2	0
	LSD1	0	LSD2	1
LED short	LOD1	0	LOD2	0
	LSD1	1	LSD2	1
Output short-to-GND	LOD1	1	LOD2	1
	LSD1	0	LSD2	0

(1) N = 4095 for 12-bit GS mode, 1023 for 10-bit GS mode, 255 for 8-bit GS mode

In some cases, users may need to turn off output channels before the 9th GCLK to disable output channels, or turn on output channels at Nth GCLK to get more brightness. LOD_LSD faults are reported as shown in Table 6. Users can ignore the fault according to the GS register setting value.

Table 6. PWM Status Lookup Table

PWM STATUS	LOD-LSD RESULT			
	LOD1-LSD1 UPDATED AT 9 th GCLK		LOD2-LSD2 UPDATED AT N th GCLK ⁽¹⁾	
PWM OK	LOD1	0	LOD2	0
	LSD1	0	LSD2	1
Channel off before 9th GCLK	LOD1	0	LOD2	0
	LSD1	1	LSD2	1
Channel on at Nth GCLK	LOD1	0	LOD2	0
	LSD1	0	LSD2	0

(1) N = 4095 for the 12-bit GS mode, 1023 for the 10-bit GS mode, 255 for the 8-bit GS mode

The LOD_LSD status is updated every PWM cycle. Figure 14 is an example of the LOD-LSD register update timing for the 12-bit GS mode.

7.3.4.2 Adjacent-Pin-Short Check

The device implements the APS check function to detect the adjacent-pin short failures during system initialization. TI recommends to do an APS check when channels are all off. The APS check can be executed by writing the APS check command.

If there is no adjacent-pin short failure, the device passes the APS check and 011b is latched into APS FLAG in the error status register. The 24-bit APS register is 0. If there are two adjacent pins shorted, 110b is latched into APS_FLAG in the error status register. The corresponding bit in the APS register is set to 1. Users can read out the 24-bit data from the APS register to check which channel has the APS failure. Table 7 shows the details of the APS_FLAG and APS register. Table 8 shows the bit arrangement of the APS register. To read this APS information, see Table 22.

Table 7. APS Flag and APS Register

REGISTER	VALUE	DESCRIPTION
APS_FLAG	011b	Pass, no adjacent pins short
	110b	Fail, adjacent pins short
Bit in APS register (24-bit total)	0b	This OUTn pin is not shorted with other pins
	1b	This OUTn pin is shorted with other pins

Table 8. Bit Arrangement of the APS Register

BIT OF APS REGISTERS	CORRESPONDING OUTPUTS
Bit 23	OUTB7
Bit 22	OUTB6
Bit 21	OUTB5
Bit 20	OUTB4
Bit 19	OUTB3
Bit 18	OUTB2
Bit 17	OUTB1
Bit 16	OUTB0
Bit 15	OUTG7
Bit 14	OUTG6
Bit 13	OUTG5
Bit 12	OUTG4
Bit 11	OUTG3
Bit 10	OUTG2
Bit 9	OUTG1
Bit 8	OUTG0
Bit 7	OUTR7

Table 8. Bit Arrangement of the APS Register (continued)

BIT OF APS REGISTERS	CORRESPONDING OUTPUTS
Bit 6	OCTR6
Bit 5	OCTR5
Bit 4	OCTR4
Bit 3	OCTR3
Bit 2	OCTR2
Bit 1	OCTR1
Bit 0	OCTR0

APS_FLAG and the APS registers are all 0 by default. After an APS check command, APS_FLAG should be 011b or 110b. Otherwise there is a failure in the APS check circuit. If the APS check result fails, the ERR pin is pulled low, the APS_FLAG value is 110b, and the ERR pin status stays unchanged until the fault is removed and the user executes an ERROR clear command. [Figure 5](#) and [Figure 9](#) show more detail.

As different LEDs have different parasitic capacitance, to make sure the APS Check function is suitable for all kinds of LEDs, the device provides two configuration bits for APS current and APS time. The APS current is selected by APS_CURRENT as shown in [Table 9](#). The APS time is selected by APS_TIME as shown in [Table 10](#).

Table 9. APS Current Selection

APS_CURRENT BIT	APS CURRENT
0b	20 μ A
1b	40 μ A

Table 10. APS Time Selection

APS_TIME BIT	ADJACENT-PIN-SHORT DETECTION TIME
0b	10 μ s
1b	20 μ s

7.3.4.3 IREF Short and IREF Open Detection

To protect the device from a reference-resistor short or open fault, the device integrates IREF short and open protection. In an IREF short or open fault condition, the device reports the fault and sets the output current to a default value to help improve the system safety.

By default, the ISF and IOF flags are 0. When the IREF current exceeds the fault-detection threshold, the ERR pin is pulled down, the ISF or IOF flag is set to 1. The error flag and ERR pin status stay unchanged until the fault is removed and there is an ERROR clear command.

Once there is an ISF or IOF failure, the output current is set to a default value, $I_{(OUT)max}$, of 10 mA, see [Table 11](#). Once the ISF or IOF failure is removed, the output current returns back to the IREF setting value immediately.

Table 11. Criteria of ISF/IOF Judgement and Corresponding Actions

I_{REF}	ISF	IOF	OUTPUT
$I_{REF} \leq 10 \mu$ A	0	1	$I_{(OUT)max} = 10$ mA
10μ A < $I_{REF} \leq 3$ mA	0	0	$I_{(OUT)max} = V_{REF} \times 40 / R_{REF}$
$I_{REF} > 3$ mA	1	0	$I_{(OUT)max} = 10$ mA

7.3.4.4 Pre-Thermal Warning Flag

The TLC6C5724-Q1 device implements a pre-thermal warning (PTW) function. Once the junction temperature exceeds the PTW threshold, the ERR pin is pulled low, the PTW flag in error status register is set to 1, the PTW_FLAG and ERR pin status stay unchanged until the junction temperature drops below $T_{PTW} - T_{HYS_PTW}$, and there is an ERROR clear command.

7.3.4.5 Thermal Error Flag

The TLC6C5724-Q1 device monitors junction temperature all the time. Once the junction temperature exceeds the thermal shutdown threshold, all of the constant-current outputs turn off, the ERR pin is pulled low, the thermal error flag and ERR pin status are set to 1 and stay unchanged until the fault is removed and there is an ERROR clear command. During this state, all the digital functions work normally, and users can read or write data through common shift registers. After the junction temperature drops below $T_{TEF} - T_{HYS_TEF}$, the device goes back to normal operation again. Users can reset the TEF flag by sending an ERROR clear command.

7.3.4.6 Negate Bit Toggle

The TLC6C5724-Q1 device implements a Negate Bit Toggle function to check the LOD-LSD registers, which is useful for safety-related applications.

There are NEG1 and NEG2 bits in the registers, and the values are both 0 by default. After executing the Negate Bit Toggle command, both NEG1 and NEG2 change to 1. The LOD-LSD results are reversed under this condition. If the LOD-LSD registers get stuck, the LOD-LSD results are not reversed, which means there is a fault in the LOD-LSD registers .

The LOD1-LSD1 registers only update on the 9th GCLK rising edge, and the LOD2-LSD2 registers only update on the Nth GCLK rising edge. So after the Negate Bit Toggle command, users must wait for at least one GS counter cycle (4096 GCLKs for the 12-bit GS counter mode, 1024 GCLKs for the 10-bit GS counter mode, or 256 GCLKs for the 8-bit GS counter mode) before reading the SID registers. So if the GCLK signal is lost, it can also be detected by the negate-bit toggle function.

7.3.4.7 LOD_LSD Self-Test

The TLC6C5724-Q1 device implements an LOD_LSD self-test function to check the LOD_LSD detection circuit to improve the system reliability. If the LOD_LSD detection circuit fails to detect the LED failure, the LOD_LSD self-test Function can identify and report the malfunction.

The LOD_LSD self-test function can be executed by sending the LOD_LSD self-test command. LOD_LSD_FLAG is 000b by default. After the LOD_LSD self-test command, if there is no fault on LOD_LSD detection circuit, and the LOD_LSD_FLAG value is 011b. If there are failures on the LOD_LSD detection circuits, the LOD_LSD_FLAG value is 110b, the ERR pin is pulled low, and the bit values stay unchanged until the fault is removed and an ERROR clear command is executed. If the LOD_LSD_FLAG is neither 011b nor 110b, there should be something wrong in the self-test procedure.

7.3.4.8 \overline{ERR} Pin

The TLC6C5724-Q1 device supports an active-low open-drain error output. [Figure 24](#) shows the error pulldown block diagram. 10-bit error status information controls the error pulldown circuit directly. But LED failure can be masked by the LED_ERR_MASK bit. The LED_ERR_MASK value is 1 by default, so an LED failure is masked from the error pulldown circuit. Even if there is an LED failure, the ERR pin is not pulled down by this LED failure. If LED_ERR_MASK is 0, the ERR pin is pulled down by an LED failure to indicate an error scenario. Users can use an MCU interrupt to read out the fault information.

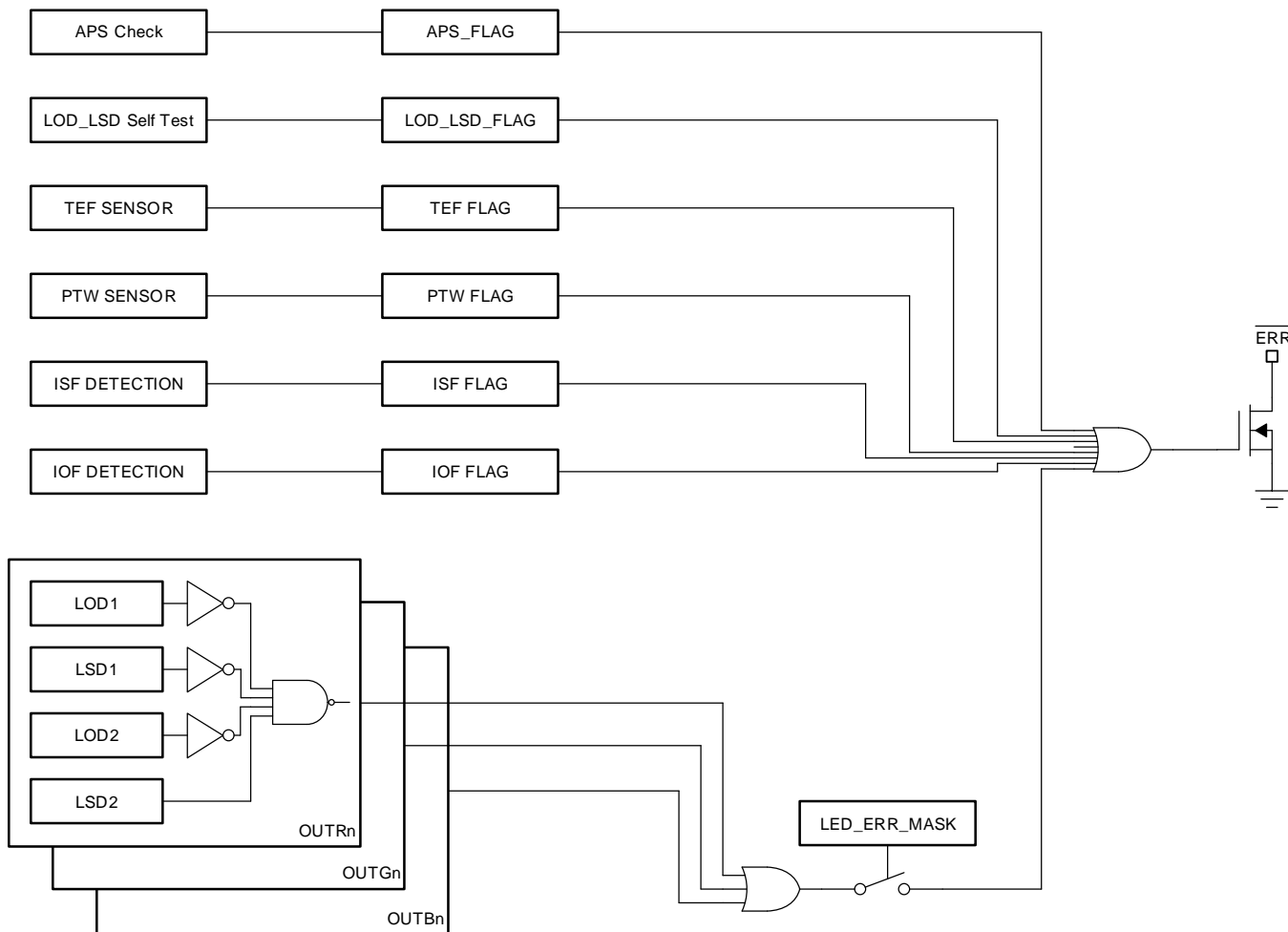


Figure 24. ERR Pin Pulldown Scheme

7.3.4.9 ERROR Clear

This command is used to clear the error flags in the error status register and APS register. The A53h 12-bit command code indicates an ERROR clear command. After executing the ERROR clear command, the 96-bit LOD_LSD registers, 1-bit NEG1, 1-bit NEG2, 10-bit error status and 24-bit adjacent-pin-short results are loaded into the common shift register. The error status registers and APS registers are reset to 0 if the error is removed. See Figure 9 for more detail.

7.3.4.10 Global Reset

This command is used to implement a power-on reset with software input. The A5Ch 12-bit command code initiates a global reset command. After executing the global reset command, all internal registers are reset to their default values. See Figure 10 for more detail.

7.3.4.11 Slew Rate Control

To improve system EMI performance, the TLC6C5724-Q1 device implements a programmable slew rate control for the output channels. This output slew rate is configured by the SLEW_RATE bit in the FC-BC-DC register. The SLEW_RATE bit is 0 by default, and the rising and falling time of the output is 200 ns. When the SLEW_RATE bit is 1, the rising and falling time of each output is 100 ns.

7.3.4.12 Channel Group Delay

Large surge currents may flow through the system if all 24 channels turn on simultaneously. These large current surge could induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC6C5724-Q1 device implements channel turn-on delay for each group to reduce the surge current. The output current sinks are grouped into four groups.

Group 1: OTR0, -G0, -B0, OTR4, -G4, -B4.

Group 2: OTR1, -G1, -B1, OTR5, -G5, -B5.

Group 3: OTR2, -G2, -B2, OTR6, -G6, -B6.

Group 4: OTR3, -G3, -B3, OTR7, -G7, -B7.

All group 2 channels turn on and off 50 ns later than group 1 channels, all group 3 channels turn on and off later than group 2 channels, and all group 4 channels turn on and off 50 ns later than group 3 channels. [Figure 1](#) shows the details.

7.4 Device Functional Modes

7.4.1 Power Up

To make the device work normally, users must provide two power supplies to the TLC6C5724-Q1 device. One is V_{CC} , 3 V–5.5 V, for device internal logic power. The other is a supply up to 8 V, which is the power supply for the LED loads. To make sure the LED diagnostics feature works normally, the LED supply must connect to the SENSE pin directly.

7.4.2 Device Initialization

After device power on, users must send the error clear command and global reset command to initialize the device and make sure there are no existing faults on the circuit.

7.4.3 Fault Mode

The TLC6C5724-Q1 has full diagnostics features. The device can detect faults and latch the faults into registers. For device faults such as IREF resistor open or short, the device enters a self-protection scenario. The device reports the faults and sets the output current to a default value. For the overtemperature fault, the device turns off the output channels and latches the fault into the TEF register. Except for these two faults, for all other faults including LED faults, the device only detects and reports the faults, but does not take actions to handle the faults, and the channels keep their configured status. Users must read out the faults and decide how to handle the faults.

7.4.4 Normal Operation

Users must program the device through the serial interface for normal operation. Users write to the FC-BC-DC registers to set the operation mode and output current, write to the grayscale registers to set the PWM duty cycle for each channel, and read the SID registers to get device fault information.

7.5 Programming

7.5.1 Register Write and Read

The TLC6C5724-Q1 device is programmable via serial interface. It contains a 288-bit common shift register to shift data from SDI into the device. The register LSB connects to SDI and the MSB connects to SDO. On each SCK rising edge, the data on SDI shifts into the register LSB and all 288 data bits shift towards the MSB. The data appears on SDO when the 288-bit common shift register overflows.

The TLC6C5724-Q1 data write command contains 288-bit data. According to the following different criteria, there are three types of data write commands: FC-BC-DC write, GS data write, and special command.

- When LATCH is high at the 288th SCK rising edge, and the 12 MSBs of the 288-bit data are 0, the 205 LSBs of 288-bit data shift to the function control (FC), brightness control (BC) and dot correction (DC) registers on the LATCH rising edge, as shown in [Figure 2](#).
- When LATCH is low at the 288th SCK rising edge, all 288-bit data shifts into the grayscale (GS) configuration registers on the LATCH rising edge, as shown in [Figure 1](#).

Programming (continued)

- When LATCH is high at the 288th SCK rising edge, and the 12 MSBs of the 288-bit data match any of the eight 12-bit command codes, the device executes the corresponding command after the LATCH rising edge, as shown in [Special Command Function](#).

When the device powers on, the default value of the 288-bit common shift register is 0.

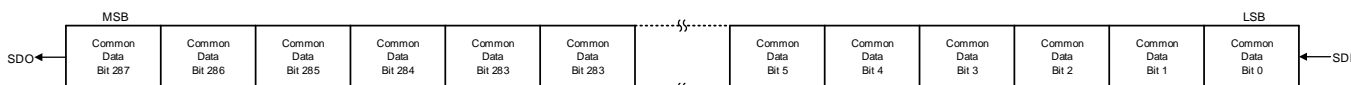


Figure 25. TLC6C5724-Q1 Common Register

7.5.1.1 FC-BC-DC Write

The device latches the 205 LSBs of data in the 288-bit common shift register into the FC-BC-DC registers at the rising edge of the latch signal when the 12 MSBs of the 288-bit data are 0.

When the device is powered on, the FC-BC-DC data latch is reset to all 0s. Therefore, data must be written to the 288-bit common shift register and latched into the FC-BC-DC registers before turning on the constant-current outputs. It is better to keep BLANK low to prevent the outputs from turning on.

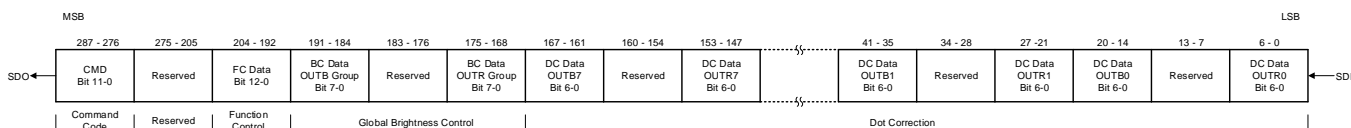


Figure 26. FC-BC-DC Register

7.5.1.1.1 FC Data Write

The FC data is 13 bits in length, located from bit 204 to bit 192. See [Table 12](#) for the detailed description. The default value for all FC data is 0, except for the LED_ERR_MASK bit which is 1.

Table 12. Function-Control Data-Bit Assignment

BIT	NAME	DESCRIPTION
204	LED_ERR_MASK	LOD-LSD failure or PWM error information mask bit 0b = Any LOD-LSD failure or PWM error pulls down the ERR pin 1b = LOD-LSD failure or PWM error is masked from affecting the ERR pin
203	SLEW_RATE	Turnon and turnoff speed configuration bit 0b = 200 ns rising and falling time. 1b = 100 ns rising and falling time.
202	LOD_VOLTAGE	LED open-detection (LOD) threshold 0b = LOD threshold is 0.3 V 1b = LOD threshold is 0.5 V
201	LSD_VOLTAGE	LED short-detection (LSD) threshold 0b = LSD threshold is $V_{SENSE} - 0.3$ V 1b = LSD threshold is $V_{SENSE} - 0.7$ V
200	APS_CURRENT	Adjacent-pin short-detection sink current 0b = 20- μ A APS current 1b = 40- μ A APS current
199	APS_TIME	Adjacent-pin short-detection time 0b = 10 μ s APS detection time 1b = 20 μ s APS detection time
198–197	GS_MODE	Grayscale-counter mode selection. 00/01b = 12-bit mode 10 = 10-bit mode 11 = 8-bit mode
196	TIMING_RESET	Display-timing reset mode 0b = Disabled 1b = Enabled

Programming (continued)

Table 12. Function-Control Data-Bit Assignment (continued)

BIT	NAME	DESCRIPTION
195	AUTO_REPEAT	Auto-display repeat mode 0b = Disabled 1b = Enabled
194	DC_RANGE_B	Dot-correction adjustment range for the BLUE color output 0b = Lower range 0%–66.7% 1b = Higher range 33.3%–100%
193	DC_RANGE_G	Dot-correction adjustment range for the GREEN color output 0b = Lower range 0%–66.7% 1b = Higher range 33.3%–100%
192	DC_RANGE_R	Dot-correction adjustment range for the RED color output 0b = Lower range 0%–66.7% 1b = Higher range 33.3%–100%

The grayscale counter has 12-bit, 10-bit and 8-bit configurations. Bits 198–197 in the FC register configure the grayscale counter mode.

Table 13. GS Counter Mode Table

GRAYSCALE COUNTER MODE (GS_MODE)		FUNCTION MODE
BIT 198	BIT 197	
0	Don't care	12-bit counter mode
1	0	10-bit counter mode, the lowest 10 bits of the 12-bit GS data are valid
1	1	8-bit counter mode, the lowest 8 bits of the 12-bit GS data are valid

7.5.1.1.2 BC Data Write

The BC data is 24 bits length which locates from bit 191 to bit 168. The data of the BC data latch are used to adjust the constant-current values for eight channel constant-current drivers of each color group. The current can be adjusted from 0% to 100% of each output current adjusted by brightness control with 8-bit resolution.

Table 14. Brightness Control Data Bit Assignments

BITS	BRIGHTNESS CONTROL DATA
191–184	OUTB0-OUTB7 group
183–176	OUTG0-OUTG7 group
175–168	OUTR0-OUTR7 group

7.5.1.1.3 DC Data Write

The DC data is 168 bits in length, located from bit 167 to bit 0. The TLC6C5724-Q1 device can adjust the output current of each channel using the DC function. The DC function has two adjustment ranges with 7-bit resolution. Table 15 shows the DC data assignments in the DC registers. The high adjustment range DC can adjust output current from 33.3% to 100% of $I_{(OUT)max}$. The low adjustment range DC can adjust output current from 0% to 66.7% of $I_{(OUT)max}$. The range control is in bits 194–192 in the function control data latch select the high or low adjustment. Bit 194 controls the OUTB DC range. Bit 193 controls the OUTG DC range, Bit 192 controls the OUTR DC range. For details, see Table 12

Table 15. DC Data Assignments

BITS	DATA	BITS	DATA
167–161	OUTB7	83–77	OUTB3
160–154	OUTG7	76–70	OUTG3
153–147	OUTR7	69–63	OUTR3
146–140	OUTB6	62–56	OUTB2

Table 15. DC Data Assignments (continued)

BITS	DATA	BITS	DATA
139–133	OUTG6	55–49	OUTG2
132–126	OUTR6	48–42	OUTR2
125–119	OUTB5	41–35	OUTB1
118–112	OUTG5	34–28	OUTG1
111–105	OUTR5	27–21	OUTR1
104–98	OUTB4	20–14	OUTB0
97–91	OUTG4	13–7	OUTG0
90–84	OUTR4	6–0	OUTR0

Table 16. Output Current vs High DC Range

DC DATA (BINARY)	DC DATA (DECIMAL)	DC DATA (HEX)	BC DATA (HEX)	CURRENT RATIO (%)	CURRENT ($I_{(OUT)max} = 40$ mA)	CURRENT ($I_{(OUT)max} = 2$ mA)
000 0000	0	00	FF	33.3	13.33	0.67
000 0001	1	01	FF	33.9	13.54	0.68
000 0010	2	02	FF	34.4	13.75	0.69
...
111 1101	125	7D	FF	99	39.58	1.98
111 1110	126	7E	FF	99.5	39.79	1.99
111 1111	127	7F	FF	100	40	2

Table 17. Output Current vs Low DC Range

DC DATA (BINARY)	DC DATA (DECIMAL)	DC DATA (HEX)	BC DATA (HEX)	CURRENT RATIO (%)	CURRENT ($I_{(OUT)max} = 40$ mA)	CURRENT ($I_{(OUT)max} = 2$ mA)
000 0000	0	00	FF	0	0.	0
000 0001	1	01	FF	0.5	0.21	0.01
000 0010	2	02	FF	1.0	0.42	0.02
...
111 1101	125	7D	FF	65.6	26.25	1.31
111 1110	126	7E	FF	66.1	26.46	1.32
111 1111	127	7F	FF	66.7	26.67	1.33

Table 18. Output Current vs BC (High DC Range)

DC DATA (BINARY)	BC DATA (DECIMAL)	BC DATA (HEX)	DC DATA (HEX)	CURRENT RATIO (%)	CURRENT ($I_{(OUT)max} = 40$ mA)	CURRENT ($I_{(OUT)max} = 2$ mA)
0000 0000	0	00	7F	0	0	0.00
0000 0001	1	01	7F	0.4	0.16	0.01
0000 0010	2	02	7F	0.8	0.32	0.02
...
1111 1101	253	FD	7F	99.2	39.69	1.98
1111 1110	254	FE	7F	99.6	39.84	1.99
1111 1111	255	FF	7F	100	40	2

7.5.1.2 Grayscale Data Write

The grayscale data, which is 288 bits long, contains a 12-bit grayscale value for each output. The grayscale value sets the channel turnon time. Figure 27 shows the GS register configuration. Figure 1 is the GS write timing diagram. Data is latched from the 288-Bit common shift register into the GS data latch at the rising edge of the LATCH pin. When data is latched into the GS registers, the new data is immediately available on the constant-current outputs. If data are latched with BLANK high, the outputs may turn on or off unexpectedly. So users should update the GS data when BLANK is low.

The 12-bit GS function has 4096 brightness steps, from 0% to 99.97% brightness. The GS function is controlled by a 12-bit GS counter. The GS counter increments on each rising edge of the grayscale reference clock, GCLK. The falling edge of BLANK resets the GS counter value to 0. The GS counter value stays 0 while BLANK is low, even if there is a GCLK input. Pulling BLANK high enables the 12-bit GS counter. The first rising edge of a GS clock after BLANK goes high increments the GS counter by 1 and turns on the outputs. Each additional rising edge increases the GS counter by 1. The GS counter monitors the number of clock pulses on the GCLK pin. The output stays on while the counter value is less than or equal to the GS setting value. The output turns off at the rising edge of the GS counter value when the counter is higher than the GS setting value. Table 20 is the on-time duty cycle of each GS data bit when 12-bit GS counter mode selected.

When the device is powered up, the 288-bit common shift register and GS data latch are reset to 0.

Equation 4 describes each output on time.

$$t_{ON} = t_{GCLK} \times GS$$

where

- t_{GCLK} is the GS clock period
 - GS is the programmed grayscale value for each outputs
- (4)

Equation 5 shows the duty cycle calculation equation.

$$\text{Duty cycle} = \frac{GS}{4096}$$
(5)

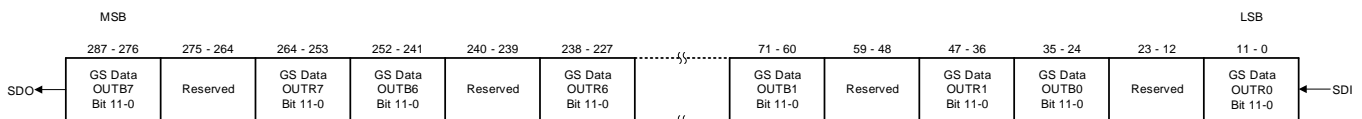


Figure 27. TLC6C5724-Q1 Grayscale Register

Once the GS data is latched into the GS registers at the rising edge of the LATCH signal, the FC-BC-DC data latch shifts into the lowest 205 bits of the common shift register. So, the FC-BC-DC data can be read out from SDO in GS write. This FC-BC-DC read function can also be realized by the read FC-BC-DC command, see FC-BC-DC Read for the timing diagram.

Table 19. Grayscale Data Bit Assignments

BITS	DATA	BITS	DATA
287–276	OUTB7	143–132	OUTB3
275–264	OUTG7	131–120	OUTG3
263–252	OUTR7	119–108	OUTR3
251–240	OUTB6	107–96	OUTB2
239–228	OUTG6	95–84	OUTG2
227–216	OUTR6	83–72	OUTR2
215–204	OUTB5	71–60	OUTB1
203–192	OUTG5	59–48	OUTG1
191–180	OUTR5	47–36	OUTR1
179–168	OUTB4	35–24	OUTB0
167–156	OUTG4	35–24	OUTG0

Table 19. Grayscale Data Bit Assignments (continued)

BITS	DATA	BITS	DATA
155–144	OUTR4	11–0	OUTR0

Table 20. GS Data vs Output On Time

GS DATA (BINARY)	GS DATA (DECIMAL)	GS DATA (HEX)	DUTY CYCLE (%)	ON-TIME BASED ON 33-MHz GS CLOCK (ns)
0000 0000 0000	0	000	0	0
0000 0000 0001	1	001	0.02	30
0000 0000 0010	2	002	0.05	61
...
0111 1111 1111	2047	7FF	49.97	62 030
1000 0000 0000	2048	800	50.00	62 061
1000 0000 0001	2049	801	50.02	62 091
...
1111 1111 1101	4093	FFD	99.93	124 030
1111 1111 1110	4094	FFE	99.95	124 061
1111 1111 1111	4095	FFF	99.98	124 091

7.5.1.3 Special Command Function

There are eight special command codes defined in the TLC6C5724-Q1 device, shown in [Table 21](#). To input the command, the level of LATCH at the last SCK before the LATCH rising edge must be high, and the highest 12 bits should be one of the listed 8 command codes. In this condition, the device ignores other bits and no data are latched into FC-BC-DC registers. Normally users can write other bits to 0 in the special command. The corresponding command function executes after the rising edge of the LATCH signal.

If no special command code is identified, the command is a NULL command and no special command is executed. The command is the same as the FC-BC-DC write function.

Table 21. Special Command Codes

COMMAND	COMMAND CODE	FUNCTION
GS read	5AFh (0101 1010 1111b)	Load GS data into common register.
SID read	5A3h (0101 1010 0011b)	Load SID data into common register.
FC-BC-DC read	5ACh (0101 1010 1100b)	Load FC-BC-DC data into common register. This reading function can also be achieved by GS data write.
APS check	53Ah (0101 0011 1010b)	Adjacent pin short detection, APS test starts at the rising edge of Latch signal, then set APS register(24bits) and APS_Flag in SID register according to the test result. Keep all channels off during this test.
LOD_LSD self-test	535h (0101 0011 0101b)	LOD-LSD detector circuit self test and set LOD_LSD_FLAG in SID register according to the test result.
Negate bit toggle	55Ah (0101 0101 1010b)	Toggle Negate Bit. When Negate Bit = 0, the 48 bits LOD-LSD detector output data will be latched into LOD1-LSD1 and LOD2-LSD2 register without invert. When Negate Bit =1, the 48 bits LOD-LSD detector output data will invert, and latch into LOD1-LSD1 and LOD2-LSD2 register.
ERROR clear	A53h (1010 0101 0011b)	Load SID data into common register, and then reset the Error status register and APS register to 0.
GLOBAL reset	A5Ch (1010 0101 1100b)	All internal registers are reset. The command has the same function as power on reset.
NULL	Different from any of the above commands	The same function as FC-BC-DC write.

7.5.1.3.1 GS Read

The GS read command loads 288-bits of GS data into the common shift register. By applying 288 SCK clocks, the GS data shifts out from the SDO pin. For details, see [Figure 3](#).

7.5.1.3.2 FC-BC-DC Read

There are two ways to read the FC-BC-DC data latch.

One way is latching data into the GS data latch. After the GS write finishes, the FC-BC-DC data latches into the lowest 205 bits of the common shift register.

Another way is using the FC-BC-DC read command. After the FC-BC-DC read command finishes, the FC-BC-DC data latches into the lowest 205 bits of the common shift register.

By applying 288 SCK clocks, the FC-BC-DC data shifts out from the SDO pin. For details, see [Figure 8](#).

7.5.1.3.3 Status Information Data Read

Status information data (SID) is 132 bits long and contains device status information and LED fault information. [Table 22](#) describes the bit mapping when SID data loads into the common shift register.

Bits 287–240 are the LED-open information for the output channels, bits 203–144 are the LED-short information for the output channels, bits 239–216 are the adjacent-pin-short information for the output channels, bits 215–206 are the error status registers, bits 205–204 are the negate bits, and other bits are reserved registers.

After power on, all error status registers are set to 0. If any one of the error-status-register flags (bits 215–206) asserts, the registers latch the faults until a reset error command is executed to clear the faults. But the LOD_LSD data continues to update every PWM cycle.

Table 22. SID Register

BITS OF COMMON SHIFT REGISTER	DESCRIPTION
287–280	LOD2 data for OUTB7–OUTB0
279–272	LOD2 data for OUTG7–OUTG0
271–264	LOD2 data for OUTF7–OUTF0
263–256	LOD1 data for OUTB7–OUTB0
255–248	LOD1 data for OUTG7–OUTG0
247–240	LOD1 data for OUTF7–OUTF0
239–232	APS data for OUTB7–OUTB0
231–224	APS data for OUTG7–OUTG0
223–216	APS data for OUTF7–OUTF0
215	Thermal error flag (TEF). 0b = Normal temperature condition, 1b = High temperature condition.
214	Pre-thermal warning (PTW). 0b = No pre-thermal warning, 1b = Pre-thermal threshold triggered.
213–211	Adjacent-pin-short check result (APS_FLAG). 011b: Pass, 110b: Fail
210	IREF resistor-short flag (ISF). 0b = IREF resistor is not shorted, 1b = IREF resistor short detected.
209	IREF resistor-open flag (IOF). 0b = IREF resistor is not open, 1b = IREF resistor open detected.
208–206	LOD-LSD detection circuit self-test result (LOD_LSD_FLAG). 011b: Pass, 110b: Fail
205	Negate bit for LOD1-LSD1 register (NEG1)
204	Negate bit for LOD2-LSD2 register (NEG2)
203–192	Reserved
191–184	LSD2 data for OUTB7–OUTB0
183–176	LSD2 data for OUTG7–OUTG0
175–168	LSD2 data for OUTF7–OUTF0
167–160	LSD1 data for OUTB7–OUTB0
159–152	LSD1 data for OUTG7–OUTG0
151–144	LSD1 data for OUTF7–OUTF0
143–0	Reserved

7.6 Register Maps

The TLC6C5724-Q1 register map includes three sections: GS registers, FC_BC_DC registers, and SID registers. Users can write to the GS registers and FC_BC_DC registers through the serial interface. Status Information can be read out through the serial interface.

7.6.1 GRAYSCALE Registers

Table 23 lists the memory-mapped registers for the GRAYSCALE. All register offset addresses not listed in Table 23 should be considered as reserved locations and the register contents should not be modified.

Grayscale Register

Table 23. GRAYSCALE Registers

Offset	Acronym	Register Name	Section
0h	OUTn_GS	Output Grayscale Register	Go

Complex bit access types are encoded to fit into small table cells. Table 24 shows the codes that are used for access types in this section.

Table 24. GRAYSCALE Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 OUTn_GS Register (Offset = 0h)

OUTn_GS is shown in Figure 28 and described in Table 25.

Return to [Summary Table](#).

OUTn Grayscale Register

Figure 28. OUTn_GS Register

287	286	285	284	283	282	281	280	279	278	277	276
OUTB7_GS											
R/W-0h											
275	274	273	272	271	270	269	268	267	266	265	264
OUTG7_GS											
R/W-0h											
263	262	261	260	259	258	257	256	255	254	253	252
OUTR7_GS											
R/W-0h											
251	250	249	248	247	246	245	244	243	242	241	240
OUTB6_GS											
R/W-0h											
239	238	237	236	235	234	233	232	231	230	229	228
OUTG6_GS											
R/W-0h											
227	226	225	224	223	222	221	220	219	218	217	216
OUTR6_GS											
R/W-0h											

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215	214	213	212	211	210	209	208	207	206	205	204
OUTB5_GS											
R/W-0h											
203	202	201	200	199	198	197	196	195	194	193	192
OUTG5_GS											
R/W-0h											
191	190	189	188	187	186	185	184	183	182	181	180
OUTR5_GS											
R/W-0h											
179	178	177	176	175	174	173	172	171	170	169	168
OUTB4_GS											
R/W-0h											
167	166	165	164	163	162	161	160	159	158	157	156
OUTG4_GS											
R/W-0h											
155	154	153	152	151	150	149	148	147	146	145	144
OUTR4_GS											
R/W-0h											
143	142	141	140	139	138	137	136	135	134	133	132
OUTB3_GS											
R/W-0h											
131	130	129	128	127	126	125	124	123	122	121	120
OUTG3_GS											
R/W-0h											
119	118	117	116	115	114	113	112	111	110	109	108
OUTR3_GS											
R/W-0h											
107	106	105	104	103	102	101	100	99	98	97	96
OUTB2_GS											
R/W-0h											
95	94	93	92	91	90	89	88	87	86	85	84
OUTG2_GS											
R/W-0h											
83	82	81	80	79	78	77	76	75	74	73	72
OUTR2_GS											
R/W-0h											
71	70	69	68	67	66	65	64	63	62	61	60
OUTB1_GS											
R/W-0h											
59	58	57	56	55	54	53	52	51	50	49	48
OUTG1_GS											
R/W-0h											
47	46	45	44	43	42	41	40	39	38	37	36
OUTR1_GS											
R/W-0h											
35	34	33	32	31	30	29	28	27	26	25	24
OUTB0_GS											
R/W-0h											
23	22	21	20	19	18	17	16	15	14	13	12
OUTG0_GS											
R/W-0h											

11	10	9	8	7	6	5	4	3	2	1	0
OUTR0_GS											
R/W-0h											

Table 25. OUTn_GS Register Field Descriptions

Bit	Field	Type	Default	Description
287–276	OUTB7_GS[11:0]	R/W	0h	Grayscale register for OUTB7
275–264	OUTG7_GS[11:0]	R/W	0h	Grayscale register for OUTG7
263–252	OUTR7_GS[11:0]	R/W	0h	Grayscale register for OUTR7
251–240	OUTB6_GS[11:0]	R/W	0h	Grayscale register for OUTB6
239–228	OUTG6_GS[11:0]	R/W	0h	Grayscale register for OUTG6
227–216	OUTR6_GS[11:0]	R/W	0h	Grayscale register for OUTR6
215–204	OUTB5_GS[11:0]	R/W	0h	Grayscale register for OUTB5
203–192	OUTG5_GS[11:0]	R/W	0h	Grayscale register for OUTG5
191–180	OUTR5_GS[11:0]	R/W	0h	Grayscale register for OUTR5
179–168	OUTB4_GS[11:0]	R/W	0h	Grayscale register for OUTB4
167–156	OUTG4_GS[11:0]	R/W	0h	Grayscale register for OUTG4
155–144	OUTR4_GS[11:0]	R/W	0h	Grayscale register for OUTR4
143–132	OUTB3_GS[11:0]	R/W	0h	Grayscale register for OUTB3
131–120	OUTG3_GS[11:0]	R/W	0h	Grayscale register for OUTG3
119–108	OUTR3_GS[11:0]	R/W	0h	Grayscale register for OUTR3
107–96	OUTB2_GS[11:0]	R/W	0h	Grayscale register for OUTB2
95–84	OUTG2_GS[11:0]	R/W	0h	Grayscale register for OUTG2
83–72	OUTR2_GS[11:0]	R/W	0h	Grayscale register for OUTR2
71–60	OUTB1_GS[11:0]	R/W	0h	Grayscale register for OUTB1
59–48	OUTG1_GS[11:0]	R/W	0h	Grayscale register for OUTG1
47–36	OUTR1_GS[11:0]	R/W	0h	Grayscale register for OUTR1
35–24	OUTB0_GS[11:0]	R/W	0h	Grayscale register for OUTB0
23–12	OUTG0_GS[11:0]	R/W	0h	Grayscale register for OUTG0
11–0	OUTR0_GS[11:0]	R/W	0h	Grayscale register for OUTR0

7.6.2 FC-BC-DC Registers

Table 26 lists the memory-mapped registers for the FC-BC-DC. All register offset addresses not listed in Table 26 should be considered as reserved locations and the register contents should not be modified.

FC-BC-DC Register

Table 26. FC-BC-DC Registers

Offset	Acronym	Register Name	Section
1h	FC-BC-DC	FC-BC-DC Register	Go

Complex bit access types are encoded to fit into small table cells. Table 27 shows the codes that are used for access types in this section.

Table 27. FC-BC-DC Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.6.2.1 FC-BC-DC Register (Offset = 1h)

FC-BC-DC is shown in [Figure 29](#) and described in [Table 28](#).

Return to [Summary Table](#).

FC-BC-DC Register

Figure 29. FC-BC-DC Register

287	286	285	284	283	282	281	280	279	278	277	276	275	274	273	272	
CMD											RESERVED					
R/W-0h											R/W-0h					
271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256	
RESERVED																
R/W-0h																
255	254	253	252	251	250	249	248	247	246	245	244	243	242	241	240	
RESERVED																
R/W-0h																
239	238	237	236	235	234	233	232	231	230	229	228	227	226	225	224	
RESERVED																
R/W-0h																
223	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208	
RESERVED																
R/W-0h																
207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192	
RESERVED			LED_ERR_MASK	SLEW_RATE	LOD_VOLTAGE	LSD_VOLTAGE	APSCURRENT	APSTIME	GS_MODE			TIMING_RESET	AUTO_REPEAT	DC_RANGE_B	DC_RANGE_G	DC_RANGE_R
R/W-0h			R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h			R/W-0h	R/W-0h	R/W-0h	R/W-0h	
191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	
OUTB_BC								OUTG_BC								
R/W-0h																
175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160	
OUTR_BC								OUTB7_DC							→	
R/W-0h								R/W-0h							→	
159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144	
← OUTG7_DC						OUTR7_DC						OUTB6_DC				
← R/W-0h						R/W-0h						R/W-0h				
143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128	
OUTB6_DC				OUTG6_DC								OUTR6_DC				
R/W-0h				R/W-0h								R/W-0h				
127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	
OUTR6_DC		OUTB5_DC								OUTG5_DC						

R/W-0h			R/W-0h						R/W-0h							
111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96	
OUTR5_DC							OUTB4_DC						OUTG4_DC			
R/W-0h						R/W-0h						R/W-0h				
95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	
OUTG4_DC				OUTR4_DC						OUTB3_DC						
R/W-0h					R/W-0h						R/W-0h					
79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	
OUTB3_DC			OUTG3_DC						OUTR3_DC						→	
R/W-0h					R/W-0h						R/W-0h					→
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	
←	OUTB2_DC						OUTG2_DC						→			
←	R/W-0h						R/W-0h						→			
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	
←	OUTR2_DC					OUTB1_DC						OUTG1_DC				
←	R/W-0h					R/W-0h						R/W-0h				
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
OUTG1_DC				OUTR1_DC						OUTB0_DC						
R/W-0h					R/W-0h						R/W-0h					
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OUTB0_DC			OUTG0_DC						OUTR0_DC							
R/W-0h					R/W-0h						R/W-0h					

Table 28. FC-BC-DC Register Field Descriptions

Bit	Field	Type	Default	Description
287–276	CMD[11:0]	R/W	0h	Command function 25Ch = Global reset 535h = LOD_LSD self-test 53Ah = APS check 55Ah = NEG-BIT toggle 5A3h = SID read 5ACh = FC_BC_DC read 5AFh = GS read A53h = ERROR clear
275–205	RESERVED	R/W	0h	Reserved
204	LED_ERR_MASK	R/W	1h	LED error mask 0h = Unmask LED error 1h = Mask LED error
203	SLEW_RATE	R/W	0h	Output slew-rate time 0h = 100 ns 1h = 200 ns
202	LOD_VOLTAGE	R/W	0h	LED open-detection voltage 0h = 0.3 V 1h = 0.5 V
201	LSD_VOLTAGE	R/W	0h	LED short-detection voltage 0h = VSENSE - 0.3 V 1h = VSENSE - 0.7 V
200	APS_CURRENT	R/W	0h	Adjacent-pin short-detection sink current 0h = 20 µA 1h = 40 µA

Table 28. FC-BC-DC Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
199	APS_TIME	R/W	0h	Adjacent-pin short-detection time 0h = 10 μ s 1h = 20 μ s
198–197	GS_MODE[1:0]	R/W	0h	Grayscale counter mode 0h or 1h = 12-bit counter mode 2h = 10-bit counter mode 3h = 8-bit counter mode
196	TIMING_RESET	R/W	0h	Display timing reset 0h = Disabled 1h = Enabled
195	AUTO_REPEAT	R/W	0h	Auto repeat 0h = Disabled 1h = Enabled
194	DC_RANGE_B	R/W	0h	Dot correction range for OUTB group 0h = Low range 1h = High range
193	DC_RANGE_G	R/W	0h	Dot correction range for OUTG group 0h = Low range 1h = High range
192	DC_RANGE_R	R/W	0h	Dot correction range for OUTR group 0h = Low range 1h = High range
191–184	OUTB_BC[7:0]	R/W	0h	Brightness control for OUTB group
183–176	OUTG_BC[7:0]	R/W	0h	Brightness control for OUTG group
175–168	OUTR_BC[7:0]	R/W	0h	Brightness control for OUTR group
167–161	OUTB7_DC[6:0]	R/W	0h	Dot correction for OUTB7
160–154	OUTG7_DC[6:0]	R/W	0h	Dot correction for OUTG7
153–147	OUTR7_DC[6:0]	R/W	0h	Dot correction for OUTR7
146–140	OUTB6_DC[6:0]	R/W	0h	Dot correction for OUTB6
139–133	OUTG6_DC[6:0]	R/W	0h	Dot correction for OUTG6
132–126	OUTR6_DC[6:0]	R/W	0h	Dot correction for OUTR6
125–119	OUTB5_DC[6:0]	R/W	0h	Dot correction for OUTG5
118–112	OUTG5_DC[6:0]	R/W	0h	Dot correction for OUTB5
111–105	OUTR5_DC[6:0]	R/W	0h	Dot correction for OUTR5
104–98	OUTB4_DC[6:0]	R/W	0h	Dot correction for OUTB4
97–91	OUTG4_DC[6:0]	R/W	0h	Dot correction for OUTG4
90–84	OUTR4_DC[6:0]	R/W	0h	Dot correction for OUTR4
83–77	OUTB3_DC[6:0]	R/W	0h	Dot correction for OUTB3
76–70	OUTG3_DC[6:0]	R/W	0h	Dot correction for OUTG3
69–63	OUTR3_DC[6:0]	R/W	0h	Dot correction for OUTR3
62–56	OUTB2_DC[6:0]	R/W	0h	Dot correction for OUTB2
55–49	OUTG2_DC[6:0]	R/W	0h	Dot correction for OUTG2

Table 28. FC-BC-DC Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
48–42	OUTR2_DC[6:0]	R/W	0h	Dot correction for OUTR2
41–35	OUTB1_DC[6:0]	R/W	0h	Dot correction for OUTB1
34–28	OUTG1_DC[6:0]	R/W	0h	Dot correction for OUTG1
27–21	OUTR1_DC[6:0]	R/W	0h	Dot correction for OUTR1
20–14	OUTB0_DC[6:0]	R/W	0h	Dot correction for OUTB0
13–7	OUTG0_DC[6:0]	R/W	0h	Dot correction for OUTG0
6–0	OUTR0_DC[6:0]	R/W	0h	Dot correction for OUTR0

7.6.3 SID Registers

Table 29 lists the memory-mapped registers for the SID. All register offset addresses not listed in Table 29 should be considered as reserved locations and the register contents should not be modified.

SID Register

Table 29. SID Registers

Offset	Acronym	Register Name	Section
2h	SID	SID Register	Go

Complex bit access types are encoded to fit into small table cells. Table 30 shows the codes that are used for access types in this section.

Table 30. SID Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.6.3.1 SID Register (Offset = 2h)

SID is shown in Figure 30 and described in Table 31.

Return to [Summary Table](#).

Status information data

Figure 30. SID Register

287	286	285	284	283	282	281	280	279	278	277	276	275	274	273	272
OUTB_LOD2								OUTG_LOD2							
R-0h								R-0h							
271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256
OUTR_LOD2								OUTB_LOD1							
R-0h								R-0h							
255	254	253	252	251	250	249	248	247	246	245	244	243	242	241	240
OUTG_LOD1								OUTR_LOD1							
R-0h								R-0h							
239	238	237	236	235	234	233	232	231	230	229	228	227	226	225	224
OUTB_APS								OUTG_APS							
R-0h								R-0h							
223	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208

OUTR_APS								TEF	PTW	APS_FLAG			ISF	IOF	→
R-0h								R-0h	R-0h	R-0h			R-0h	R-0h	→
207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192
←	LOD_LSD_FLAG	NEG1	NEG0	RESERVED											
←	R-0h	R-0h	R-0h	R-0h											
191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176
OUTB_LSD2								OUTG_LSD2							
R-0h								R-0h							
175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160
OUTR_LSD2								OUTB_LSD1							
R-0h								R-0h							
159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144
OUTG_LSD1								OUTR_LSD1							
R-0h								R-0h							
143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
RESERVED															
R-0h															
127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
RESERVED															
R-0h															
111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
RESERVED															
R-0h															
95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
RESERVED															
R-0h															
79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
RESERVED															
R-0h															
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
RESERVED															
R-0h															
47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
RESERVED															
R-0h															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED															
R-0h															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED															
R-0h															

Table 31. SID Register Field Descriptions

Bit	Field	Type	Default	Description
287–280	OUTB_LOD2[7:0]	R	0h	LOD2 for OUTB7–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
279–272	OUTG_LOD2[7:0]	R	0h	LOD2 for OUTG7–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected

Table 31. SID Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
271–264	OUTR_LOD2[7:0]	R	0h	LOD2 for OUTR7–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
263–256	OUTB_LOD1[7:0]	R	0h	LOD1 for OUTB7–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
255–248	OUTG_LOD1[7:0]	R	0h	LOD1 for OUTG7–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
247–240	OUTR_LOD1[7:0]	R	0h	LOD1 for OUTR7–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
239–232	OUTB_APS[7:0]	R	0h	APS status for OUTB7–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
231–224	OUTG_APS[7:0]	R	0h	APS status for OUTG7–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
223–216	OUTR_APS[7:0]	R	0h	APS status for OUTR7–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
215	TEF	R	0h	Thermal error flag 0h = No fault detected 1h = Fault detected
214	PTW	R	0h	Pre-thermal warning flag 0h = No fault detected 1h = Fault detected
213–211	APS_FLAG[2:0]	R	0h	APS test flag fault 3h = APS test passes 6h = APS test fails
210	ISF	R	0h	ISF fault 0h = No fault detected 1h = Fault detected
209	IOF	R	0h	IOF fault 0h = No fault detected 1h = Fault detected
208–206	LOD_LSD_FLAG[2:0]	R	0h	LOD_LSD self-test flag 3h = LOD_LSD self test passes 6h = LOD_LSD self-test fails
205	NEG1	R	0h	Neg1 bit value
204	NEG0	R	0h	Neg0 bit value
203–92	RESERVED	R	0h	RESERVED
191–184	OUTB_LSD2[7:0]	R	0h	LSD2 for OUTB7–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected

Table 31. SID Register Field Descriptions (continued)

Bit	Field	Type	Default	Description
183–176	OUTG_LSD2[7:0]	R	0h	LSD2 for OUTG7–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
175–168	OUTR_LSD2[7:0]	R	0h	LSD2 for OUTR7–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
167–60	OUTB_LSD1[7:0]	R	0h	LSD1 for OUTB7–OUTB0. For each channel: 0h = No fault detected 1h = Fault detected
159–52	OUTG_LSD1[7:0]	R	0h	LSD1 for OUTG7–OUTG0. For each channel: 0h = No fault detected 1h = Fault detected
151–144	OUTR_LSD1[7:0]	R	0h	LSD1 for OUTR7–OUTR0. For each channel: 0h = No fault detected 1h = Fault detected
143–0	RESERVED	R	0h	RESERVED

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Below is a typical application for an automotive local dimming application.

8.2 Typical Application

In automotive LCD display applications such as a solid-state cluster or center information display, LED backlighting is one of the key parts for the display. Today most LED backlighting is the traditional edge-lit type, which means the backlighting is globally dimmed. This method consumes much power and causes light leakage from the liquid crystals in the black areas, as the backlighting is always turned on. Recently, local-dimming backlighting, a direct-lit type of backlighting, has been proposed to overcome this drawback. The lighting level of the backlighting follows the display contents. The lighting level is dynamically adjusted by the content of the image blocks for local-dimming control. When an image block is bright, the lighting level of the backlighting turns high also. Conversely, the backlighting level is adjusted to low in a black region. This arrangement reduces power dissipation and light leakage from the LCD and creates pure black, increasing the image contrast ratio.

Users can use the TLC6C5724-Q1 device to drive LED backlighting in local dimming applications. Depending how many zones are in the display, users can connect different numbers of TLC6C5724-Q1 devices in a daisy chain to drive the LEDs.

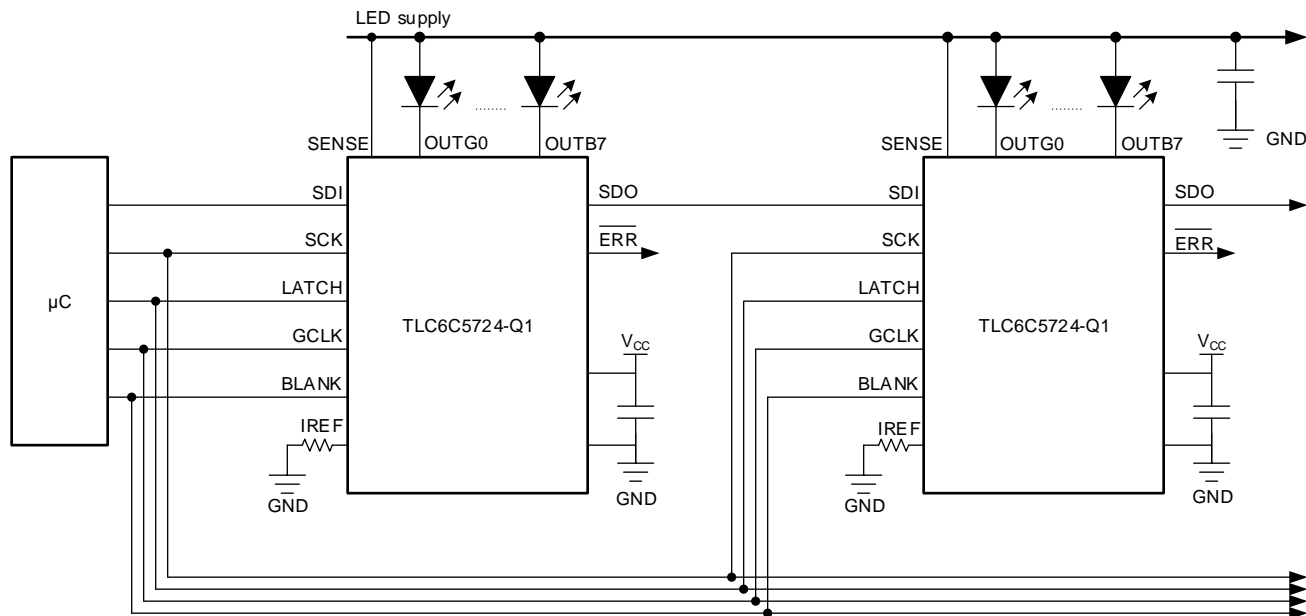


Figure 31. Typical Block Diagram for Local Dimming

Typical Application (continued)

8.2.1 Design Requirements

Table 32 shows the design requirements for the local dimming application.

Table 32. Design Requirements

PARAMETER	VALUE
LCD size	12.3 inches
Zones	128
Number of LEDs per string	1
LED current	50 mA

8.2.2 Detailed Design Procedure

As the backlighting includes 128 zones, each TLC6C5724-Q1 device can drive 24 zones, so a total of six TLC6C5724-Q1 units are needed.

According to [Maximum Constant-Sink-Current Setting](#), to realize a 50-mA output current, users can choose a 0.96-kΩ reference resistor.

Users can use a daisy chain connection to control all of the six TLC6C5724-Q1 devices through one serial interface, just as [Figure 31](#) shows. [Figure 32](#) shows how to send the data into cascaded devices, where M is the number of cascading devices.

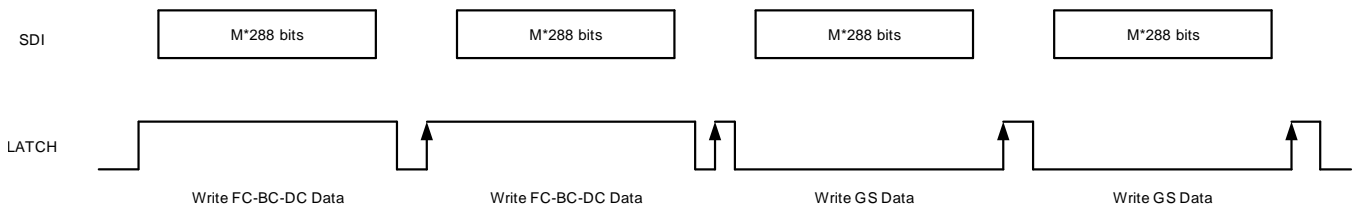


Figure 32. Cascading Data Write

8.2.3 Application Curves

Below are two test waveforms. [Figure 33](#) shows different PWM duty cycles for different output channels, which can realize a local dimming feature. [Figure 34](#) shows a data-write waveform typical for each write of M × 288 bits of data into the serial interface.

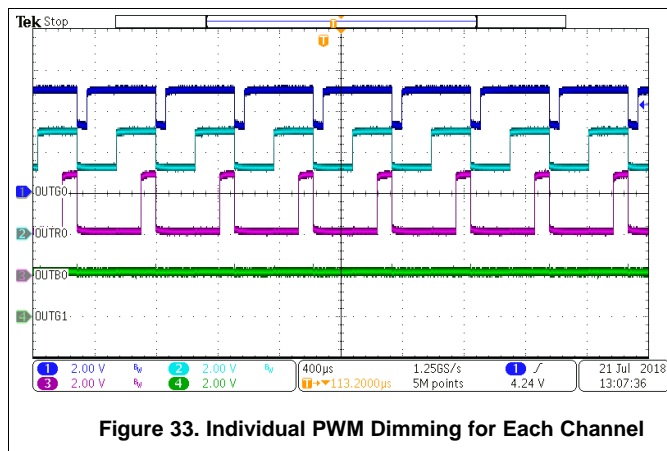


Figure 33. Individual PWM Dimming for Each Channel

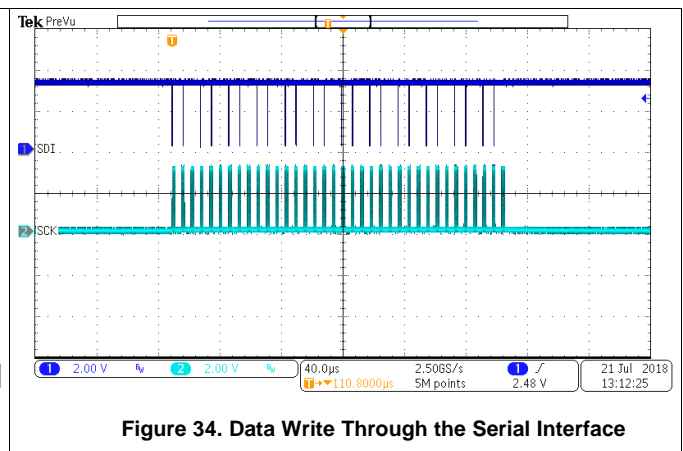


Figure 34. Data Write Through the Serial Interface

9 Power Supply Recommendations

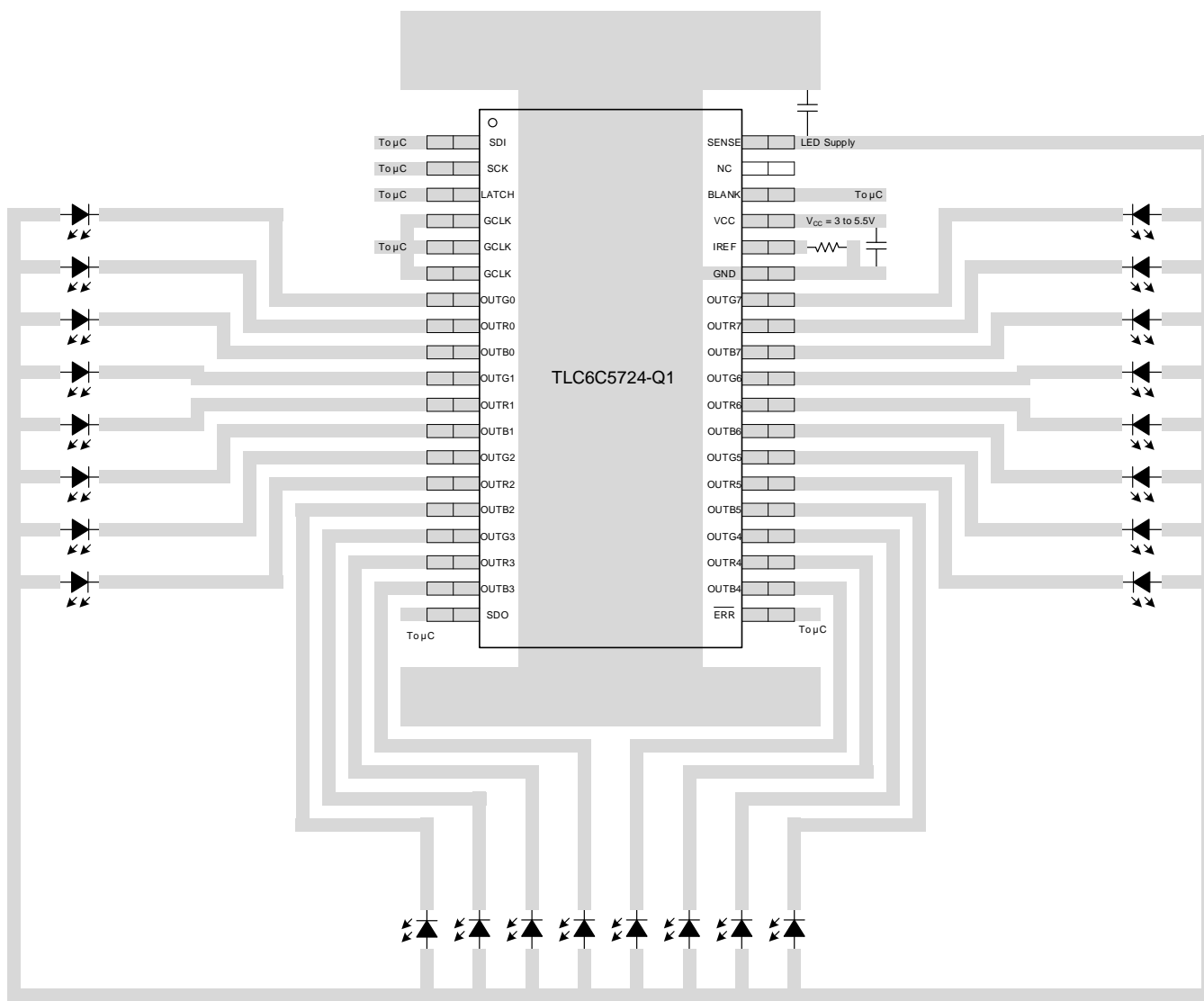
The TLC6C5724-Q1 device requires two power supplies. One is V_{CC} , which can range from 3 V to 5.5 V. The other is V_{LED} , which can go up to 8 V. Users must add a capacitor on the V_{CC} power supply to filter noise. Place the capacitor as close to the V_{CC} pin and SENSE pin as possible.

10 Layout

10.1 Layout Guidelines

Figure 35 shows a layout example for the TLC6C5724-Q1 device. To improve the thermal performance, TI recommends to use the GND plane to dissipate the heat. To filter the supply noise, users can put the capacitor as close to the V_{CC} and SENSE pins as possible. The IREF resistor also should be be connected as close to IREF pin as possible.

10.2 Layout Example



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Figure 35. TLC6C5724-Q1 Example Layout Diagram

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish ⁽³⁾	MSL Peak Temp ⁽⁴⁾	Op Temp (°C)	Device Marking ⁽⁵⁾⁽⁶⁾
TLC6C5724QDAPRQ1	ACTIVE	HTSSOP	DAP	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C5724Q

- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.
- (4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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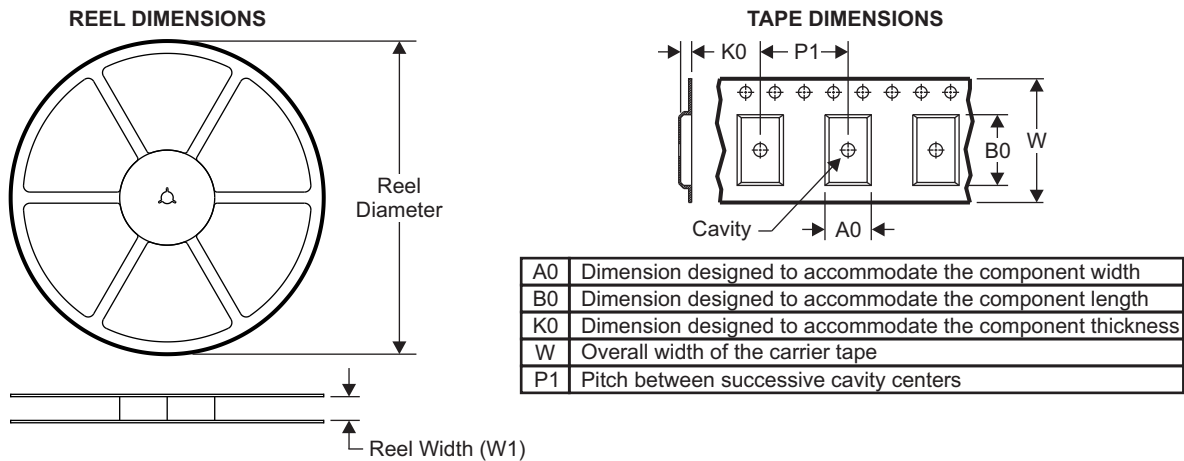
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TLC6C5724-Q1

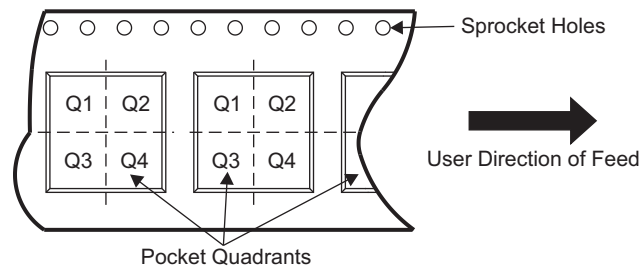
SLASEK2A – DECEMBER 2017 – REVISED AUGUST 2018

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12.1.2 Tape and Reel Information

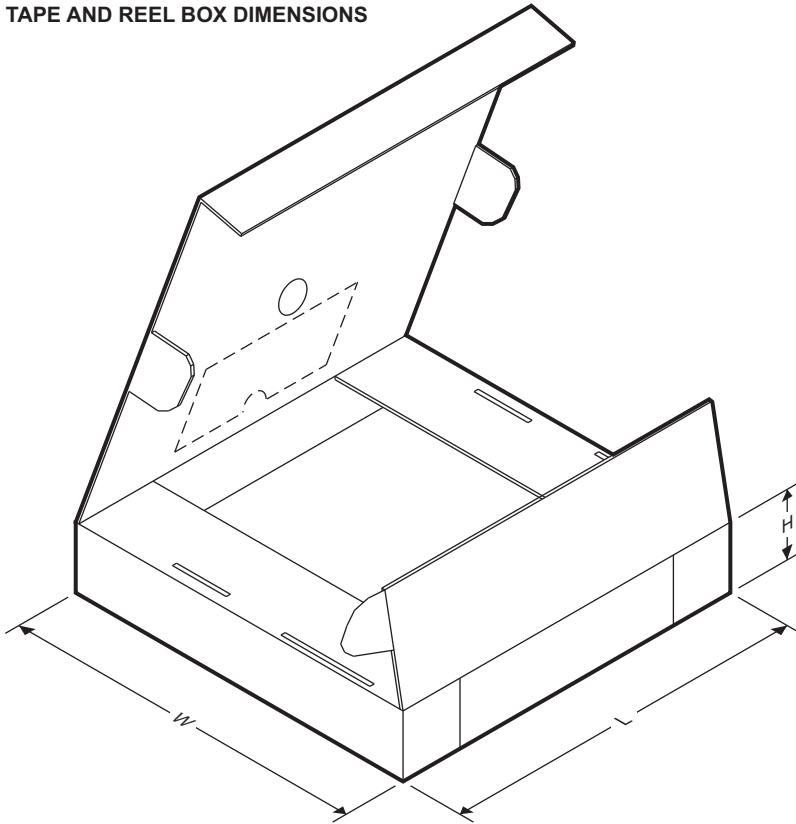


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6C5724QDAPRQ1	HTSSOP	DAP	38	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C5724QDAPRQ1	HTSSOP	DAP	38	2000	350.0	350.0	43.0

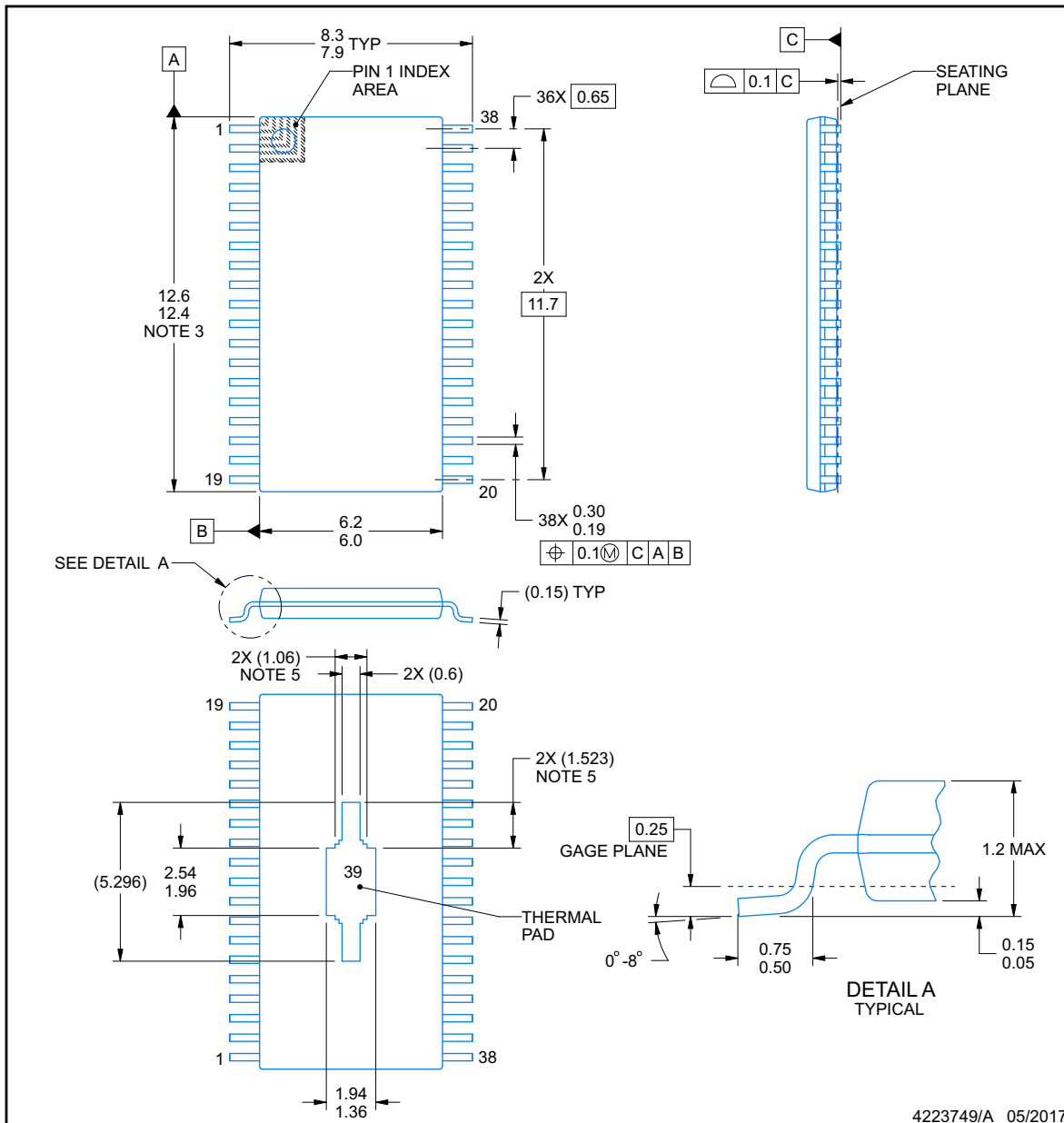
PACKAGE OUTLINE

DAP0038E



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223749/A 05/2017

NOTES:

PowerPAD is a trademark of Texas Instruments.

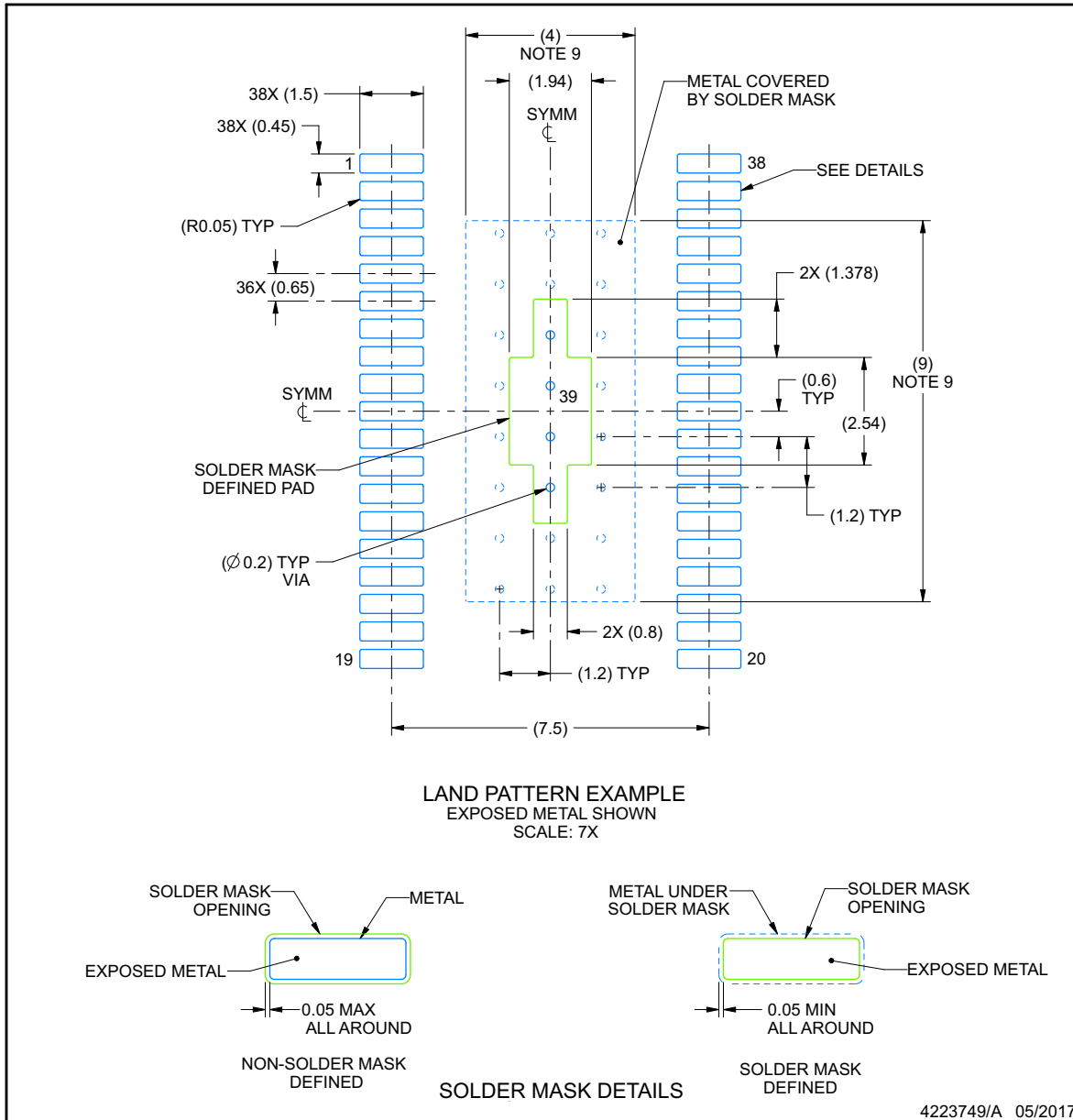
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

DAP0038E

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

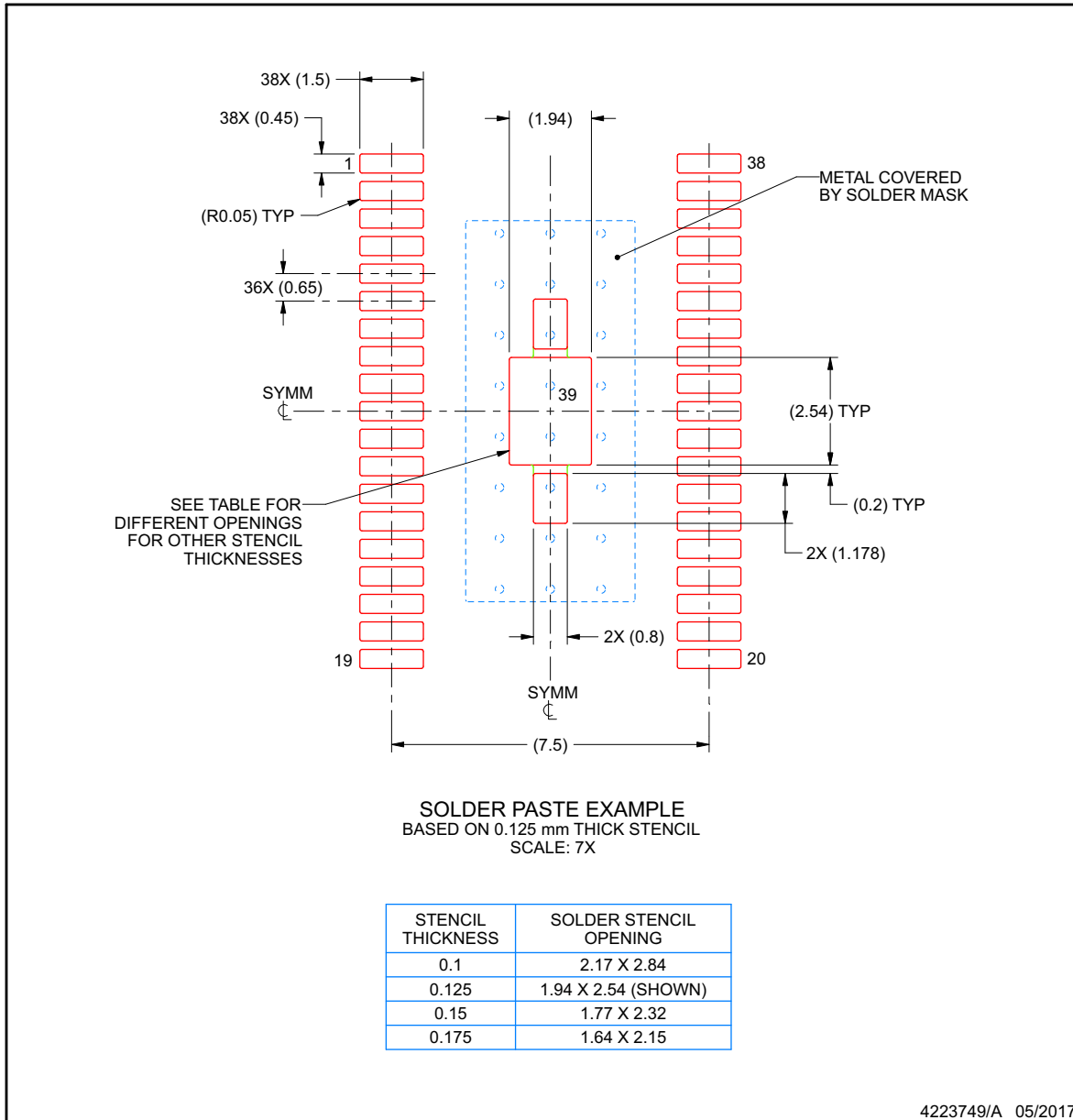
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DAP0038E

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

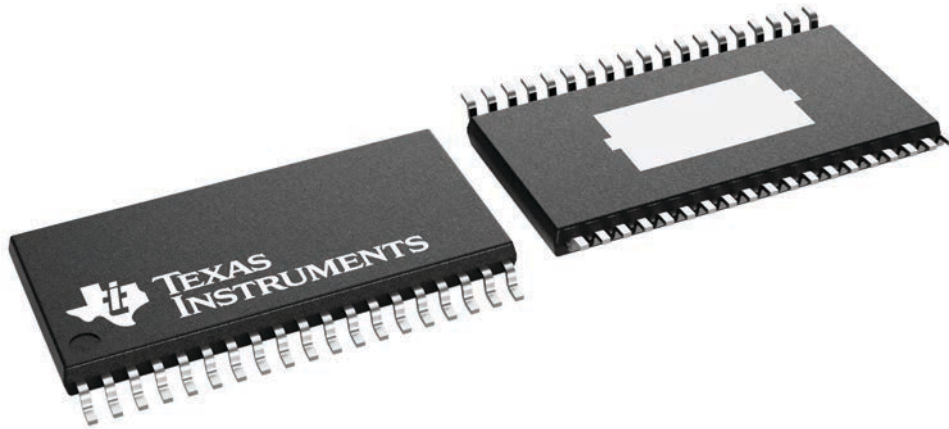
DAP 38

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 12.5, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231599/A

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