TLVx171-Q1 36-V, Single-Supply, General-Purpose Operational Amplifier for Cost-Sensitive Automotive Systems

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level:
    - Level 3A for TLV171-Q1 and TLV2171-Q1
    - Level 2 for TLV4171-Q1
  - Device CDM ESD Classification Level
    - Level C4A for TLV171-Q1
    - Level C6 for TLV2171-Q1and TLV4171-Q1
- Supply Range:
  - Single-Supply: 4.5 V to 36 V
  - Dual-Supply ±2.25 V to ±18 V
- Low Noise: 16 nV/√Hz at 1 kHz
- Low Offset Drift: ±1 µV/°C (Typical)
- Input Range Includes Negative Supply
- Input Range Operates to Positive Supply With Reduced Performance
- Rail-to-Rail Output
- Gain Bandwidth: 3 MHz
- Low Quiescent Current: 525 µA per Amplifier
- Common-Mode Rejection: 120 dB (Typical)
- Low Input Bias Current: 10 pA

2 Applications

- Automotive
  - ADAS
  - Body Electronics
  - Lighting
  - Current Sensing
  - Power Train

3 Description

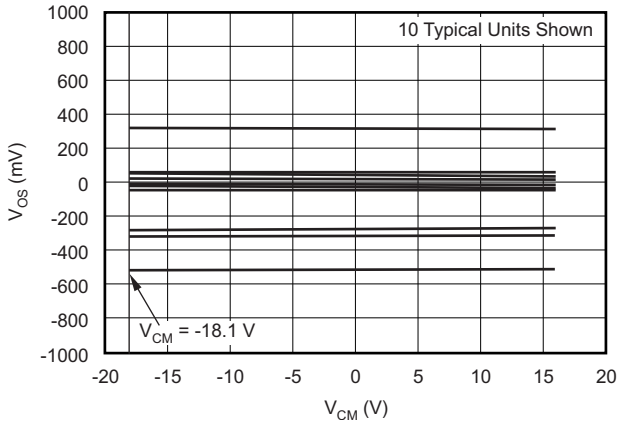
The TLVx171-Q1 family of devices is a 36-V, single-supply, low-noise operational amplifier (op amp) with the ability to operate on supplies ranging from 4.5 V (± 2.25 V) to 36 V (±18 V). This series is available in multiple packages and offers low offset, drift, and low quiescent current. The single, dual, and quad versions all have identical specifications for maximum design flexibility.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV171-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
TLV2171-Q1	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
TLV4171-Q1	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Offset Voltage vs Common-Mode Voltage: V_{SUPPLY} = ±18 V



Offset Voltage vs Power Supply

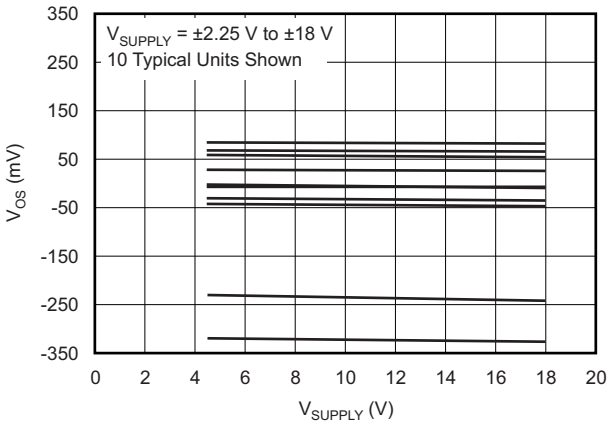


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Table 1. Revision History

DATE	REVISION	NOTES
April 2017	SBOS858	Initial release.

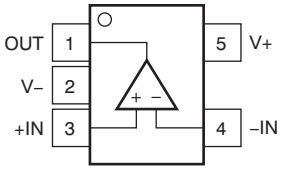
4 Description (continued)

Unlike most op amps, which are specified at only one supply voltage, the TLVx171-Q1 family of devices is specified from 4.5 V to 36 V. Input signals beyond the supply rails do not cause phase reversal. The TLVx171-Q1 family of devices is stable with capacitive loads up to 300 pF. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. The device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The TLVx171-Q1 op amp family is specified from –40°C to +125°C.

5 Pin Configuration and Functions

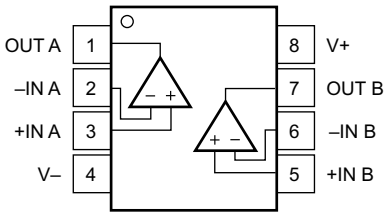
TLV171-Q1 DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN	3	I	Noninverting input
–IN	4	I	Inverting input
OUT	1	O	Output
V+	5	—	Positive (highest) power supply
V–	2	—	Negative (lowest) power supply

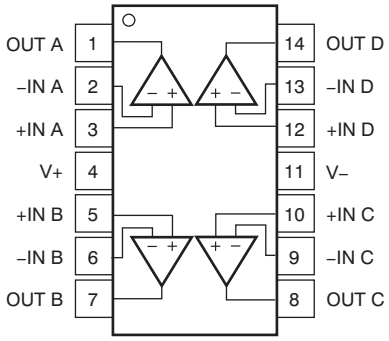
TLV2171-Q1 D or DGK Packages
8-Pin SOIC or VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

TLV4171-Q1 D and PW Packages
14-Pin SOIC and TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_S			40	V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current		±10	mA
Output short circuit(2)		Continuous		
Junction temperature, T_J			150	°C
Latch-up per JESD78D		Class 1		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
TLV171-Q1 IN DBV PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011	±500	
TLV2171-Q1 IN D AND DGK PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011	±1000	
TLV4171-Q1 IN D AND PW PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified operating temperature	–40		125	°C

6.4 Thermal Information: TLV171-Q1

THERMAL METRIC(1)		TLV171-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	277.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	193.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	121.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	109.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Thermal Information: TLV2171-Q1

THERMAL METRIC(1)		TLV2171-Q1 D (SOIC) 8 PINS	TLV2171-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	186.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	78	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	107.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	15.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	106.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Thermal Information: TLV4171-Q1

THERMAL METRIC(1)		TLV4171-Q1 D (SOIC) 14 PINS	TLV4171-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

at T_A = 25°C, V_S = 4.5 V to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			0.75	±2.7	mV
	Input offset voltage over temperature	T_A = –40°C to 125°C			±3	mV
dV_{OS}/dT	Input offset voltage drift (over temperature)	T_A = –40°C to 125°C		1		µV/°C
PSRR	Input offset voltage over temperature vs power supply	V_S = 4.5 V to 36 V	90	120		dB

Electrical Characteristics (continued)

at T_A = 25°C, V_S = 4.5 V to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT						
I_B	Input bias current			±10		pA
I_{OS}	Input offset current			±4		pA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		3		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		27		$nV/\sqrt{Hz}$
		f = 1 kHz		16		$nV/\sqrt{Hz}$
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range(1)		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio (over temperature)	V_S = ±2.25 V (V–) – 0.1 V < V_{CM} < (V+) – 2 V	90	120		dB
		V_S = ±18 V (V–) – 0.1 V < V_{CM} < (V+) – 2 V	94	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain (over temperature)	V_S = 4.5 V to 36 V (V–) + 0.35 V < V_O < (V+) – 0.35 V	94	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			3		MHz
SR	Slew rate	G = 1		1.5		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V G = 1, 10-V step		6		µs
		To 0.01% (12 bit), V_S = ±18 V G = 1, 10-V step		10		µs
	Overload recovery time	$V_{±IN}$ × Gain > V_S		2		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz V_O = 3 V_{RMS}		0.0002%		
OUTPUT						
V_O	Voltage output swing from rail (over temperature)	R_L = 10 kΩ A_{OL} ≥ 110 dB	(V–) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current	Sourcing		25		mA
		Sinking		–37		
C_{LOAD}	Capacitive load drive		See *Typical Characteristics*			pF
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 A		150		Ω
POWER SUPPLY						
V_S	Specified voltage range	T_A = –40°C to 125°C	4.5		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A, T_A = –40°C to 125°C		525	695	µA

(1) The input range can be extended beyond (V+) – 2 V up to V+ at reduced performance. See *Typical Characteristics* and *Detailed Description* for additional information.

6.8 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

Table 2. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage vs Common-Mode Voltage	Figure 2
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 3
Input Bias Current vs Temperature	Figure 5
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 6
CMRR and PSRR vs Frequency (Referred-to Input)	Figure 7
0.1Hz to 10Hz Noise	Figure 8
Input Voltage Noise Spectral Density vs Frequency	Figure 9
Quiescent Current vs Supply Voltage	Figure 10
Open-Loop Gain and Phase vs Frequency	Figure 11
Closed-Loop Gain vs Frequency	Figure 12
Open-Loop Gain vs Temperature	Figure 13
Open-Loop Output Impedance vs Frequency	Figure 14
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 15,
No Phase Reversal	Figure 17
Small-Signal Step Response (100 mV)	Figure 18, Figure 19
Large-Signal Step Response	Figure 20, Figure 21
Large-Signal Settling Time (10-V Positive Step)	Figure 22
Large-Signal Settling Time (10-V Negative Step)	Figure 23
Short-Circuit Current vs Temperature	Figure 24
Maximum Output Voltage vs Frequency	Figure 25

6.8.1 Typical Characteristics

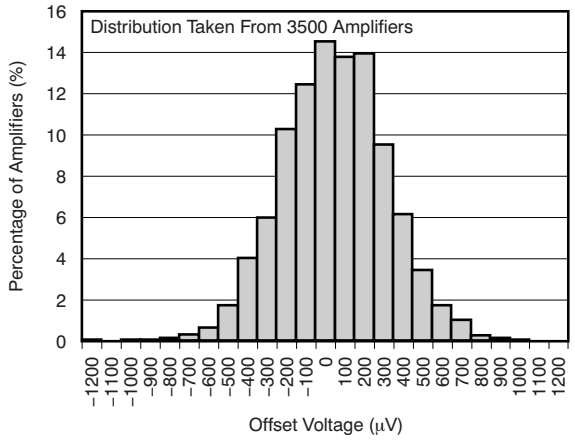


Figure 1. Offset Voltage Production Distribution

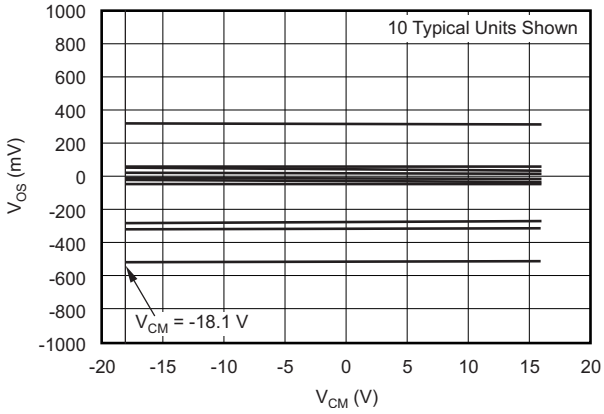


Figure 2. Offset Voltage vs Common-Mode Voltage: V_{SUPPLY} (V) = ±18 V

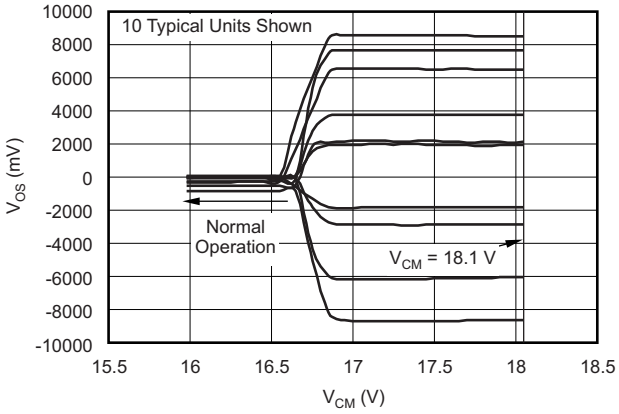


Figure 3. Offset Voltage vs Common-Mode Voltage: V_{SUPPLY} (V) = ±18 V (Upper Stage)

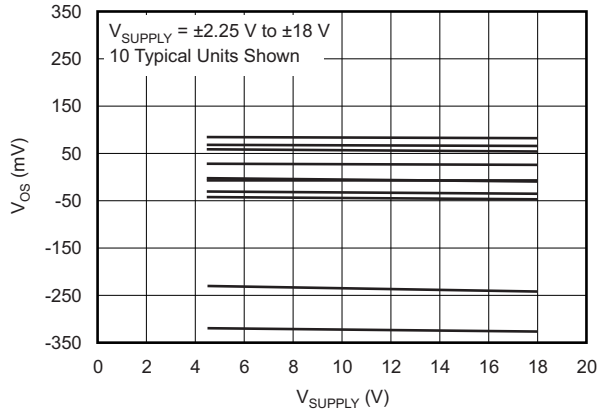


Figure 4. Offset Voltage vs Power Supply

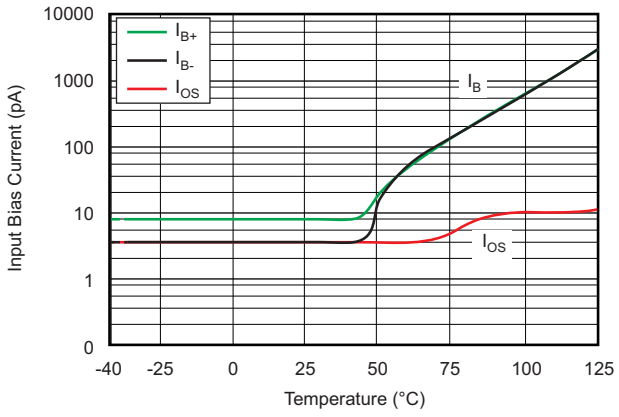


Figure 5. Input Bias Current vs Temperature

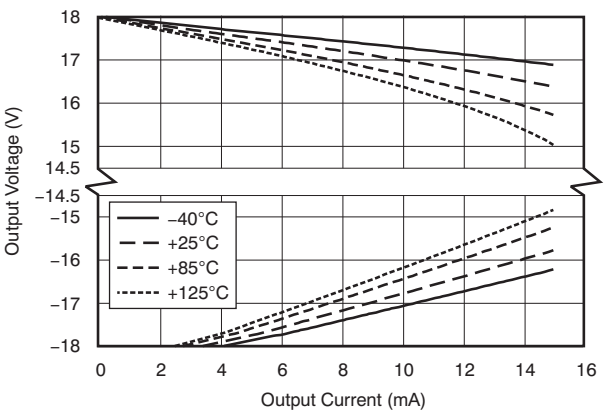


Figure 6. Output Voltage Swing vs Output Current (Maximum Supply)

Typical Characteristics (continued)

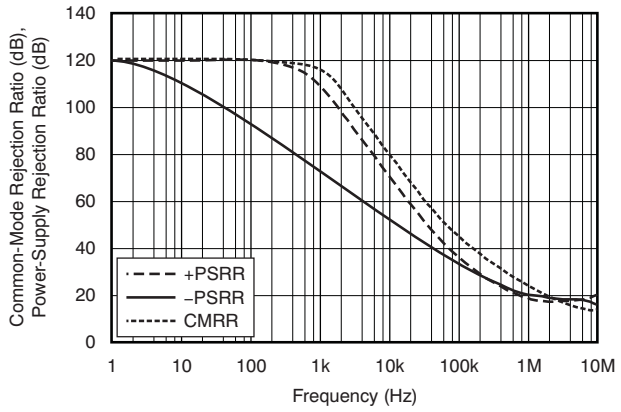


Figure 7. CMRR and PSRR vs Frequency (Referred-to Input)

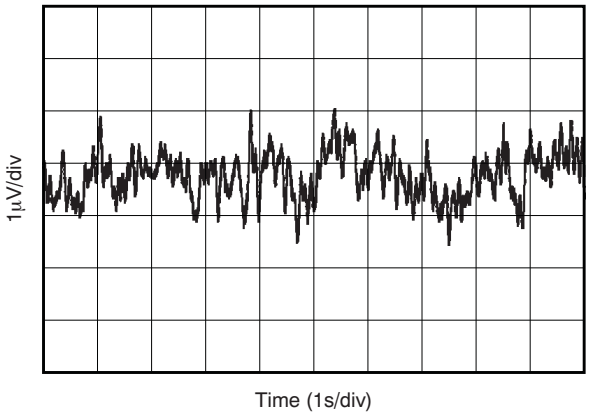


Figure 8. 0.1- to 10-Hz Noise

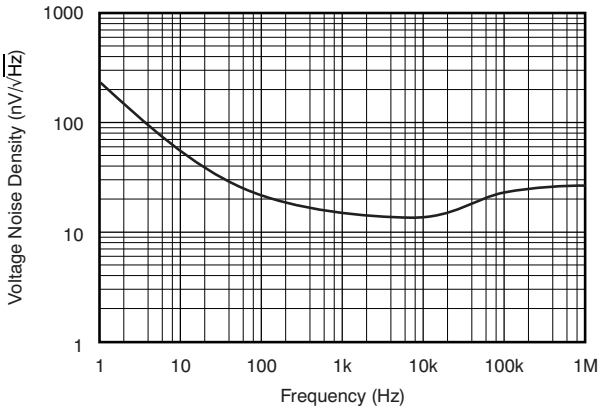


Figure 9. Input Voltage Noise Spectral Density vs Frequency

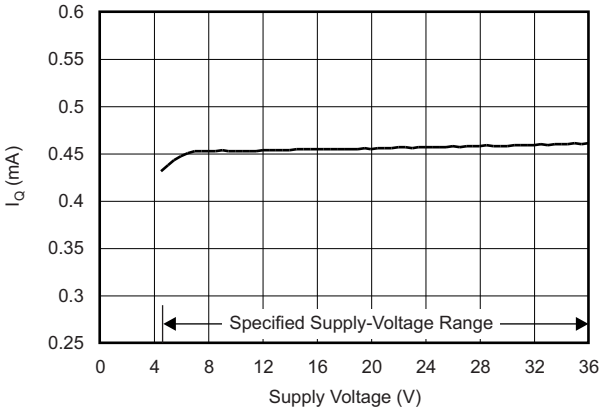


Figure 10. Quiescent Current vs Supply Voltage

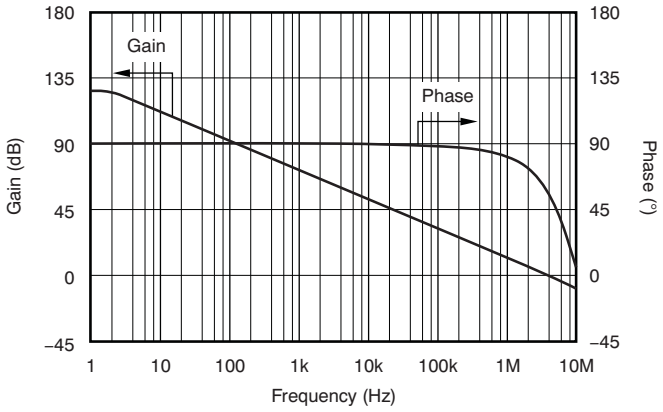


Figure 11. Open-Loop Gain and Phase vs Frequency

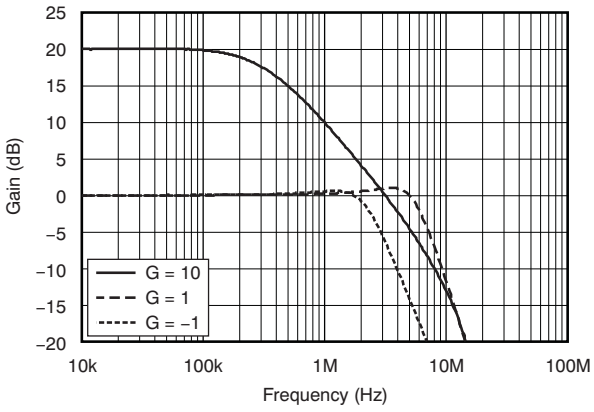


Figure 12. Closed-Loop Gain vs Frequency

Typical Characteristics (continued)

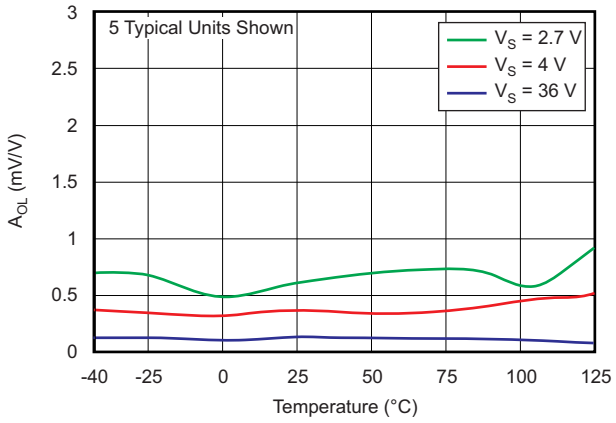


Figure 13. Open-Loop Gain vs Temperature

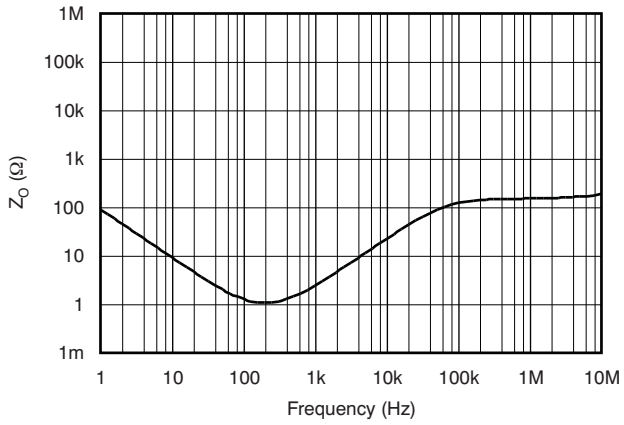
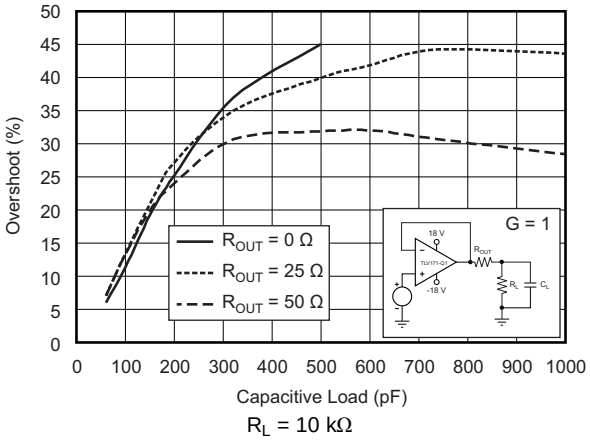


Figure 14. Open-Loop Output Impedance vs Frequency



R_L = 10 kΩ

Figure 15. Noninverting Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

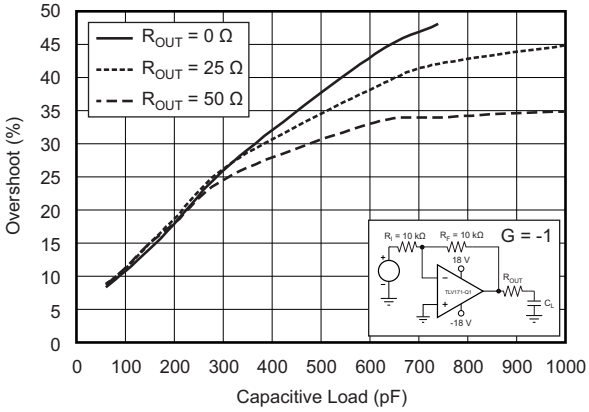


Figure 16. Inverting Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

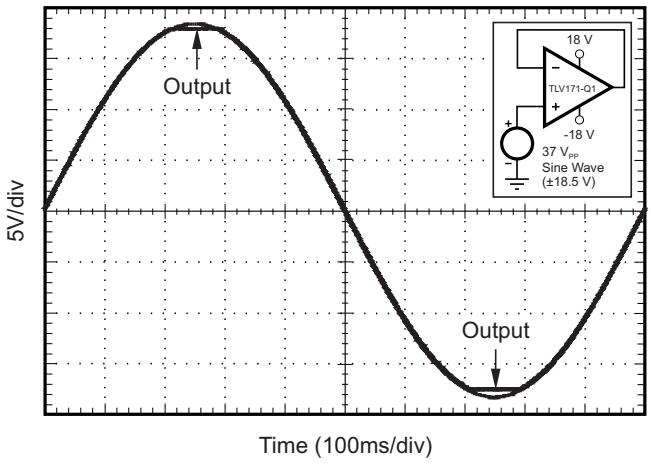
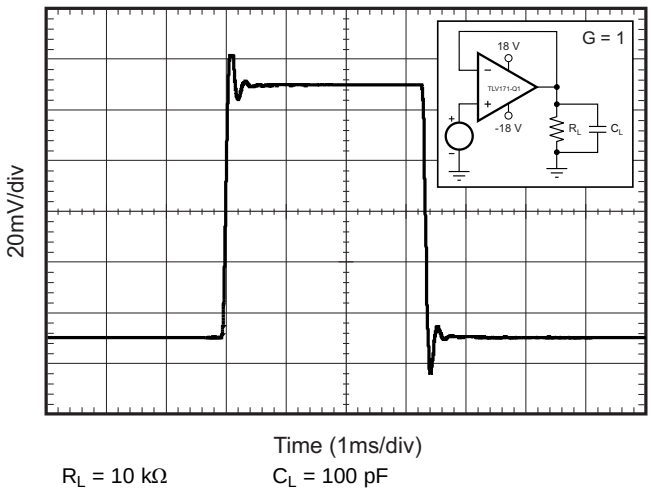


Figure 17. No Phase Reversal



R_L = 10 kΩ C_L = 100 pF

Figure 18. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

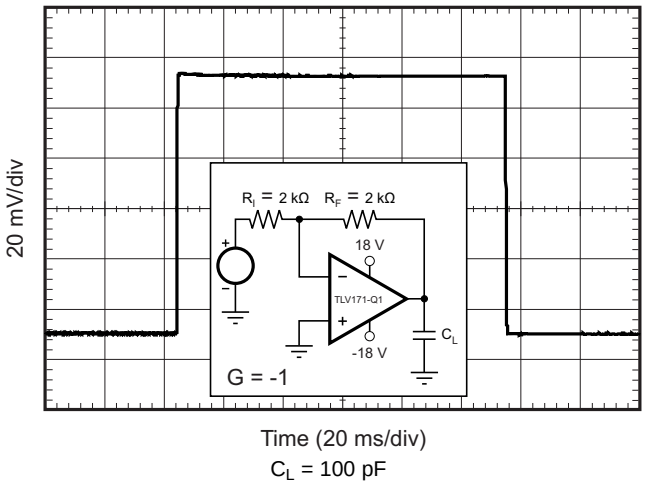


Figure 19. Small-Signal Step Response (100 mV)

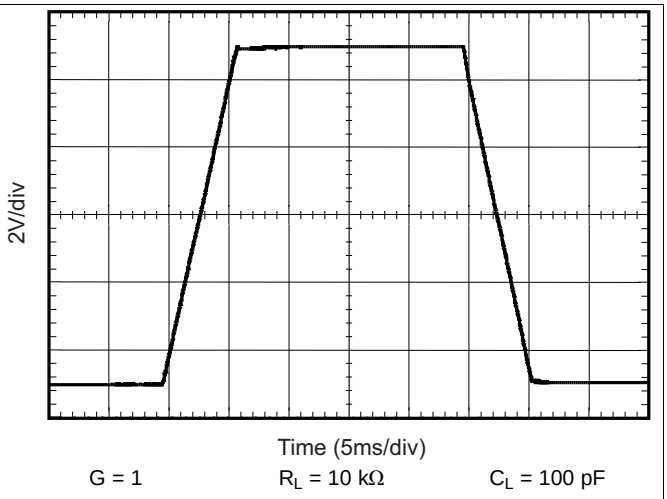


Figure 20. Large-Signal Step Response

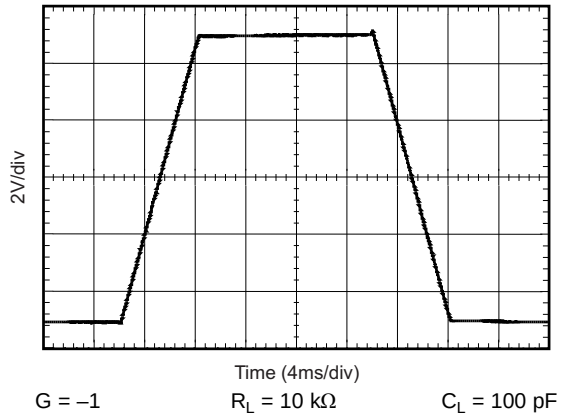


Figure 21. Large-Signal Step Response

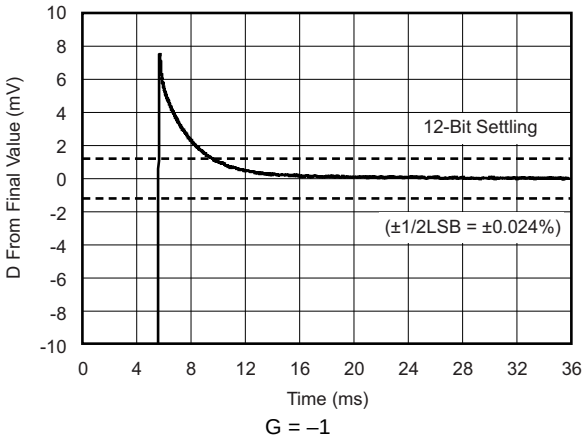


Figure 22. Large-Signal Settling Time (10-V Positive Step)

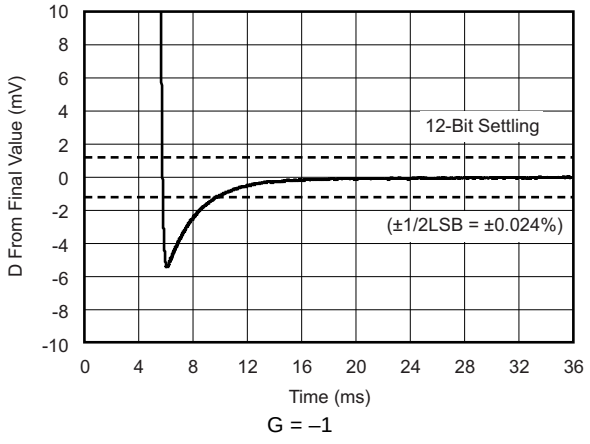


Figure 23. Large-Signal Settling Time (10-V Negative Step)

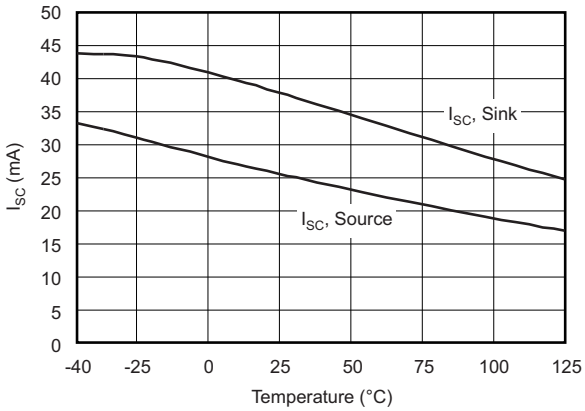


Figure 24. Short-Circuit Current vs Temperature

Typical Characteristics (continued)

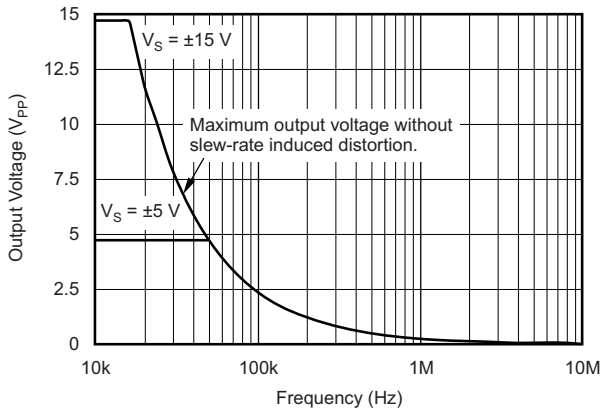


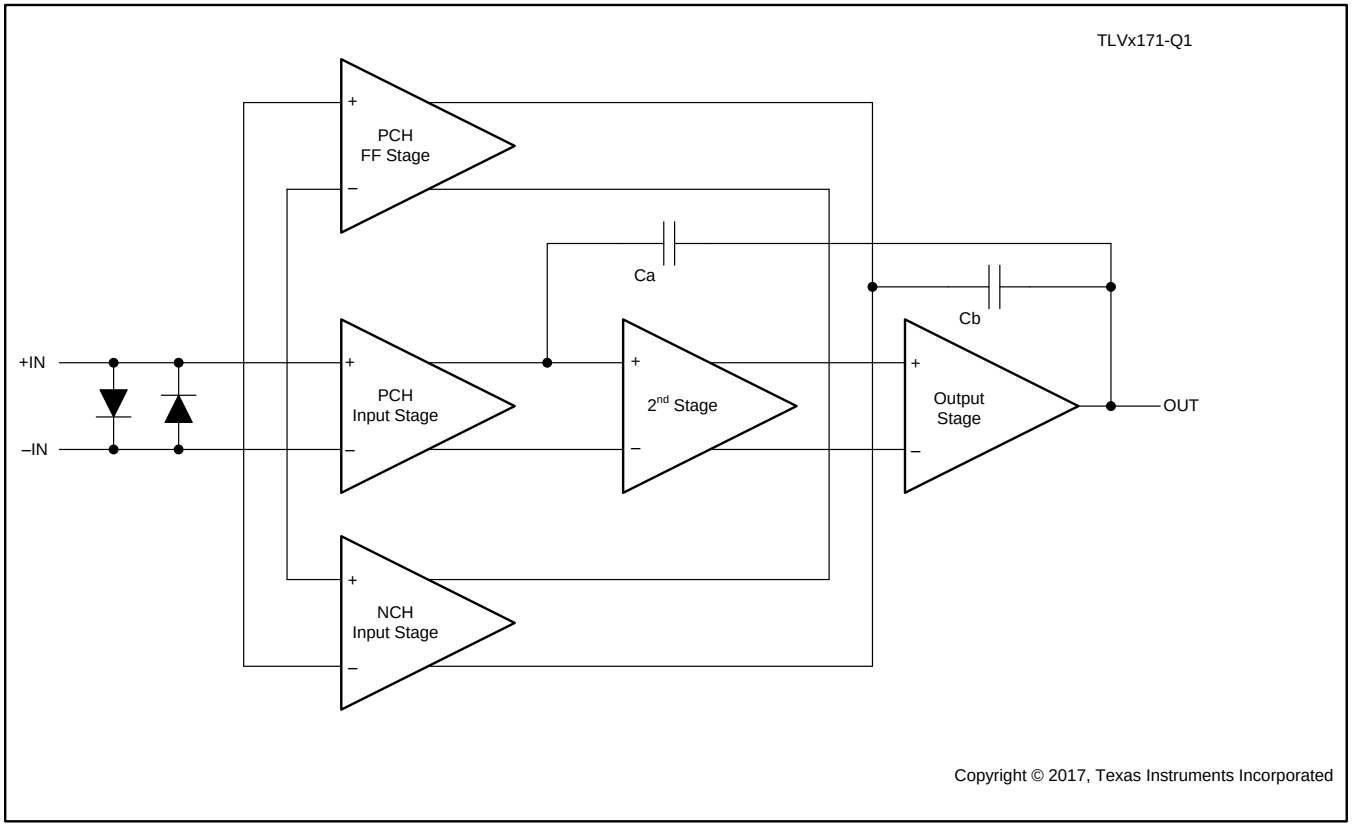
Figure 25. Maximum Output Voltage vs Frequency

7 Detailed Description

7.1 Overview

The TLVx171-Q1 family of operational amplifiers provides high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 1 µV/°C (typical) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, AOL, and superior THD.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Characteristics

The TLVx171-Q1 family of devices is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in *Typical Characteristics*.

7.3.2 Phase-Reversal Protection

The TLVx171-Q1 family of devices has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the TLVx171-Q1 family of devices prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. Figure 26 shows this performance.

Feature Description (continued)

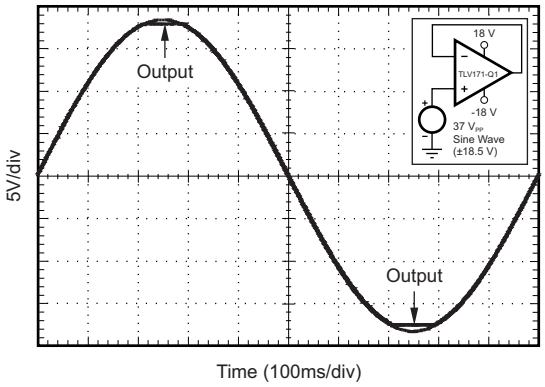


Figure 26. No Phase Reversal

7.3.3 Capacitive Load and Stability

The dynamic characteristics of the TLVx171-Q1 family of devices are optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 27 and Figure 28 shows small-signal overshoot versus capacitive load for several values of R_{OUT}. For details of analysis techniques and application circuits, see *Applications Bulletin AB-028*, available for download from TI.com.

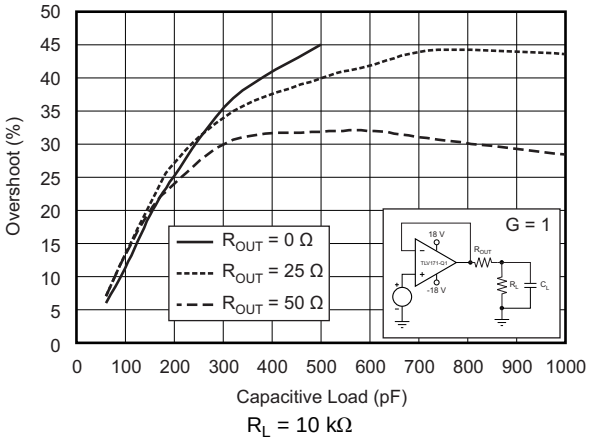


Figure 27. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

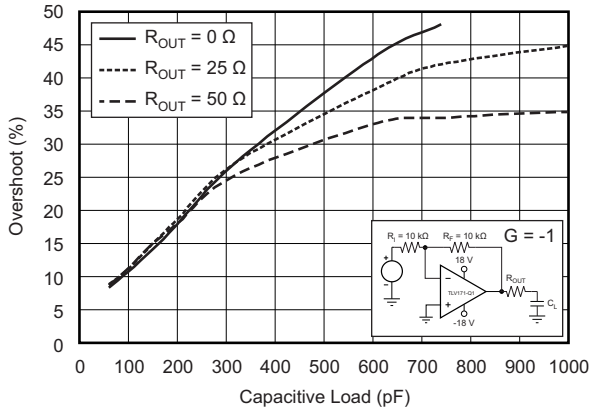


Figure 28. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

7.4 Device Functional Modes

7.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the TLVx171-Q1 family of devices extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is listed in Table 3.

Table 3. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
Offset voltage vs temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at f = 1kHz		30		nV/$\sqrt{\text{Hz}}$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV171-Q1 operational amplifier family provides high overall performance, making the device ideal for many general-purpose applications. The excellent offset drift of only 1 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.1.1 Electrical Overstress

Designers often ask questions about the capability of an op amp to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in *Absolute Maximum Ratings*. Figure 29 shows how a series input resistor can be added to the input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.

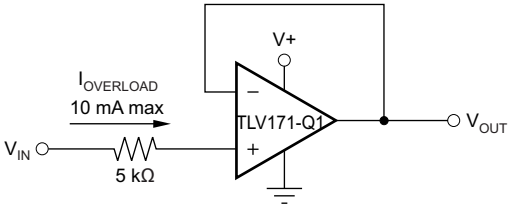


Figure 29. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If the ability of the supply to absorb this current is uncertain, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.2 Typical Application

8.2.1 Capacitive Load Drive Solution Using an Isolation Resistor

The TLVx171-Q1 device can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open loop gain of the system to ensure the circuit has sufficient phase margin.

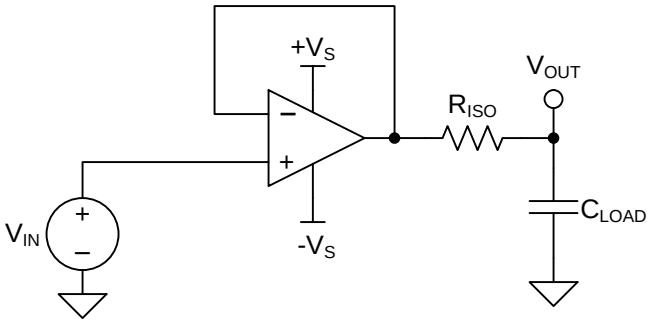


Figure 30. Unity-Gain Buffer with R_{ISO} Stability Compensation

8.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μF, 0.1 μF, and 1 μF
- Phase margin: 45° and 60°

8.2.1.2 Detailed Design Procedure

Figure 31 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 31. Not shown in Figure 31 is the open-loop output resistance of the op amp, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade. Figure 31 shows the concept. The 1/β curve for a unity-gain buffer is 0 dB.

Typical Application (continued)

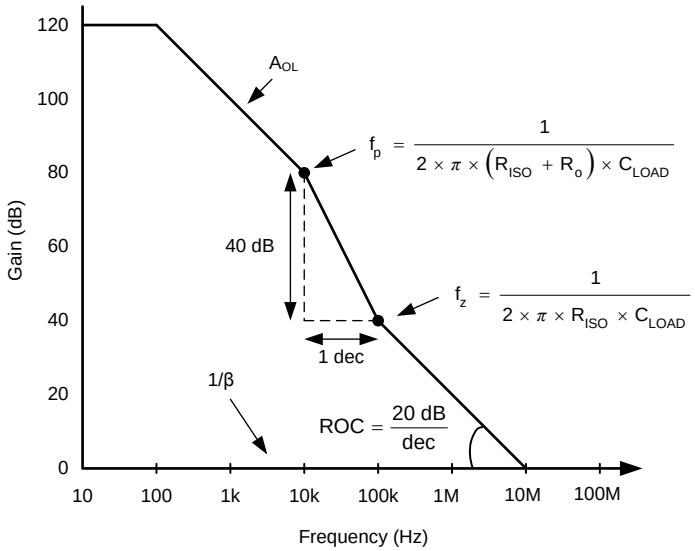


Figure 31. Unity-Gain Amplifier with R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. Table 4 lists the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the TLVx171-Q1, see *Capacitive Load Drive Solution using an Isolation Resistor*.

Table 4. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

8.2.1.3 Application Curve

The TLVx171-Q1 series meets the supply voltage requirements of 30 V. The TLVx171-Q1 device was tested for various capacitive loads and R_{ISO} was adjusted to achieve an overshoot corresponding to Table 4. Figure 32 shows the test results.

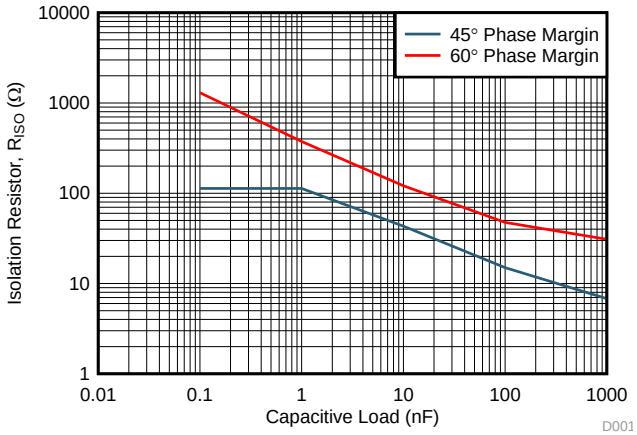


Figure 32. R_{ISO} vs C_{LOAD}

9 Power Supply Recommendations

The TLV171-Q1 family of devices is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see *Layout*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. See *Circuit Board Layout Techniques* for detailed information.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 33, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

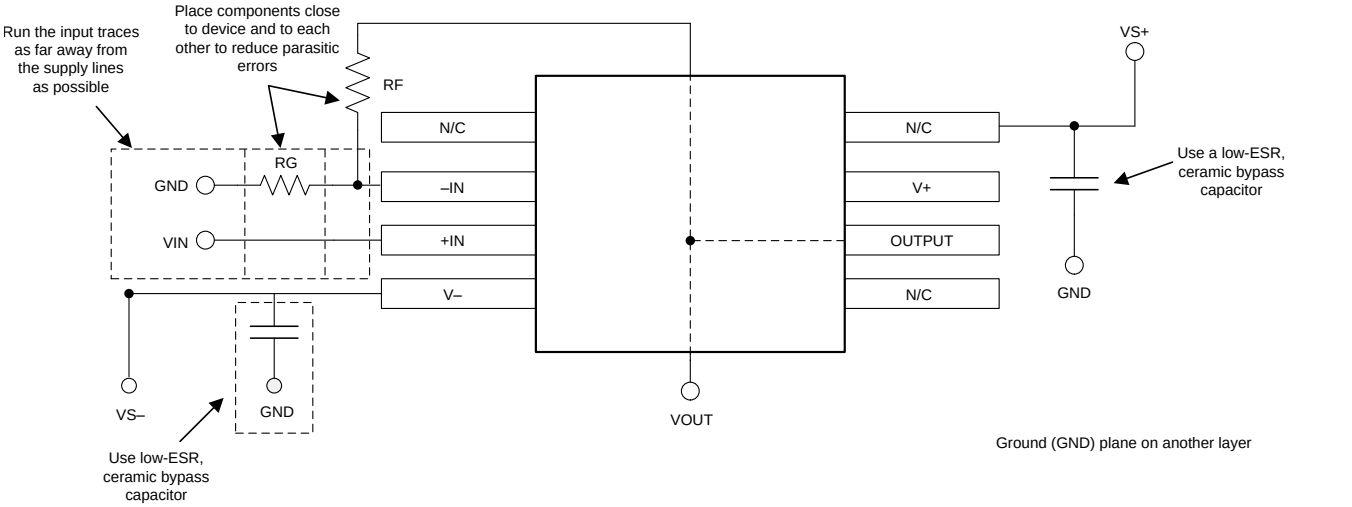


Figure 33. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Applications Bulletin AB-028* (SBOA015)
- *Capacitive Load Drive Solution using an Isolation Resistor* (TIDU032)
- *Circuit Board Layout Techniques* (SLOA089)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV171-Q1	Click here	Click here	Click here	Click here	Click here
TLV2171-Q1	Click here	Click here	Click here	Click here	Click here
TLV4171-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV171QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1CJT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV171-Q1 :

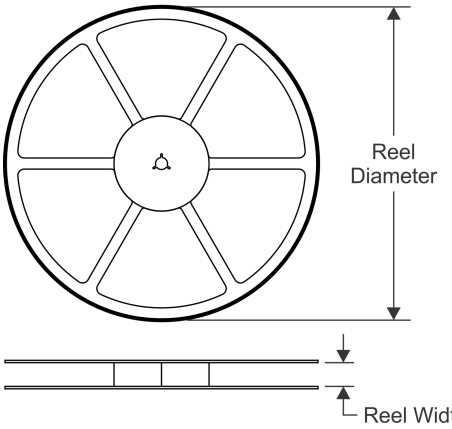
- Catalog: TLV171

NOTE: Qualified Version Definitions:

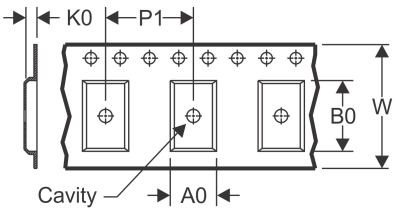
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

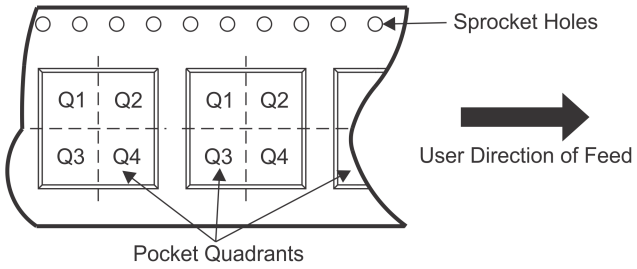


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

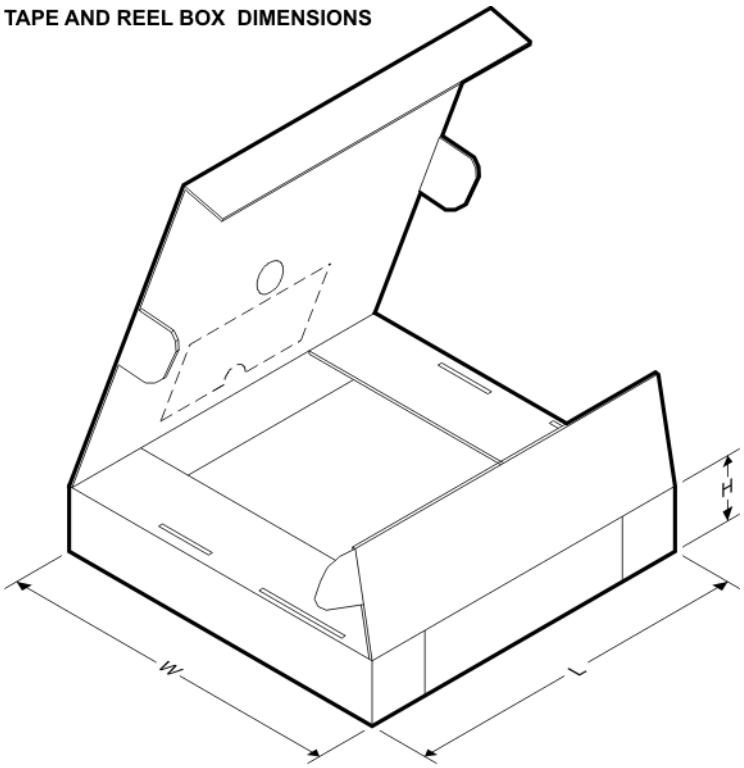
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV171QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

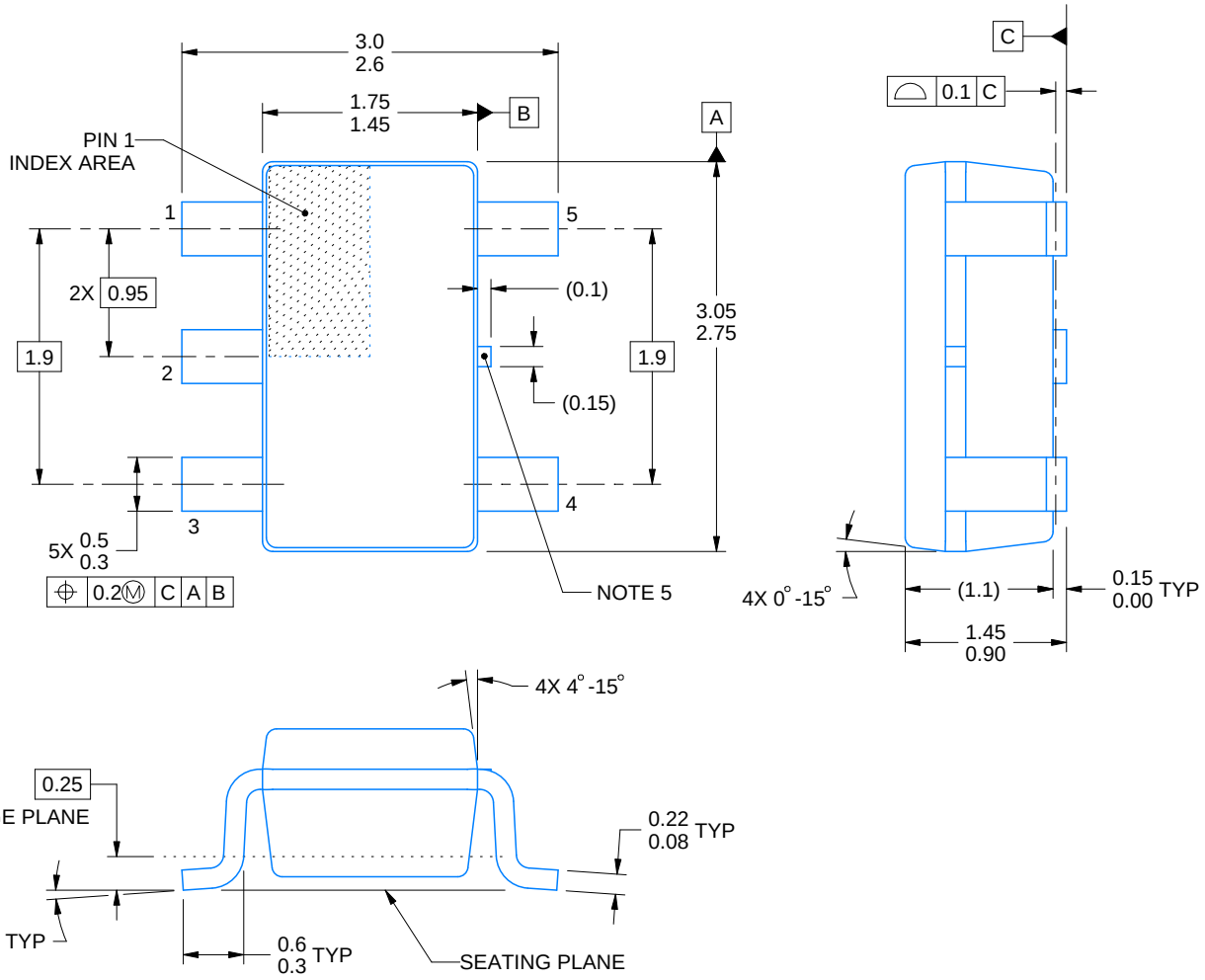
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV171QDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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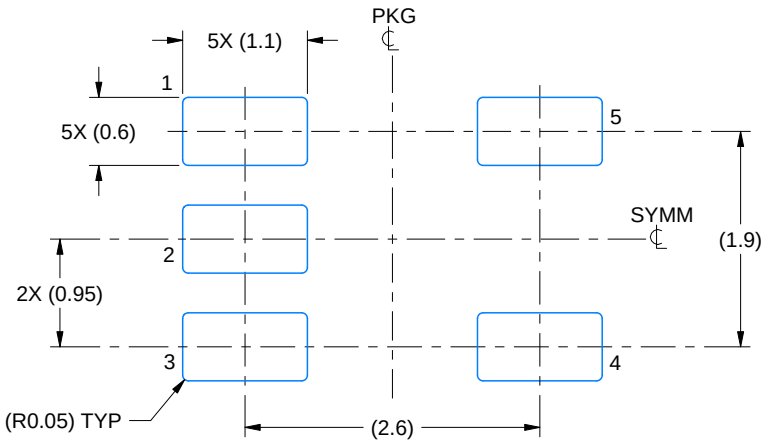
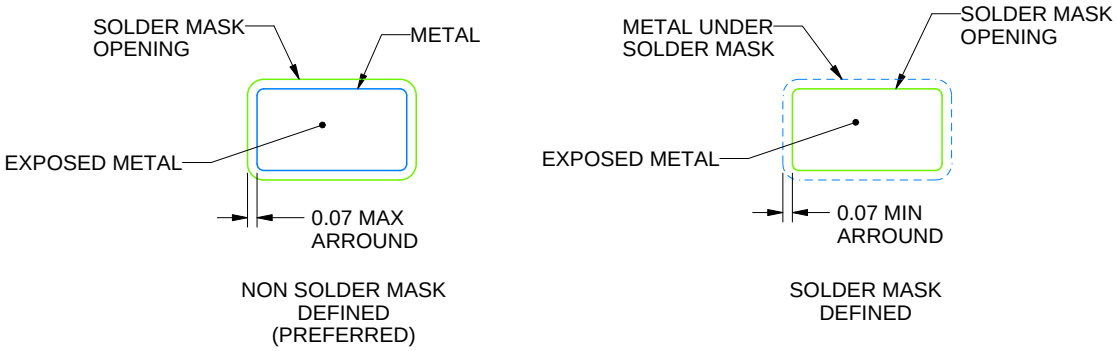
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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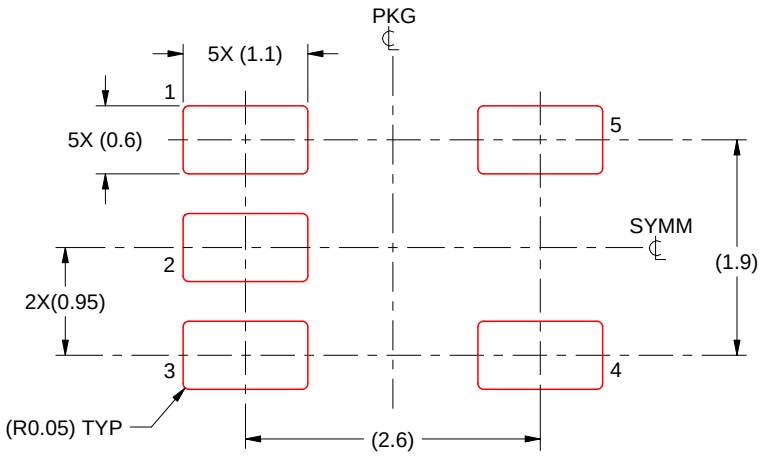
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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