TMUX6219-Q1 Automotive 36V, Low Ron, 2:1 (SPDT) Switch with 1.8V Logic

1 Features

- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature
- Functional safety-capable
  - Documentation avaialable to aid functional safety system design
- Dual supply range: ±4.5V to ±18V
- Single supply range: 4.5V to 36V
- Low on-resistance: 2.1Ω
- Low charge injection: -10pC
- High current support: 330mA (maximum) (VSSOP)
- High current support: 440mA (maximum) (WSON)
- 1.8V logic compatible
- Fail-safe logic
- Rail-to-rail operation
- Bidirectional signal path
- Break-before-make switching

2 Applications

- EV charging station power module
- Advanced driver assistance systems (ADAS)
- Automotive gateway
- Analog and digital multiplexing / demultiplexing
- Automotive head unit
- Telematics control unit
- Emergency call (eCall)
- Infotainment
- Body control modules (BCM)
- Body electronics and lighting
- Battery management systems (BMS)
- HVAC controller module
- ADAS domain controller

3 Description

The TMUX6219-Q1 is a complementary metal-oxide semiconductor (CMOS) switch in a single channel, 2:1 (SPDT) configuration. The device works with single supply (4.5V to 36V), dual supplies (±4.5V to ±18V), or asymmetric supplies (such as V_{DD} = 5V, V_{SS} = −8V). The TMUX6219-Q1 supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from V_{SS} to V_{DD}.

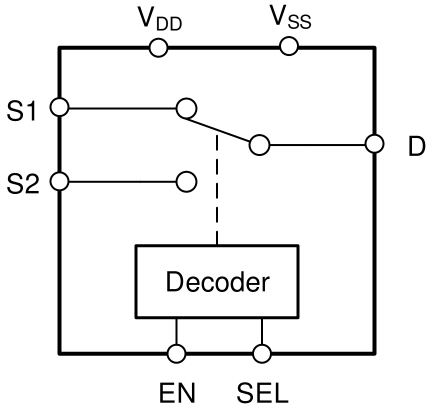
The TMUX6219-Q1 can be enabled or disabled by controlling the EN pin. When disabled, both signal path switches are off. When enabled, the SEL pin can be used to turn on signal path 1 (S1 to D) or signal path 2 (S2 to D). All logic control inputs support logic levels from 1.8V to V_{DD}, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

The TMUX6219-Q1 is part of the precision switches and multiplexers family of devices. These devices have very low on and off leakage currents and low charge injection, allowing them to be used in high precision measurement applications.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE [2]
TMUX6219-Q1	DGK (VSSOP, 8)	3mm × 4.9mm
	RQX (WSON, 8)	2mm × 3mm

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TMUX6219-Q1 Block Diagram

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4 Pin Configuration and Functions

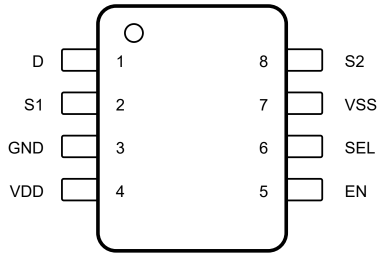


Figure 4-1. DGK Package, 8-Pin VSSOP (Top View)

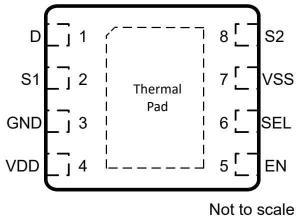


Figure 4-2. RQX Package, 8-Pin WSON (Top View)

Table 4-1. Pin Functions

PIN			TYPE[(1)]	DESCRIPTION[(2)]
NAME	DGK	RQX		
D	1	1	I/O	Drain pin. Can be an input or output.
S1	2	2	I/O	Source pin 1. Can be an input or output.
GND	3	3	P	Ground (0V) reference
V_{DD}	4	4	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between V_{DD} and GND.
EN	5	5	I	Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on.
SEL	6	6	I	Logic control input, has internal pull-down resistor. Controls the switch connection as shown in Section 7.5.
V_{SS}	7	7	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1μF to 10μF between V_{SS} and GND.
S2	8	8	I/O	Source pin 2. Can be an input or output.
Thermal Pad			—	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to Section 7.4 for what to do with unused pins.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$V_{DD}–V_{SS}$	Power supply voltage differential		38	V
V_{DD}	Supply voltage	–0.5	38	V
V_{SS}	Supply voltage	–38	0.5	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SEL, EN)(3)	–0.5	38	V
I_{SEL} or I_{EN}	Logic control input pin current (SEL, EN)(3)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)(3)	V_{SS}–0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current(3)	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)		I_{DC} + 10 %(4)	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation(5)		460	mW

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For DGK package: P_{tot} derates linearly above T_A = 70°C by 6.7mW/°C.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Thermal Information

THERMAL METRIC(1)		TMUX6219-Q1	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	152.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} - V_{SS} (1)	Power supply voltage differential	4.5		36	V
V_{DD}	Positive power supply voltage	4.5		36	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
V_{SEL} or V_{EN}	Address or enable pin voltage	0		36	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} (2)	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 36 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

5.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC})		T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PACKAGE	**TEST CONDITIONS**				
DGK (VSSOP)	±15 V Dual Supply	330	210	120	mA
	+36 V Single Supply(1)	300	190	110	mA
	+12 V Single Supply	240	160	100	mA
	±5 V Dual Supply	240	160	100	mA
	+5 V Single Supply	180	120	80	mA

(1) Specified for nominal supply voltage only.

5.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		2.1	2.9	Ω
			–40°C to +85°C			3.8	Ω
			–40°C to +125°C			4.5	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		0.05	0.25	Ω
			–40°C to +85°C			0.3	Ω
			–40°C to +125°C			0.35	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10 mA Refer to On-Resistance	25°C		0.5	0.6	Ω
			–40°C to +85°C			0.7	Ω
			–40°C to +125°C			0.85	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.01		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Off-Leakage Current	25°C	–0.3	0.1	0.3	nA
			–40°C to +85°C	–3		3	nA
			–40°C to +125°C	–50		50	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to Off-Leakage Current	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–70		70	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V Refer to On-Leakage Current	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–70		70	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.005	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	40	µA
			–40°C to +85°C			48	µA
			–40°C to +125°C			62	µA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		3	10	µA
			–40°C to +85°C			15	µA
			–40°C to +125°C			25	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		120	175	ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			210	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		100	170	ns
			–40°C to +85°C			185	ns
			–40°C to +125°C			200	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		100	180	ns
			–40°C to +85°C			195	ns
			–40°C to +125°C			210	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 100ns R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.19		ms
			–40°C to +85°C		0.2		ms
			–40°C to +125°C		0.2		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Propagation Delay	25°C		700		ps
Q_{INJ}	Charge injection	V_D = 0 V, C_L = 1 nF Refer to Charge Injection	25°C		–10		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–75		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–55		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–117		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–106		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		40		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.18		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–64		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0005		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		33		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		48		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		148		pF

5.8 36 V Single Supply: Electrical Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 30 V I_D = –10 mA Refer to On-Resistance	25°C		2.5	3.2	Ω
			–40°C to +85°C			4.2	Ω
			–40°C to +125°C			4.9	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 30 V I_D = –10 mA Refer to On-Resistance	25°C		0.1	0.2	Ω
			–40°C to +85°C			0.25	Ω
			–40°C to +125°C			0.3	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 30 V I_S = –10 mA Refer to On-Resistance	25°C		0.3	1	Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			2	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 18 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.009		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V Refer to Off-Leakage Current	25°C	–0.5	0.1	0.5	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–70		70	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V Refer to Off-Leakage Current	25°C	–2	0.1	2	nA
			–40°C to +85°C	–10		10	nA
			–40°C to +125°C	–80		80	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is on V_S = V_D = 30 V or 1 V Refer to On-Leakage Current	25°C	–2	0.1	2	nA
			–40°C to +85°C	–10		10	nA
			–40°C to +125°C	–80		80	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.005	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 39.6 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		28	50	µA
			–40°C to +85°C			58	µA
			–40°C to +125°C			70	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.9 36 V Single Supply: Switching Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		110	170	ns
			–40°C to +85°C			185	ns
			–40°C to +125°C			200	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		110	180	ns
			–40°C to +85°C			190	ns
			–40°C to +125°C			200	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		90	180	ns
			–40°C to +85°C			195	ns
			–40°C to +125°C			200	ns
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		44		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 100ns R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.17		ms
			–40°C to +85°C		0.19		ms
			–40°C to +125°C		0.19		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Propagation Delay	25°C		920		ps
Q_{INJ}	Charge injection	V_D = 18 V, C_L = 1 nF Refer to Charge Injection	25°C		–13		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Off Isolation	25°C		–75		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–55		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–117		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–106		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, Refer to Bandwidth	25°C		38		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.19		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–60		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} =18 V, V_{BIAS} = 18 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0004		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		35		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		49		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		146		pF

5.10 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		4.6	6	Ω
			–40°C to +85°C			7.5	Ω
			–40°C to +125°C			8.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		0.08	0.2	Ω
			–40°C to +85°C			0.32	Ω
			–40°C to +125°C			0.35	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA Refer to On-Resistance	25°C		1.2	2	Ω
			–40°C to +85°C			2.2	Ω
			–40°C to +125°C			2.4	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.017		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Off-Leakage Current	25°C	–1	0.1	1	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–50		50	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to Off-Leakage Current	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–70		70	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V Refer to On-Leakage Current	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–70		70	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.005	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		10	35	µA
			–40°C to +85°C			45	µA
			–40°C to +125°C			55	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.11 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		180	185	ns
			–40°C to +85°C			215	ns
			–40°C to +125°C			235	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		120	180	ns
			–40°C to +85°C			210	ns
			–40°C to +125°C			230	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		130	210	ns
			–40°C to +85°C			235	ns
			–40°C to +125°C			250	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		40		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 100ns R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.19		ms
			–40°C to +85°C		0.2		ms
			–40°C to +125°C		0.2		ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Propagation Delay	25°C		740		ps
Q_{INJ}	Charge injection	V_D = 6 V, C_L = 1 nF Refer to Charge Injection	25°C		–6		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Charge Injection	25°C		–75		dB
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–55		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–117		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–106		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		42		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.3		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–65		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0009		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		38		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 6 V, f = 1 MHz	25°C		56		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 6 V, f = 1 MHz	25°C		150		pF

5.12 ±5 V Dual Supply: Electrical Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = –5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = –5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_{DD} = +4.5 V, V_{SS} = –4.5 V V_S = –4.5 V to +4.5 V I_D = –10 mA Refer to On-Resistance	25°C		4	7.2	Ω
			–40°C to +85°C			8.6	Ω
			–40°C to +125°C			10	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –4.5 V to +4.5 V I_D = –10 mA Refer to On-Resistance	25°C		0.1	0.3	Ω
			–40°C to +85°C			0.35	Ω
			–40°C to +125°C			0.4	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –4.5 V to +4.5 V I_D = –10 mA Refer to On-Resistance	25°C		1.3	2.2	Ω
			–40°C to +85°C			2.5	Ω
			–40°C to +125°C			2.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.019		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is off V_S = +4.5 V / –4.5 V V_D = –4.5 V / + 4.5 V Refer to Off-Leakage Current	25°C	–1	0.1	1	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–50		50	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is off V_S = +4.5 V / –4.5 V V_D = –4.5 V / + 4.5 V Refer to Off-Leakage Current	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–50		50	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = +5.5 V, V_{SS} = –5.5 V Switch state is on V_S = V_D = ±4.5 V Refer to On-Leakage Current	25°C	–2	0.1	2	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–50		50	nA
LOGIC INPUTS (SEL / EN pins)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.005	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = +5.5 V, V_{SS} = –5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		20	35	µA
			–40°C to +85°C			40	µA
			–40°C to +125°C			50	µA
I_{SS}	V_{SS} supply current	V_{DD} = +5.5 V, V_{SS} = –5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		0.001	5	µA
			–40°C to +85°C			8	µA
			–40°C to +125°C			15	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

5.13 ±5 V Dual Supply: Switching Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = –5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = –5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		300	400	ns
			–40°C to +85°C			490	ns
			–40°C to +125°C			550	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		220	300	ns
			–40°C to +85°C			350	ns
			–40°C to +125°C			380	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Turn-on and Turn-off Time	25°C		210	280	ns
			–40°C to +85°C			330	ns
			–40°C to +125°C			350	ns
t_{BBM}	Break-before-make time delay	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 100ns R_L = 300 Ω, C_L = 35pF Refer to Turn-on (VDD) Time	25°C		0.19		ms
			–40°C to +85°C		0.19	1	ms
			–40°C to +125°C		0.19	1	ms
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF Refer to Propagation Delay	25°C		650		ps
Q_{INJ}	Charge injection	V_D = 0 V, C_L = 1 nF Refer to Charge Injection	25°C		–5		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–55		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–117		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–106		dB
BW	–3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, Refer to Bandwidth	25°C		43		MHz
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω , C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–68		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 5 V, V_{BIAS} = 0 V R_L = 10 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.001		%
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 5 V, V_{BIAS} = 0 V R_L = 10 MΩ , C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0006		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		40		pF
$C_{D(OFF)}$	Drain off capacitance	V_S = 0 V, f = 1 MHz	25°C		60		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S = 0 V, f = 1 MHz	25°C		150		pF

5.14 Typical Characteristics

at T_A = 25°C

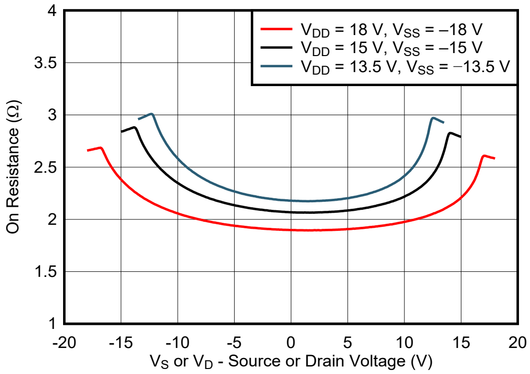


Figure 5-1. On-Resistance vs Source or Drain Voltage – Dual Supply

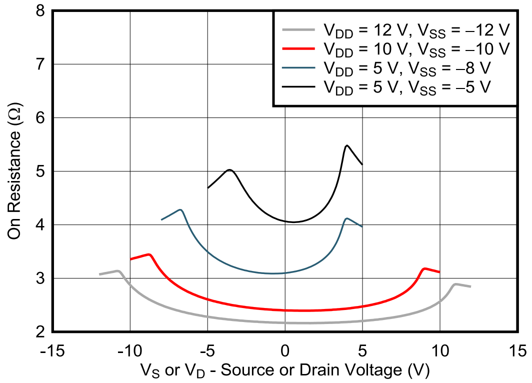


Figure 5-2. On-Resistance vs Source or Drain Voltage – Dual Supply

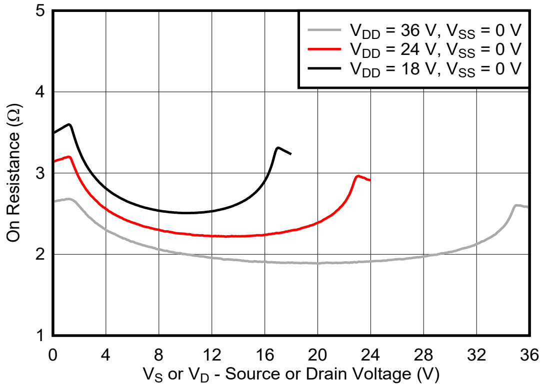


Figure 5-3. On-Resistance vs Source or Drain Voltage – Single Supply

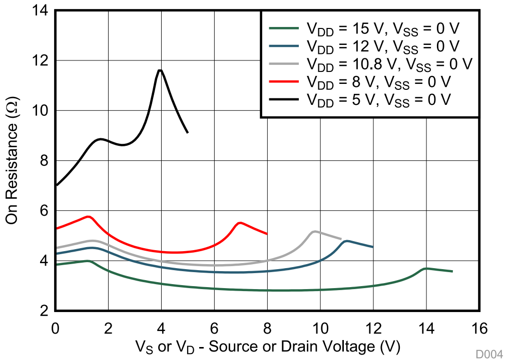
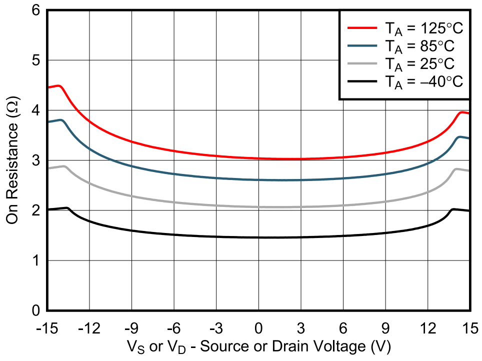
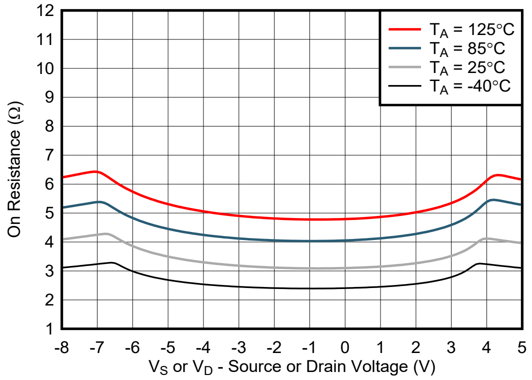


Figure 5-4. On-Resistance vs Source or Drain Voltage – Single Supply



V_{DD} = 15 V, V_{SS} = −15 V

Figure 5-5. On-Resistance vs Temperature

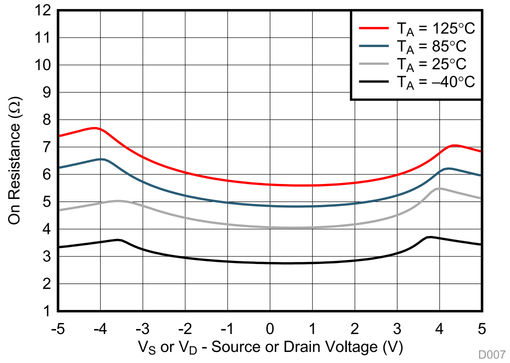


V_{DD} = 5 V, V_{SS} = −8 V

Figure 5-6. On-Resistance vs Temperature

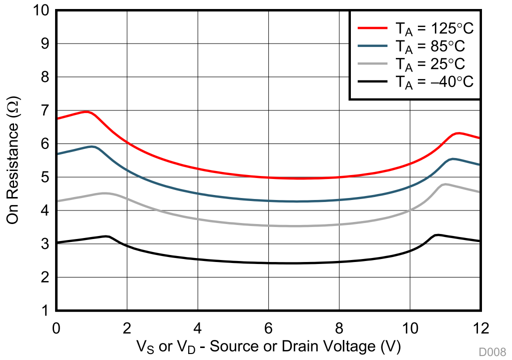
5.14 Typical Characteristics (continued)

at T_A = 25°C



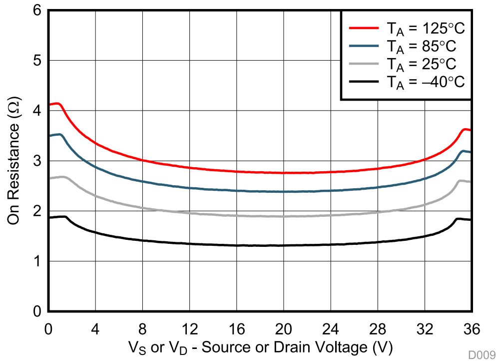
V_{DD} = 5 V, V_{SS} = −5 V

Figure 5-7. On-Resistance vs Temperature



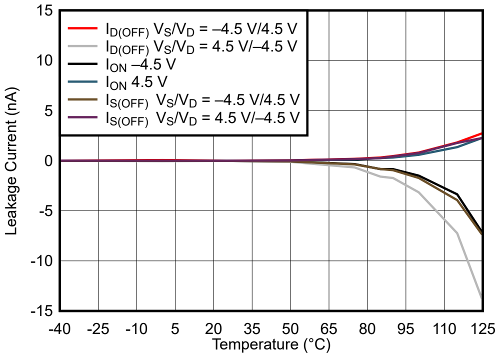
V_{DD} = 12 V, V_{SS} = 0 V

Figure 5-8. On-Resistance vs Temperature



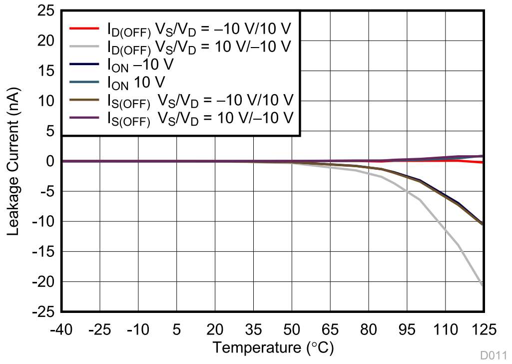
V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-9. On-Resistance vs Temperature



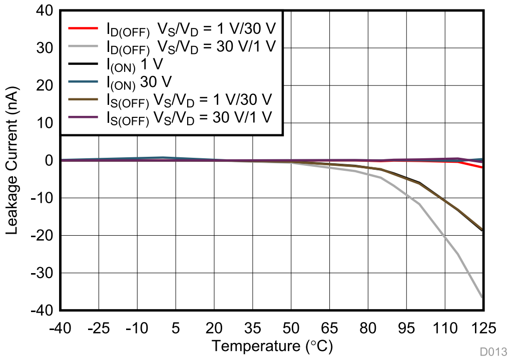
V_{DD} = 5 V, V_{SS} = −5 V

Figure 5-10. Leakage Current vs Temperature



V_{DD} = 15 V, V_{SS} = −15 V

Figure 5-11. Leakage Current vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-12. Leakage Current vs Temperature

5.14 Typical Characteristics (continued)

at T_A = 25°C

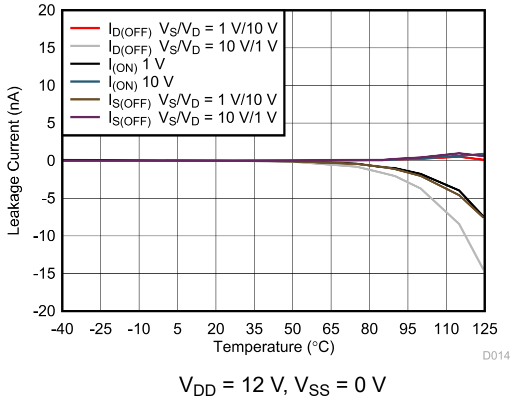


Figure 5-13. Leakage Current vs Temperature

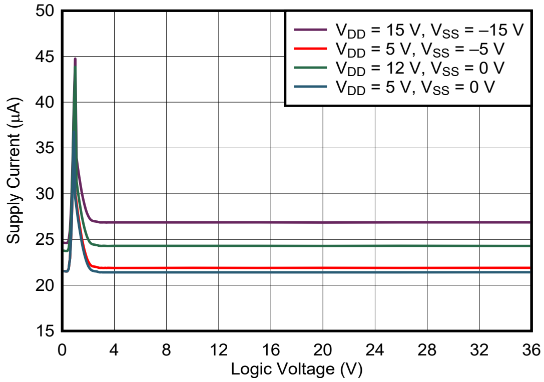


Figure 5-14. Supply Current vs Logic Voltage

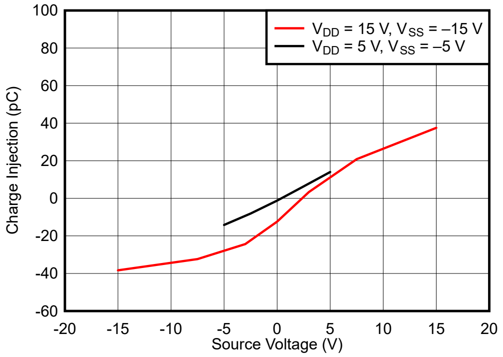


Figure 5-15. Charge Injection vs Source Voltage – Dual Supply

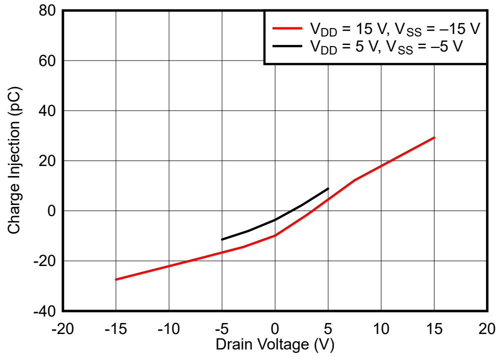


Figure 5-16. Charge Injection vs Drain Voltage – Dual Supply

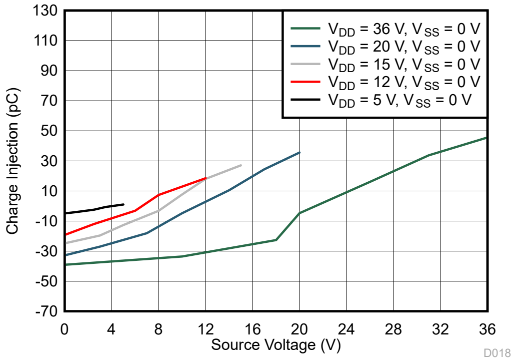


Figure 5-17. Charge Injection vs Source Voltage – Single Supply

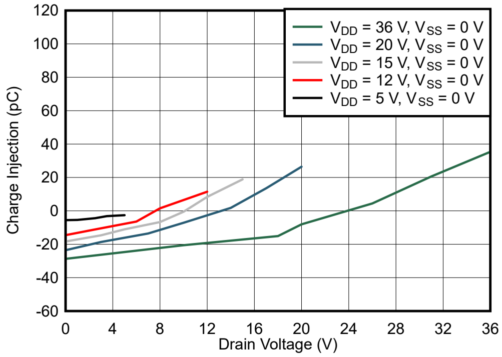
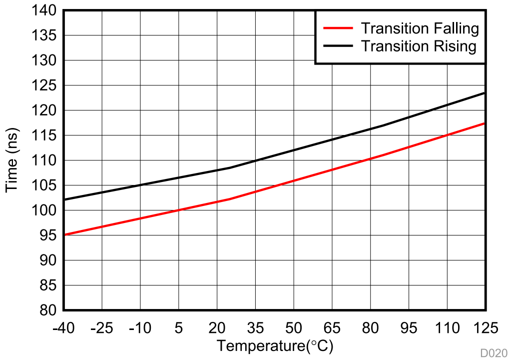


Figure 5-18. Charge Injection vs Drian Voltage – Single Supply

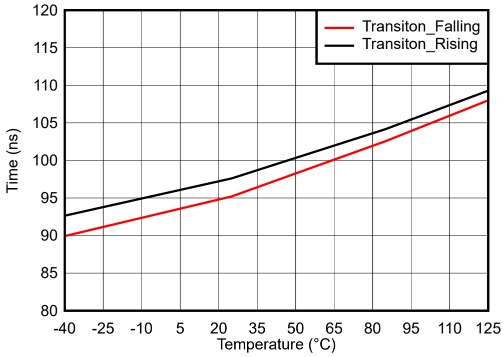
5.14 Typical Characteristics (continued)

at T_A = 25°C



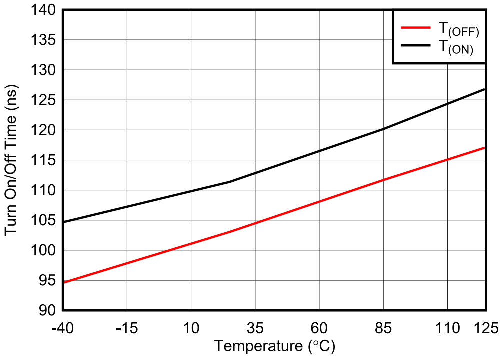
V_{DD} = 15 V, V_{SS} = −15 V

Figure 5-19. $T_{TRANSITION}$ vs Temperature



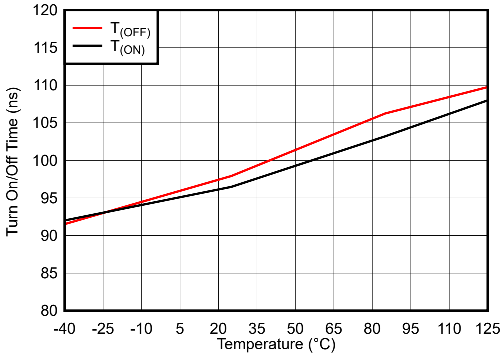
V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-20. $T_{TRANSITION}$ vs Temperature



V_{DD} = 15 V, V_{SS} = −15 V

Figure 5-21. T_{ON} and T_{OFF} vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

Figure 5-22. T_{ON} and T_{OFF} vs Temperature

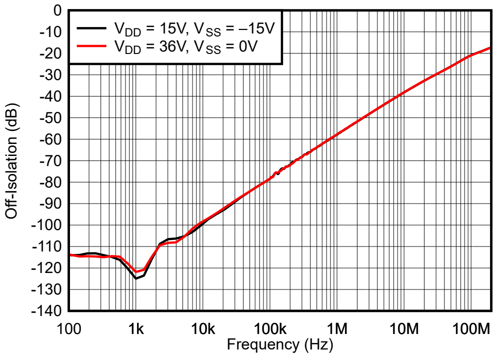
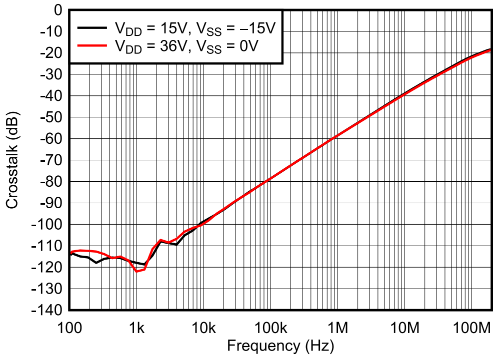


Figure 5-23. Off-Isolation vs Frequency

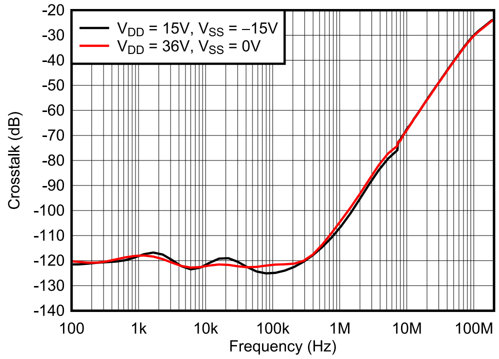


Switch *ON* (EN = 1)

Figure 5-24. Crosstalk vs Frequency

5.14 Typical Characteristics (continued)

at T_A = 25°C



Switch *OFF* (EN = 0)

Figure 5-25. Crosstalk vs Frequency

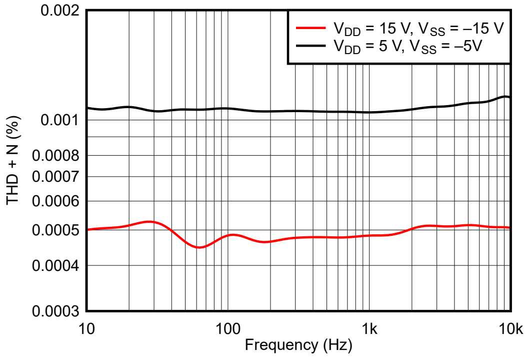


Figure 5-26. THD+N vs Frequency (Dual Supply)

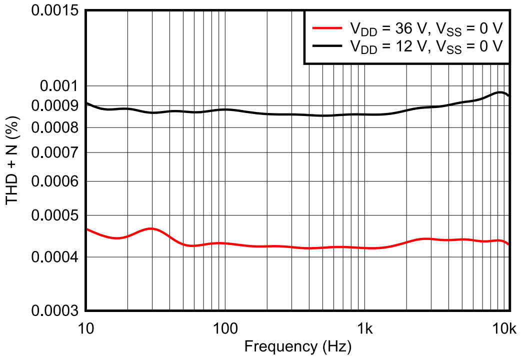
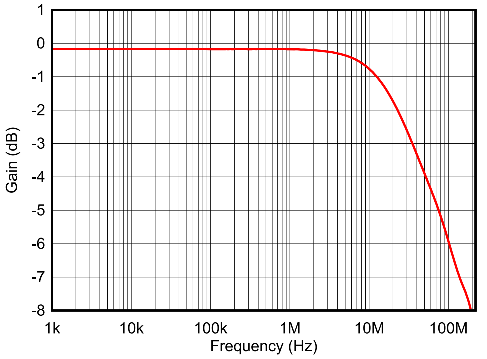
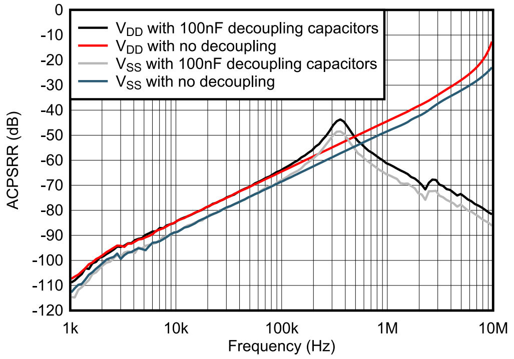


Figure 5-27. THD+N vs Frequency (Single Supply)



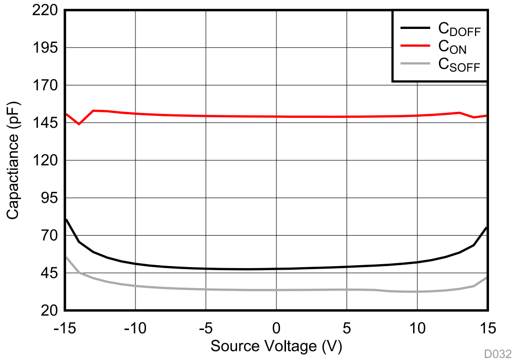
V_{DD} = 15 V, V_{SS} = −15 V

Figure 5-28. On Response vs Frequency



V_{DD} = +15 V, V_{SS} = −15 V

Figure 5-29. ACPSRR vs Frequency

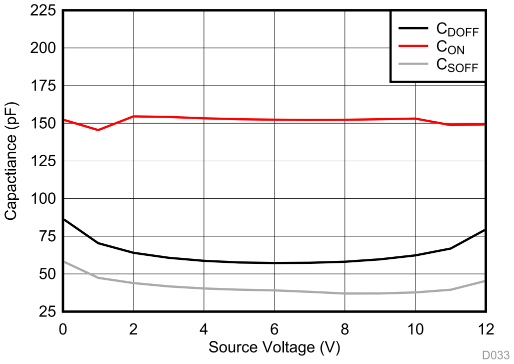


V_{DD} = +15 V, V_{SS} = −15 V

Figure 5-30. Capacitance vs Source Voltage or Drain Voltage

5.14 Typical Characteristics (continued)

at T_A = 25°C



V_{DD} = 12 V, V_{SS} = 0 V

Figure 5-31. Capacitance vs Source Voltage or Drain Voltage

6 Parameter Measurement Information

6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. Figure 6-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using the following setup, where R_{ON} is computed as $R_{ON} = V / I_{SD}$:

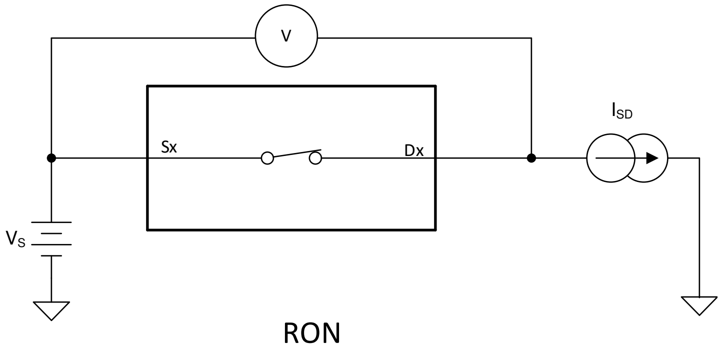


Figure 6-1. On-Resistance

6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

Figure 6-2 shows the setup used to measure both off-leakage currents.

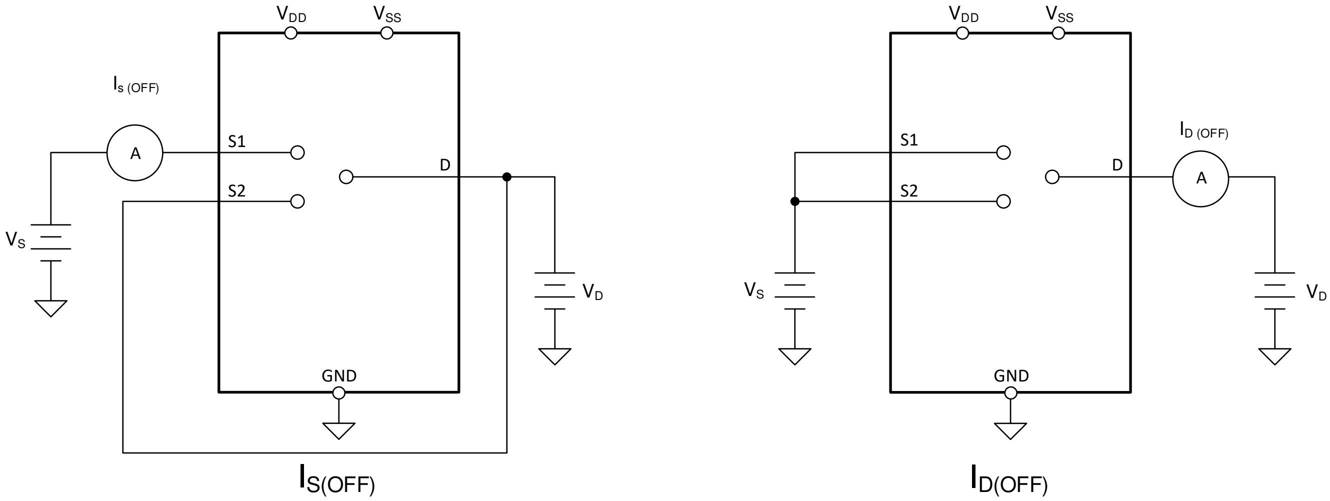


Figure 6-2. Off-Leakage Measurement Setup

6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

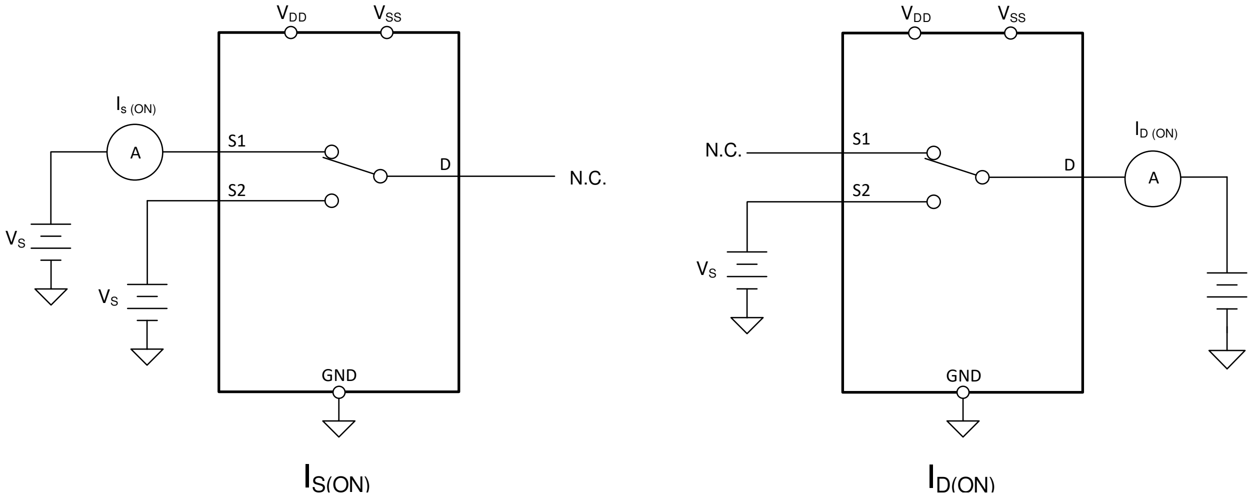


Figure 6-3. On-Leakage Measurement Setup

6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

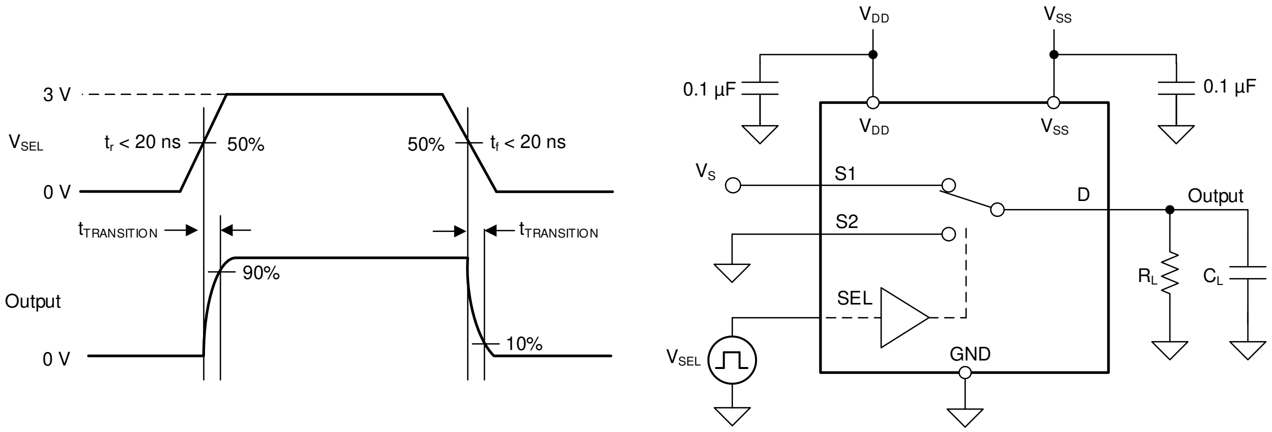


Figure 6-4. Transition-Time Measurement Setup

6.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-5 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 6-5 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

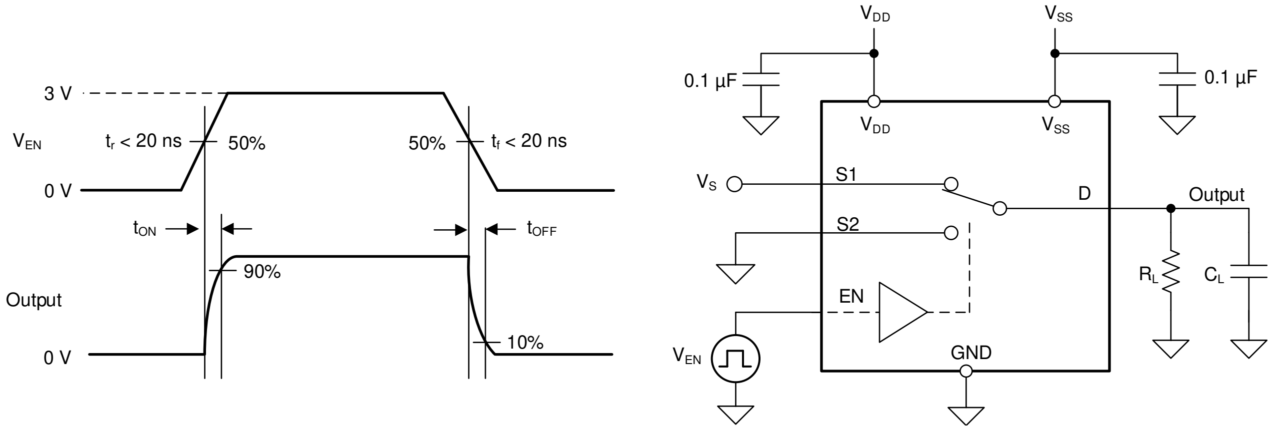


Figure 6-5. Turn-On and Turn-Off Time Measurement Setup

6.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 6-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

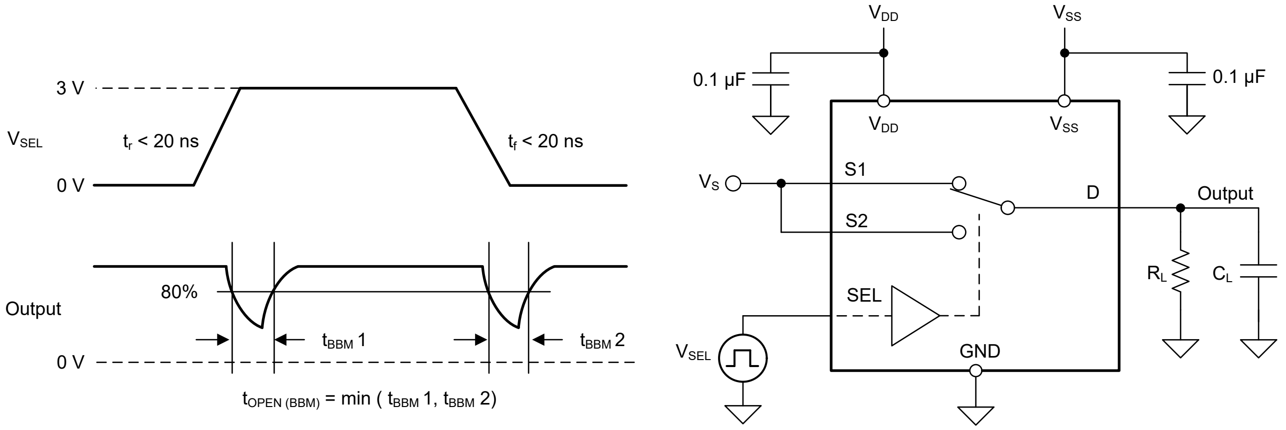


Figure 6-6. Break-Before-Make Delay Measurement Setup

6.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. Figure 6-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

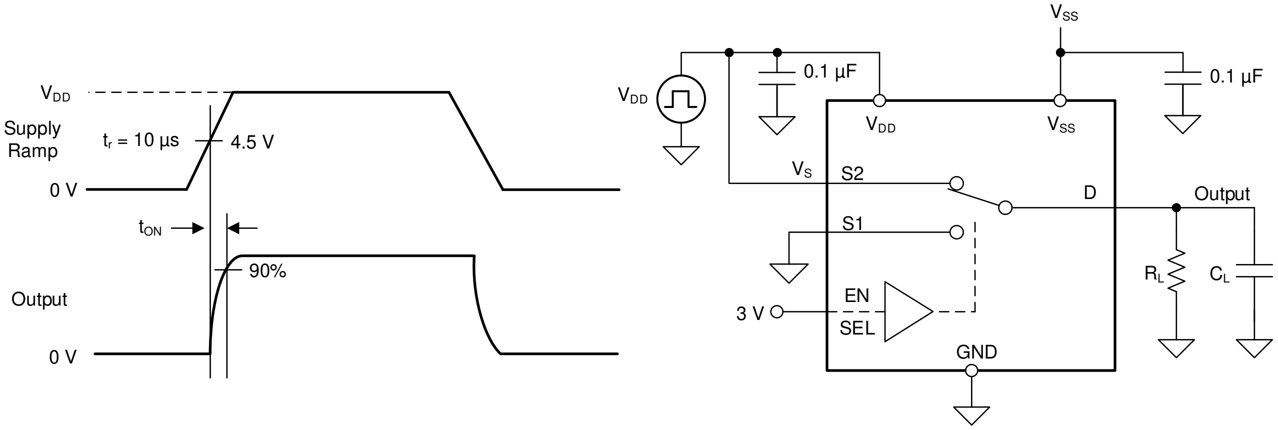


Figure 6-7. $t_{ON\ (VDD)}$ Time Measurement Setup

6.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. Figure 6-8 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

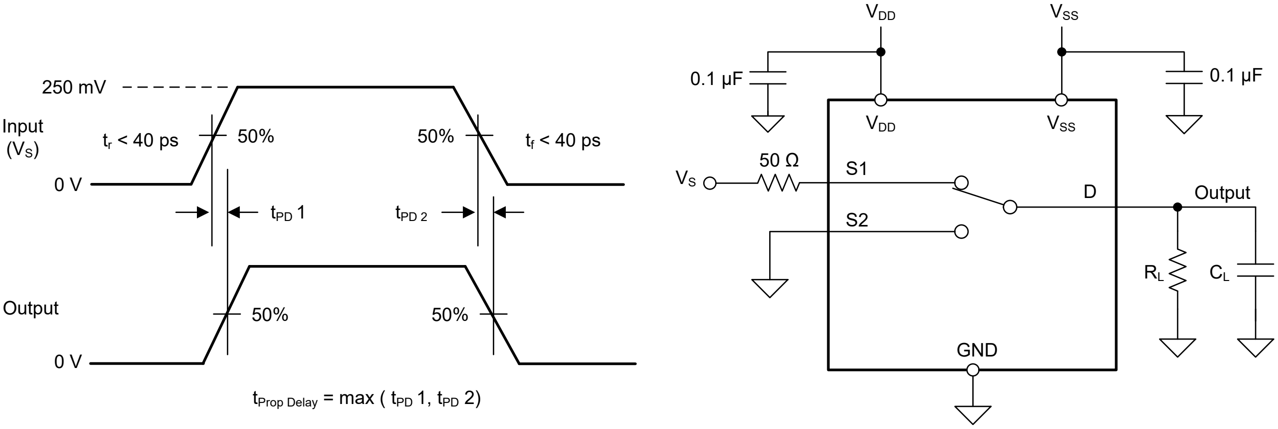


Figure 6-8. Propagation Delay Measurement Setup

6.9 Charge Injection

The TMUX6219-Q1 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 6-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

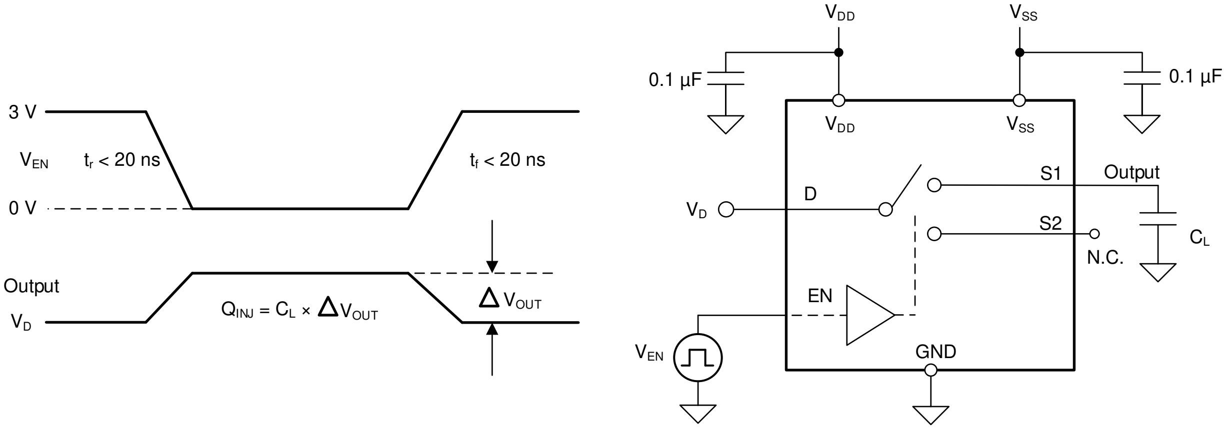
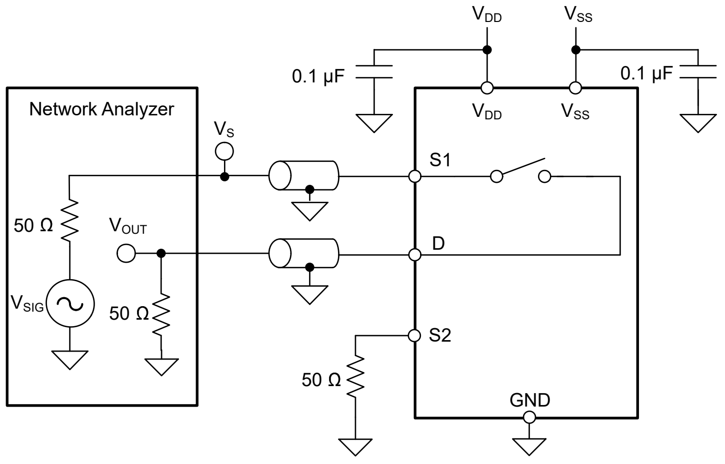


Figure 6-9. Charge-Injection Measurement Setup

6.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 6-10 shows the setup used to measure, and the equation used to calculate off isolation.

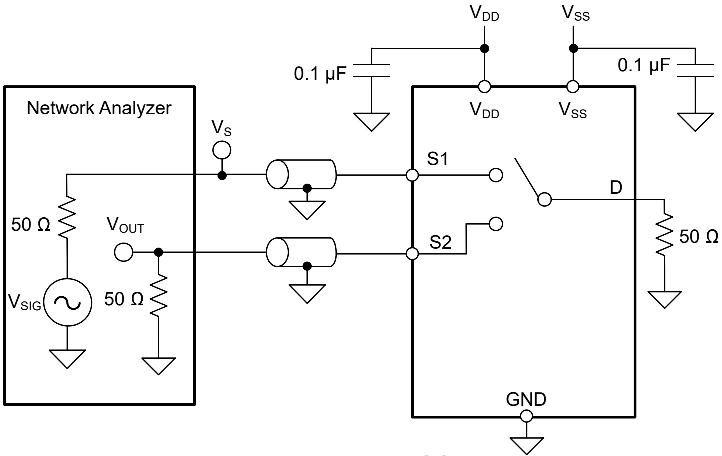


$$\text{Off Isolation} = 20 \times \text{Log}\,\frac{V_{OUT}}{V_S}$$

Figure 6-10. Off Isolation Measurement Setup

6.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 6-11 shows the setup used to measure, and the equation used to calculate crosstalk.

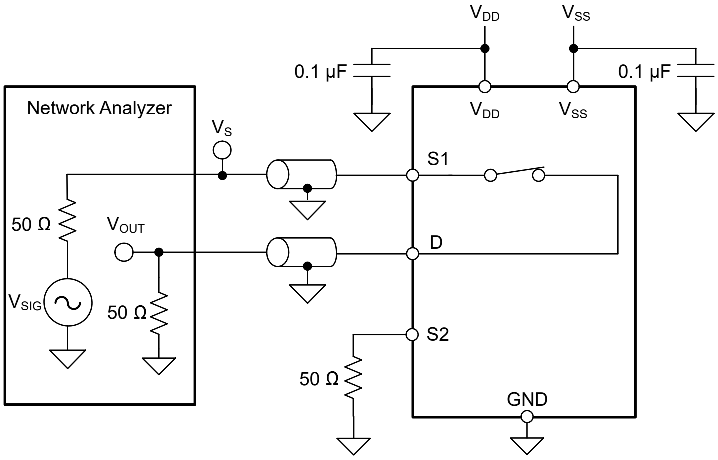


$$\text{Crosstalk} = 20 \times \text{Log} \frac{V_{OUT}}{V_S}$$

Figure 6-11. Crosstalk Measurement Setup

6.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 6-12 shows the setup used to measure bandwidth.



$$\text{Bandwidth} = 20 \times \text{Log} \frac{V_{OUT}}{V_S}$$

Figure 6-12. Bandwidth Measurement Setup

6.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output.

The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

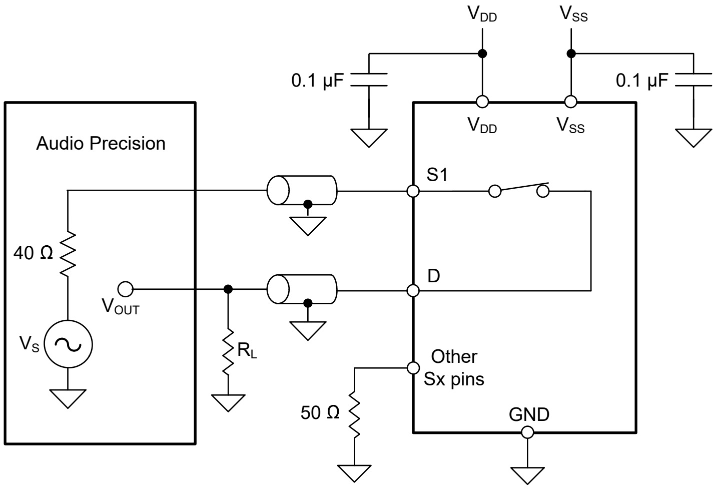
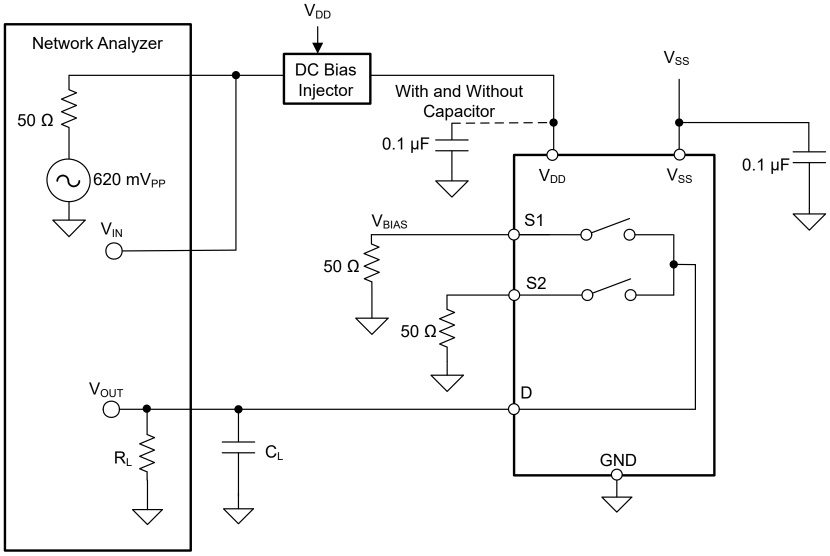


Figure 6-13. THD + N Measurement Setup

6.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mV_{PP}. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

This helps stabilize the supply and immediately filter as much of the supply noise as possible.



$$PSRR = 20 \times Log\frac{V_{OUT}}{V_{IN}}$$

Figure 6-14. ACPSRR Measurement Setup

7 Detailed Description

7.1 Overview

The TMUX6219-Q1 is a 2:1, 1-channel switch. Each input is turned on or turned off based on the state of the select line and enable pin.

7.2 Functional Block Diagram

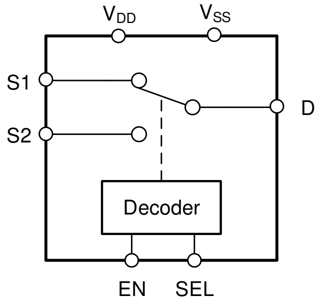


Figure 7-1. TMUX6219-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 Bidirectional Operation

The TMUX6219-Q1 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

7.3.2 Rail to Rail Operation

The valid signal path input or output voltage for TMUX6219-Q1 ranges from V_{SS} to V_{DD}.

7.3.3 1.8V Logic Compatible Inputs

The TMUX6219-Q1 has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the TMUX6219-Q1 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8V logic implementations refer to Simplifying Design with 1.8V logic Muxes and Switches.

7.3.4 Fail-Safe Logic

The TMUX6219-Q1 supports Fail-Safe Logic on the control input pins (EN and SEL) allowing for operation up to 36V above ground, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX6219-Q1 to be ramped to +36V while V_{DD} and V_{SS} = 0V. The logic control inputs are protected against positive faults of up to +36V in powered-off condition, but do not offer protection against negative overvoltage conditions.

7.3.5 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX62xx family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX62xx family of switches and multiplexers to be used in harsh environments.

7.3.6 Ultra-Low Charge Injection

The TMUX6219-Q1 has a transmission gate topology, as shown in Figure 7-2. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

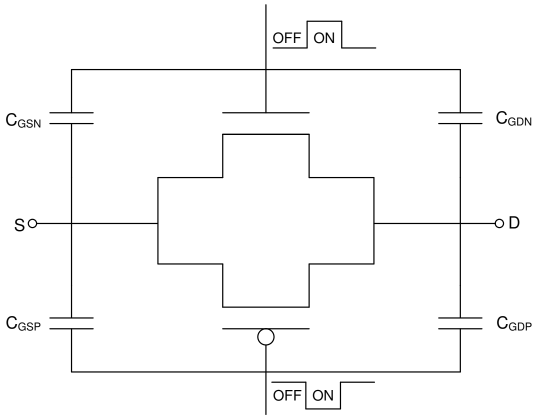


Figure 7-2. Transmission Gate Topology

The TMUX6219-Q1 contains specialized architecture to reduce charge injection on the source (Sx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the drain (D). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the drain (D) instead of the source (Sx). As a general rule, Cp should be 20× larger than the equivalent load capacitance on the source (Sx). Figure 7-3 shows charge injection variation with source voltage with different compensation capacitors on the Drain side.

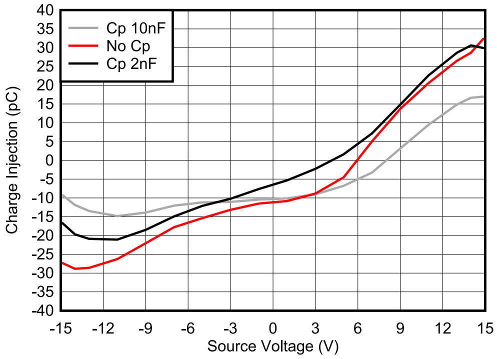


Figure 7-3. Charge Injection Compensation

7.4 Device Functional Modes

When the EN pin of the TMUX6219-Q1 is pulled high, one of the switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both of the switches are in an open state regardless of the state of the SEL pin. The control pins can be as high as 36V.

The TMUX6219-Q1 can be operated without any external components except for the supply decoupling capacitors. The EN pin has an internal pull-up resistor of 4 MΩ and SEL pin has internal pull-down resistor of 4 MΩ. If unused, the EN pin must be tied to V_{DD} and SEL pin must be tied to GND to ensure the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (S1, S2, or D) should be connected to GND.

7.5 Truth Tables

Table 7-1 provides the truth tables for the TMUX6219-Q1.

Table 7-1. TMUX6219-Q1 Truth Table

EN	SEL	Selected Source Connected To Drain (D) Pin
0	X(1)	All sources are off (HI-Z)
1	0	S1
1	1	S2

(1) X denotes *do not care*.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

TMUX6219-Q1 is part of the precision switches and multiplexers family of devices. TMUX6219-Q1 offers low RON, low on and off leakage currents and ultra-low charge injection performance. These properties make TMUX6219-Q1 ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

8.2 Typical Application

8.2.1 PWM Signal Generation (EV Charging Station)

One application of the TMUX6219-Q1 is in Electric Vehicle Service Equipment (EVSE). The EVSE is a system that monitors and controls the high voltage power path from the grid to the vehicle. One key feature of an EVSE is the pilot signal wire communication support that requires a 1-kHz, ±12-V PWM signal to be transmitted down the length of the charger cable to the vehicle.

The TMUX6219-Q1 can be used to generate 1kHz ±12V PWM signal for EVSE control pilot. A 1kHz square wave at ±12V generated by the EVSE on the control pilot line is used to detect the presence of the vehicle, communicate the maximum allowable charging current, and control charging.

Figure 8-1 shows the TMUX6219-Q1 configured for PWM signal generation for EVSE control pilot.

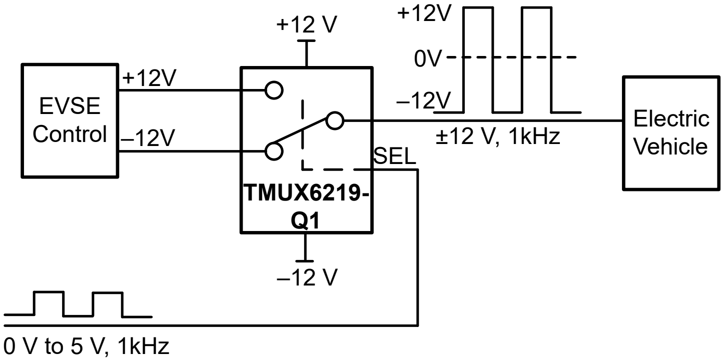


Figure 8-1. PWM Signal Generation (EV Charging Station)

8.2.2 Design Requirements

For the design example, use the parameters listed in Table 8-1 .

Table 8-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	12V
Supply (V_{SS})	−12V
MUX I/O signal range	−12V to 12V (Rail-to-Rail)
Control logic thresholds	1.8V compatible (up to V_{DD})
EN	EN pulled high to enable the switch

8.2.3 Detailed Design Procedure

The application shown in Figure 8-1 demonstrates how to generate a ±12V PWM signal that is created by toggling the TMUX6219-Q1. This PWM signal generated by the EVSE on the control pilot line signals to the car the available current of the charger, and the car will respond with a charging status. This handshake results in a safe method for supplying power to vehicle. The TMUX6219-Q1 can support 1.8V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX6219-Q1 can be operated without any external components except for the supply decoupling capacitors. The select pin has an internal pull-down resistor to prevent floating input logic. All inputs to the switch must fall within the recommend operating conditions of the TMUX6219-Q1 including signal range and continuous current. For this design with a positive supply of 12V on V_{DD}, and negative supply of −12V on V_{SS}, the signal range can be 12V to −12V. The max continuous current (I_{DC}) can be up to 330mA as shown in the *Recommended Operating Conditions table* for wide-range current measurement.

8.3 Power Supply Recommendations

The TMUX6219-Q1 operates across a wide supply range of of ±4.5V to ±18V (4.5V to 36V in single-supply mode). It also performs well with asymmetrical supplies such as V_{DD} = 8V and V_{SS} = –12V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to power and ground planes. Always ensure the ground (GND) connection is established before supplies are ramped.

8.4 Layout

8.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 8-2 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

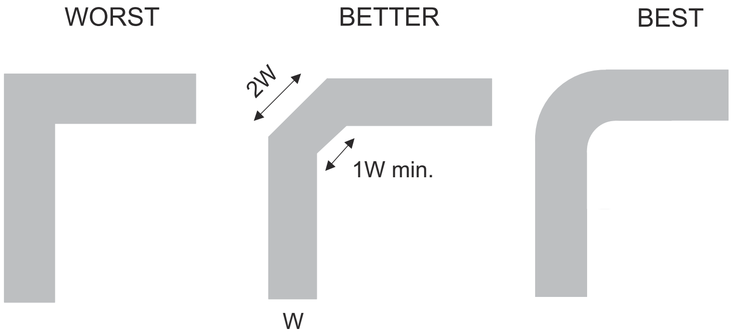


Figure 8-2. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 8-3 shows an example of a PCB layout with the TMUX6219-Q1. Some key considerations are as follows:

- Decouple the supply pins with a 0.1µF and 1µF capacitor, and place the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

8.4.2 Layout Example

Figure 8-3. TMUX6219-Q1 DGK Layout Example

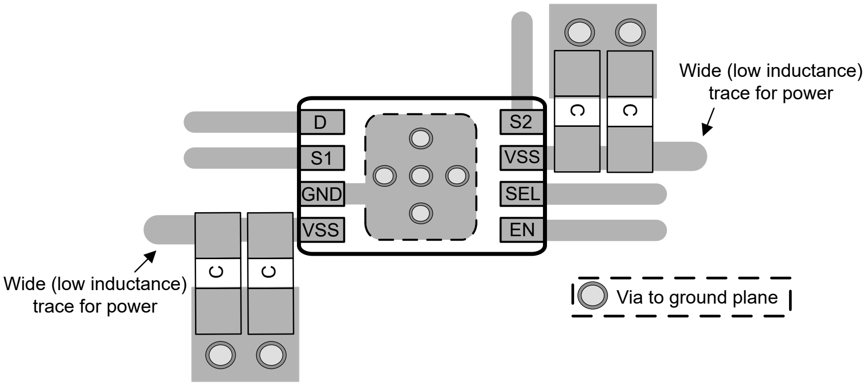


Figure 8-4. TMUX6219-Q1 RQX Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report
- Texas Instruments, *Simplifying Design with 1.8V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application report
- Texas Instruments, *TMUX6219-Q1 Functional Safety, FIT Rate, Failure Mode Distribution and Pin FMA* functional safety FIT rate, FMD and Pin-FMA

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2021) to Revision B (July 2024)	**Page**
• Updated IIH max specification	6

Changes from Revision * (January 2021) to Revision A (June 2021)	**Page**
• Changed the document status From: *Advanced Information* To: *Production Data*	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX6219DGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X219 Q	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TMUX6219-Q1 :

- Catalog : TMUX6219

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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