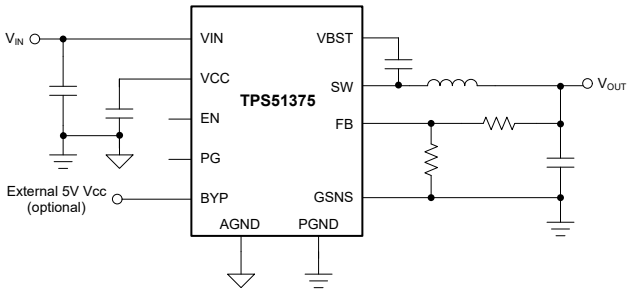
TPS51375 4.5V to 24V, 12A Continuous Current, 26A Maximum Current, Synchronous Buck Converter

1 Features

- 4.5V to 24V input voltage range
- 0.6V to 5.5V output voltage
- Integrated 10mΩ and 5mΩ FETs
- Support 12A continuous output current
- 270uA low quiescent current
- ± 1.0% reference voltage accuracy (25°C)
- D-CAP3™ control mode architecture control for fast transient response optimizing 0.77V output
- Support POSCAP and all MLCC output capacitor
- Differential remote sensing
- ULQ™ extended battery life during system standby
- Built-in output discharge function
- Integrated power-good indicator
- Fixed 600kHz switching frequency
- 26A fixed OC limit
- Fixed 1.0ms soft-start time
- Large duty cycle operation
- Cycle-by-cycle overcurrent protection
- Latched output OV and UV protections
- Non-latched UVLO and OT protections
- –40°C to 125°C operating junction temperature
- 19-pin, 3.0mm × 4.0mm, HotRod™ WQFN package
- Create a custom design using the TPS51375 with the WEBENCH® Power Designer

2 Applications

- Notebook and PC computers
- Ultrabook, handheld tablet computers
- Industrial PC, single-board computers
- Non-military drone
- Distributed power systems



Simplified Schematic

3 Description

The device is a monolithic, 12A, synchronous buck converter with integrated MOSFETs that enable high efficiency and offer ease-of-use with minimum external component count for space-conscious power systems. The TPS51375 employs D-CAP3 control mode that provides fast transient response and excellent line and load regulation with internal compensation. The ULQ extended battery life feature is extremely beneficial for long battery life in low power operation. The large duty operation greatly improves the load transient performance when input voltage is low.

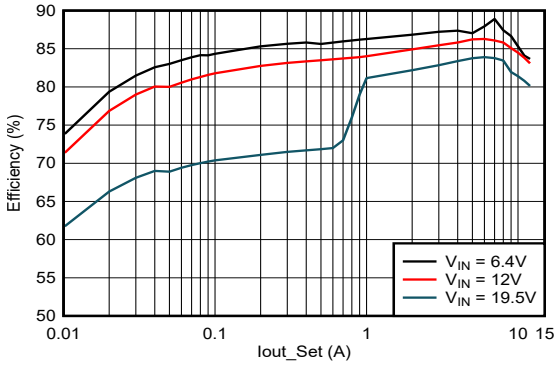
Other features include differential remote sensing, Eco-mode operation for high light load efficiency, VCC switch-over function for further optimized light load efficiency, and body braking for load transient improvement under low output voltage. TPS51375 supports VCCPRIM_VNNAON power rails in Intel Meteor Lake and Arrow Lake platform.

The TPS51375 integrates a power-good indicator and provides an output discharge function. The device provides complete protection, including OVP, UVP, OCP, OTP, and UVLO. The device is available in a 19-pin, 3.0mm × 4.0mm HotRod package, and the junction temperature is specified from –40°C to 125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS51375	VBH (WQFN-HR, 19)	4mm × 3mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Efficiency vs Output Current (V_{OUT} = 0.77V)

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4 Pin Configuration and Functions

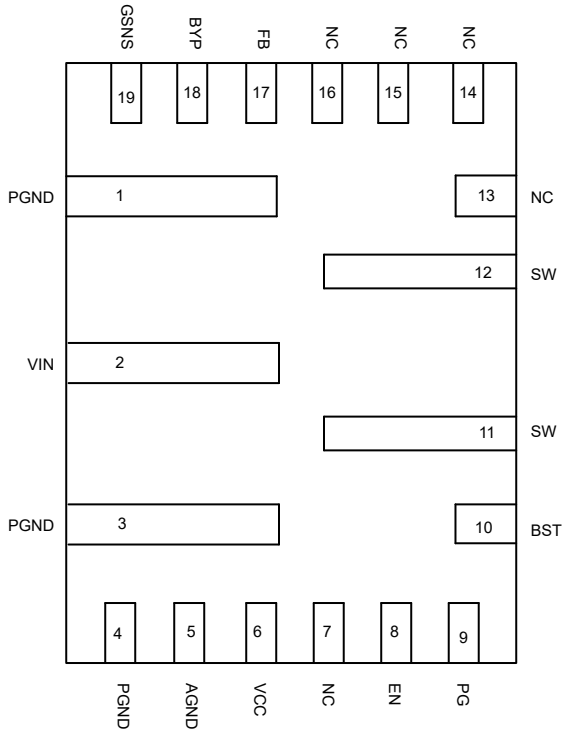


Figure 4-1. 19-Pin WQFN-HR, VBH Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
PGND	1,3,4	G	Power GND terminal for the controller circuit and the internal circuitry.
VIN	2	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
AGND	5	G	Ground of internal analog circuitry. Connect AGND to PGND at a single point close to AGND.
VCC	6	O	Internal 5V LDO output. Power supply for internal analog circuits and driving. Decouple this pin to ground with a 2.2µF ceramic capacitor.
NC	7, 13 – 16		Leave the pin floating or connect to GND.
EN	8	I	Enable input of buck converter.
PG	9	O	Power-good indicator pin. This pin asserts low if the output voltage of buck is out of range due to thermal shutdown, dropout, over-voltage, EN shutdown or during slow start.
BST	10	I	Boot-strap pin. Supply high side gate driver. Connect a 0.1µF ceramic capacitor between this pin and the SW pin.
SW	11,12	O	Switching node connection to the inductor and bootstrap capacitor for buck. This pin voltage swings from a diode voltage below the ground up to input voltage of buck.
FB	17	I	Output feedback. Connect FB to the output voltage with a feedback resistor divider.
BYP	18	I	External 5V bypass power supply input. Decouple this pin to GND with a 1uF ceramic capacitor. Leave this pin floating or connect this pin to GND if not used. This BYP external voltage must come after VIN voltage on and quit before VIN off.
GSNS	19	I	The return connection for a remote voltage sensing configuration. Short to AGND for single-end sense configuration.

(1) I = input, O = output, P = power, G = ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	28	V
	VBST	–0.3	32	V
	VBST-SW	–0.3	6	V
	EN, FB, BYP	–0.3	6	V
	PGND, AGND, GSNS	–0.3	0.3	V
Output voltage	SW	–1	28	V
	SW (10ns transient)	–3	28	V
	PG, VCC	–0.3	6	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	V

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VIN	4.5	24	V
	VBST	–0.3	29.5	V
	VBST-SW	–0.3	5.5	V
	EN, FB, BYP	–0.3	5.5	V
	PGND, AGND, GSNS	–0.3	0.3	V
Output voltage	SW	–1	24	V
	PG,VCC	–0.3	5.5	V
I_{OUT}	Continuous output current		12	A
T_J	Operating junction temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS51375 VBH (WQFN-HR) 19 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.7	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance (4-layer custom board)[2]	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) The effective $R_{\theta JA}$ is simulated based on TPS51375EVM.

5.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
VIN	Input voltage range		4.5		24	V
I_{VIN}	Non-switching supply current	No load, V_{EN} = 5V, non-switching		270		µA
I_{VINSDN}	Shutdown supply current	No load, V_{EN} = 0V		3		µA
VCC OUTPUT						
V_{CC}	VCC output voltage	V_{IN} > 5.2V, I_{VCC} ≤ 1mA, Bypasss switch off	4.6	4.9	5.2	V
FEEDBACK VOLTAGE						
V_{FB}	Feedback regulation voltage	T_J = 25°C	594	600	606	mV
		T_J = –40°C to 125°C	591	600	609	mV
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	CCM operation, TPS51375		600		kHz
$t_{ON(MIN)}$	SW minumum on time[1]			60		ns
$t_{OFF(MIN)}$	SW minimum off time[1]			130		ns
MOSFET and DRIVERS						
$R_{DS(ON)H}$	High side switch resistance	T_J = 25°C		10		mΩ
$R_{DS(ON)L}$	Low side switch resistance	T_J = 25°C		5		mΩ
OUTPUT DISCHARGE and SOFT START						
R_{DIS}	Discharge resistance	V_{EN} = 0V		50		Ω
t_{SS}	Soft-start time	Internal soft-start time		1		ms
POWER GOOD						
t_{PGDLY}	PG delay rising	PG from low to high		160		us
	PG delay falling	PG from high to low		30		us
V_{PGTH}	PG threshold	VFB falling (fault)		83		%
		VFB rising (good)		90		%
		VFB rising (fault)		120		%
		VFB falling (good)		115		%
V_{PG_L}	PG sink current capability	I_{OL} = 4mA			0.4	V
I_{PGLK}	PG leak current	V_{PGOOD} = 5.5V			1	µA
CURRENT LIMIT						

5.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V, unless otherwise noted.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
I_{OCL}	Overcurrent threshold (valley)	Valley current limit on LS FET, T_J = 25°C	22	26	30	A
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	T_J = 25°C	1			V
V_{ENL}	EN low-level input voltage	T_J = 25°C			0.4	V
I_{EN}	Enable internal pull down current	V_{EN} = 0.3V		2		µA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	OVP trip threshold			120		%
t_{OVPDLY}	OVP prop deglitch			256		us
V_{UVP}	UVP trip threshold			60		%
t_{UVPDLY}	UVP prop deglitch			200		us
UVLO						
V_{UVLO}	VIN UVLO threshold	Wake up		4.25	4.45	V
		Shutdown	3.4	3.6		V
		Hysteresis		0.65		V
OVERTEMPERATURE PROTECTION						
T_{OTP}	OTP trip threshold(1)	Shutdown temperature		160		°C
T_{OTPHSY}	OTP hysteresis(1)	Hysteresis		20		°C

(1) Specified by design. Not production tested.

5.6 Typical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12V, unless otherwise noted.

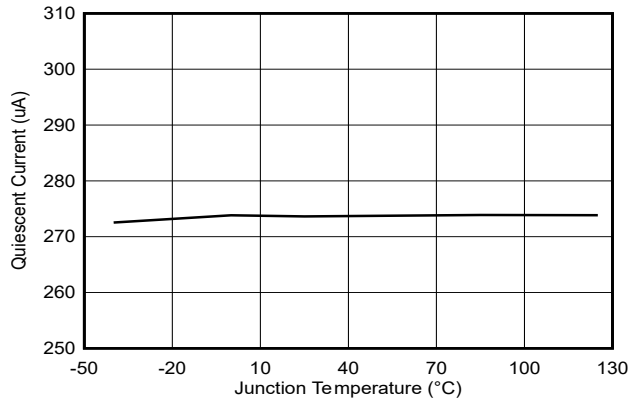


Figure 5-1. Supply Current vs Junction Temperature

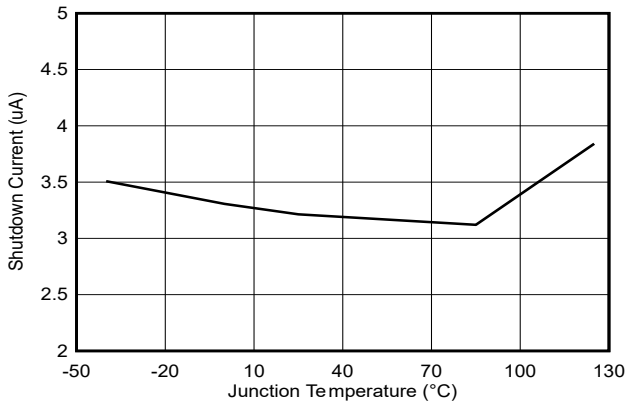


Figure 5-2. Shutdown Current vs Junction Temperature

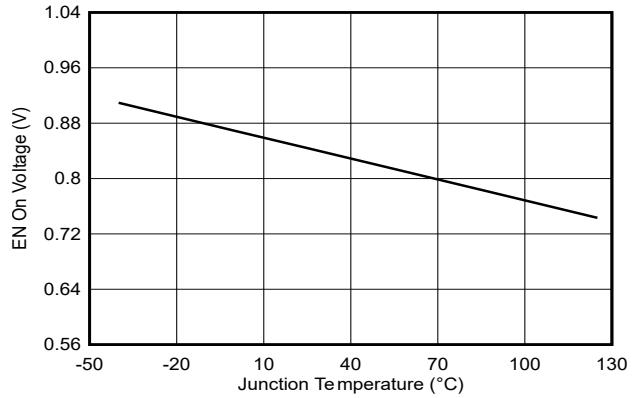


Figure 5-3. Enable On Voltage vs Junction Temperature

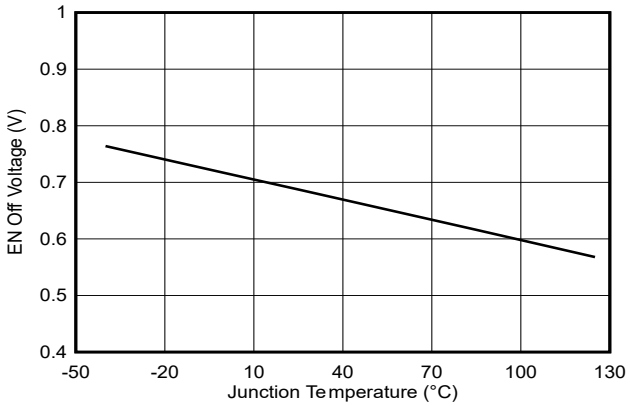


Figure 5-4. Enable Off Voltage vs Junction Temperature

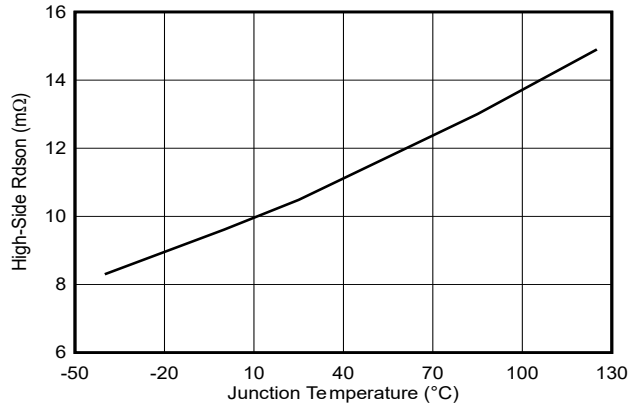


Figure 5-5. High-Side $R_{DS(on)}$ vs Junction Temperature

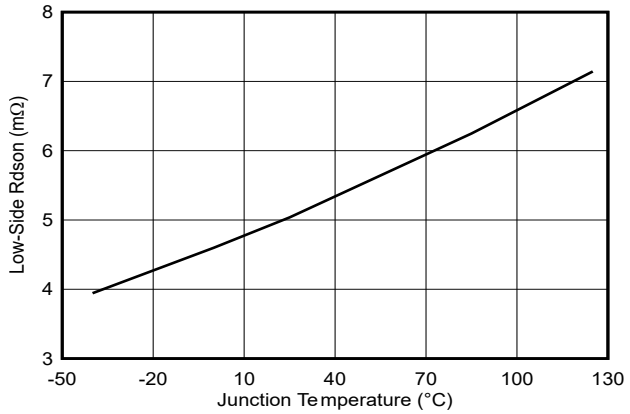


Figure 5-6. Low-Side $R_{DS(on)}$ vs Junction Temperature

5.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V, unless otherwise noted.

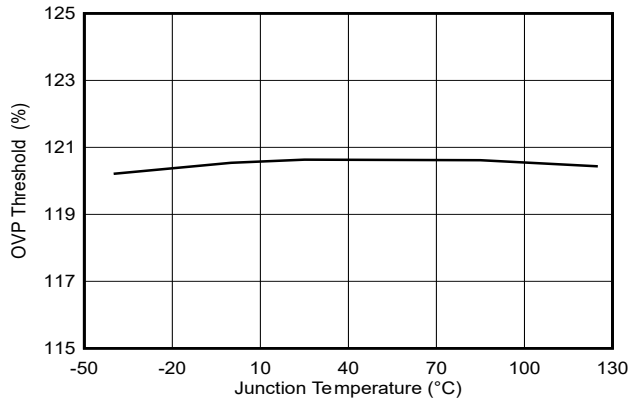


Figure 5-7. OVP Threshold vs Junction Temperature

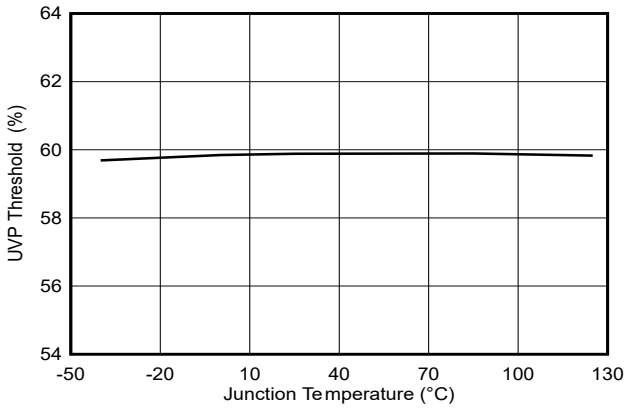


Figure 5-8. UVP Threshold vs Junction Temperature

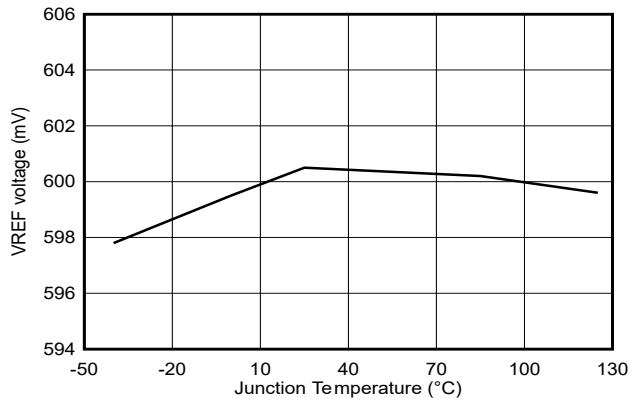


Figure 5-9. VREF Voltage vs Junction Temperature

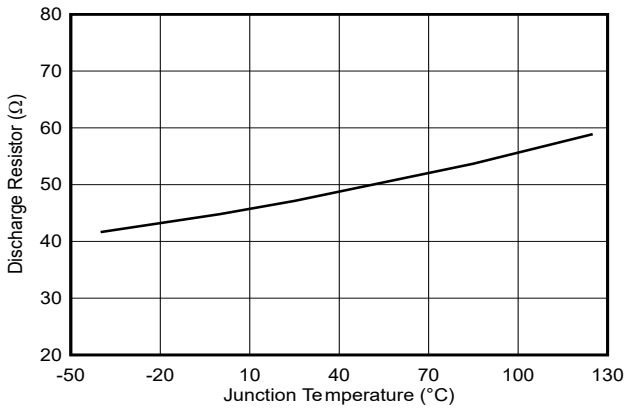


Figure 5-10. Discharge Resistor vs Junction Temperature

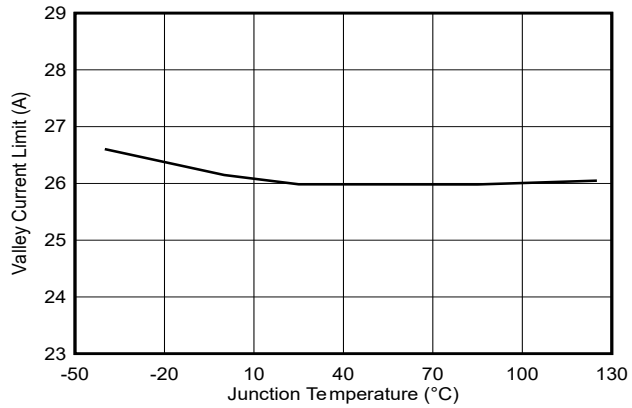


Figure 5-11. Valley Current Limit vs Junction Temperature

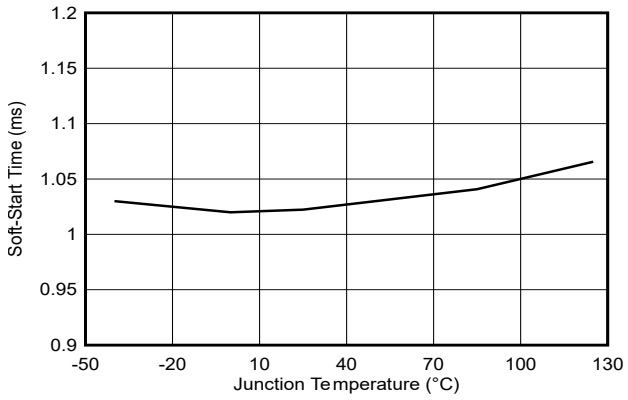


Figure 5-12. Soft-Start Time vs Junction Temperature

5.6 Typical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12V, unless otherwise noted.

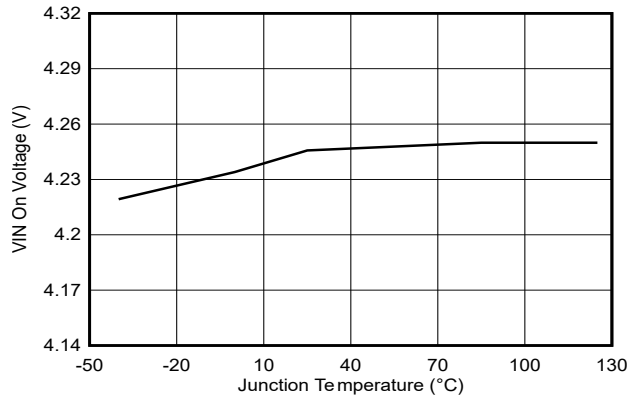


Figure 5-13. VIN UVLO Rising vs Junction Temperature

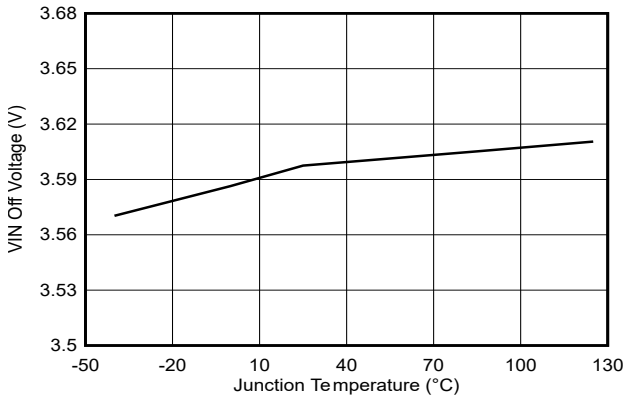


Figure 5-14. VIN UVLO Falling vs Junction Temperature

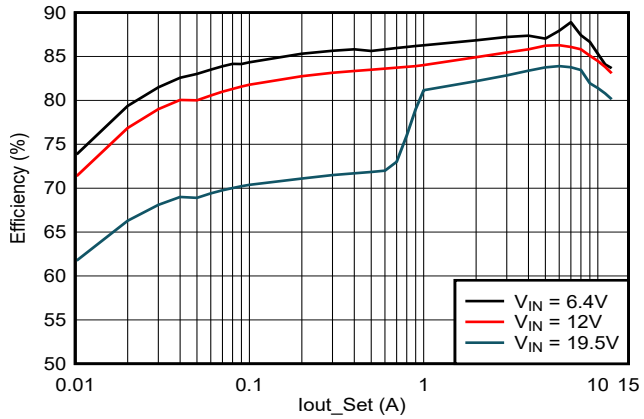


Figure 5-15. Efficiency vs Load Current, F_{SW} = 600kHz, V_{OUT} = 0.77V

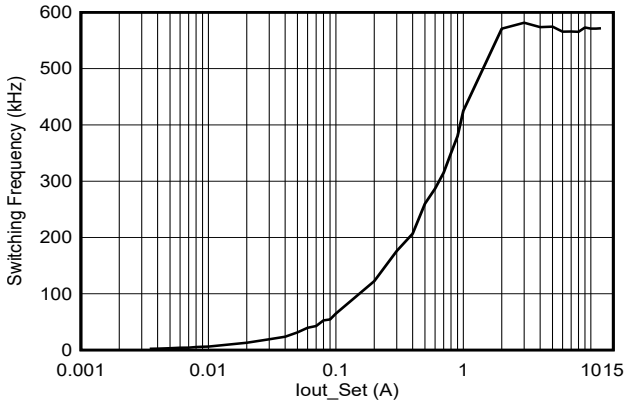


Figure 5-16. Switching Frequency vs Load Current, F_{SW} = 600kHz

6 Detailed Description

6.1 Overview

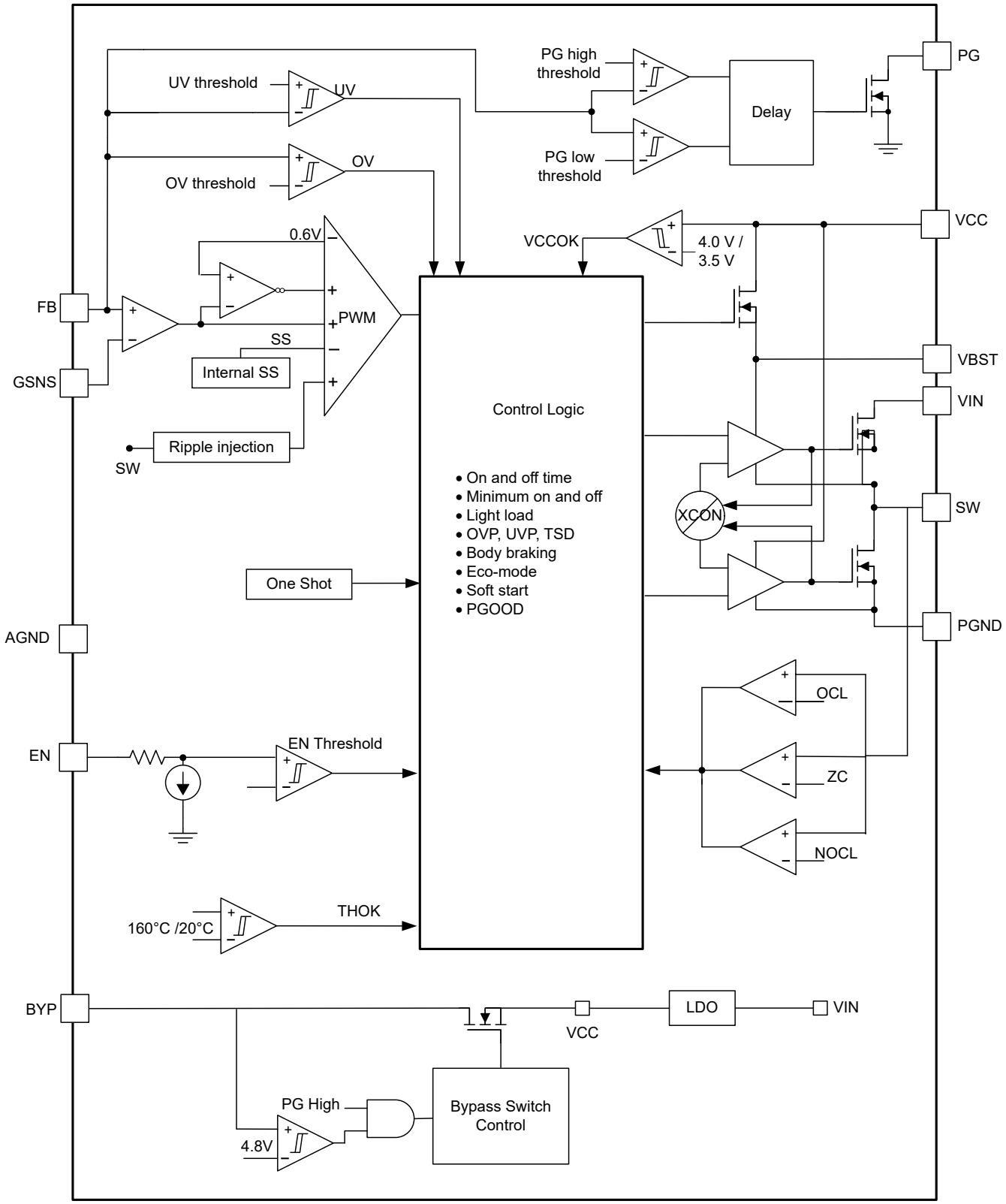
TPS51375 is 12A, peak 26A, integrated FETs, synchronous step-down converters which can operate from 4.5V to 24V input voltage (VIN), and the output voltage is from 0.6V to 5.5V. The device has 10mΩ and 5mΩ integrated MOSFETs that enable high efficiency up to 12A. The device employs D-CAP3 control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM, Eco-mode operation at lighter load condition. DCM, Eco-mode allows the TPS51375 to maintain high efficiency at light load. D-CAP3 control mode allows the use of low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

TPS51375 has 5V internal VCC LDO that creates bias for all internal circuitry. The undervoltage lockout (UVLO) circuit monitors the VCC pin voltage to protect the internal circuitry from low input voltages. External 5V bypass power supply can be used to improve efficiency. TPS51375 has an internal pulldown current source on the EN pin, require external pullup circuit to enable buck converter.

TPS51375 supports 600kHz switching frequency. The internal soft-start time is fixed 1ms to simplify the design circuit and reduce the external components.

TPS51375 can support VCCPRIM_VNNAON power rails in Intel Meteor Lake and Arrow Lake platform.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 PWM Operation and D-CAP3™ Control Mode

The main control loop of the buck is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP3 control mode. The D-CAP3 control mode combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. The D-CAP3 control mode is stable even with virtually no ripple at the output. The TPS51375 also includes an error amplifier that makes the output voltage high accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one-shot timer expires. This one-shot duration is set proportional to the converter input voltage, V_{IN}, and is inversely proportional to the output voltage, V_{OUT}, to maintain a pseudo-fixed frequency over the input voltage range, hence called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ripple generation circuit is added to the reference voltage to emulate the output ripple. This action enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode.

For any control topology that is compensated internally, there is a range of the output filter the control topology can support. The output filter used with the TPS51375 is a low-pass L-C circuit. This L-C filter has a double-pole frequency calculated in Equation 1.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the external output set-point resistor divider network and the internal gain of the TPS51375. The low-frequency L-C double pole has a 180 degree lag in-phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a mid-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency. The inductor and capacitor selected for the output filter must be such that the double pole is placed close enough to the mid-frequency zero so that the phase boost provided by this mid-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system must usually be targeted to be less than one-third of the switching frequency (F_{SW}).

6.3.2 Remote Sense

The TPS51375 device offers remote sense function through the FB and GSNS pins. Remote sense function compensates a potential voltage drop on the PCB traces, thus helps maintain VOUT tolerance under steady state operation and load transient event. Connecting the FB voltage divider resistors to the remote location allows sensing the output voltage at a remote location. The connections from the FB voltage divider resistors to the remote location must be a pair of PCB traces with at least 12-mil trace width, and must implement Kelvin sensing across a high bypass capacitor of 0.1µF or higher. The ground connection of the remote sensing signal must be connected to the GSNS pin. The VOUT connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor, RFB_LS, terminated at the GSNS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources, such as inductor and SW nodes, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below. Single-ended Vo sensing is often used for local sensing. For this configuration, connect the higher FB resistor, RFB_HS, to a high-frequency local bypass capacitor of 0.1µF or higher, and short GSNS to AGND.

6.3.3 Body Braking

During load step down, the converter senses the amplitude of the output voltage change. If the output voltage change is big enough, TPS51375 implements a body braking function that turns off both high-side and low-side FET and allows power to dissipate through the low-side body diode, reducing overshoot. This approach is very effective, while having some impact on efficiency during transient.

6.3.4 5V LDO and BYP Function

The VCC pin is the output of the internal 5V linear regulator that creates the bias for all the internal circuitry and MOSFET gate drivers. The VCC pin must be bypassed with a 2.2µF capacitor. The UVLO circuit monitors the VCC pin voltage and disables the output when VCC falls below the UVLO threshold.

An external voltage that is connected to the BYP pin can override the internal LDO, switching to the external rail after a higher voltage is detected. This action enhances the efficiency of the converter because the quiescent current now runs off this external rail instead of the input power supply. This BYP external voltage must come after VIN voltage on and quit before VIN off.

The devices is integrated with a VCC switchover function which supports connecting the BYP pin to VOUT directly if the VOUT is set to higher than 4.8V. The VCC switchover function is designed to bypass internal 5V LDO with the power from VOUT. The VCC switchover is a seamless behavior of regulator and does not need any additional configuration.

The VCC pin switchover function is asserted when three conditions are present:

- PGOOD is not pulled low
- VOUT voltage is higher than 4.8V
- BYP pin is short to VOUT.

In this switchover condition, one thing occurs: the VCC output is connected to VOUT by internal switchover MOSFET.

6.3.5 Soft Start

The TPS51375 has an internal 1ms soft start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is prebiased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme makes sure that the converters ramp up smoothly into regulation point.

6.3.6 Large Duty Operation

The TPS51375 can support large duty operation by the internal T_{ON} extension function. When V_{IN}/V_{OUT} < 1.18 and the V_{FB} keeps lower than internal V_{REF}, the switching frequency is allowed to smoothly drop to make T_{ON} extended to implement the large duty operation and also improve the performance of the load transient performance. The TPS51375 can support up to 98% duty cycle operation.

6.3.7 Power Good

The Power-Good (PGOOD) pin is an open-drain output. TI recommends a pullup resistor of 100kΩ to pull the voltage up to VCC. After V_{FB} is between 90% and 115% of the target output voltage, the PGOOD is pulled high after a 200us deglitch time. The PGOOD pin is pulled low when:

- FB pin voltage is lower than 83% or greater than 120% of the target output voltage
- In OVP, UVP, or thermal shutdown event
- During the soft-start period

6.3.8 Overcurrent Protection and Undervoltage Protection

The TPS51375 has overcurrent protection and undervoltage protection. The output overcurrent protection (OCP) is implemented using a cycle-by-cycle low-side MOSFET valley current detection. The switching current is monitored by measuring the MOSFET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. When the load current is higher than the $I_{OCL(VALLEY)}$ added by one half of the peak-to-peak inductor ripple current, the OCP is triggered and the output current is being limited, the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects the fall, and the device is shut off after a wait time of 200µs. This protection is a latched function. The fault latching can be reset by EN going low or VCC power cycling.

6.3.9 Overvoltage Protection

The TPS51375 has an overvoltage protection feature. When the output voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high, and the output discharges and latches after a wait time of 256µs. This function is a latching operation, so this function must reset by EN going low or VIN power cycling.

6.3.10 UVLO Protection

The VIN undervoltage lockout (UVLO) protection monitors the VIN pin voltage to protect the internal circuitry from low input voltage. When the VIN voltage is lower than the UVLO threshold voltage, the device shuts off and outputs are discharged to prevent misoperation of the device. The converter begins operation again when the input voltage exceeds the threshold by a hysteresis of 650mV (typical). This protection is a non-latch protection.

6.3.11 Output Voltage Discharge

TPS51375 has a 50ohm discharge switch that discharges the output VOUT through the Vout pin during any event of fault like output overvoltage, output undervoltage, thermal shutdown, or if the VIN voltage is below the UVLO and when the EN pin voltage is below the turn-on threshold.

6.3.12 Standby Operation

The TPS51375 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 3µA when in standby condition. EN pin is pulled low internally. When floating, the part is disabled by default.

6.3.13 Thermal Shutdown

The TPS51375 monitors the internal die temperature. If the temperature exceeds the threshold value (typically 160°C), the device is shut off and the output is discharged. This protection is a non-latch protection. The device restarts operation when the temperature goes below the thermal shutdown threshold.

6.4 Device Functional Modes

6.4.1 Advanced Eco-mode Control

The advanced Eco-mode control schemes to maintain high light load efficiency. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as in continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes longer. This action makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use Equation 2 to calculate the light load current where the transition to Eco-mode operation happens ($I_{OUT(LL)}$).

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance (L_{OUT}) so that the inductor peak-to-peak ripple current is approximately between 20% and 40% of $I_{OUT(max)}$ (peak current in the application). Sizing the inductor properly so that the valley current does not hit the negative low-side current limit is important.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The schematic in Figure 7-1 shows a typical application for TPS51375 with 0.77V output. This design converts an input voltage range of 4.5V to 24V down to 0.77V with a maximum continuous output current of 12A.

7.2 Typical Application

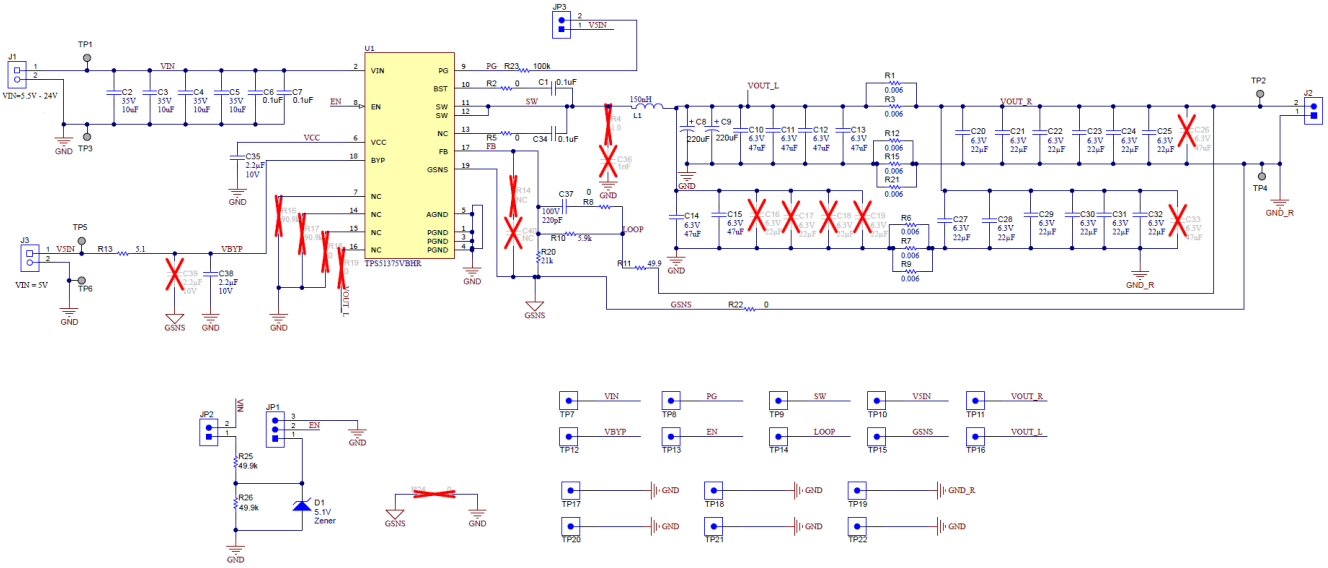


Figure 7-1. VCCPRIM_VNNAON 0.77V, 12A Continuous Current Reference Design

7.2.1 Design Requirements

Table 7-1 lists the design parameters for this example.

Table 7-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	Output voltage			0.77		V
I_{OUT}	Output current			12		A
V_{IN}	Input voltage		4.5	19.5	24	V
$V_{OUT(ripple)}$	Output voltage ripple	0A – 12A loading		10		mV_{P-P}
$V_{OUT(min)}$	Minimum output voltage	0A – 10A loading, 10A/us	720			mV
$V_{OUT(max)}$	Maximum output voltage	7A – 17A loading, 10A/us			827.5	mV
F_{SW}	Switching frequency			600		kHz
R_{PATH_VOUT}	VOUT path parasitic resistance			3		mΩ
R_{PATH_GND}	GND path parasitic resistance			1.5		mΩ
T_A	Ambient temperature			25		°C

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS51375 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 External Component Selection

7.2.2.2.1 Remote Sense Amplifier and Adjusting the Output Voltage

Remote sensing of the output voltage is provided through a dedicated high speed, low offset instrumentation type amplifier. Connect the output voltage setting resistive divider described below from the output voltage sensing point to the GSNS pin. The center point is to be connected to the FB pin. Note the GSNS pin is to be tied to the converter output voltage return at a location near to the load. The output voltage is programmed with a resistor divider from the converter output (V_{OUT}) to the FB pin as shown in Figure 7-2. Use 1% tolerance or better divider resistors.

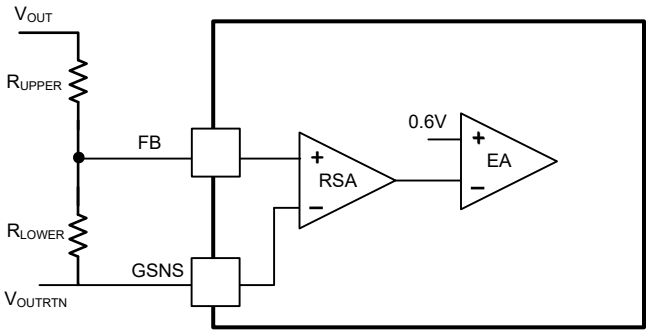


Figure 7-2. FB Resistor Divider With Remote Sense

To change the output voltage of the application, change the value of the upper feedback resistor. By changing this resistor, the user can change the output voltage above 0.6V. See Equation 3.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{UPPER}}{R_{LOWER}}\right) \quad (3)$$

7.2.2.2.2 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See Table 7-3 for recommended inductor values.

Use Equation 4 and Equation 5 to calculate the RMS and peak currents through the inductor. Make sure that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{I^2_{OUT} + \frac{1}{12} \times \left[\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}}\right]^2} \quad (4)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (5)$$

Under transient and short-circuit conditions, the inductor current can increase up to the current limit of the device. Choosing an inductor with a saturation current higher than the peak current under current limit condition is safe.

7.2.2.2.3 Output Capacitor Selection

After selecting the inductor, the output capacitor must be optimized. In D-CAP3 control mode, the regulator reacts within one cycle to the change in the duty cycle, so good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in Table 7-2 and Table 7-3. Ceramic capacitors have very low ESR making ESR ripple negligible, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$.

Table 7-2. Recommended Component Values for VCCPRIM_VNNAON

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	R_{FF} (kΩ)	C_{FF} (pF)
0.77	21	5.9	0.15	500	1000	NA	220

Table 7-3. Recommended Component Values for General Purpose Application

V_{OUT} (V)	F_{sw} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	R_{FF} (kΩ)	C_{FF} (pF)
3.3	600	1.5	88	198	NA	30
5.0	600	1.5	88	198	NA	30

7.2.2.2.4 Input Capacitor Selection

The TPS51375 requires input decoupling capacitors on power supply input pin VIN, and the bulk capacitors are needed depending on the application. Use Equation 6 to calculate the minimum input capacitance required.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{IN(ripple)} \times V_{IN} \times F_{SW}} \quad (6)$$

TI recommends using a high-quality X5R or X7R input decoupling capacitors of nominal 44µF/35V on the input voltage pin VIN. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. Use Equation 7 to calculate the input ripple current:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \quad (7)$$

7.2.2.2.5 Bootstrap Capacitor Selection

A 0.1µF ceramic capacitor must be connected between the BST and SW pins for proper operation. The capacitor must be rated for at least 10V to minimize DC bias derating.

A resistor can be added in series with the BST capacitor to slow down the turn-on of the high-side MOSFET and reduce overshoot rising edge overshoot on the SW pin. This action comes with the tradeoff of more power loss and lower efficiency. As a best practice, include a 0Ω placeholder in prototype designs in case parasitic inductance in the PCB layout results in more voltage overshoot at the SW pin than is normal. This practice helps keep the voltage within the ratings of the device and reduces the high frequency noise on the SW node.

7.2.3 Application Curves

Figure 7-3 through Figure 7-18 apply to the circuit of Figure 7-1. V_{IN} = 12V, F_{SW} = 600kHz, T_A = 25°C, unless otherwise specified.

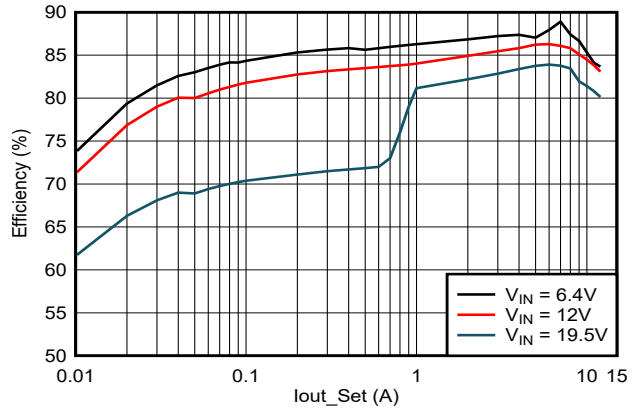


Figure 7-3. Efficiency Curve(V_{OUT} = 0.77V)

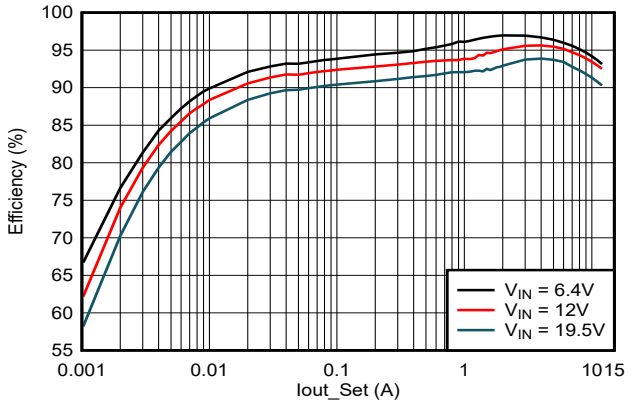


Figure 7-4. Efficiency Curve(V_{OUT} = 3.3V)

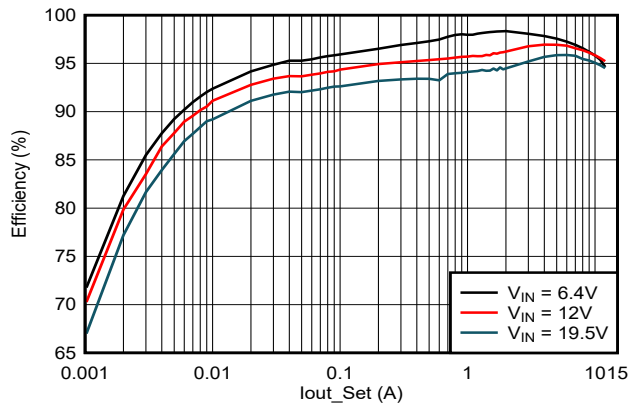


Figure 7-5. Efficiency Curve(V_{OUT} = 5V)

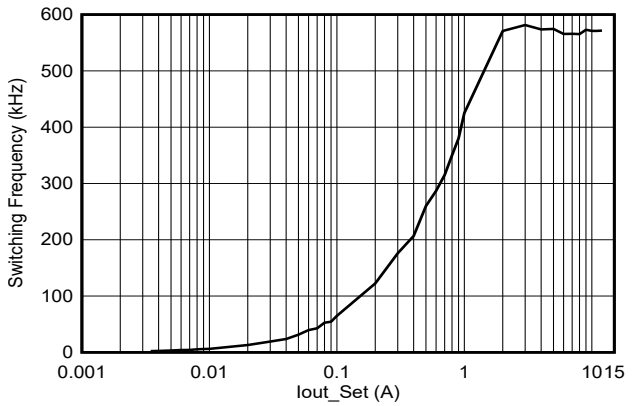


Figure 7-6. Switching Frequency vs Output Load

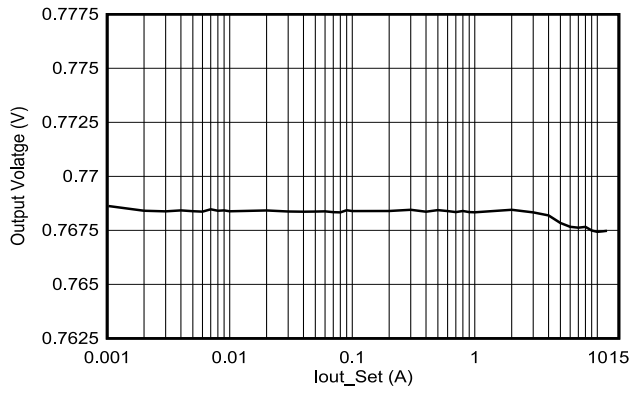


Figure 7-7. Load Regulation, V_{IN} = 12V

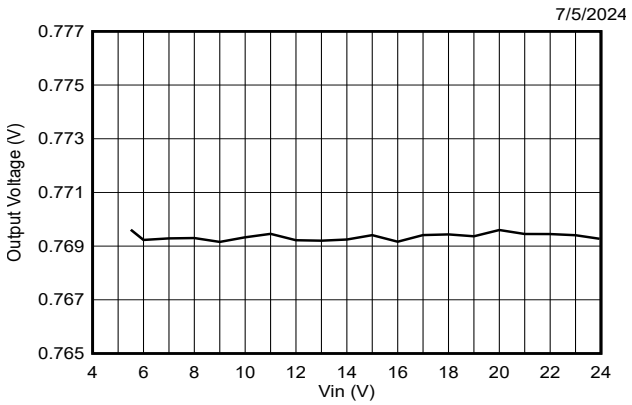


Figure 7-8. Line Regulation, I_{OUT} = 12A

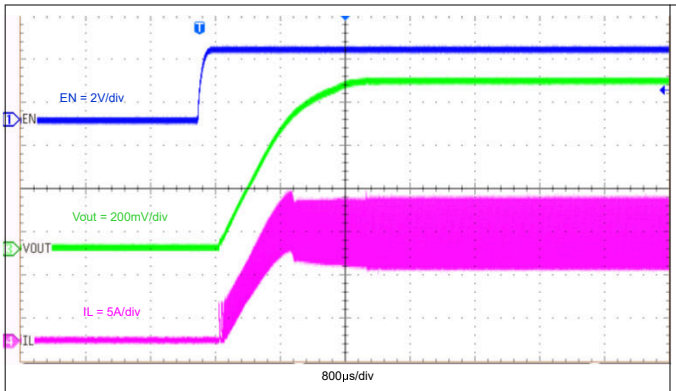


Figure 7-9. Start-Up Through EN, I_{OUT} = 12A

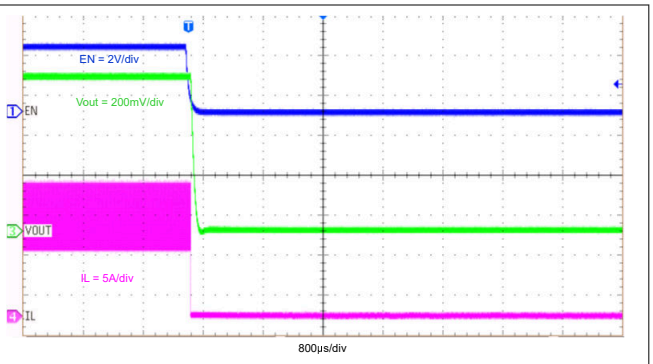


Figure 7-10. Shutdown Through EN, I_{OUT} = 12A

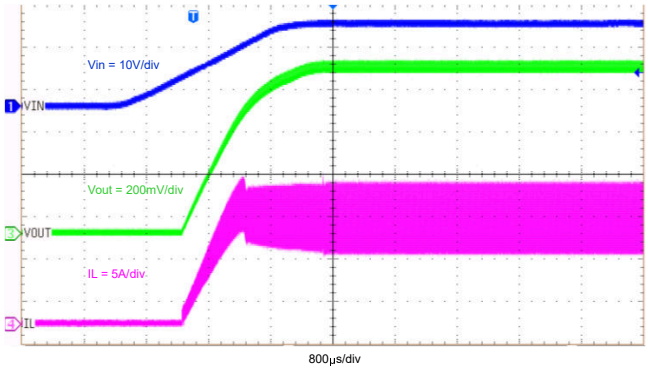


Figure 7-11. Start-Up Relative to VIN Rising, I_{OUT} = 12A

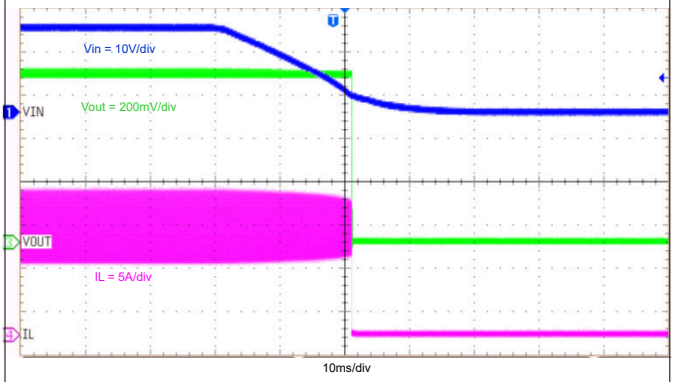


Figure 7-12. Shutdown Relative to VIN Falling, I_{OUT} = 12A

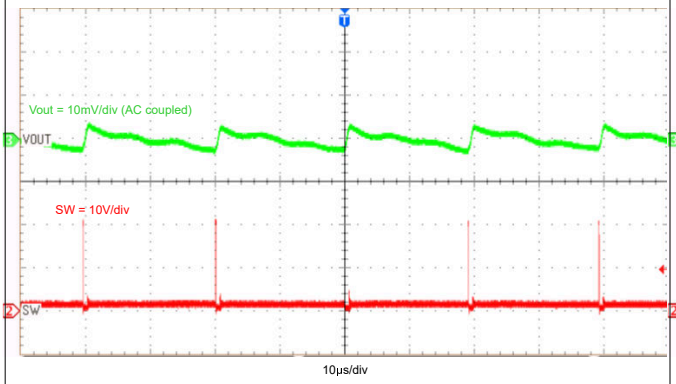


Figure 7-13. Output Voltage Ripple, I_{OUT} = 0.1A

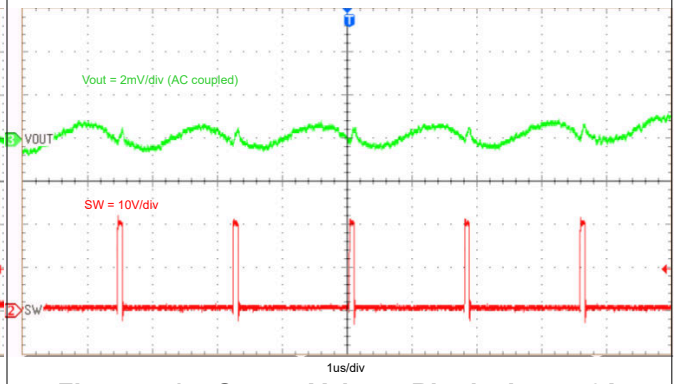


Figure 7-14. Output Voltage Ripple, I_{OUT} = 6A

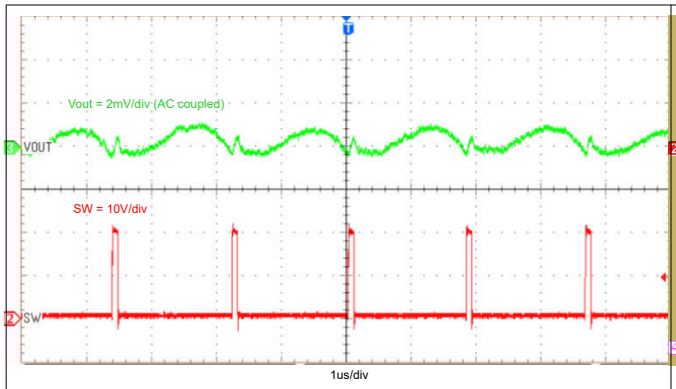


Figure 7-15. Output Voltage Ripple, I_{OUT} = 12A

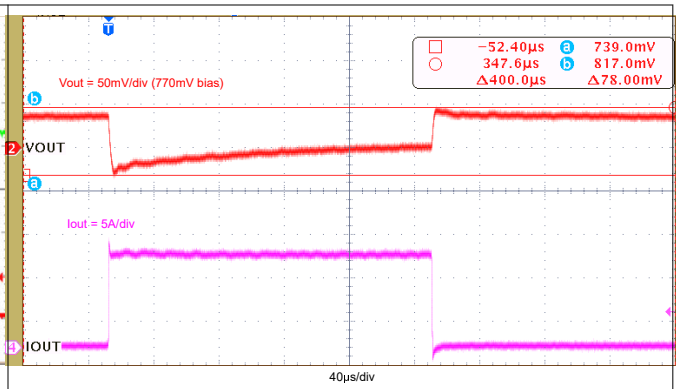


Figure 7-16. Transient Response, 0A to 10A, Slew Rate = 10A/µs

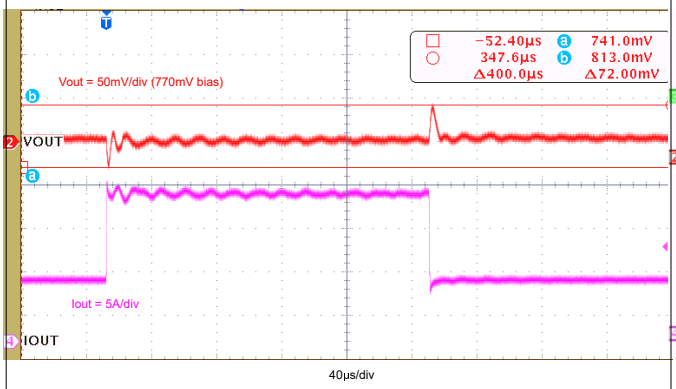


Figure 7-17. Transient Response, 7A to 17A, Slew Rate = 10A/µs

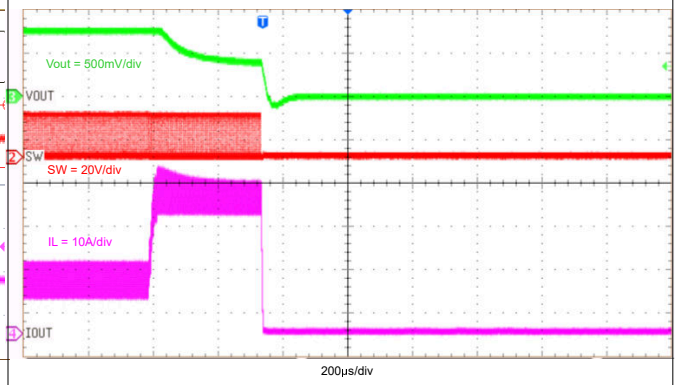


Figure 7-18. Normal Operation to Output Hard Short

7.3 Power Supply Recommendations

The TPS51375 is intended to be powered by a well-regulated DC voltage. The input voltage range is 4.5V to 24V. The TPS51375 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far away from the TPS51375 circuit, TI recommends some additional input bulk capacitance. Typical values are 100µF to 470µF.

7.4 Layout

7.4.1 Layout Guidelines

- Make note that the PCB layout of any DC/DC converter is critical to the excellent performance of the design. Bad PCB layout can disrupt the operation of a good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitors and power ground. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this fact, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance.
- Use a four-layer PCB for good thermal performance and with maximum ground plane. 3-inch × 2.75-inch, top and bottom layer PCB with 2oz copper is used as example.
- Place the decoupling capacitors right across VIN and VCC as close as possible.
- Place output inductors and capacitors with IC at the same layer. The SW routing must be as short as possible to minimize EMI, and must be a width plane to carry big current. Enough vias must be added to the PGND connection of output capacitors and also as close to the output pin as possible.
- Place BST resistor and capacitor with IC at the same layer, close to BST and SW plane. TI recommends > 10-mil width trace to reduce line parasitic inductance.
- Make feedback 10 mil and routed away from the switching node, BST node, or other high speed digital signal.
- Make VIN trace wide to reduce the trace impedance and provide enough current capability.
- Place multiple vias under the device near VIN and PGND and near input capacitors to reduce parasitic inductance and improve thermal performance.

7.4.2 Layout Example

Figure 7-19 shows the recommended top-side layout. Component reference designators are the same as the circuit shown in *TPS51375 Step-Down Converter Evaluation Module* EVM user's guide.

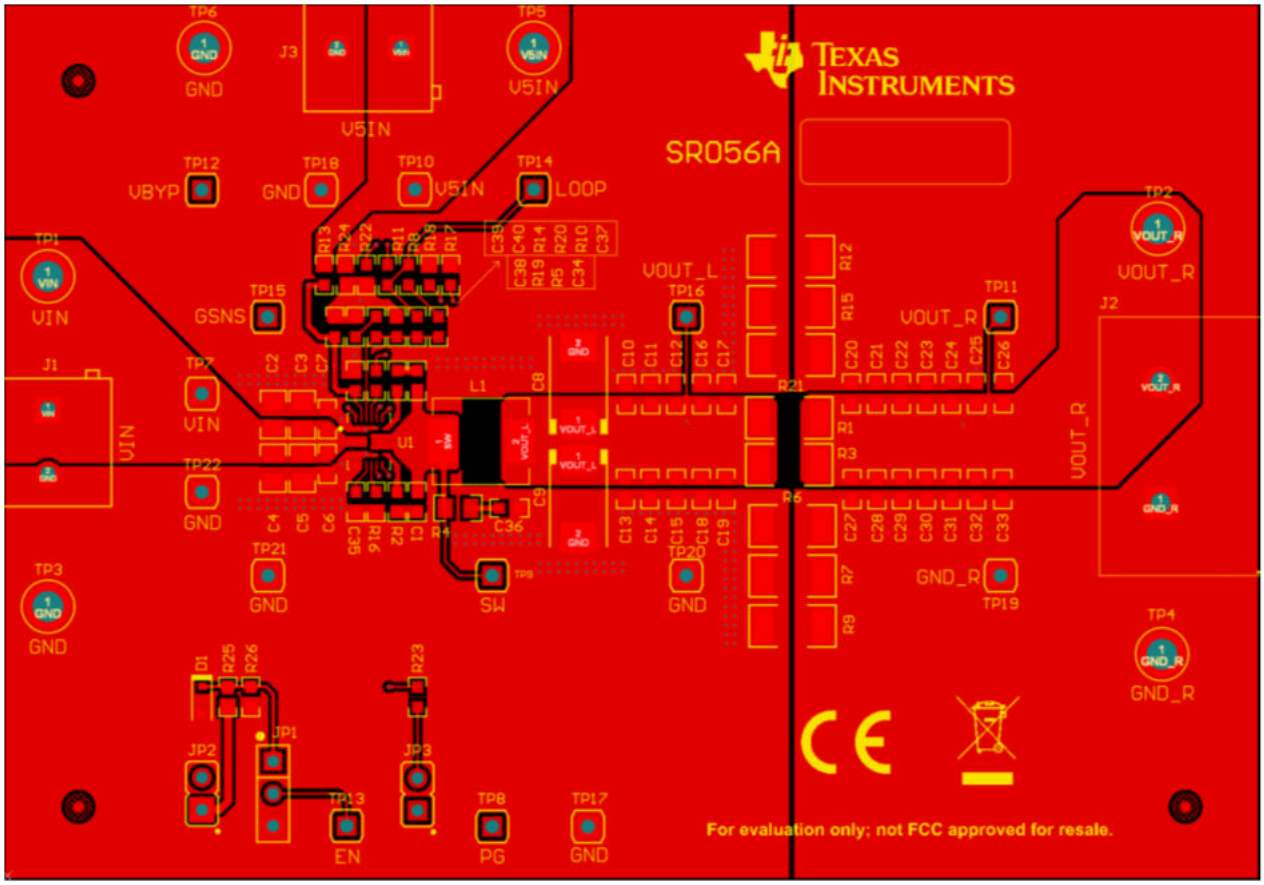


Figure 7-19. Top-Side Layout

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS51375 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
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- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

Texas Instruments, *TPS51375 Step-Down Converter Evaluation Module* EVM user's guide

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

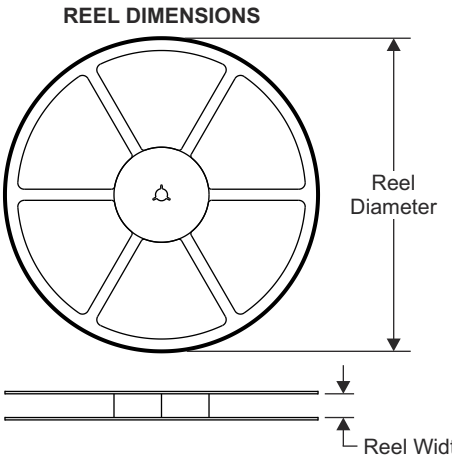
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

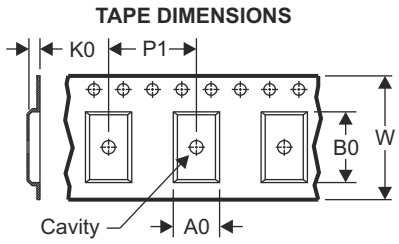
Changes from Revision * (July 2024) to Revision A (August 2024)	Page
• Changed document status from Advance Information to Production Data	1

10 Mechanical, Packaging, and Orderable Information

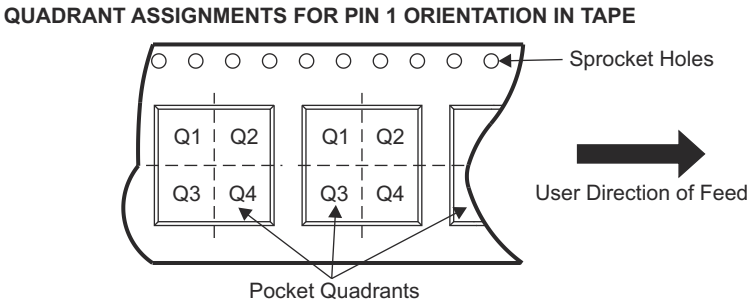
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information



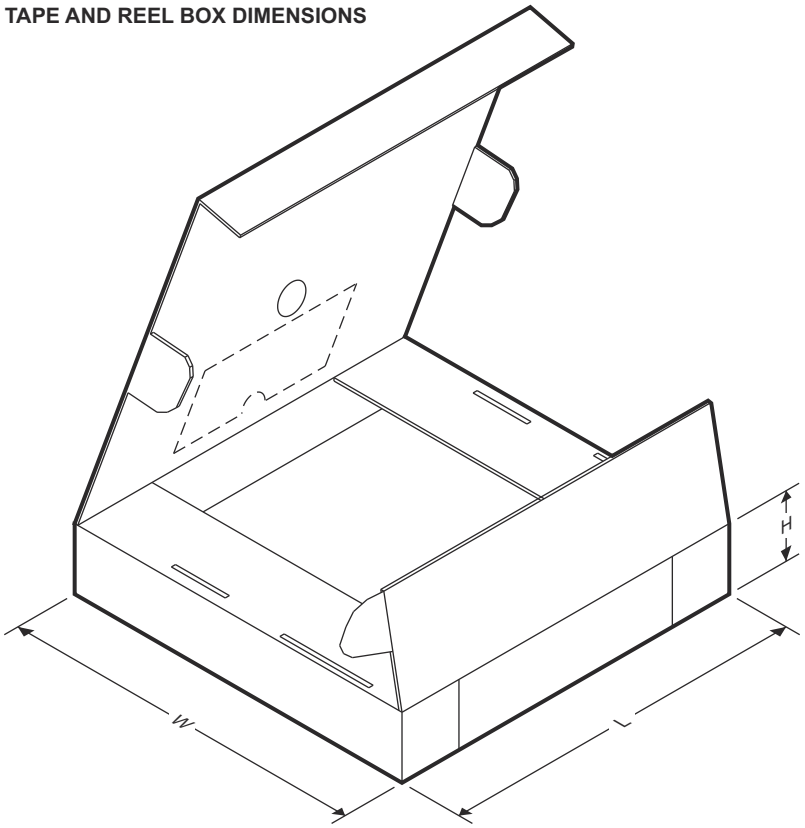


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51375VBHR	WQFN-HR	VBH	19	4000	330	12.4	3.3	4.3	0.85	8	12	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51375VBHR	WQFN-HR	VBH	19	4000	367	367	35

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51375VBHR	ACTIVE	WQFN-FCRLF	VBH	19	4000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	51375	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

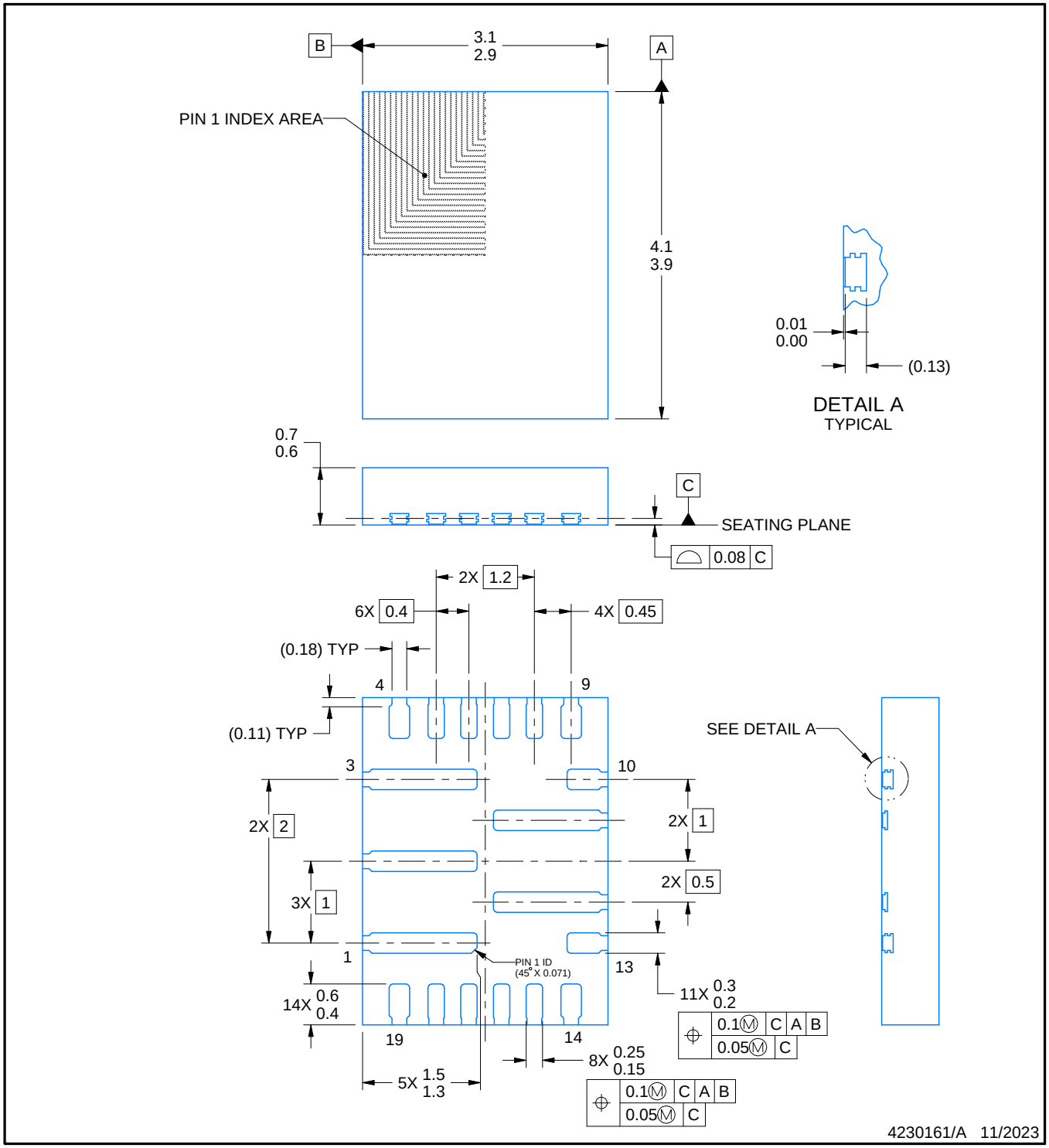
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

VBH0019A

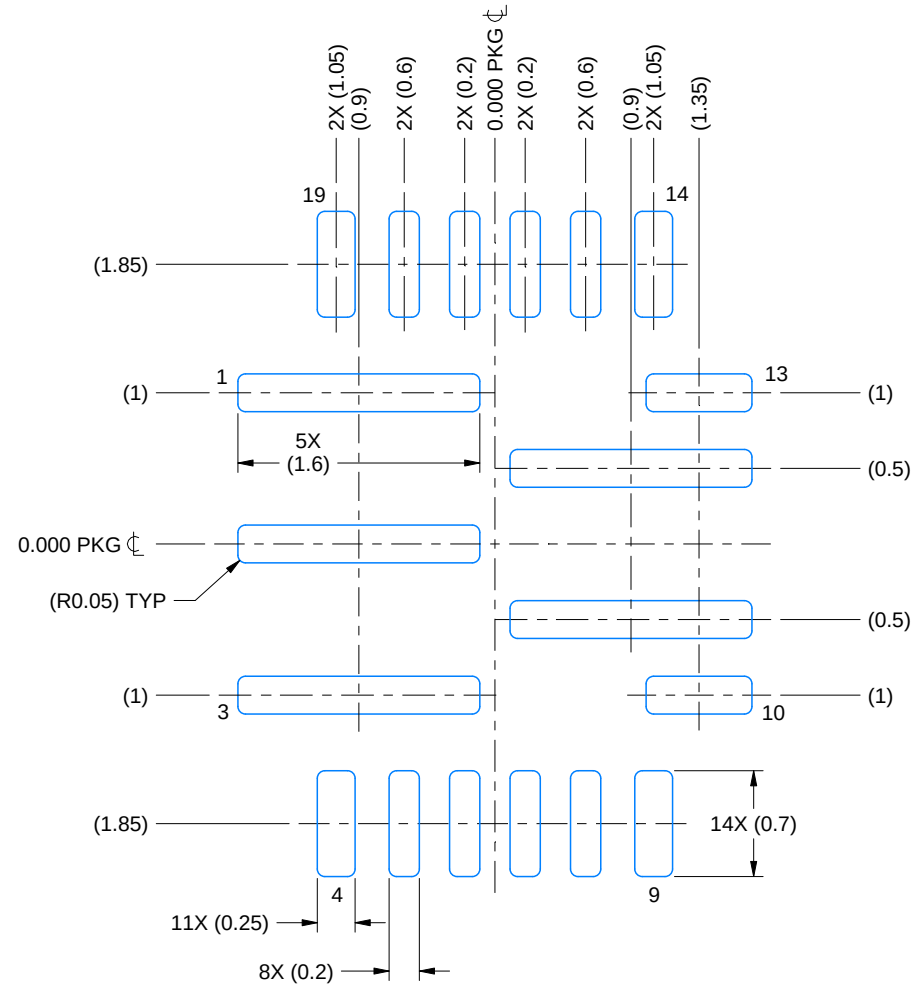
WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

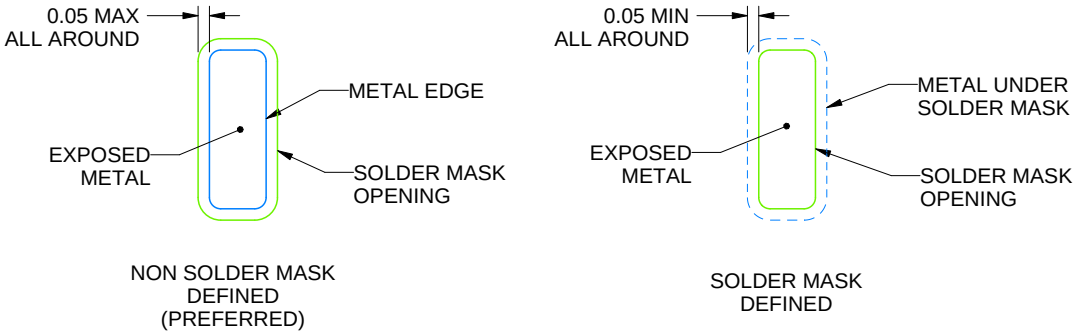


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

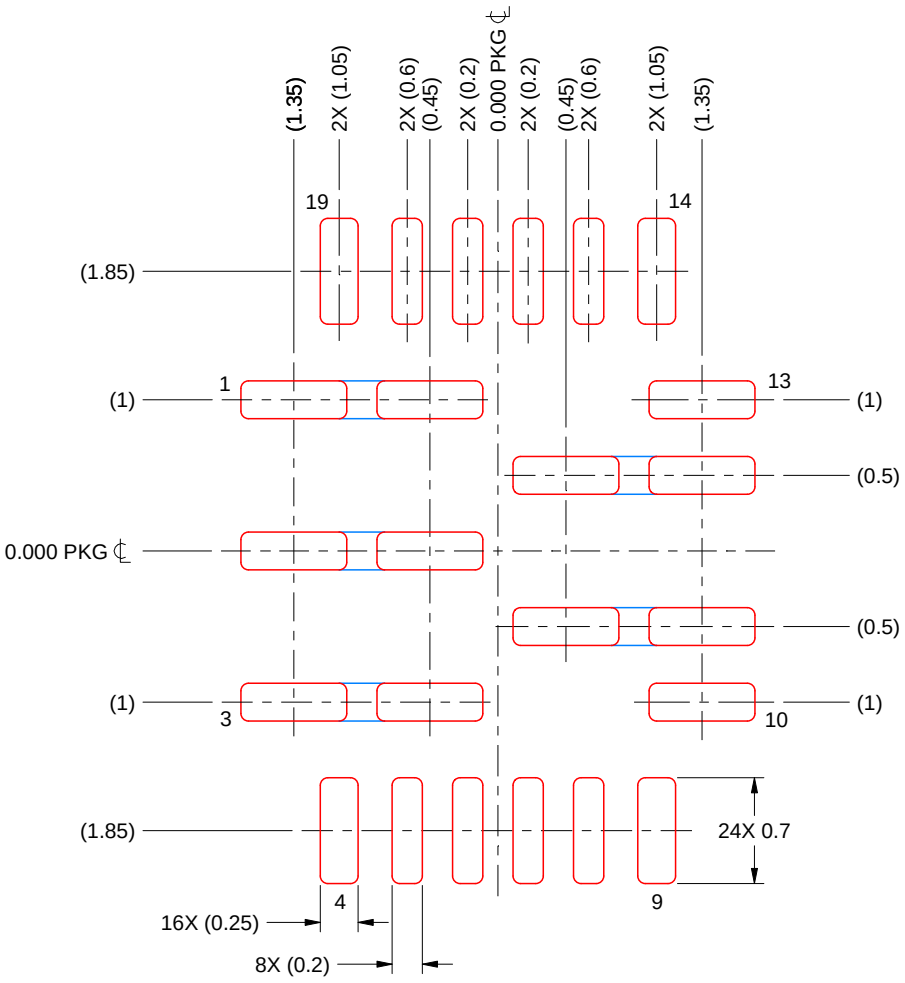
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VBH0019A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 20X

PRINTED SOLDER PASTE BY AREA UNDER PACKAGE
PINS 1, 2, 3, 11 & 12: 88%

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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