TPS53313 6-A Step-Down Regulator With Integrated Switcher

1 Features

- 4.5-V to 16-V Conversion Voltage Range
- Adjustable Output Voltage Ranging from 0.6 V to 0.7 × V_{IN}
- Continuous 6-A Output Current
- Supports All MLCC Output Capacitors
- Selectable SKIP Mode or Forced CCM
- Selectable Soft-Start Time (1 ms, 3 ms, or 6 ms)
- Selectable 4-5 A, 6-A or 9-A Peak Current Limit
- Optimized Efficiency at Light and Heavy Loads
- Voltage Mode Control
- Programmable Switching Frequency from 250 kHz to 1.5 MHz
- Synchronizes to External Clock
- $R_{DS(on)}$ Sensing for Zero Crossing Detection and Overcurrent Protection
- Soft-Stop Output Discharge During Disable
- Overcurrent, Overvoltage, and Undervoltage Protection With Hiccup
- Overtemperature Protection
- Open-Drain, Power Good Indication
- Internal Bootstrap Switch
- 4 mm × 4 mm, 24-Pin VQFN Package

2 Applications

- POL Applications for 5-V
- 12-V Step-Down Rails

3 Description

TPS53313 provides a 5-V or 12-V synchronous buck converter that integrates two N-Channel MOSFETs. Due to low $R_{DS(on)}$ and TI proprietary SmoothPWM™ skip mode of operation, it optimizes the efficiency at light-load condition without compromising the output voltage ripple.

The TPS53313 features programmable (from 250 kHz to 1.5 MHz) switching frequency with selectable skip mode or forced CCM mode operation. The device provides prebiased startup, soft-stop, integrated bootstrap switch, power good function, and EN/input UVLO protection. It supports input voltages from 4.5 V to 16 V and no extra bias voltage is needed. The output voltage is adjustable from 0.6 V up to 0.7 × V_{IN}.

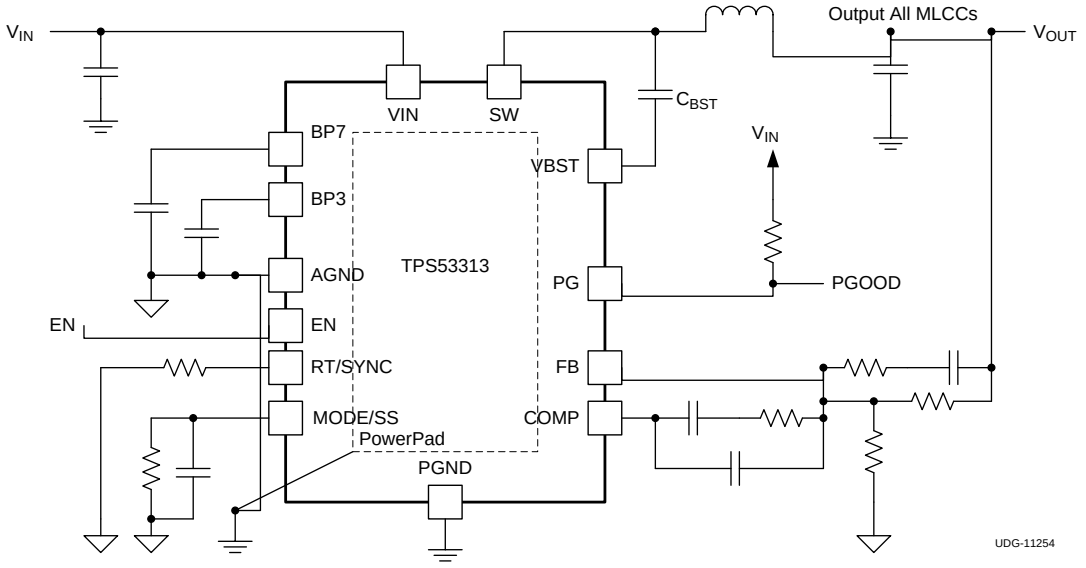
The TPS53313 is available in a 4 mm × 4 mm, 24-pin VQFN package (Green RoHs compliant and Pb free) and operates from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS53313	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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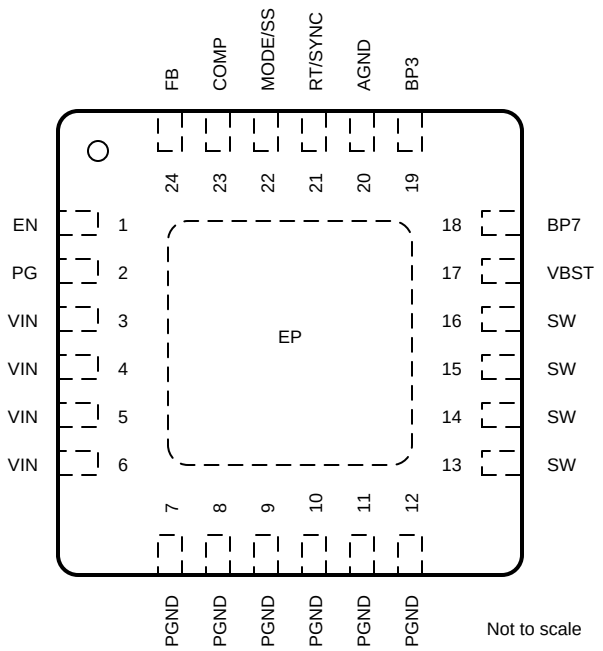
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2011) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table; see POA at the end of the data sheet	1

5 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	EN	I	Enable pin
2	PG	O	Power good output flag. Open drain output. Pull up to an external rail through a resistor.
3	VIN	P	Gate driver supply and power conversion voltage
4	VIN	P	Gate driver supply and power conversion voltage
5	VIN	P	Gate driver supply and power conversion voltage
6	VIN	P	Gate driver supply and power conversion voltage
7	PGND	P	Device power ground terminal
8	PGND	P	Device power ground terminal
9	PGND	P	Device power ground terminal
10	PGND	P	Device power ground terminal
11	PGND	P	Device power ground terminal
12	PGND	P	Device power ground terminal
13	SW	O	Output inductor connection to integrated power devices
14	SW	O	Output inductor connection to integrated power devices
15	SW	O	Output inductor connection to integrated power devices
16	SW	O	Output inductor connection to integrated power devices
17	VBST	P	Supply input for high-side MOSFET (bootstrap terminal). Connect capacitor from this pin to SW terminal.
18	BP7	P	Bias for internal circuitry and driver
19	BP3	P	Input bias supply for analog functions
20	AGND	G	Device analog ground terminal
21	RT/SYNC	I/O	Synchronized to external clock. Program the switching frequency by connecting with a resistor to GND.

(1) B = Bidirectional, G = Ground, I = Input, O = Output, P = Supply

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
22	MODE/SS	I	Mode configuration pin. Connect with a resistor to GND sets different modes and soft-start time, parallel a capacitor (or no capacitor) with the resistor changes the current limit threshold. Shorting MODE/SS pin to supply inhibits the device; shorting MODE/SS pin to AGND is equivalent to 10-kΩ resistor setting is *not recommended* (see Table 1 and Table 2 for resistor and capacitor settings).
23	COMP	O	Error amplifier compensation terminal. Type III compensation method is generally recommended for stability.
24	FB	I	Voltage feedback pin. Use for OVP, UVP, and power good determination

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

			MIN	MAX	UNIT
Input voltage	VIN		–0.3	20	V
	VBST		–0.3	27	
	VBST to SW		–0.3	7	
	SW (bidirectional)	DC	–2	20	
		transient < 20 ns	–3	20	
	EN	V_{VIN} ≥ 17	–0.3	17	
		V_{VIN} < 17	–0.3	V_{VIN} + 0.1	
	FB, MODE/SS		–0.3	3.6	
Output voltage	COMP, RT/SYNC, BP3		–0.3	3.6	V
	BP7		–0.3	7	
	PGD		–0.3	17	
Ground pin (GND)			–0.3	0.3	V
Output current				6	A
Operating temperature, T_J			–40	150	°C
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.
(3) Voltage values are with respect to the corresponding LL terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

				MIN	MAX	UNIT
	Input voltage	VIN (main supply)		4.5	16	V
		VBST		–0.1	22	
		VBST to SW		–0.1	6.5	
		SW (bidirectional)	dc	–1	18	
			transient < 20 ns	–2	18	
		EN		–0.1	V_{VIN} + 0.1	
		FB, MODE/SS		–0.1	3.5	
	Output voltage	COMP, RT/SYNC, BP3		–0.1	3.5	V
		BP7		–0.1	6.5	
		PGD		–0.1	14	
	Ground pin (GND)			–0.1	0.1	V
T_A	Ambient temperature			–40	85	°C
T_J	Junction temperature			–40	125	°C

(1) Voltage values are with respect to the corresponding LL terminal.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.4 Thermal Information

THERMAL METRIC[1]		TPS53313 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range, V_{VIN} = 12 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{VIN}	VIN supply voltage	Nominal input voltage range	4.5		16	V
V_{POR}	VIN POR threshold	Ramp up, EN = HIGH	4	4.23	4.4	V
$V_{POR(hys)}$	VIN POR hysteresis			200		mV
I_{STBY}	Standby current	EN = LOW, V_{IN} = 12 V		58		µA
R_{BOOT}	Bootstrap on-resistance			10		Ω
REFERENCE						
V_{VREF}	Internal precision reference voltage			0.6		V
TOL_{VREF}	VREF tolerance		–1%		1%	
ERROR AMPLIFIER						
UGBW[1]	Unity gain bandwidth		14			MHz
A_{OL}[1]	Open loop gain		80			dB
I_{FBINT}	FB input leakage current	Sourced from FB pin		50		nA
$I_{EA(max)}$	Output sinking and sourcing current			5		mA
SR[1]	Slew rate			5		V/µs
ENABLE						
R_{ENPD}[1]	Enable pulldown resistor			800		kΩ
V_{ENH}	EN logic high	V_{VIN} = 4.5 V	1.8			V
V_{ENHYS}	EN hysteresis	V_{VIN} = 4.5 V			0.6	V
I_{EN}	EN pin current	V_{EN} = 0 V			1	µA
		V_{EN} = 3.3 V		3.3	5	
		V_{EN} = 14 V		17.8	27.5	
SOFT-START						
t_{SS_1}	Delay after EN asserts	EN = High		0.65		ms
t_{SS_2}	Soft start ramp_up time	0 V ≤ V_{SS} ≤ 0.6 V, 39-kΩ or no resistor to MODE/SS pin		1		ms
		0 V ≤ V_{SS} ≤ 0.6 V, 20-kΩ or 160-kΩ resistor to MODE/SS pin		3		
		0 V ≤ V_{SS} ≤ 0.6 V, 10-kΩ or 82-kΩ resistor to MODE/SS pin		6		
$t_{PGDENDLY}$	PGD startup delay time	V_{SS} = 0.6 V to PGD (SSOK) going high, t_{SS} = 1 ms		0.2		ms

(1) Ensured by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range, V_{VIN} = 12 V, PGND = GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RAMP						
	Ramp amplitude	4.5 V ≤ V_{VIN} ≤ 14.4 V		V_{VIN}/9		V
		14.4 V ≤ V_{VIN} ≤ 16 V		1.6		
PWM						
$t_{MIN(off)}$	Minimum OFF time	f_{SW} = 1 MHz		150		ns
$t_{MIN(on)}$	Minimum ON time	No load			90	ns
D_{MAX}	Maximum duty cycle	f_{SW} = 1 MHz		80%		
SWITCHING FREQUENCY						
f_{SW}	Switching frequency tolerance	f_{SW} = 1 MHz, R_T = 45.3 kΩ	–10%		10%	
SOFT DISCHARGE						
R_{SFTDIS}	Soft-discharge transistor resistance	EN = Low, V_{IN} = 4.5 V, V_{OUT} = 0.6 V		120		Ω
OVERCURRENT AND ZERO CROSSING						
I_{OCPL}	Overcurrent limit on high-side FET (peak)	When I_{OUT} exceeds this threshold for 4 consecutive cycles, 2.2-nF capacitor to MODE/SS pin		4.5		A
		When I_{OUT} exceeds this threshold for 4 consecutive cycles, no capacitor to MODE/SS pin		6		A
		When I_{OUT} exceeds this threshold for 4 consecutive cycles, 10-nF capacitor to MODE/SS pin		9		
I_{OCPH}	One time overcurrent shut-off on the low-side FET (peak)	Immediately shut down when sensed current reach this value, 2.2-nF capacitor to MODE/SS pin		4.5		A
		Immediately shut down when sensed current reach this value, no capacitor to MODE/SS pin		6		A
		Immediately shut down when sensed current reach this value, 10-nF capacitor to MODE/SS pin		9		
V_{ZXOFF}	Zero crossing comparator internal offset	SW – PGND, SKIP mode		–3		mV
POWER GOOD						
V_{PGDL}	Power good low threshold	Measured at the FB pin w/r/t VREF	80%	83%	86%	
V_{PGDH}	Power good high threshold	Measured at the FB pin w/r/t VREF	114%	117%	120%	
$V_{PG(hys)}$	Power good hysteresis			2		
$V_{IN(min\_pg)}$	Minimum Vin voltage for valid PG at startup.	Measured at V_{IN} with 1-mA (or 2-mA) sink current on PG pin at startup			1	V
$V_{PG(pd)}$	Power good pull-down voltage	Pull down voltage with 4-mA sink current		0.2	0.4	V
$I_{PG(leak)}$	Power good leakage current	Hi-Z leakage current, apply 3.3-V in off state		12	16.2	µA
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
T_{OVPDLY}	Overvoltage protection delay time	Time from FB out of +17% of VREF to OVP fault		2		µs
T_{UVPDLY}	Undervoltage protection delay time	Time from FB out of –17% of VREF to UVP fault		10		µs
THERMAL SHUTDOWN						
THSD(1)	Thermal shutdown	Shutdown controller, attempt soft-stop	130	140	150	°C
$THSD_{HYST}$(1)	Thermal shutdown hysteresis	Controller restarts after temperature drops		40		°C

6.6 Typical Characteristics

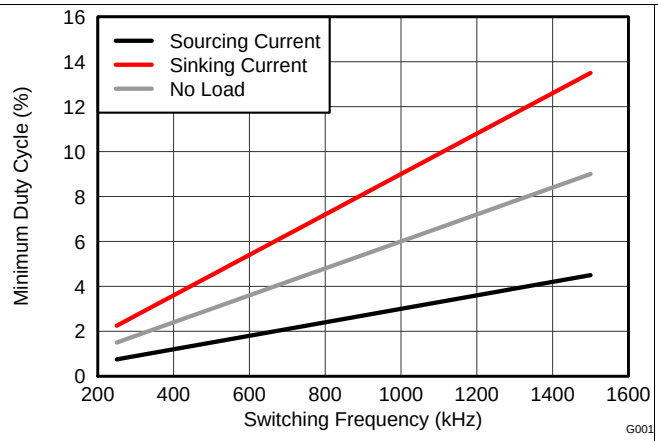


Figure 1. Ensured Minimum Duty Ratio

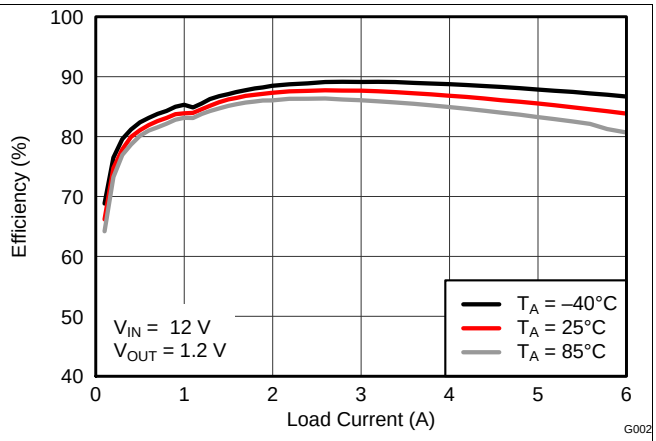


Figure 2. Efficiency, V_{IN} = 12 V

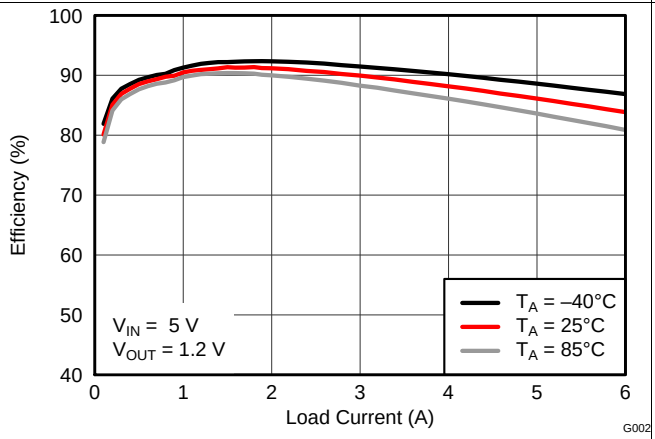


Figure 3. Efficiency, V_{IN} = 5 V

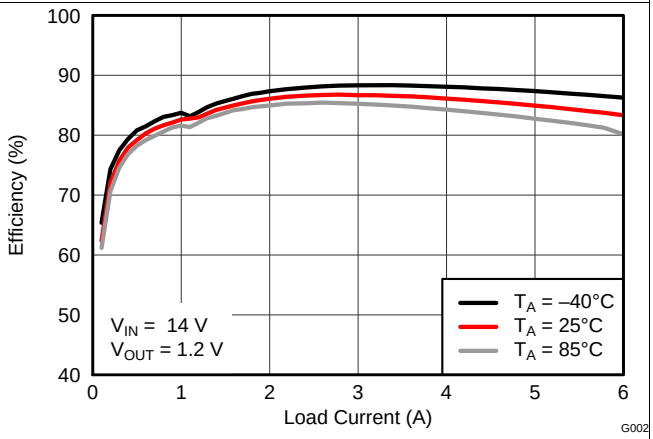


Figure 4. Efficiency, V_{IN} = 14 V

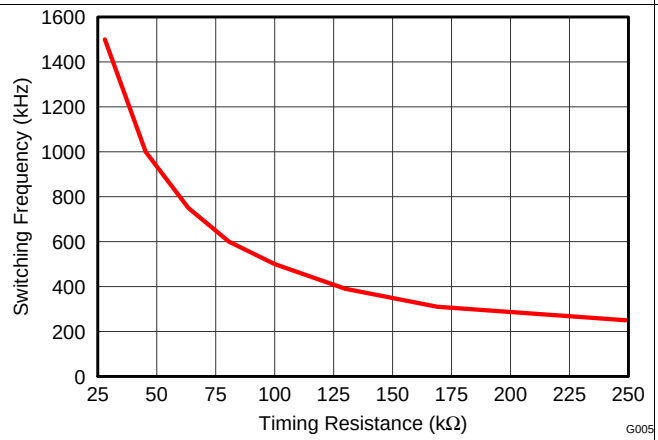


Figure 5. Switching Frequency vs Timing Resistance (R_T)

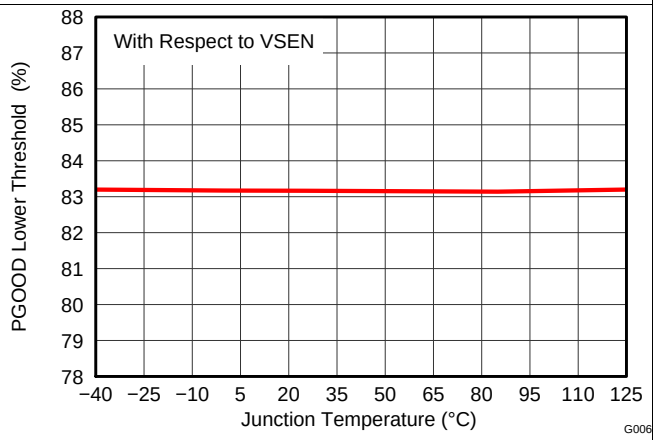


Figure 6. PGOOD Lower Threshold vs Junction Temperature

Typical Characteristics (continued)

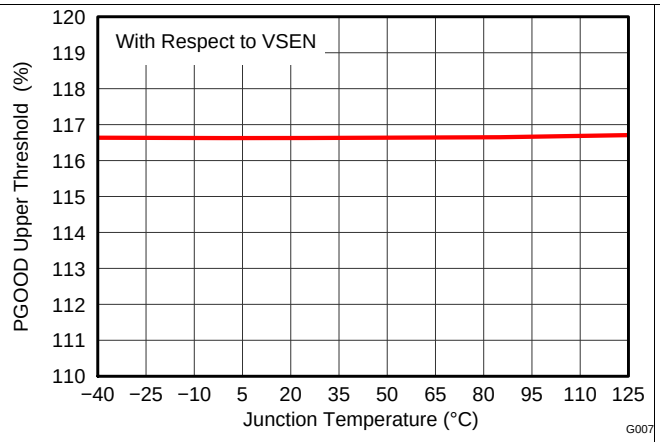


Figure 7. PGOOD Upper Threshold vs Junction Temperature

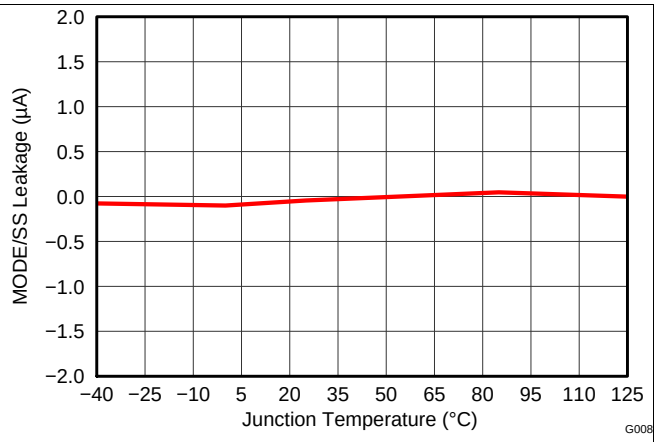


Figure 8. MODE/SS Leakage Current vs Junction Temperature

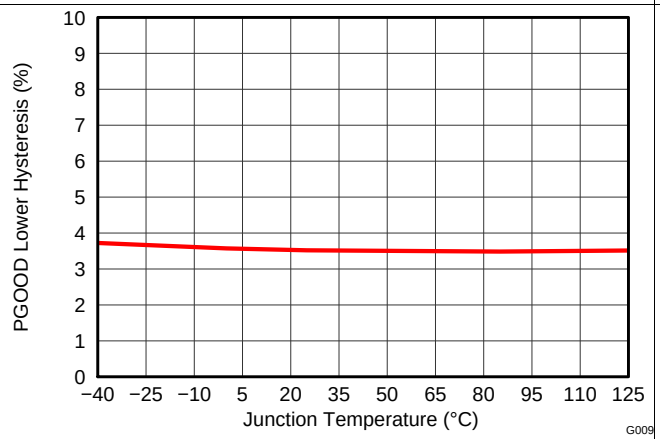


Figure 9. PGOOD Lower Hysteresis vs Junction Temperature

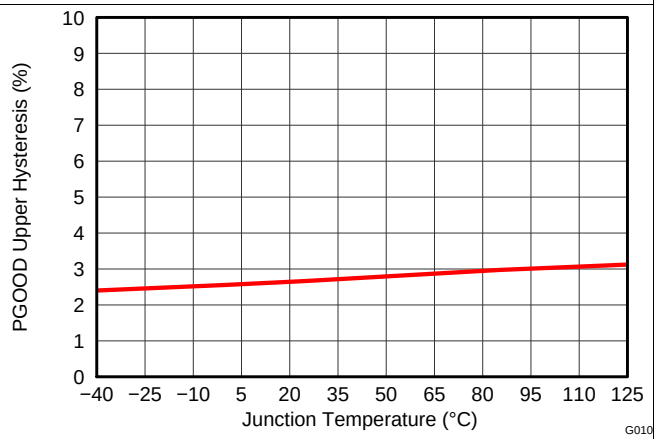


Figure 10. PGOOD Upper Hysteresis vs Junction Temperature

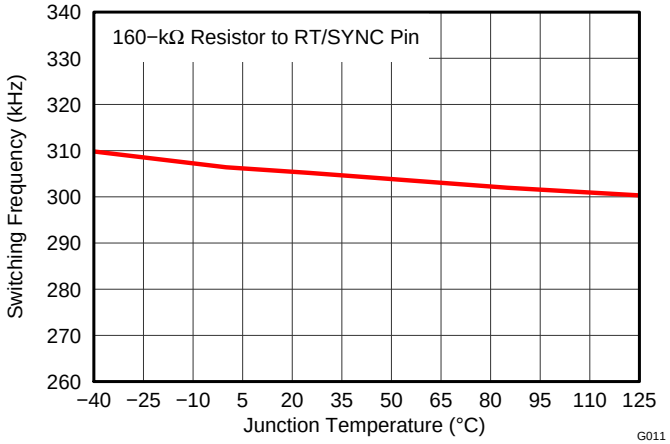


Figure 11. Switching Frequency vs Junction Temperature

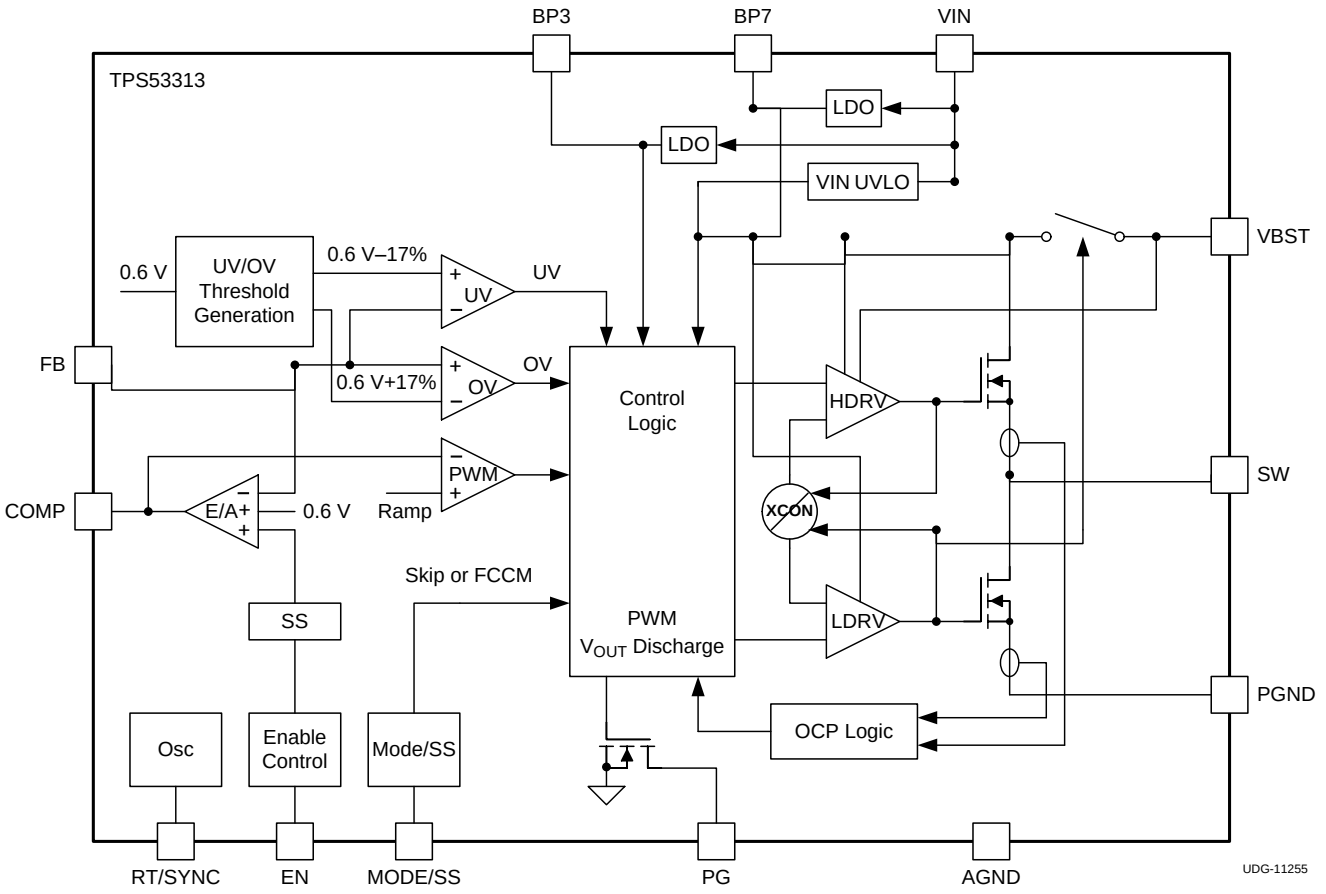
7 Detailed Description

7.1 Overview

The TPS53313 is a high-efficiency switching regulator with two integrated N-channel MOSFETs and is capable of delivering up to 6 A of load current. The TPS53316 provides output voltage from 0.6 V up to 0.7 × V_{IN} from 4.5-V to 16-V wide input voltage range. The output voltage accuracy is better than ±1% over load, line, and temperature.

This device can operate in either forced continuous conduction mode (FCCM) or skip mode with selectable soft-start time to fit various application needs. Skip mode operation provides reduced power loss and increases the efficiency at light load. The unique, patented PWM modulator enables smooth light load to heavy load transition while maintaining fast load transient.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft-Start Operation

The soft-start operation reduces the inrush current during the start-up time. A slow rising reference is generated by the soft-start circuitry and sent to the input of the error amplifier. When the soft-start ramp voltage is less than 600 mV, the error amplifier uses this ramp voltage as the reference. When the ramp voltage reaches 600 mV, a fixed 600-mV reference voltage is used for the error amplifier. The soft-start time has selectable values of 1 ms, 3 ms, and 6 ms.

Feature Description (continued)

7.3.2 Power Good

The TPS53313 monitors the output voltage through the FB pin. If the FB voltage is within 117% and 83% of the reference voltage, the power good signal remains high. If the FB voltage is outside of this range, the PG pin pin is pulled low by the internal open drain output.

During start up, the power good signal has a 200-µs delay after the FB voltage falls into the power good range limit when the soft-start time is set to 1 ms. There is also 10-µs delay during shut down.

7.3.3 UVLO Function

The TPS53313 provides UVLO protection for input voltage, VIN. If the input voltage is lower than UVLO threshold voltage minus the hysteresis, the device shut off. When the voltage rises above the threshold voltage, the device restarts. The typical UVLO rising threshold is 4.23 V. Hysteresis of 200 mV for input voltage is provided to prevent glitch.

7.3.4 Overcurrent (OC) Protection

The TPS53313 provides peak current protection and continuously monitors the current flowing through high-side and low-side MOSFETs. If the current through the high-side FET exceeds the current limit threshold, the high-side FET turns off and the low-side FET turns on. An overcurrent (OC) counter starts to increment every switching cycle to count the occurrence of the overcurrent events. The converter shuts down immediately when the OC counter reaches 4. The OC counter resets if the detected current is less than 6 A (with 6-A OC setting) after an OC event.

Another set of overcurrent circuitry monitors the current through low-side FET. If the current through the low-side FET exceeds 6 A (with 6-A OC setting), the overcurrent protection is engaged and turns off both high-side and low-side FETs immediately.

Therefore, the device is fully protected against overcurrent during both on-time and off-time. Also, the OC threshold is selectable and can be set to 4.5 A, 6 A, or 9 A by connecting different capacitor in parallel with MODE/SS pin. After OC events, the device stops switching and enters hiccup mode. A re-start is attempted after a hiccup waiting time. If the fault condition is not cleared, hiccup mode operation may continue indefinitely

7.3.5 Overvoltage and Undervoltage Protection

The TPS53313 monitors the voltage divided feedback voltage to detect the overvoltage and undervoltage conditions. When the feedback voltage is greater than 117% of the reference, overvoltage protection is triggered, the high-side MOSFET turns off and the low-side MOSFET turns on. Then the output voltage drops and the FB voltage reaches the undervoltage threshold. At that point the low-side MOSFET turns off and the device goes into tri-state logic.

When the feedback voltage is lower than 83% of the reference voltage, the undervoltage protection counter starts. If the feedback voltage remains lower than the undervoltage threshold voltage after 10 µs, the device turns off both the high-side and low-side MOSFETs and then goes into tri-state logic.

After the undervoltage events, the device stops switching and enters hiccup mode. A restart is attempted after a hiccup waiting time. If the fault condition is not cleared, hiccup mode operation may continue indefinitely.

7.3.6 Overtemperature Protection

The TPS53313 continuously monitors the die temperature. If the die temperature exceeds the threshold value (140°C typical), the device shuts off. When the device is cooled to 40°C below the overtemperature threshold, it restarts and returns to normal operation.

7.3.7 Output Discharge

When the EN pin is low, the TPS53313 discharges the output capacitors through an internal MOSFET switch between SW and GND while the high-side and low-side MOSFETs are maintained in the OFF state. The typical discharge switch on resistance is 120 Ω. This function is disabled when V_{VIN} is less than 1 V.

Feature Description (continued)

7.3.8 Switching Frequency Setting and Synchronization

The clock frequency is programmed by the value of the resistor connected from the RT/SYNC pin to GND. The switching frequency is programmable between 250 kHz and 1.5 MHz.

Also, TPS53313 is able to synchronize to external clock. The synchronization is fulfilled by connecting the RT/SYNC pin to external clock source. If no external pulse is received from RT/SYNC pin, the device continues to operate the internal clock.

7.4 Device Functional Modes

7.4.1 Operation Mode

The TPS53313 has 6 operation modes determined by the MODE/SS pin connection as listed in Table 1. The current limit thresholds and associated capacitance selections are shown in Table 2.

Table 1. Operation Mode Selection

MODE/SS PIN CONNECTION	OPERATION MODE	t_{SS} SOFT-START TIME (ms)
10 kΩ to GND	FCCM	6
20 kΩ to GND	FCCM	3
39 kΩ to GND	FCCM	1
82 kΩ to GND	Skip mode	6
160 kΩ to GND	Skip mode	3
Floating	Skip mode	1

Table 2. Capacitor Selection

MODE/SS PIN SETTING (nF)	CURRENT LIMIT THRESHOLD (A)
No capacitor	6
2.2	4.5
10	9

In forced continuous conduction mode (FCCM), the high-side FET is ON during the on-time and low-side FET is ON during the off-time. The switching is synchronized to the internal clock thus the switching frequency is fixed.

In this mode, the switching frequency remains constant over the entire load range which is suitable for applications that need tight control of switching frequency.

In skip mode, the high-side FET is on during the on-time and low-side FET is on during the off-time until the inductor current reaches zero. An internal zero-crossing comparator detects the zero crossing of inductor current from positive to negative. When the inductor current reaches zero, the comparator sends a signal to the logic control and turns off the low-side FET. The on-pulse in skip mode is designed to be 25% higher than CCM to provide hysteresis to avoid chattering between CCM and skip mode.

Also, the overcurrent protection threshold can be set to 4.5 A, 6 A or 9 A by changing the capacitor that is in parallel with MODE/SS pin. Specifically, a 6-A current limit threshold is set without an external capacitor, the 4.5 A current limit threshold is set with a 2.2-nF capacitor, and the 9-A current limit threshold is set when a 10-nF capacitor is in parallel with MODE/SS pin.

7.4.2 Light Load Operation

In skip mode, when the load current is less than half of inductor ripple current, the inductor current reaches zero by the end of OFF-Time. The light load control scheme then turns off the low-side MOSFET when inductor current reaches zero. Since there is no negative inductor current, the energy delivered to the load per switching cycle is increased compared to the normal PWM mode operation. The controller then reduces the switching frequency to maintain the output voltage regulation. The switching loss is reduced and thus efficiency is improved.

In skip mode, when the load current decreases, the switching frequency also decreases continuously in discontinuous conduction mode (DCM). When the load current is 0 A, the minimum switching frequency is reached. It is also required that the difference between V_{VBST} and V_{SW} to be higher than 3.3 V to ensure the supply for high-side gate driver.

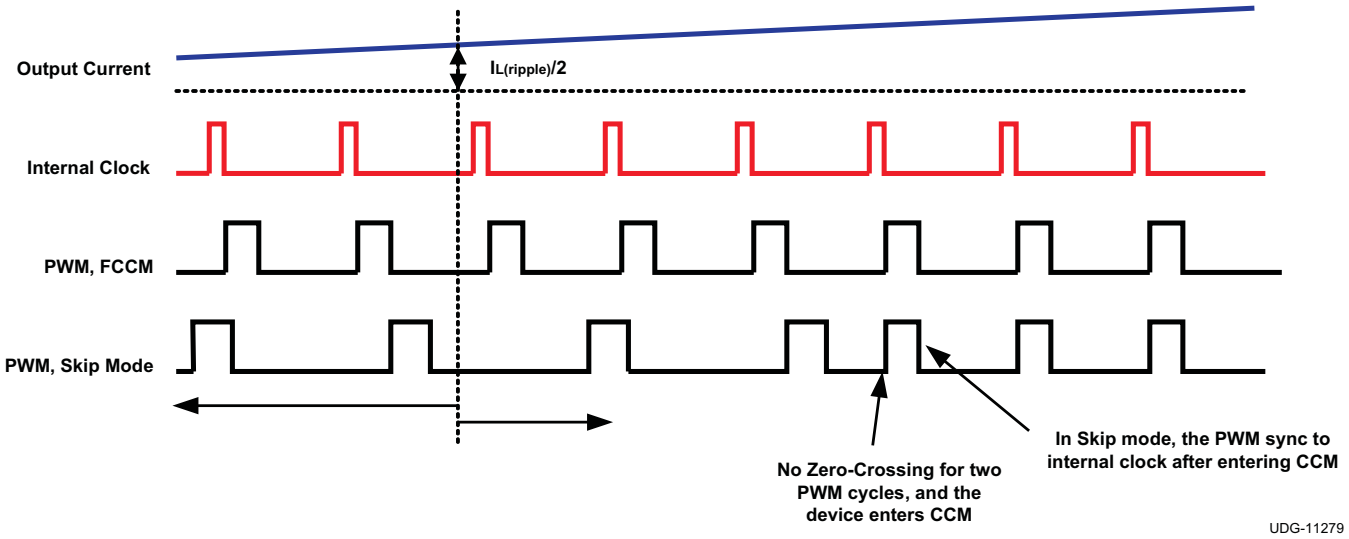


Figure 12. TPS53313 Operation Modes in Light and Heavy Load Conditions

7.4.3 Forced Continuous Conduction Mode

When choosing FCCM, the TPS53313 is operating in continuous conduction mode in both light and heavy load condition. In this mode, the switching frequency remains constant over the entire load range which is suitable for applications need tight control of switching frequency at a cost of lower efficiency at light load.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS53313 device is a high-efficiency synchronous-buck converter. The device suits low output voltage point-of-load applications with 6-A or lower output current in computing and similar digital consumer applications.

8.2 Typical Application

This design example describes a voltage-mode, 6-A synchronous buck converter with integrated MOSFETs. The device provides a fixed 1.2-V output at up to 6-A from a 12-V input bus.

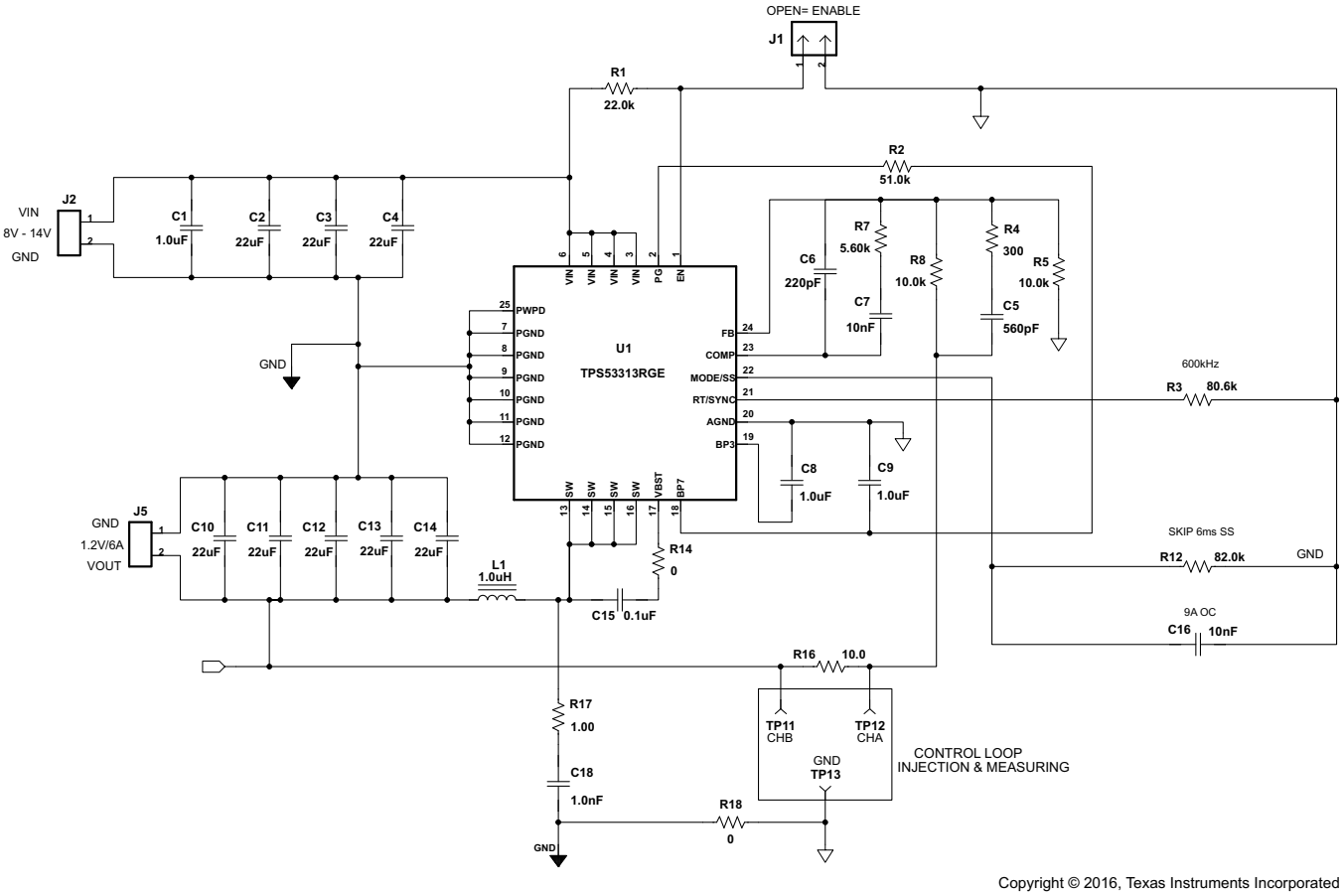


Figure 13. Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

This design example illustrates the design process and component selection for a single-output synchronous buck converter using the TPS53313. The design example schematic of a is shown in Figure 13. The specification of the converter is listed in Table 3.

Table 3. Design Example Converter Specifications

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		10.8	12	13.2	V
V_{OUT}	Output voltage			1.2		V
V_{RIPPLE}	Output ripple	I_{OUT} = 6 A		1% of V_{OUT}		V
I_{OUT}	Output current				6	A
f_{SW}	Switching frequency			600		kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Inductor Selection

The inductance value should be determined to give the ripple current of approximately 20% to 40% of maximum output current. The inductor ripple current is determined by Equation 1.

$$I_{L(ripple)} = \frac{1}{L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

The inductor also requires a low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation.

8.2.2.2 Output Capacitor Selection

The output capacitor selection is determined by output ripple and transient requirement. When operating in CCM, the output ripple has three components:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)} \quad (2)$$

$$V_{RIPPLE(C)} = \frac{I_{L(ripple)}}{8 \times C_{OUT} \times f_{SW}} \quad (3)$$

$$V_{RIPPLE(ESR)} = I_{L(ripple)} \times ESR \quad (4)$$

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L} \quad (5)$$

When ceramic output capacitor is chosen, the ESL component is usually negligible. In the case when multiple output capacitors are used, the total ESR and ESL should be the equivalent of the all output capacitors in parallel.

When operating in DCM, the output ripple is dominated by the component determined by capacitance. It also varies with load current and can be expressed as shown in Equation 6.

$$V_{RIPPLE(DCM)} = \frac{\left(\alpha \times I_{L(ripple)} - I_{OUT}\right)^2}{2 \times f_{SW} \times C_{OUT} \times I_{L(ripple)}}$$

where

- α is the DCM on-time coefficient and can be expressed as shown in Equation 7. (6)

$$\alpha = \frac{t_{ON(DCM)}}{t_{ON(CCM)}} \quad (7)$$

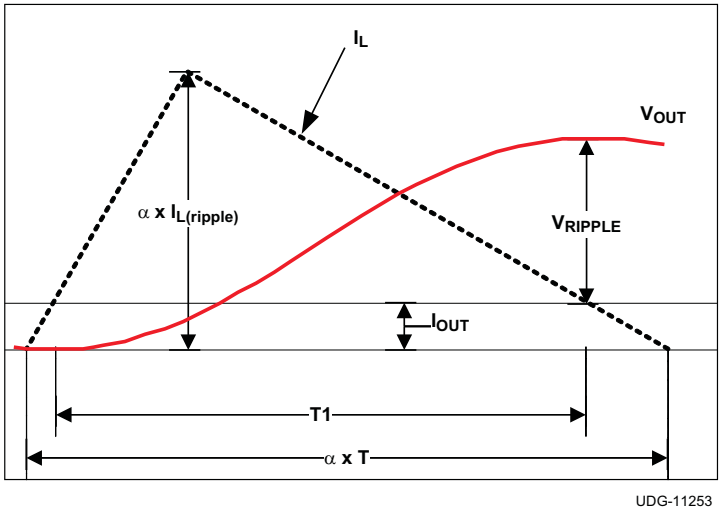


Figure 14. DCM Output Voltage Ripple

8.2.2.3 Input Capacitor Selection

The selection of input capacitor should be determined by the ripple current requirement. The ripple current generated by the converter needs to be absorbed by the input capacitors as well as the input source. The RMS ripple current from the converter can be expressed as shown in Equation 8.

$$I_{IN(ripple)} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad (8)$$

where

- D is the duty cycle and can be expressed as shown in Equation 9.

$$D = \frac{V_{OUT}}{V_{IN}} \quad (9)$$

To minimize the ripple current drawn from the input source, sufficient input decoupling capacitors should be placed close to the device. The ceramic capacitor is recommended due to its low ESR and low ESL. The input voltage ripple can be calculated as below when the total input capacitance is determined by Equation 10.

$$V_{IN(ripple)} = \frac{I_{OUT} \times D}{f_{SW} \times C_{IN}} \quad (10)$$

8.2.2.4 Output Voltage Setting Resistors Selection

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Equation 11. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended value for R1 is from 1k to 5k. Determine R2 using Equation 11.

$$R2 = \frac{0.6}{V_{OUT} - 0.6} \times R1 \quad (11)$$

8.2.2.5 Compensation Design

The TPS53313 employs voltage mode control. To effectively compensate the power stage and ensure fast transient response, Type III compensation is typically used.

$$G_{CO} = 4 \times \frac{1 + s \times C_{OUT} \times ESR}{1 + s \times \left(\frac{L}{DCR + R_{LOAD}} + C_{OUT} \times (ESR + DCR) \right) + s^2 \times L \times C_{OUT}} \quad (12)$$

The output LC filter introduces a double pole which can be calculated as shown in Equation 13.

$$f_{DP} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}} \quad (13)$$

The ESR zero of can be calculated as shown in Equation 14.

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}} \quad (14)$$

Figure 15 and Figure 16 shows the configuration of Type III compensation and typical pole and zero locations. Equation 15 through Equation 17 describe the compensator transfer function and poles and zeros of the Type III network.

$$G_{EA} = \frac{(1 + s \times C1 \times (R1 + R3))(1 + s \times R4 \times C2)}{(s \times R1 \times (C2 + C3)) \times (1 + s \times C1 \times R3) \times \left(1 + s \times R4 \frac{C2 \times C3}{C2 + C3}\right)} \quad (15)$$

$$f_{Z1} = \frac{1}{2 \times \pi \times R4 \times C2} \quad (16)$$

$$f_{Z2} = \frac{1}{2 \times \pi \times (R1 + R3) \times C1} \cong \frac{1}{2 \times \pi \times R1 \times C1} \quad (17)$$

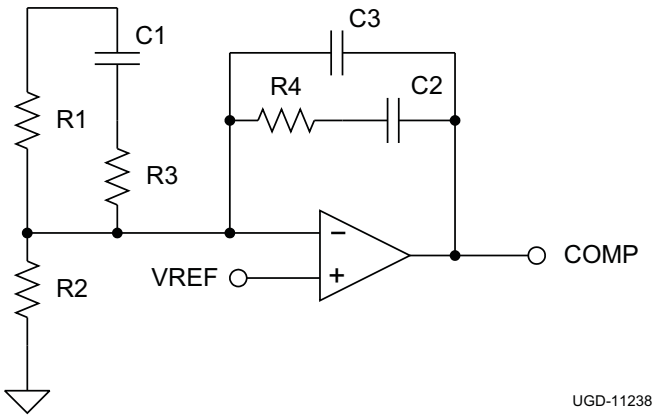


Figure 15. Type III Compensation Network Schematic

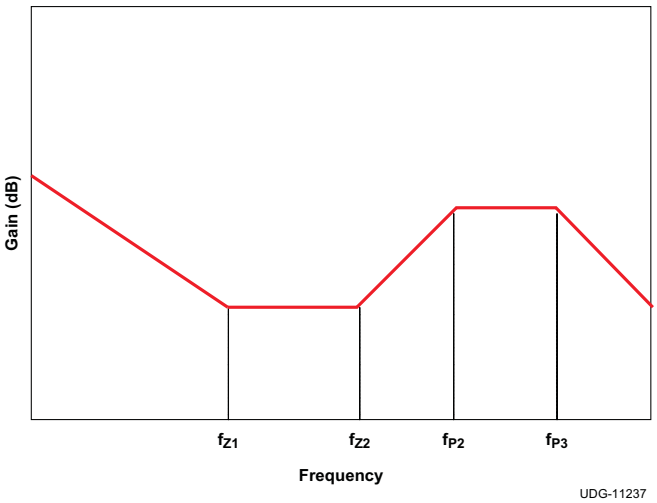


Figure 16. Type III Compensation Network Waveform

$$f_{P1} = 0 \quad (18)$$

$$f_{P2} = \frac{1}{2 \times \pi \times R3 \times C1} \quad (19)$$

$$f_{P3} = \frac{1}{2 \times \pi \times R4 \times \left(\frac{C2 \times C3}{C2 + C3}\right)} \cong \frac{1}{2 \times \pi \times R4 \times C3} \quad (20)$$

The two zeros can be placed near the double pole frequency to cancel the response from the double pole. One pole can be used to cancel ESR zero, and the other non-zero pole can be placed at half switching frequency to attenuate the high frequency noise and switching ripple. Suitable values can be selected to achieve a compromise between high phase margin and fast response. A phase margin higher than 45° is required for stable operation.

For DCM operation, a capacitor with a value between 100 pF and 220 pF is recommended for C3 when the output capacitance is between 22 µF and 220 µF.

8.2.3 Application Curves

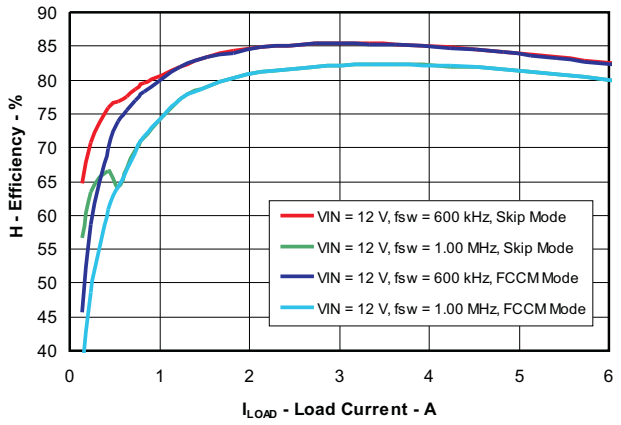


Figure 17. Efficiency

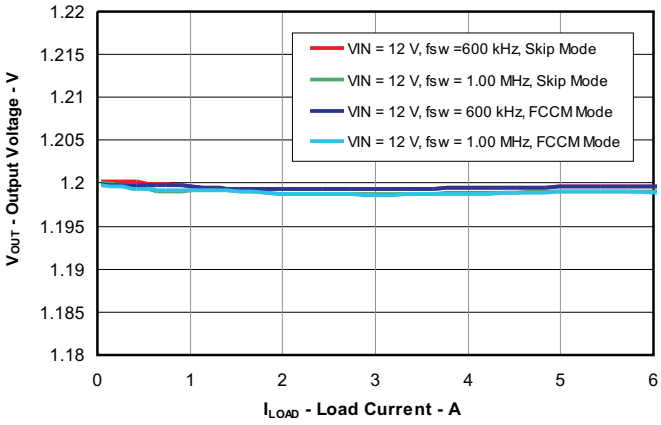


Figure 18. Load Regulation

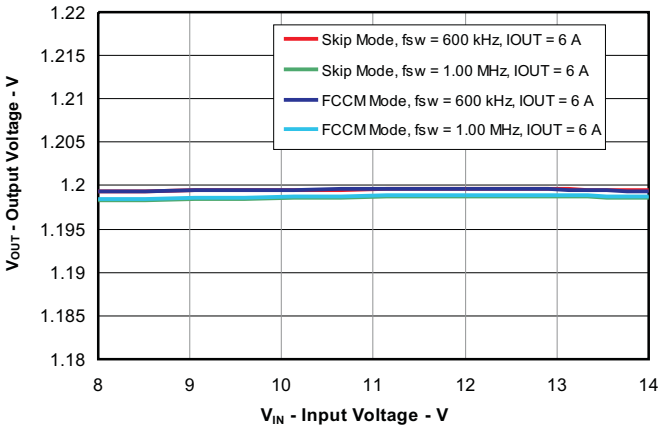
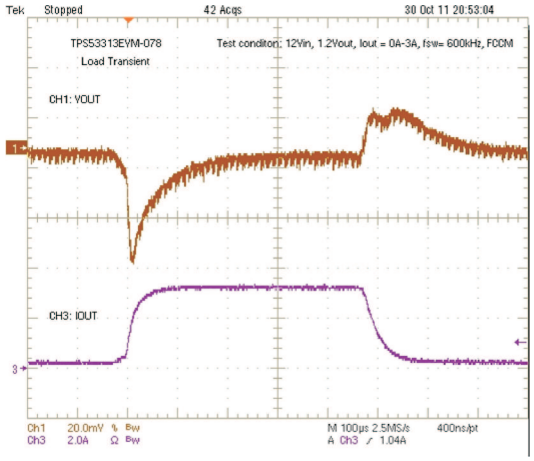
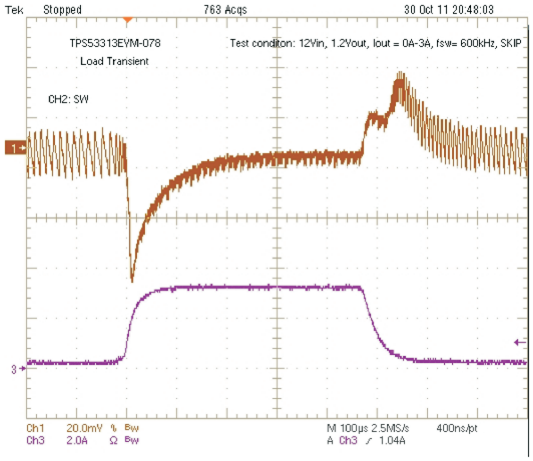


Figure 19. Line Regulation



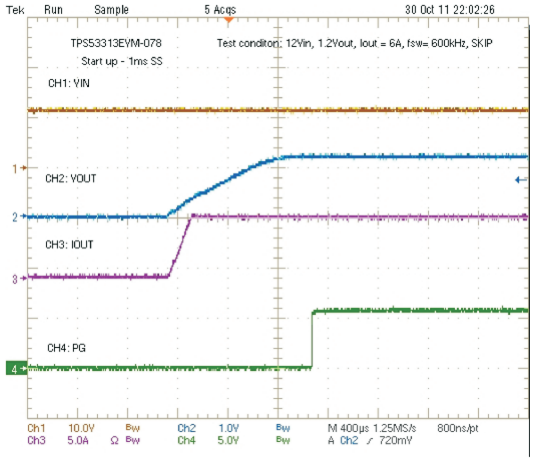
12-V VIN, 1.2-V VOUT, f_{SW} = 600 kHz

Figure 20. Output Load, 0-A to 3-A Transient Under FCCM Mode



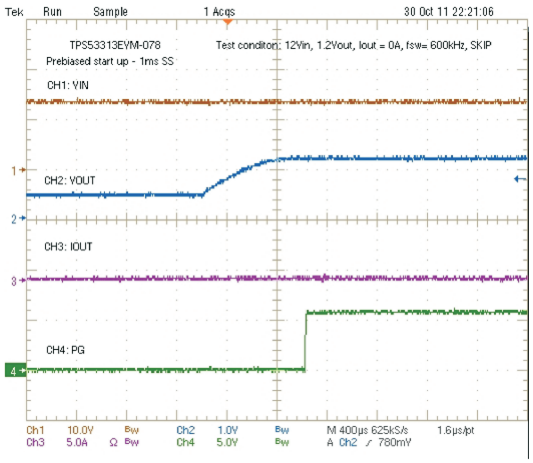
12-V VIN, 1.2-V VOUT, f_{SW} = 600 kHz

Figure 21. Output Load, 0-A to 3-A Transient Under Skip Mode



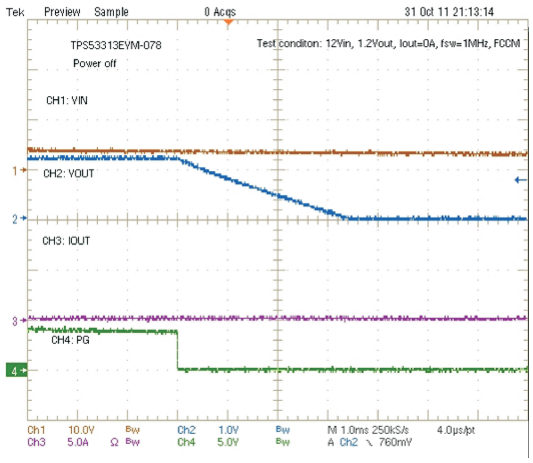
12-V VIN, 1.2-V VOUT, 6-A IOUT, 1-ms SS

Figure 22. Start-Up Waveform



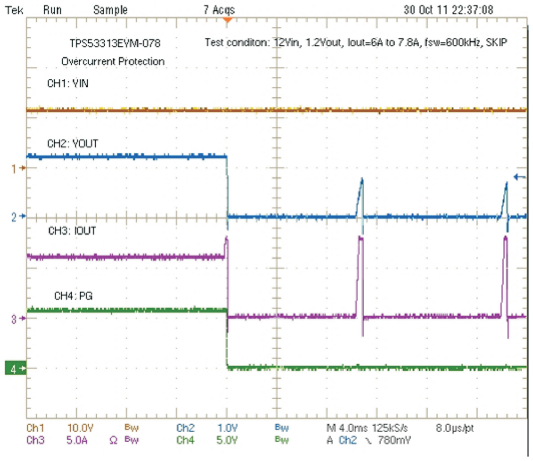
12-V VIN, 1.2-V VOUT, 0-A IOUT, 1-ms SS

Figure 23. Pre-bias Start-Up Waveform



12-V VIN, 1.2-V VOUT, 0-A IOUT

Figure 24. Shut-Down Waveform



12-V VIN, 1.2-V VOUT, IOUT increases from 6 A to 7.8 A

Figure 25. Overcurrent Protection Waveform

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range from 4.5 V to 16 V. This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme (see recommendations in *Layout*).

10 Layout

10.1 Layout Guidelines

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout:

- Separate the power ground and analog ground planes. Connect them together at one location.
- Use 6 vias to connect the thermal pad to power ground.
- Place VIN, BP7 and BP3 decoupling capacitors as close to the device as possible.
- Use wide traces for VIN, PGND and SW. These nodes carry high-current and also serve as heat sinks.
- Place feedback and compensation components as close to the device as possible.
- Keep analog signals (FB, COMP) away from noisy signals (SW, VBST).

10.2 Layout Example

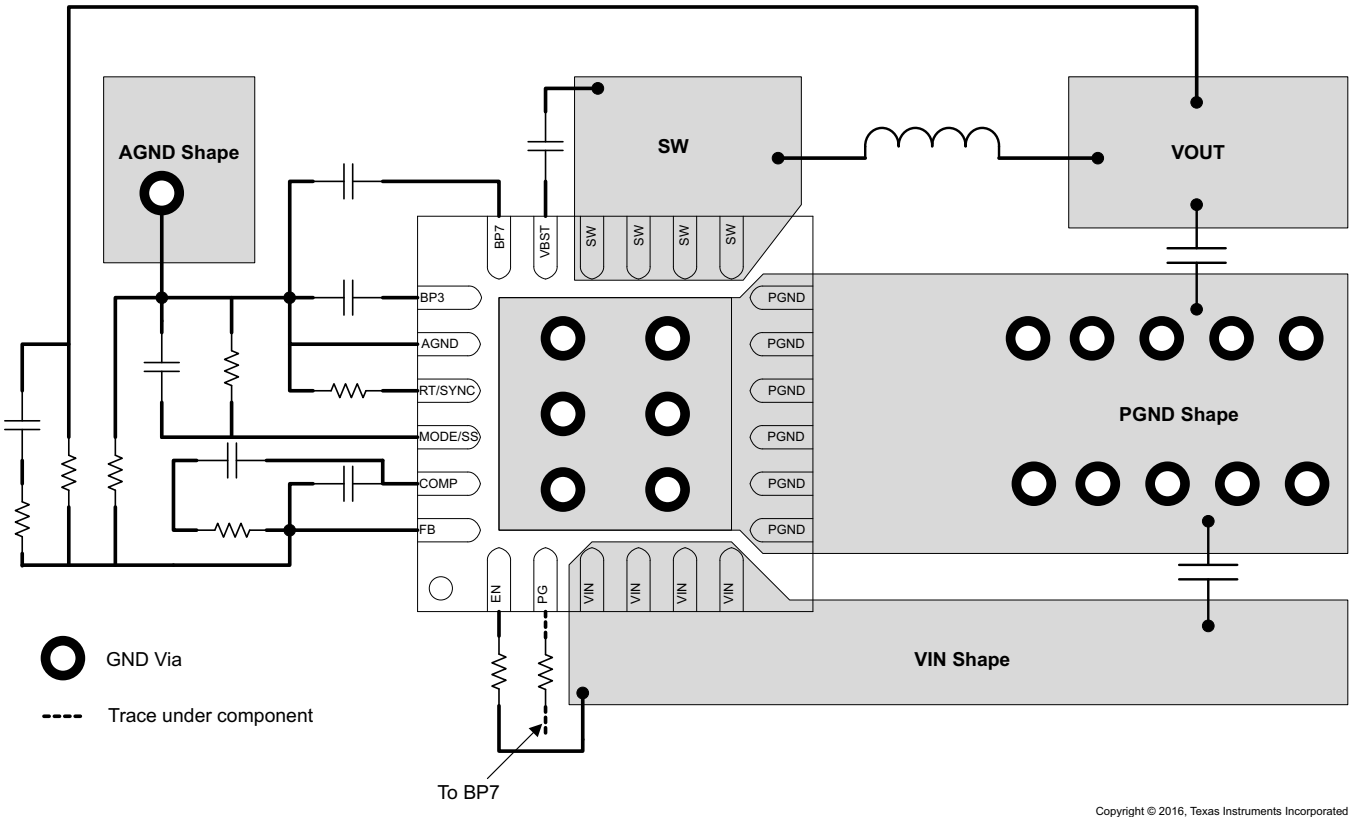


Figure 26. TPS53313 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

SmoothPWM, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53313RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 53313	Samples
TPS53313RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 53313	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

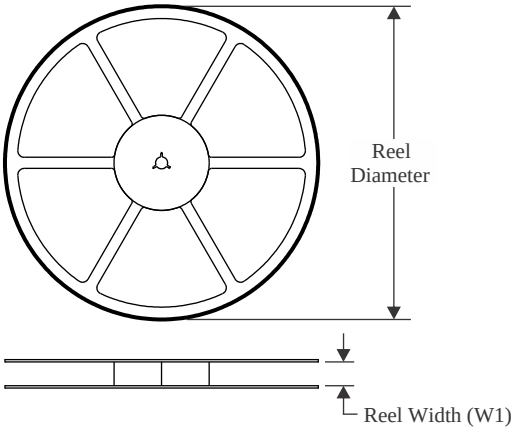
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

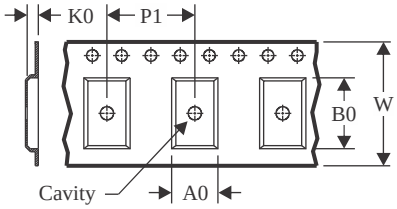
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

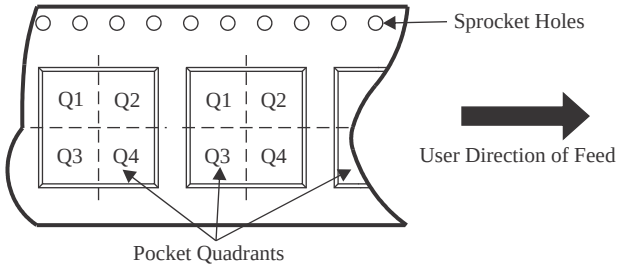


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

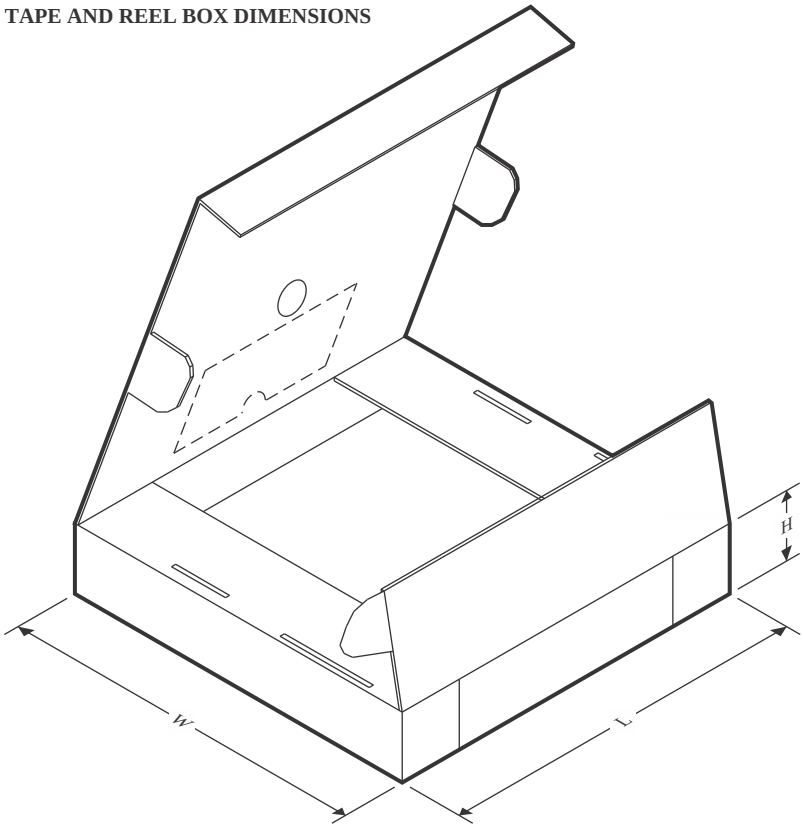
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53313RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53313RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



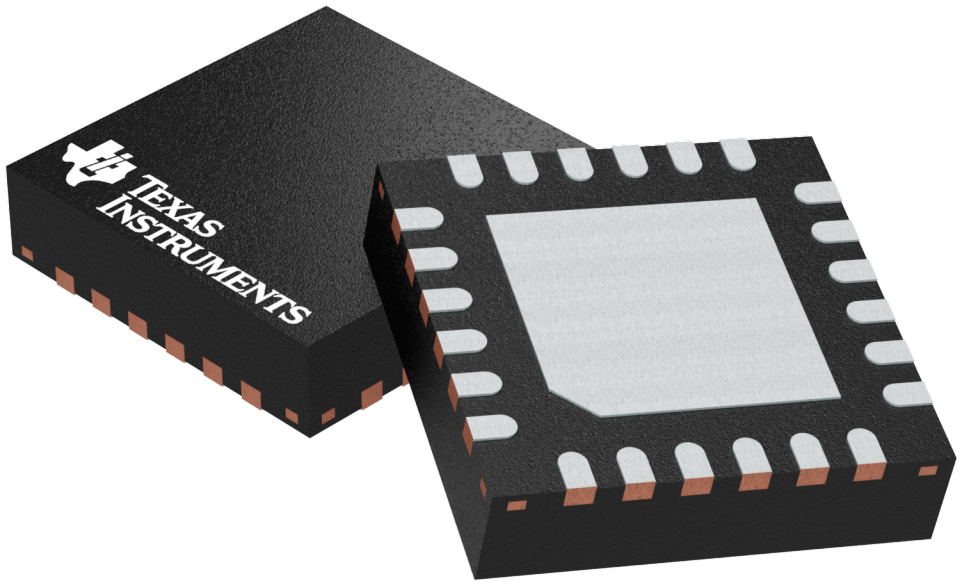
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53313RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS53313RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

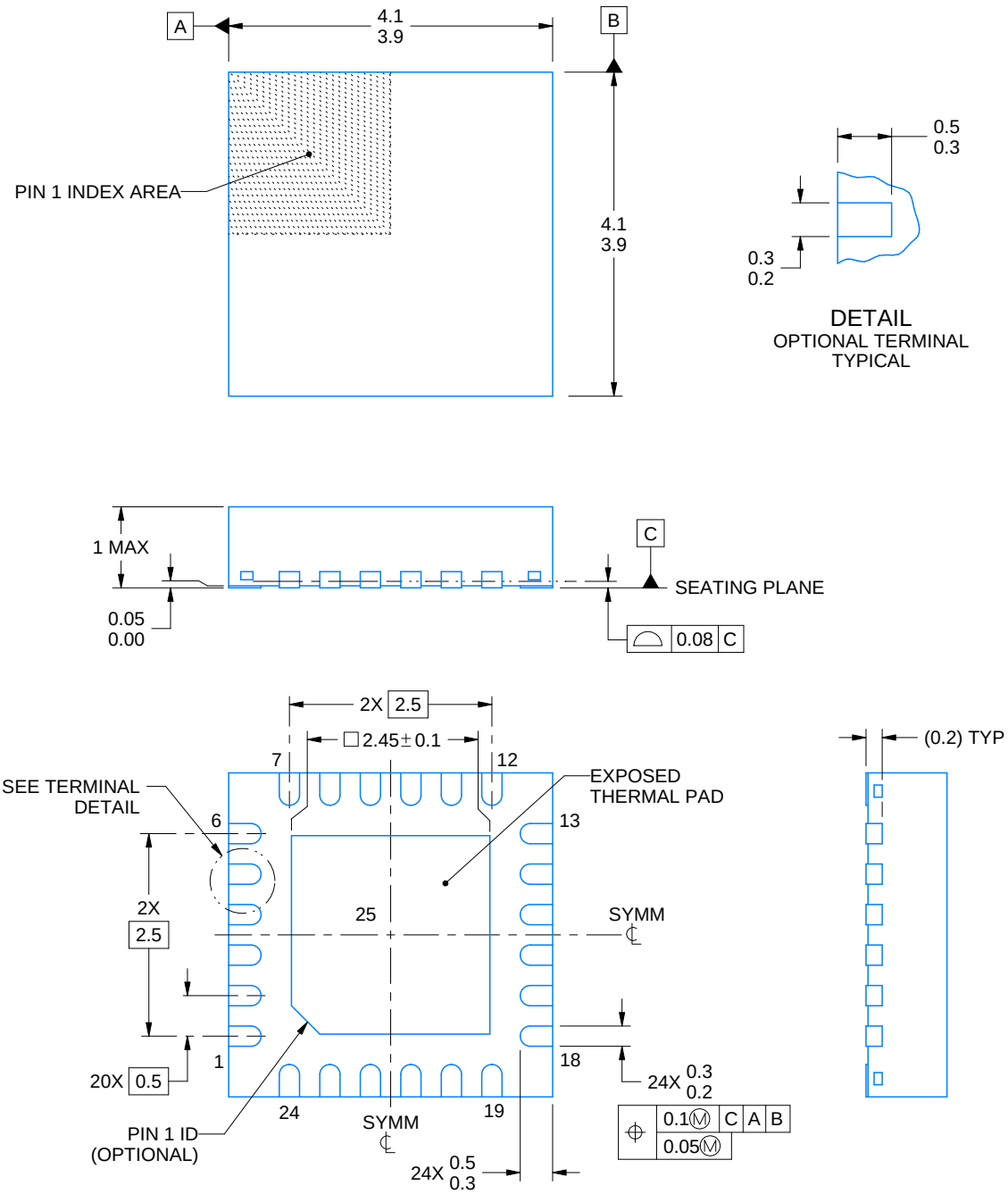
4204104/H

PACKAGE OUTLINE

RGE0024B

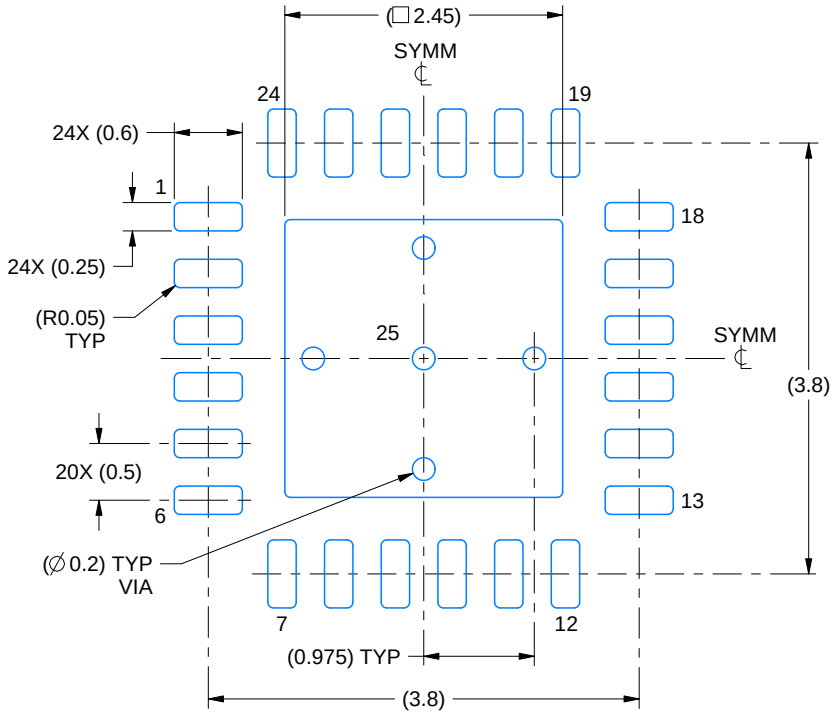
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

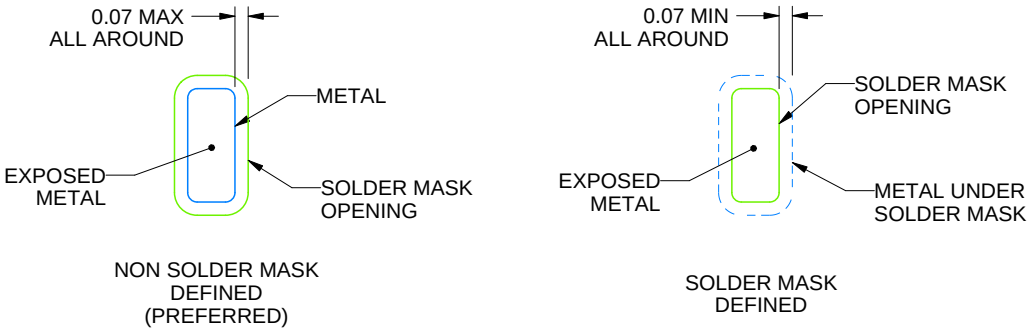


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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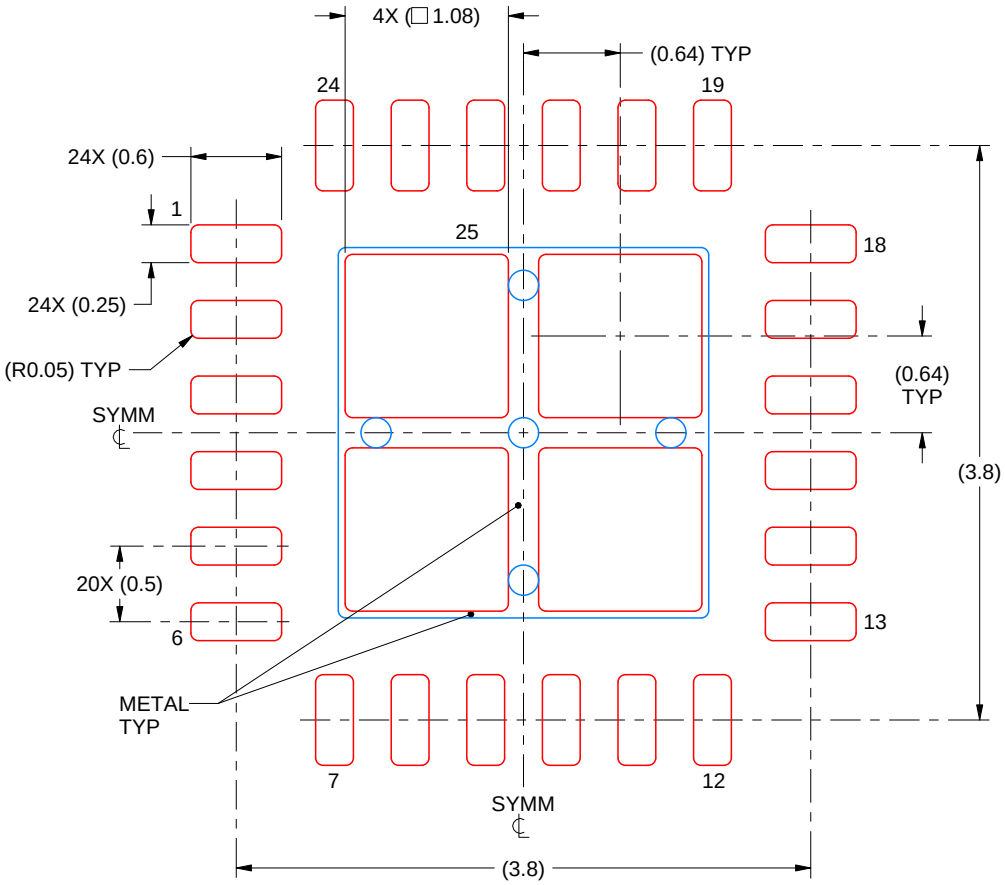
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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