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4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.3	6	V
V+	Positive-output supply voltage range ⁽²⁾	-0.3	7	V
V-	Negative-output supply voltage range ⁽²⁾	0.3	-7	V
V+ - V-	Supply voltage difference ⁽²⁾		13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON, EN)		V
		Receiver		
V _O	Output voltage range	Driver		V
		Receiver (INVALID)		
T _J	Operating virtual junction temperature		150	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

4.2 Recommended Operating Conditions

See [Figure 7-1](#) and ⁽¹⁾

		MIN	NOM	MAX	UNIT	
Supply voltage		V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, EN, FORCEOFF, FORCEON	V _{CC} = 3.3 V		V	
			V _{CC} = 5 V			
V _{IL}	Driver and control low-level input voltage	DIN, EN, FORCEOFF, FORCEON		0.8	V	
V _I	Driver and control input voltage	DIN, EN, FORCEOFF, FORCEON		0	V	
	Receiver input voltage			-25		
T _A	Operating free-air temperature	TRSF3223EC	0	70	°C	
		TRSF3223EI	-40	85		

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

4.3 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		RIN1, RIN2, DOUT1 and DOUT2 pins to GND	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	
	All pins except RIN1, RIN2, DOUT1 and DOUT2 pins	±3000	
	All pins	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

4.4 ESD Ratings - IEC Specifications

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge ⁽¹⁾	±8,000	V
		IEC 61000-4-2 Air-gap Discharge ⁽¹⁾	±15,000	

(1) A minimum of 1-μF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating.

4.5 Thermal Information

THERMAL METRIC ⁽¹⁾		DB (SOIC)	DW (SOIC)	PW (TSSOP)	RGW (VQFN)	UNIT
		20 PINS	20 PINS	20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	76.2	76.8	89.7	32.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	36.8	39.6	29.0	23.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	33.9	41.5	41.9	11.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	6.7	12.6	1.9	0.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	33.6	40.9	41.3	11.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT	
I _I	Input leakage current	EN, FORCEOFF, FORCEON		±0.01	±1	μA	
I _{CC}	Supply current	Auto-powerdown disabled	V _{CC} = 3.3 V or 5 V, T _A = 25°C, No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V _{CC}		0.3	1.3	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	
		Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded		1	10	μA

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

4.7 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	DOOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL}	Low-level output voltage	DOOUT at R _L = 3 kΩ to GND	-5	-5.4		V
I _{IH}	High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS}	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V, V _O = 0 V				
r _o	Output resistance	V _{CC} , V ₊ , and V ₋ = 0 V, V _O = ±2 V	300	10M		Ω
I _{OZ}	Output leakage current	FORCEOFF = GND, V _{CC} = 3 V to 3.6 V, V _O = ±12 V			±25	μA
		FORCEOFF = GND, V _{CC} = 4.5 V to 5.5 V, V _O = ±12 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

4.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate (see Figure 5-1)	R _L = 3 kΩ, One DOOUT switching	C _L = 1000 pF		250			kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V		1000			
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V		1000			
t _{sk(p)}	Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 5-2		300			ns
SR(tr)	Slew rate, transition region (see Figure 5-1)	R _L = 7 kΩ, C _L = 150 pF to 1000 pF		8		90	V/μs
		R _L = 3 kΩ	C _L = 1000 pF		12	60	
			C _L = 150 pF to 250 pF		24	150	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

4.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6	V _{CC} – 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT–}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.6	1.4		
V _{hys}	Input hysteresis (V _{IT+} – V _{IT–})			0.5		V
I _{OZ}	Output leakage current	EN = V _{CC}		±0.05		μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5		kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

4.10 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 5-3	150	ns
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See Figure 5-3	150	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 5-4	200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 5-4	200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See Figure 5-3	50	ns

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

4.11 Electrical Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$	-2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$	-0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	$I_{OH} = 1\text{ mA}$, $\overline{FORCEOFF} = V_{CC}$	$V_{CC} - 0.6$		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	$I_{OL} = 1.6\text{ mA}$, $\overline{FORCEOFF} = V_{CC}$		0.4	V

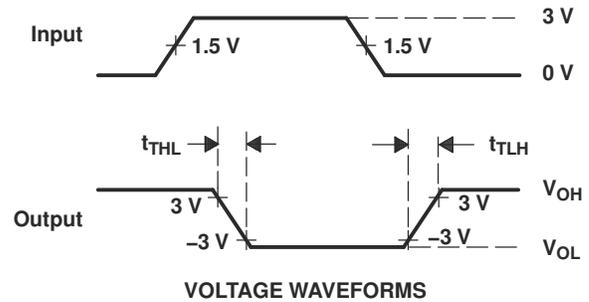
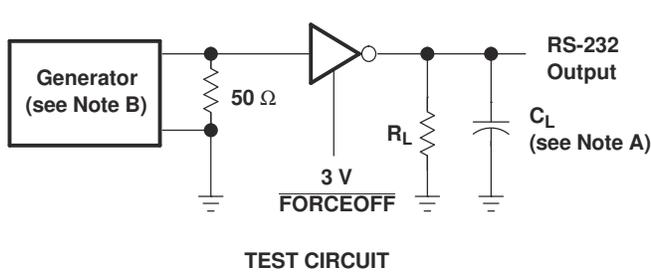
4.12 Switching Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-5](#))

PARAMETER		TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	μs
t_{en}	Supply enable time	100	μs

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

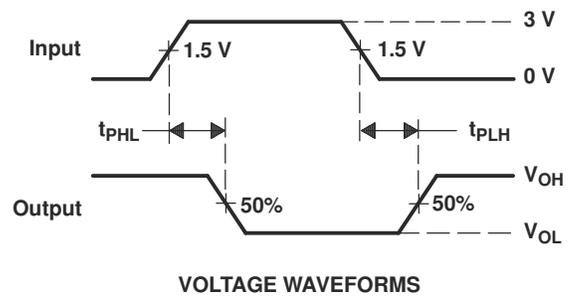
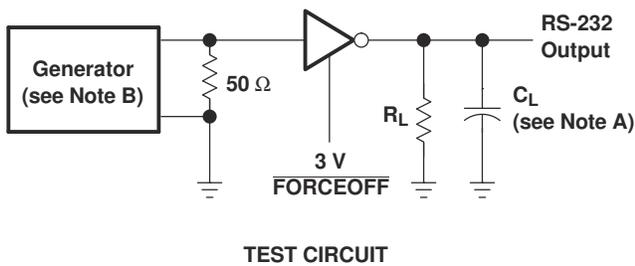
5 Parameter Measurement Information



$$SR(tr) = \frac{6V}{t_{THL} \text{ or } t_{TLH}}$$

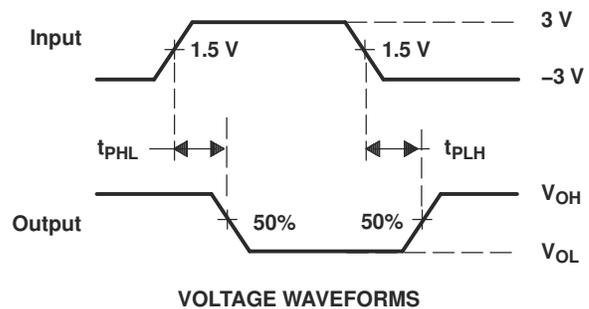
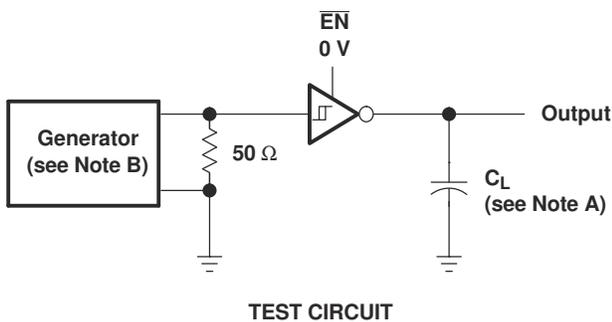
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 5-1. Driver Slew Rate



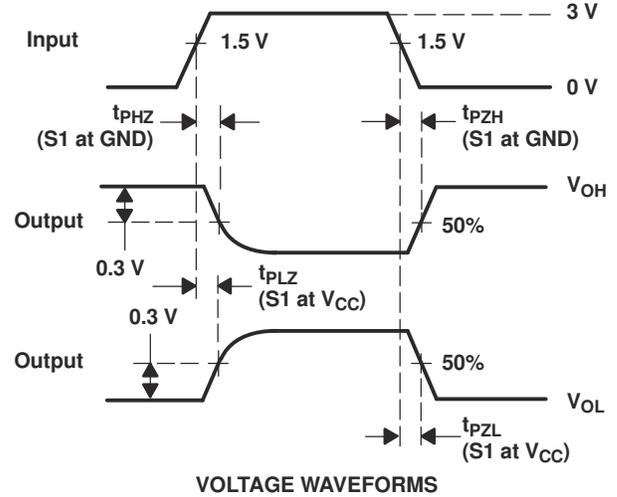
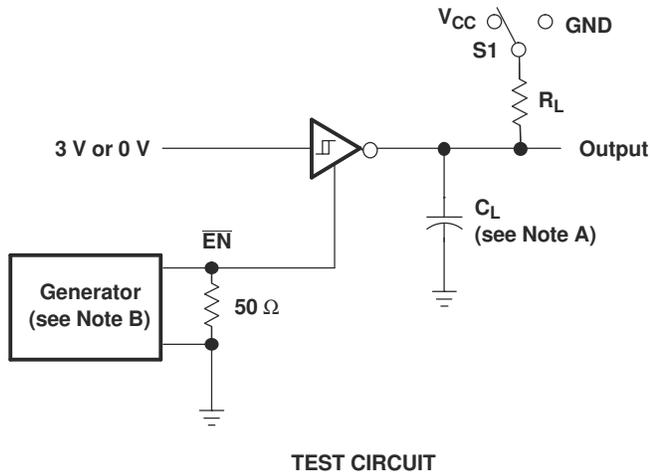
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 5-2. Driver Pulse Skew



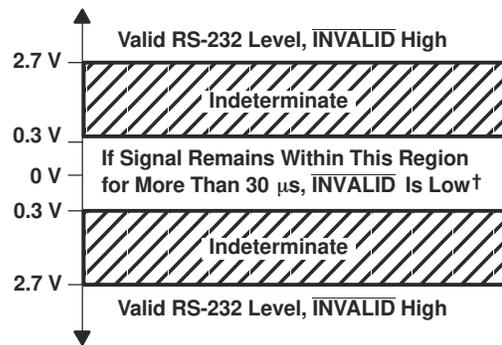
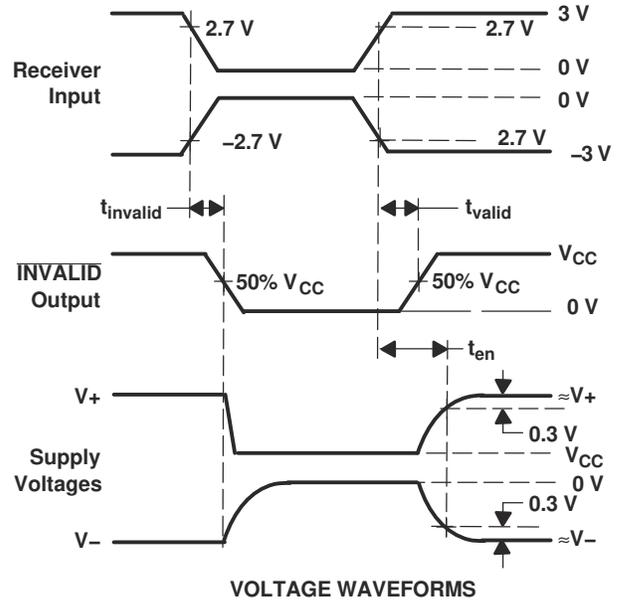
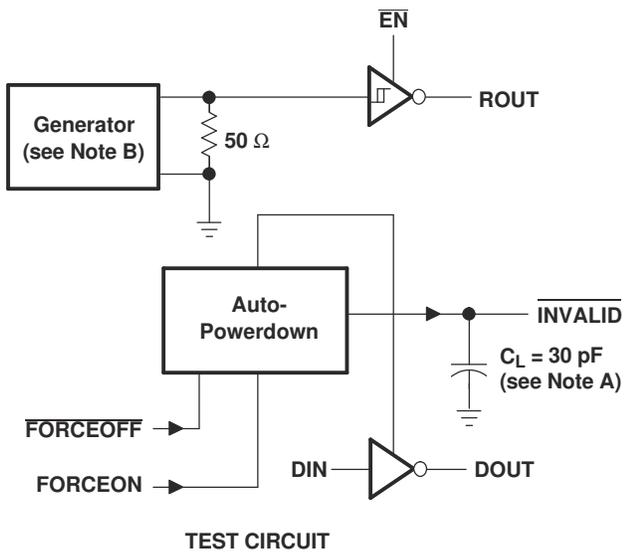
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 5-3. Receiver Propagation Delay Times



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\ \text{ns}$, $t_f \leq 10\ \text{ns}$.

Figure 5-4. Receiver Enable and Disable Times



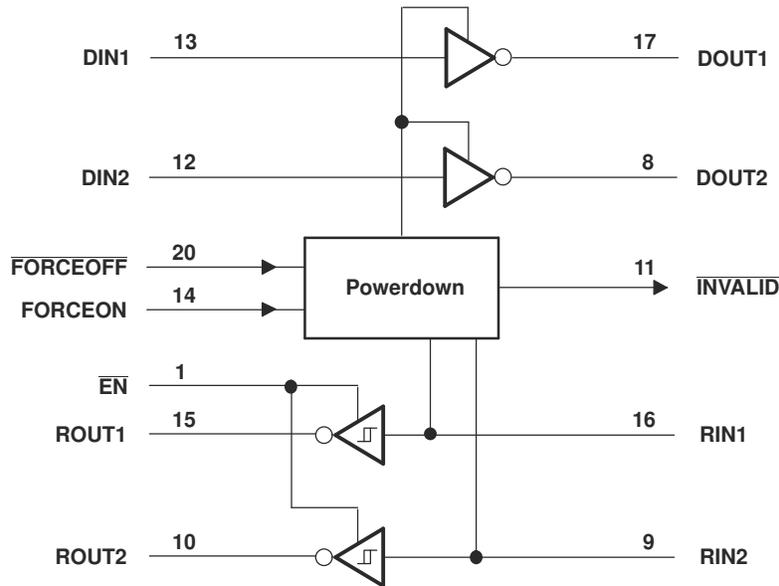
† Auto-powerdown disables drivers and reduces supply current to 1 μ A

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

6 Detailed Description

6.1 Functional Block Diagram



Pin numbers are for the DB, DW, and PW packages.

Figure 6-1. Logic Diagram (Positive Logic)

6.2 Device Functional Modes

Function Tables (Each Driver)

INPUTS ⁽¹⁾				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Function Tables (Each Receiver)

INPUTS ⁽¹⁾			OUTPUT ROUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

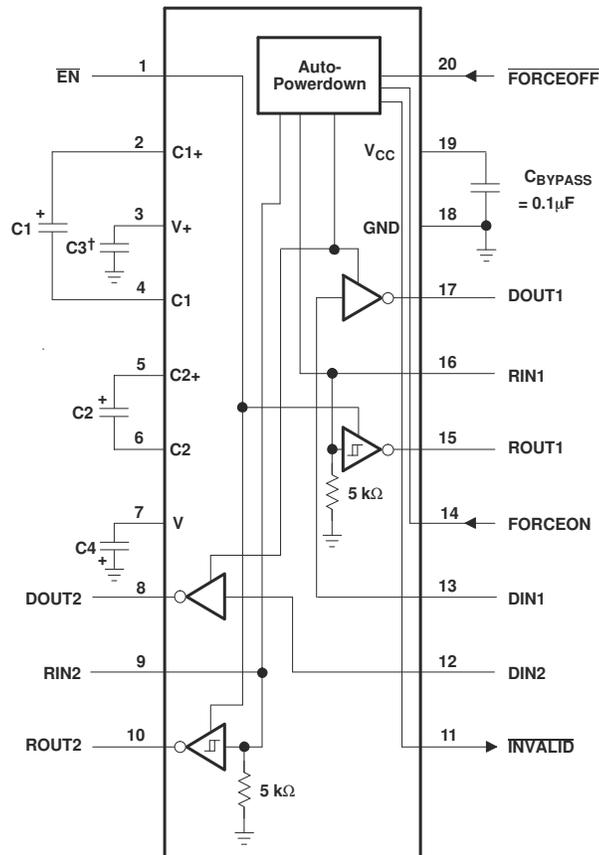
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Typical Application



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 7-1. Typical Operating Circuit and Capacitor Values

7.1.1 Detailed Design Procedure

TRSF3223E has integrated charge-pump that generates positive and negative rails needed for RS-232 signal levels. Main design requirement is that charge-pump capacitor terminals must be connected with recommended capacitor values. Charge-pump rail voltages and device supply pin must be properly bypassed with ceramic capacitors.

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2011) to Revision B (December 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added the <i>ESD Ratings</i> tables.....	3
• Added the <i>Thermal Information</i> table.....	4
• Changed the I _{CC} Auto-powerdown disabled max value from 1 mA to 1.3 mA in the <i>Electrical Characteristics</i>	4

Changes from Revision * (August 2007) to Revision A (September 2011)	Page
• Added the RGW package to the datasheet.	1
• Deleted the RHL package from the datasheet.	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRSF3223ECPWR	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	0 to 70	RT23EC
TRSF3223EIDBR	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIDBR.A	Active	Production	SSOP (DB) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIDWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3223EI
TRSF3223EIDWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRSF3223EI
TRSF3223EIPW	Obsolete	Production	TSSOP (PW) 20	-	-	Call TI	Call TI	-40 to 85	RT23EI
TRSF3223EIPWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIPWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIPWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIPWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT23EI
TRSF3223EIRGWR	Active	Production	VQFN (RGW) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RT23EI
TRSF3223EIRGWR.A	Active	Production	VQFN (RGW) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RT23EI

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

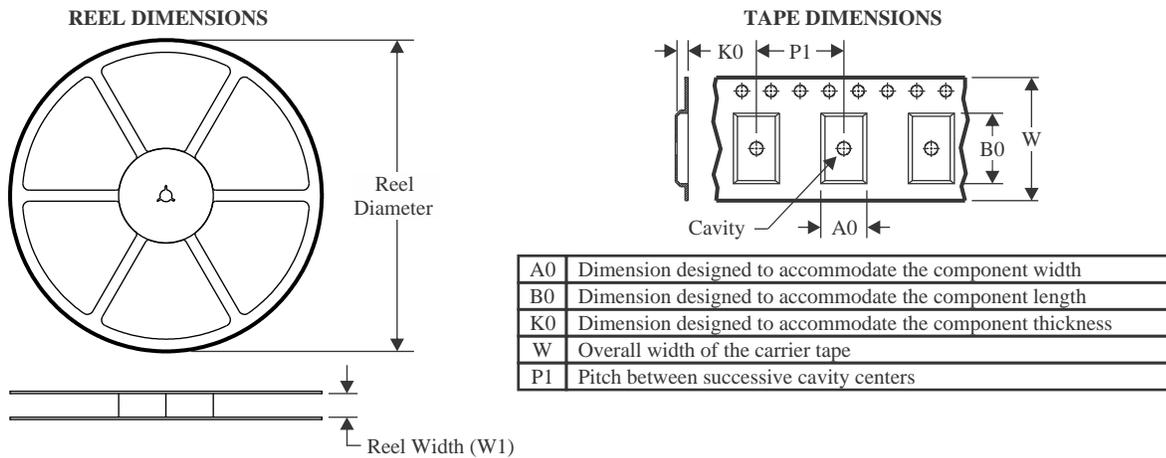
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3223EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
TRSF3223EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TRSF3223EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TRSF3223EIPWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TRSF3223EIRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3223EIDBR	SSOP	DB	20	2000	353.0	353.0	32.0
TRSF3223EIDWR	SOIC	DW	20	2000	356.0	356.0	45.0
TRSF3223EIPWR	TSSOP	PW	20	2000	353.0	353.0	32.0
TRSF3223EIPWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
TRSF3223EIRGWR	VQFN	RGW	20	3000	353.0	353.0	32.0

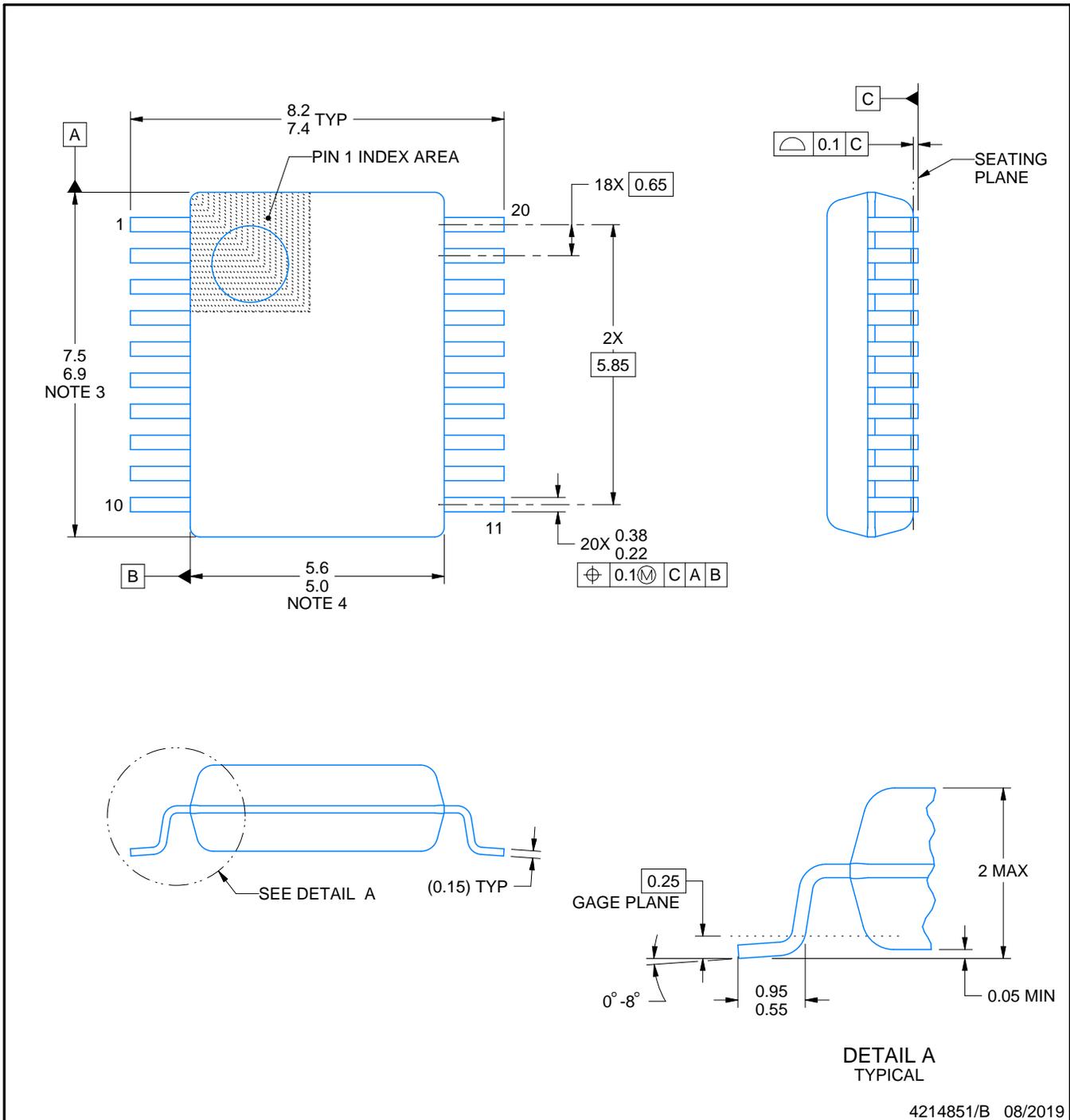
DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

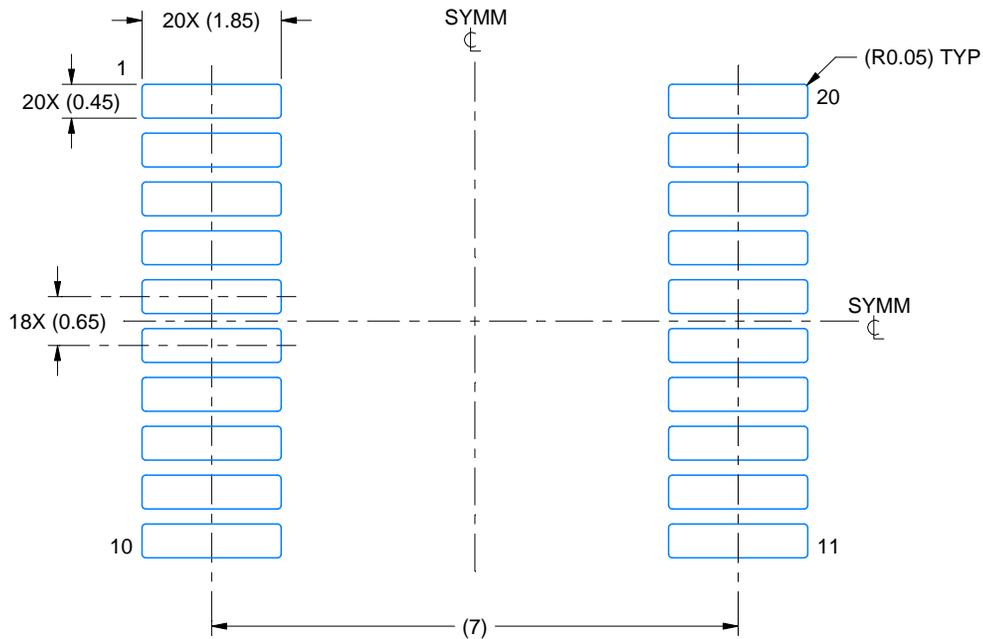
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

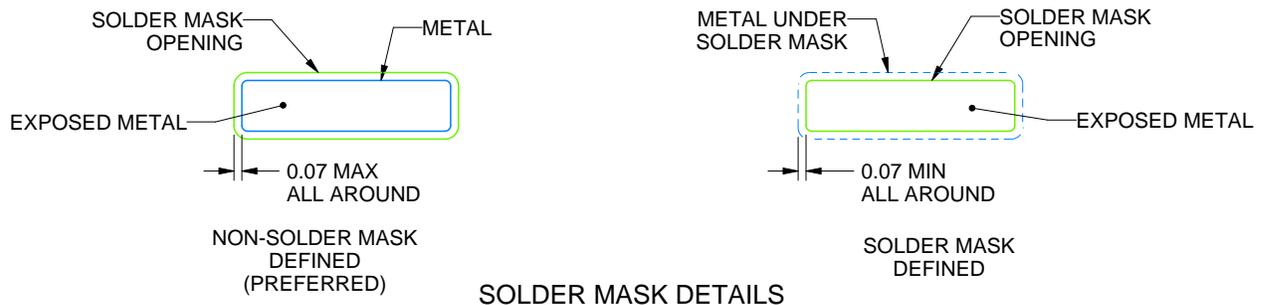
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

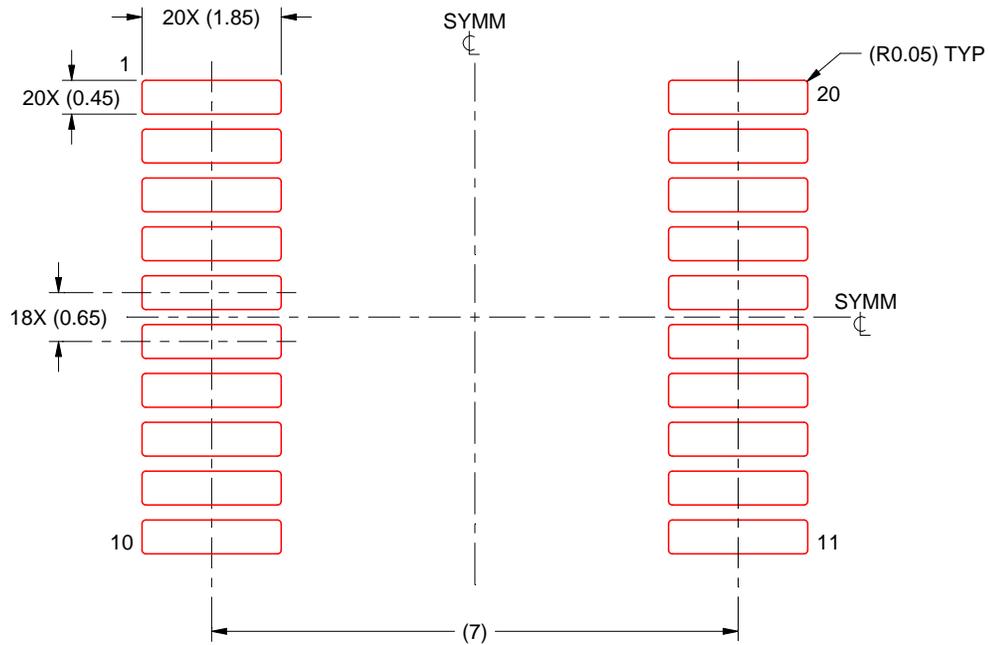
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

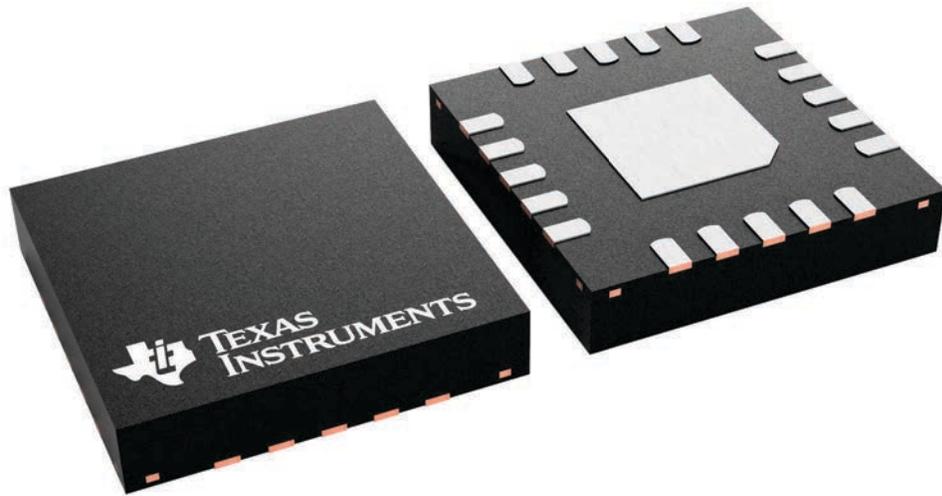
RGW 20

VQFN - 1 mm max height

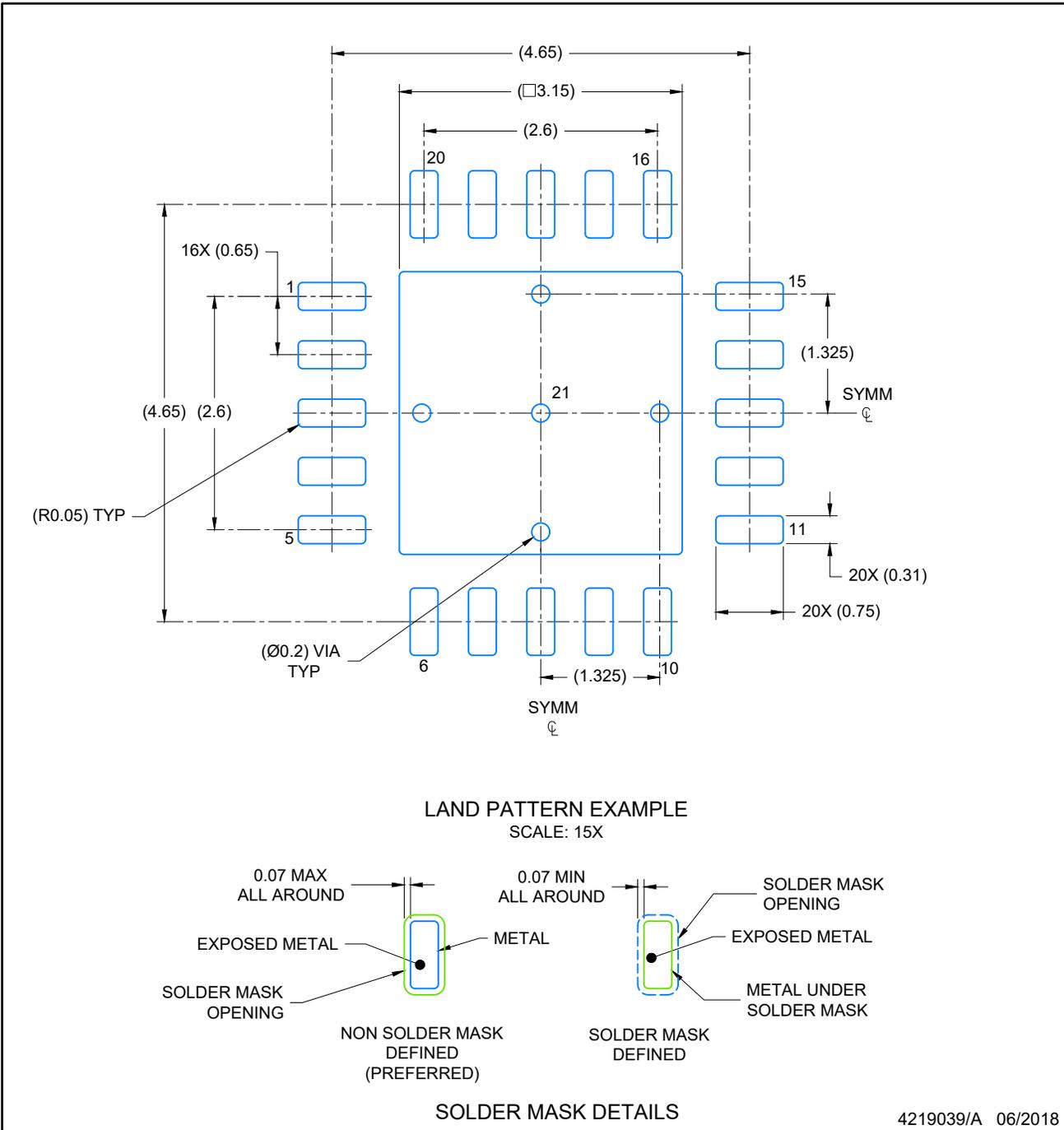
5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227157/A



NOTES: (continued)

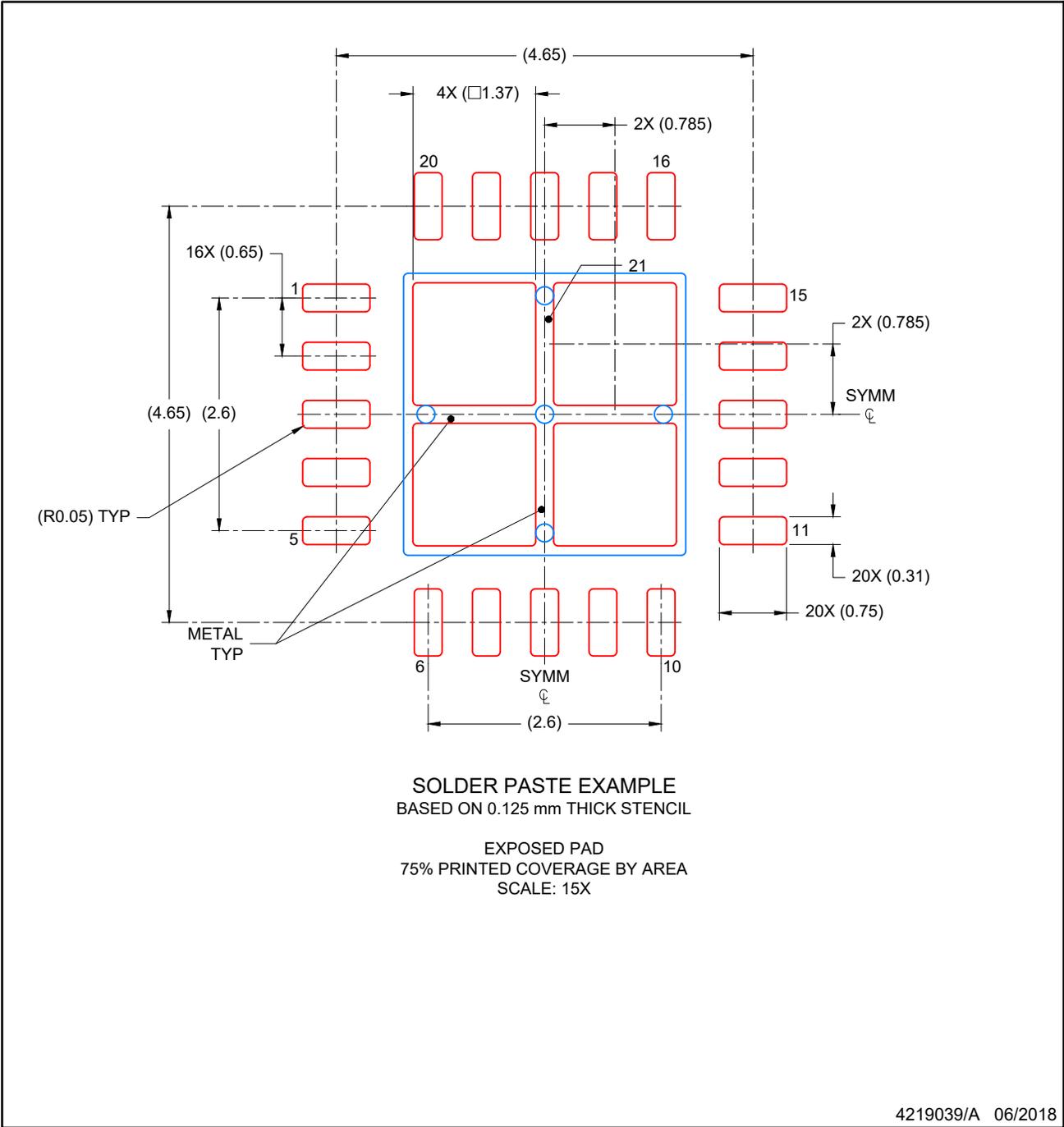
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGW0020A

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

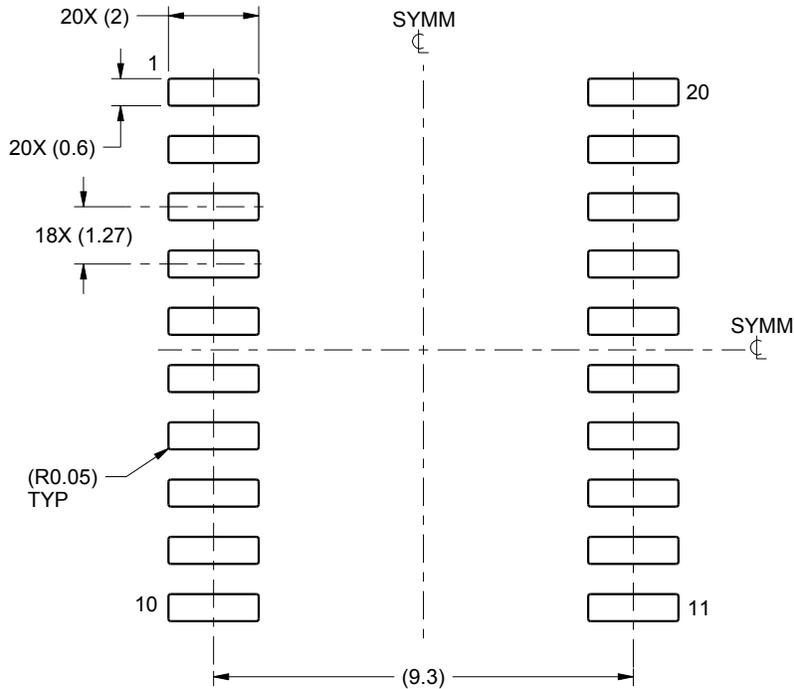
- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

EXAMPLE BOARD LAYOUT

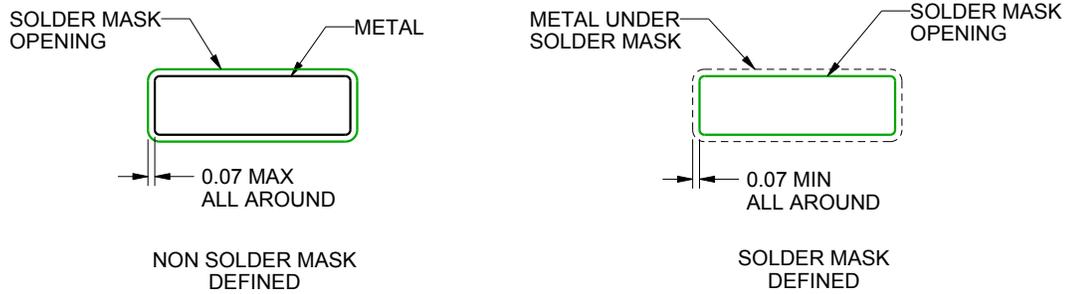
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

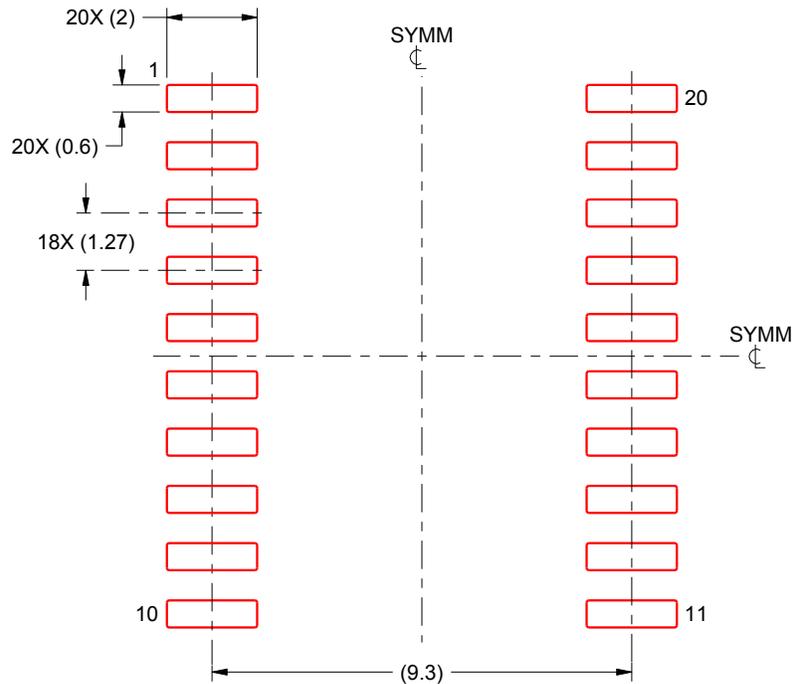
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

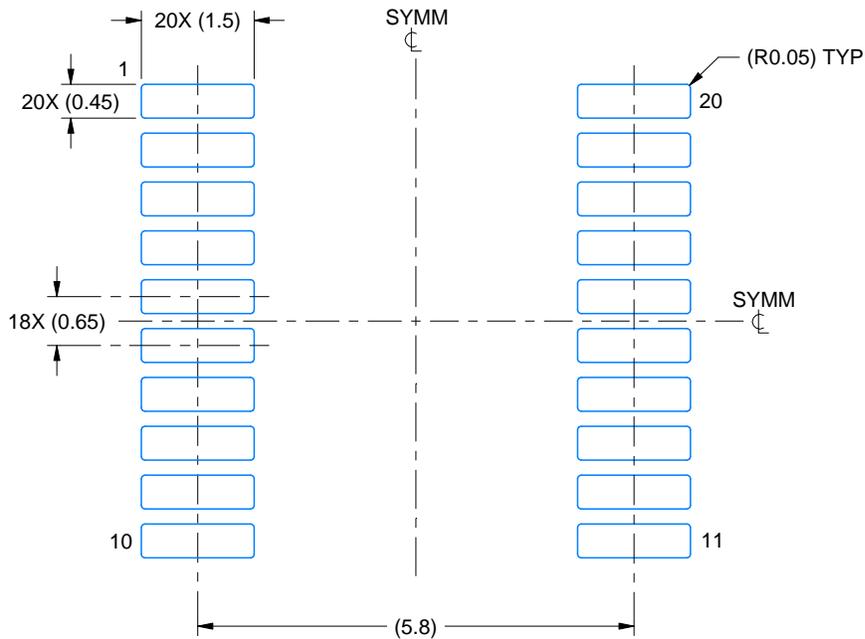
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

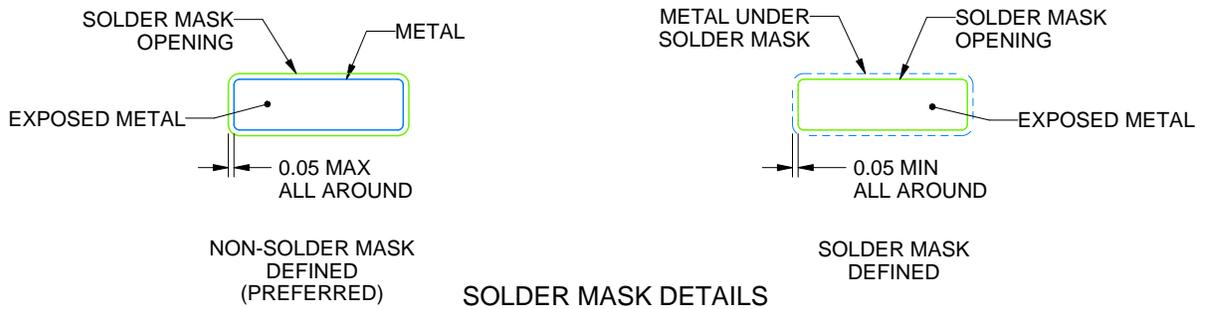
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

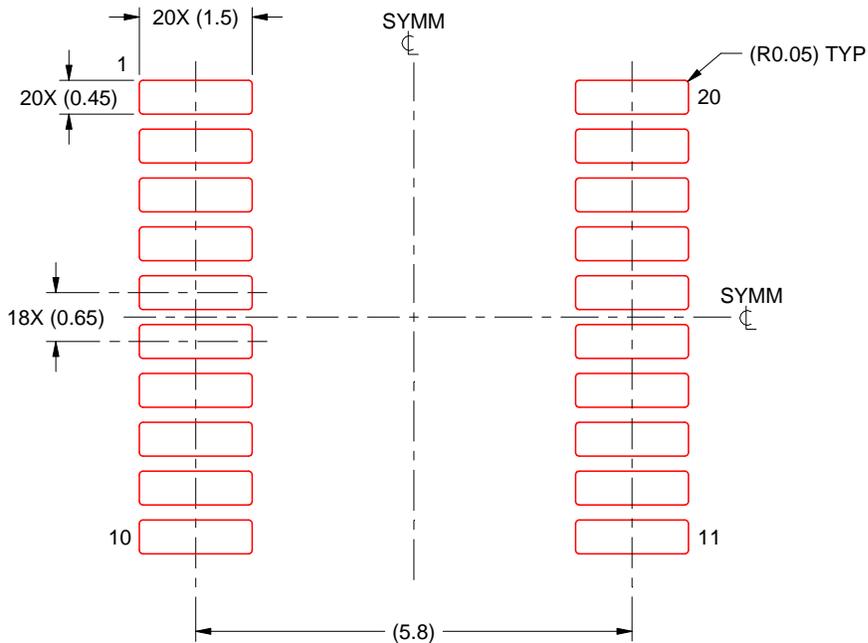
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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