(iSphynx II) 1394 Integrated PHY and Link-Layer Controller for SBP-2 Products and DPP Products

FEATURES

- **IEEE 1394a-2000 Compliant**
- **Single 3.3-V Supply**
- **Internal 1.8-V Circuit to Reduce Power Consumption**
- **Integrated 400-Mbps Two-Port Physical Layer (PHY)**
- **Internal Voltage Regulator**
- **IEEE 1394 Related Functions:**
  - **Automated Read Response for ConfigROM Register Access**
  - **Automated Single Retry Protocol and Split Transaction Control**
- **SBP-2 Related Functions:**
  - **Supports Four Initiators by Automated Transactions and More Can Be Supported Through Firmware.**
  - **Automated Management ORB Fetching**
  - **Automated Linked Command ORB Fetching**
  - **Automated PageTable Fetching**
  - **Automated Status Block Transmit**
- **Ability to Support Direct Print Protocol (DPP) Mode**
- **Data Transfers:**
  - **Auto Address Increment of Direct/Indirect Addressing on Data Transfer (Packetizer)**
  - **Automated Header Insert/Strip for DMA Data Transfers**
  - **8-/16-Bit Asynchronous and Synchronous DMA I/F With Handshake and Burst Mode**
  - **Supports ATAPI (Ultra-DMA) Mode and SCSI Mode**
  - **8-/16-Bit Data/Address Multiplex Microcontroller and 8-/16-Bit Separated Data/Address Bus**
  - **Three FIFO Configurations That Support High Performance for the DMA and for Command Exchanges**
    - **Asynchronous Command FIFO: 1512 Bytes**
    - **Config ROM/LOG FIFO: 504 Bytes**
    - **DMA FIFO: 4728 Bytes**

DESCRIPTION

The TSB43AA82A is a high performance 1394 integrated PHY and link layer controller. It is compliant with the IEEE 1394-1995 and IEEE 1394a-2000 specifications and supports asynchronous transfers.

TSB43AA82A has a generic 16-/8-bit host bus interface. It supports parallel or multiplexed connections to the microcontroller (MCU) at rates up to 40 MHz.

The TSB43AA82A offers large data transfers with three mutually independent FIFOs: 1) the asynchronous command FIFO with 1512 Bytes, 2) the DMA FIFO with 4728 bytes and 3) the Config ROM/LOG FIFO with 504 bytes.

The features of the TSB43AA82A support the serial bus protocol 2 (SBP-2). It handles up to four initiators with the SBP-2 transaction/timer manager. This SBP-2 transaction engine supports fully automated operation request block (ORB) fetches and fully automated memory page table fetches for both read and write transactions. Automated responses to other node requests are provided; this includes responding to another node's read request to the Config ROM and issuing ack_busy_X for a single retry. Various control registers enable the user to program IEEE 1394 asynchronous transaction settings. The user can program the number of retries and the split transaction time-out value by setting the time limit register in the CFR.

The TSB43AA82A also supports the direct print protocol (DPP). The asynchronous receive FIFO (ARF) in the TSB43AA82A is large enough to satisfy the connection register area, the DRF receiving FIFO can be used as the segment data unit (SDU) register to fulfill the large data transfer.

This document is not intended to serve as a tutorial on IEEE 1394; users are referred to IEEE Std 1394-1995 and IEEE 1394a-2000 .(1)

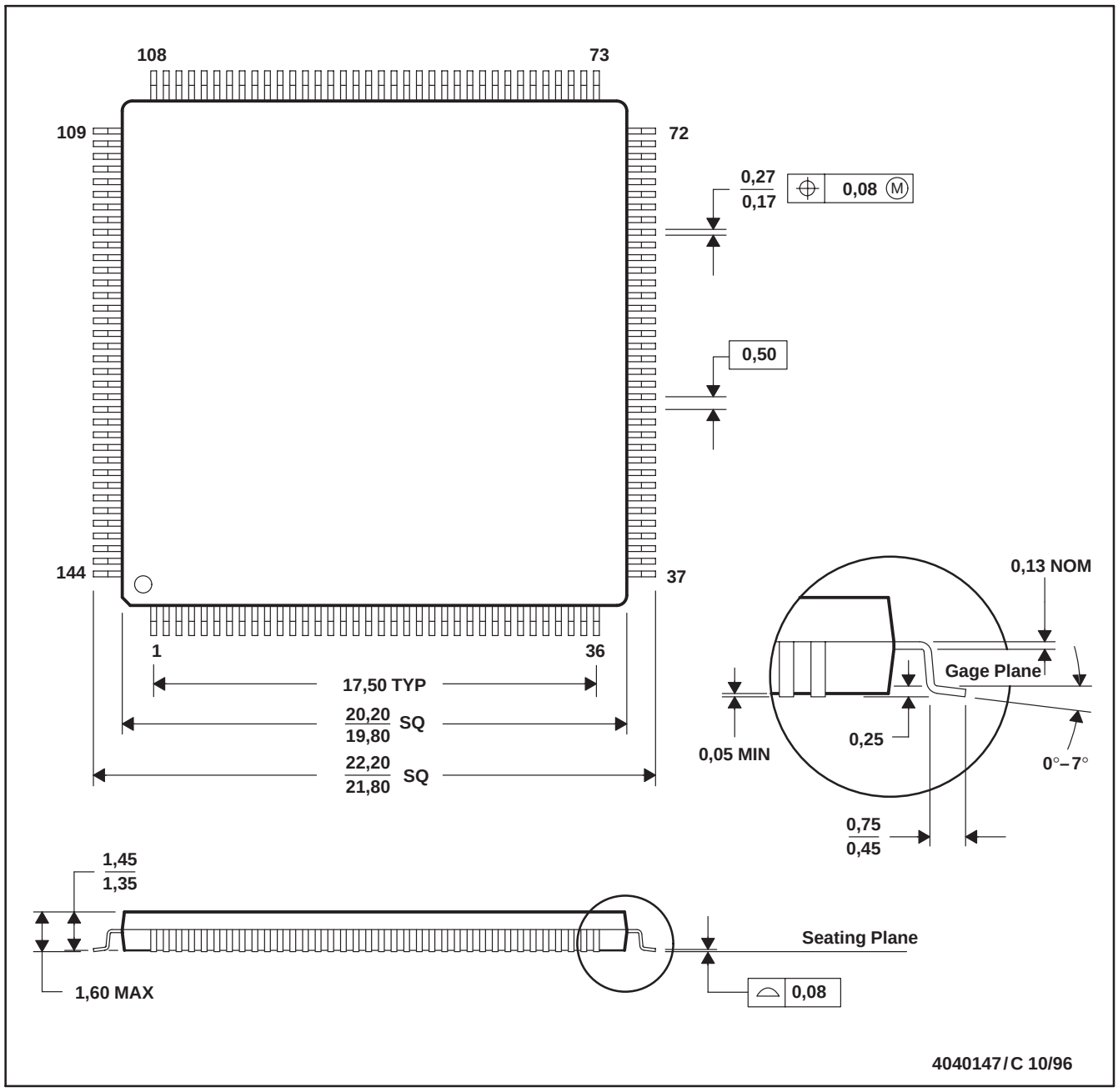
NOTE:

This product is for high-volume CE applications only. For a complete datasheet or more information contact support@ti.com.

(1) IEEE Std 1394-1995, *IEEE Standard for a High Performance Serial Bus* IEEE Std 1394a–2000, *IEEE Standard for a High Performance Serial Bus – Amendment 1*

MTQF017A – OCTOBER 1994 – REVISED DECEMBER 1996

PGE (S-PQFP-G144) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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