TEXAS INSTRUMENTS

UA78M
SLVS059U – JUNE 1976 – REVISED MAY 2024

UA78M 35V, 500mA, Positive-Voltage Linear Regulator

1 Features

- Input voltage range (V_{IN}): 5.3V to 35V
- Output voltage range (V_{OUT}): 3.3V to 12V
- Output current (I_{OUT}): Up to 500mA
- Quiescent current I_Q: 4.5mA
- Built-in short-circuit current limiting and thermal protection
- Stable without any external components
- Operating temperature range:
  - Legacy chip C versions: 0°C to +125°C
  - Legacy chip I version: –40°C to +125°C
  - New chip: –40°C to +125°C
- Packages:
  - 3-pin, 6.5mm × 7mm SOT-223
  - 3-pin, 6.6mm × 10.11mm TO-252

2 Applications

- On-board charging
- Washers and dryers
- Residential lighting
- Battery backup units (BBU)
- Air conditioner outdoor units

3 Description

The UA78M fixed-voltage integrated-circuit voltage regulators is designed for a wide range of applications. Use the UA78M for on-card regulation to eliminate noise and distribution problems associated with single-point regulation. The UA78M is also used with power-pass elements to make high-current voltage regulators. The UA78M delivers up to 500mA of output current. Additionally, the UA78M does not need an external capacitor for stable operation across the load current range. The internal current-limiting and thermal-shutdown features of this regulator help protect the device from overload.
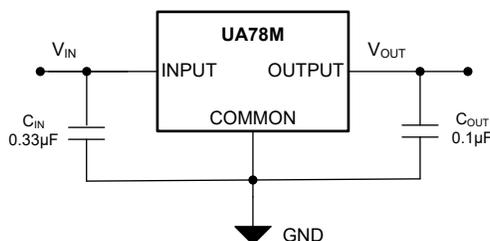
The UA78M is characterized for the junction temperature range of –40°C to +125°C. See the *Device Nomenclature* table for more details.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
UA78M	DCY (SOT-223, 3)	6.5mm × 7mm
	KVU (TO-252, 3)	6.6mm × 10.11mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.

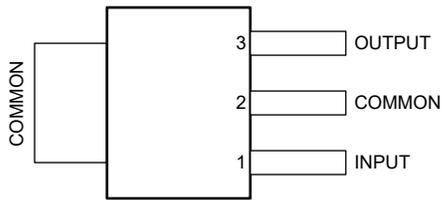(2) The package size (length × width) is a nominal value and includes pins, where applicable.
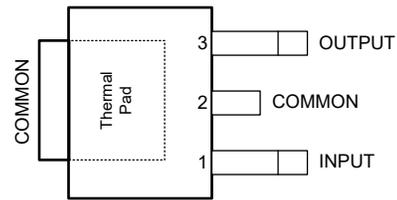

Simplified Schematic

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Product Folder Links: *UA78M*

4 Pin Configuration and Functions

Figure 4-1. DCY Package, 3-Pin SOT-223 (Top View)

Figure 4-2. KVU Package, 3-Pin TO-252 (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
COMMON	2	—	Ground
INPUT	1	I	Input pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the input capacitor as close to the INPUT and COMMON pins of the device as possible.
OUTPUT	3	O	Output pin. Use the recommended capacitor value as listed in the *Recommended Operating Conditions* table. Place the output capacitor as close to the OUTPUT and COMMON pins of the device as possible.

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Input voltage, V_I (for Legacy Chip)	UA78M33C, UA78M33I, UA78M05C, UA78M05I, UA78M06C, UA78M08C, UA78M09C, UA78M10C, UA78M12C		35	V
Input voltage, V_I (for New Chip)	UA78M33C, UA78M33I, UA78M05C, UA78M05I		45	V
Output voltage, V_o (for New Chip)		-0.3	12	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	TYP	MAX	UNIT
VI	Input voltage	UA78M33C , UA78M33I (Legacy chip)	5.3		25	V
		UA78M33C, UA78M33I (New chip)	5.3		30	
		UA78M05C, UA78M05I (Legacy chip)	7		25	
		UA78M05C, UA78M05I (New chip)	7		30	
		UA78M06 (Legacy chip)	8		25	
		UA78M08 (Legacy chip)	10.5		25	
		UA78M09 (Legacy chip)	11.5		26	
		UA78M10 (Legacy chip)	12.5		28	
		UA78M12 (Legacy chip)	14.5		30	
C_{IN} [2]	Input capacitor [3]	Input capacitor [3]		0.33		µF
C_{OUT} [2]	Output capacitor [4]	Output capacitor [4]		0.1		µF
I_O	Output current				500	mA
T_J	Operating junction temperature	UA78MxxC (Legacy chip)	0		125	°C
		UA78MxxI (Legacy chip)	−40		125	
		UA78MxxC , UA78MxxI (New chip)	−40		125	

(1) All voltages are with respect to GND.
(2) UA78M regulator doesn't need any external capacitors for the the LDO stability.
(3) An input capacitor with value of 0.33 µF is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(4) An output capacitor with value of 0.1 µF is recommended to improve the load and line transient performance of the UA78L regulator.

5.4 Thermal Information

THERMAL METRIC[1]		UA78Mxx				UNIT
		DCY (Legacy Chip)	DCY (New Chip)	KCS (Legacy Chip only)	KVU (Legacy Chip only)	
		3 PINS	3 PINS	3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	53	77.7	19	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	30.6	44.6	17	–	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	3	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics: UA78M33 (Both Legacy and New Chip)

specified at T_J = 25°C, V_I = 8 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Output voltage	V_I = 8V to 20V, and I_O = 5mA to 350mA	Legacy chip		3.2	3.3	3.4	V
		New chip		3.2	3.3	3.4	
		T_J = full range	Legacy chip	3.1	3.3	3.5	
		T_J = –40°C to 125°C	New chip	3.1	3.3	3.5	
Output voltage line regulation	I_O = 200mA, V_{IN} = 5.3V to 25V	Legacy chip			9	100	mV
		New chip			28	50	
	I_O = 200mA, V_{IN} = 8V to 25V	Legacy chip			3	50	
		New chip			9	20	
Ripple rejection	V_I = 8V to 18V, f = 120Hz	I_O = 100mA, T_J = full range	Legacy chip	62			dB
		I_O = 100mA, T_J = –40°C to 125°C	New chip	57			
		I_O = 300mA	Legacy chip	62	80		
			New chip	56	62		
Output voltage load regulation	V_I = 8V and I_O = 5mA to 500mA	Legacy chip			20	100	mV
		New chip			20	40	
Temperature coefficient of output voltage	I_O = 5mA	T_J = full range	Legacy chip		–1		mV/°C
		T_J = –40°C to 125°C	New chip		–1		
Output noise voltage	f = 10 Hz to 100 kHz, and T_J = 25°C	Legacy chip			40	200	µV
		New chip			80	200	
Dropout voltage		Legacy chip			2.0		V
		New chip			2.0		
Bias current		Legacy chip			4.5	6	mA
		New chip		3.5	4.5	6	
Bias current change	V_I = 8V to 25V, I_O = 200mA	T_J = full range	Legacy chip			0.8	mA
		T_J = –40°C to 125°C	New chip			0.8	
	I_O = 5 mA to 350mA	T_J = full range	Legacy chip			0.5	
		T_J = –40°C to 125°C	New chip			0.5	
Short-circuit output current	V_I = 35V	Legacy chip			300		mA
	V_I = 30V	New chip			400		

5.5 Electrical Characteristics: UA78M33 (Both Legacy and New Chip) (continued)

specified at T_J = 25°C, V_I = 8 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Peak output current		Legacy chip			700		mA
		New chip			735		

(1)   Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

5.6 Electrical Characteristics: UA78M05 (Both Legacy and New Chip)

specified at T_J = 25°C, V_I = 10V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Output voltage	V_I = 7V to 20V, and I_O = 5mA to 350mA	Legacy chip and New chip		4.8	5	5.2	V
		T_J = full range	Legacy chip	4.75		5.25	
	V_I = 7.2V to 20V, and I_O = 5mA to 350mA	T_J = –40°C to 125°C	New chip	4.75		5.25	
Output voltage line regulation	I_O = 200mA, V_{IN} = 7V to 25V	Legacy chip			3	100	mV
	I_O = 200mA, V_{IN} = 7.2V to 25V	New chip			13	30	
	I_O = 200mA, V_{IN} = 8V to 25V	Legacy chip			1	50	
		New chip			13	30	
Ripple rejection	V_I = 8V to 18V, f = 120Hz	I_O = 100mA, T_J = full range	Legacy chip	62			dB
		I_O = 100mA, T_J = –40°C to 125°C	New chip	56			
		I_O = 300mA	Legacy chip	62	80		
			New chip	52	58		
Output voltage load regulation	I_O = 5mA to 500mA	Legacy chip			20	100	mV
		New chip			25	60	
	I_O = 5mA to 200mA	Legacy chip			10	50	
		New chip			5	20	
Temperature coefficient of output voltage	I_O = 5mA	T_J = full range	Legacy chip		–1		mV/°C
		T_J = –40°C to 125°C	New chip		–1		
Output noise voltage	f = 10 Hz to 100 kHz	Legacy chip			40	200	µV
		New chip			120	200	
Dropout voltage		Legacy chip			2.0		V
		New chip			2.0		
Bias current		Legacy chip			4.5	6	mA
		New chip		3.5	4.5	6	
Bias current change	V_I = 8V to 25V, I_O = 200mA	T_J = full range	Legacy chip			0.8	mA
		T_J = –40°C to 125°C	New chip			0.8	
	I_O = 5 mA to 350mA	T_J = full range	Legacy chip			0.5	
		T_J = –40°C to 125°C	New chip			0.5	
Short-circuit output current	V_I = 35V	Legacy chip			300		mA
	V_I = 30V	New chip			400		
Peak output current		Legacy chip			700		mA
		New chip			760		

(1)   Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

Product Folder Links: *UA78M*

5.7 Electrical Characteristics: UA78M06C (Legacy Chip Only)

specified at T_J = 25°C, V_I = 11V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Output voltage	V_I = 8V to 21V, and I_O = 5mA to 350mA		5.75	6	6.25	V
		T_J = 0°C to 125°C	5.7		6.3	
Output voltage line regulation	I_O = 200mA, V_{IN} = 8V to 25V			5	100	mV
	I_O = 200mA, V_{IN} = 9V to 25V			1.5	50	
Ripple rejection	V_I = 8V to 18V, f = 120Hz	I_O = 100mA, T_J = 0°C to 125°C	59			dB
		I_O = 300mA	59	80		
Output voltage load regulation	I_O = 5mA to 500mA			20	120	mV
	I_O = 5mA to 200mA			10	60	
Temperature coefficient of output voltage	I_O = 5mA	T_J = 0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz,			45		µV
Dropout voltage				2.0		V
Bias current			3.5	4.5	6	mA
Bias current change	V_I = 9V to 25V, I_O = 200mA	T_J = 0°C to 125°C			0.8	mA
	I_O = 5 mA to 350mA	T_J = 0°C to 125°C			0.5	
Short-circuit output current	V_I = 35V			270		mA
Peak output current				700		mA

(1)   Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

5.8 Electrical Characteristics: UA78M08C (Legacy Chip Only)

specified at T_J = 25°C, V_I = 14V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Output voltage	V_I = 10.5V to 23V, and I_O = 5mA to 350mA		7.7	8	8.3	V
		T_J = 0°C to 125°C	7.6		8.4	
Output voltage line regulation	I_O = 200mA, V_{IN} = 10.5V to 25V			6	100	mV
	I_O = 200mA, V_{IN} = 11V to 25V			2	50	
Ripple rejection	V_I = 11V to 21.5V, f = 120Hz	I_O = 100mA, T_J = 0°C to 125°C	56			dB
		I_O = 300mA	56	80		
Output voltage load regulation	I_O = 5mA to 500mA			25	160	mV
	I_O = 5mA to 200mA			10	80	
Temperature coefficient of output voltage	I_O = 5mA	T_J = 0°C to 125°C		−1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz,			52		µV
Dropout voltage				2.0		V
Bias current				4.5	6	mA
Bias current change	V_I = 9V to 25V, I_O = 200mA	T_J = 0°C to 125°C			0.8	mA
	I_O = 5 mA to 350mA	T_J = 0°C to 125°C			0.5	
Short-circuit output current	V_I = 35V			250		mA
Peak output current				700		mA

(1)   Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

5.9 Electrical Characteristics: UA78M09 (Legacy Chip Only)

at specified junction temperature, V_I = 16 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Output voltage	V_I = 11.5V to 24V, and I_O = 5mA to 350mA		8.6	9	9.4	V
		T_J = 0°C to 125°C	8.5		9.5	
Output voltage line regulation	I_O = 200mA, V_{IN} = 11.5V to 26V			6	100	mV
	I_O = 200mA, V_{IN} = 12V to 26V			2	50	
Ripple rejection	V_I = 13V to 23V, f = 120Hz	I_O = 100mA, T_J = 0°C to 125°C	56			dB
		I_O = 300mA	56	80		
Output voltage load regulation	I_O = 5mA to 500mA			25	180	mV
	I_O = 5mA to 200mA			10	90	
Temperature coefficient of output voltage	I_O = 5mA	T_J = 0°C to 125°C		-1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			58		µV
Dropout voltage				2.0		V
Bias current				4.6	6	mA
Bias current change	V_I = 11.5V to 26V, I_O = 200mA	T_J = 0°C to 125°C			0.8	mA
	I_O = 5 mA to 350mA	T_J = 0°C to 125°C			0.5	
Short-circuit output current	V_I = 35V			250		mA
Peak output current				700		mA

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

5.10 Electrical Characteristics: UA78M10 (Legacy Chip Only)

at specified junction temperature, V_I = 17 V, C_{IN} = 0.33 µF, C_{OUT} = 0.1µF, and I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Output voltage	V_I = 12.5V to 25V, and I_O = 5mA to 350mA		9.6	10	10.4	V
		T_J = 0°C to 125°C	9.5		10.5	
Output voltage line regulation	I_O = 200mA, V_{IN} = 12.5V to 28V			7	100	mV
	I_O = 200mA, V_{IN} = 14V to 28V			2	50	
Ripple rejection	V_I = 15V to 25V, f = 120Hz	I_O = 100mA, T_J = 0°C to 125°C	59			dB
		I_O = 300mA	55	80		
Output voltage load regulation	I_O = 5mA to 500mA			25	200	mV
	I_O = 5mA to 200mA			10	100	
Temperature coefficient of output voltage	I_O = 5mA	T_J = 0°C to 125°C		-1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			64		µV
Dropout voltage				2.0		V
Bias current				4.7	6	mA
Bias current change	V_I = 12.5V to 28V, I_O = 200mA	T_J = 0°C to 125°C			0.8	mA
	I_O = 5 mA to 350mA	T_J = 0°C to 125°C			0.5	
Short-circuit output current	V_I = 35V			245		mA
Peak output current				700		mA

(1) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

Product Folder Links: *UA78M*

5.11 Electrical Characteristics: UA78M12 (Legacy Chip Only)

at specified at T_J = 25°C, V_I = 19 V, C_{IN} = 0.33 μF, C_{OUT} = 0.1μF and I_O = 350 mA (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
Output voltage	V_I = 14.5V to 27V, and I_O = 5mA to 350mA		11.5	12	12.5	V
		T_J = 0°C to 125°C	11.4		12.6	
Output voltage line regulation	I_O = 200mA, V_{IN} = 14.5V to 30V			8	100	mV
	I_O = 200mA, V_{IN} = 16V to 30V			2	50	
Ripple rejection	V_I = 15V to 25V, f = 120Hz	I_O = 100mA,T_J = 0°C to 125°C	55			dB
		I_O = 300mA	55	80		
Output voltage load regulation	I_O = 5mA to 500mA			25	240	mV
	I_O = 5mA to 200mA			10	120	
Temperature coefficient of output voltage	I_O = 5mA	T_J = 0°C to 125°C		-1		mV/°C
Output noise voltage	f = 10 Hz to 100 kHz			75		μV
Dropout voltage				2.0		V
Bias current				4.8	6	mA
Bias current change	V_I = 14.5V to 30V, I_O = 200mA	T_J = 0°C to 125°C			0.8	mA
	I_O = 5 mA to 350mA	T_J = 0°C to 125°C			0.5	
Short-circuit output current	V_I = 35V			240		mA
Peak output current				700		mA

(1)   Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.
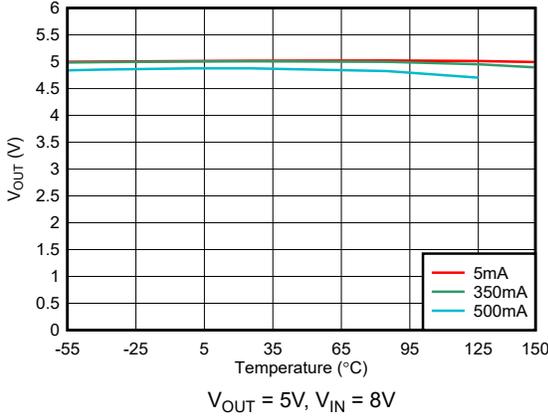
5.12 Typical Characteristics

Figure 5-1. Output Voltage vs Temperature (New Chip)

V_{OUT} = 5V, V_{IN} = 8V
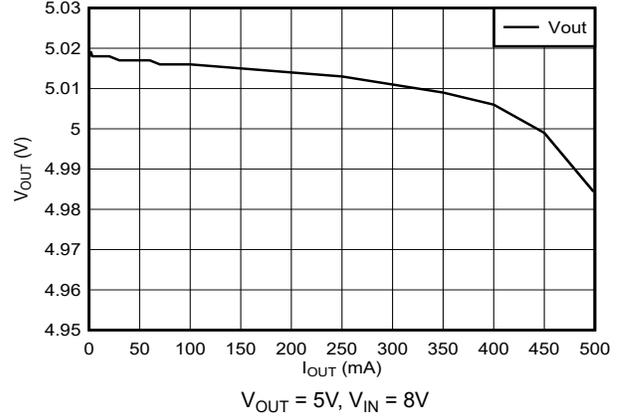
Figure 5-2. Load Regulation at T$_J$ = 25°C (New Chip)

V_{OUT} = 5V, V_{IN} = 8V
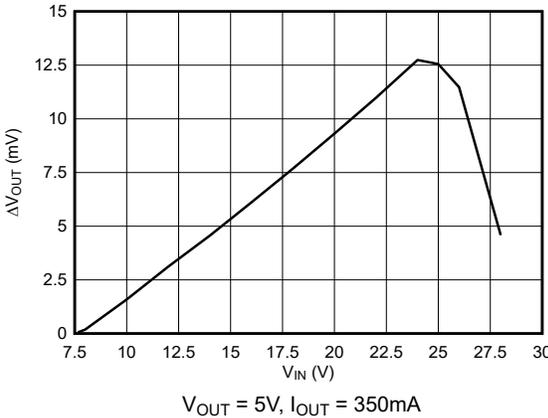
Figure 5-3. Line Regulation at T$_J$ = 25°C (New Chip)

V_{OUT} = 5V, I_{OUT} = 350mA

Figure 5-4. Bias Current vs Input Voltage at T$_J$ = 25°C (New Chip)
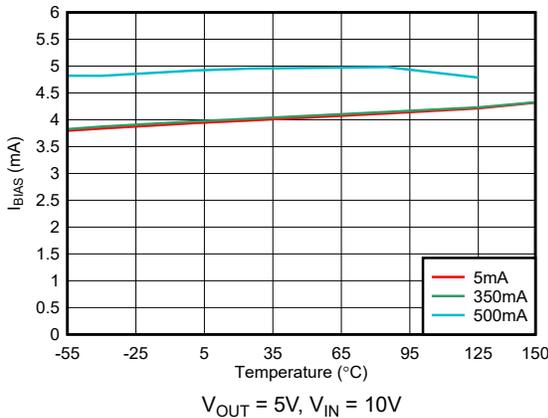
Figure 5-5. Bias Current vs Temperature (New Chip)

V_{OUT} = 5V, V_{IN} = 10V
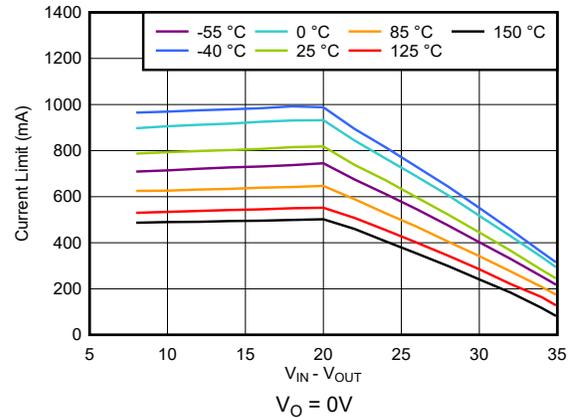
Figure 5-6. I$_{CL}$ vs Input Voltage (New Chip)

V_O = 0V

Product Folder Links: *UA78M*

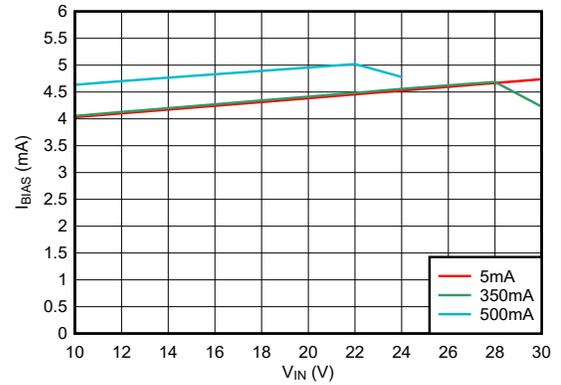## 5.12 Typical Characteristics (continued)

V_O = 3.3V
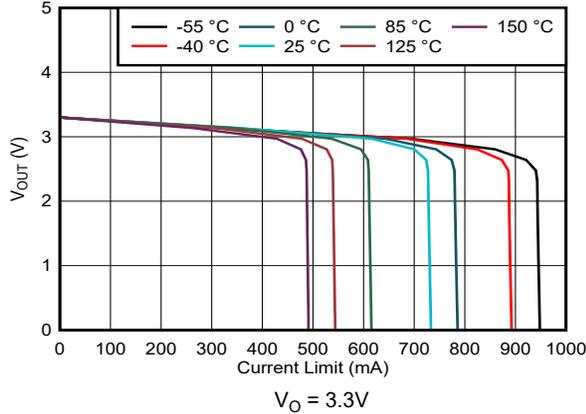
Figure 5-7. Output Voltage vs I_{CL} (New Chip)

V_O = 5V
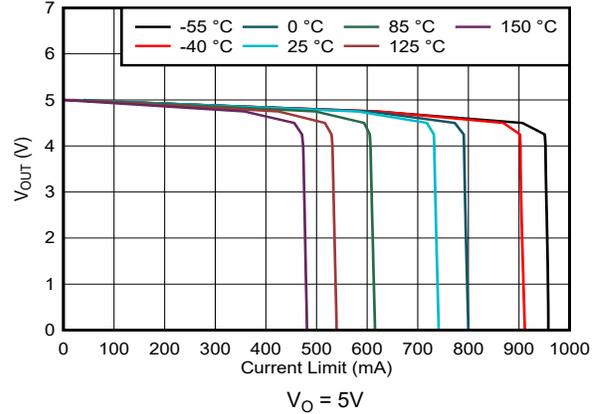
Figure 5-8. Output Voltage vs I_{CL} (New Chip)

V_I = 8V to 18V, T_J = 25°C
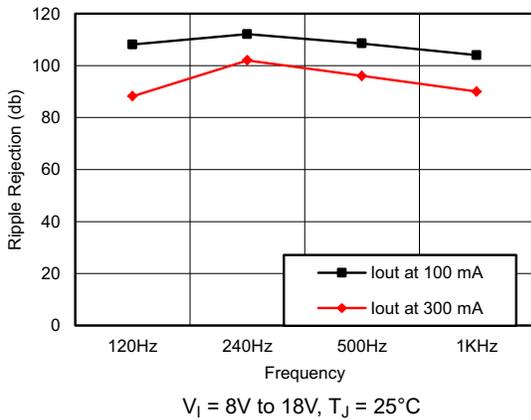
Figure 5-9. PSRR vs Frequency and I_O (Legacy Chip)

V_I = 13V, V_O = 5V

Figure 5-10. PSRR vs Frequency and I_O (New Chip)

V_{IN} = 10V, V_{OUT} = 5V, I_{OUT} = 100mA, C_{OUT} = 0.1μF

Figure 5-11. Noise vs Frequency (New Chip)

6 Detailed Description

6.1 Overview

The UA78M fixed-voltage, integrated-circuit voltage regulator is designed for a wide range of applications. The UA78M supports a wide range of input voltages and delivers 500mA of load current.

This device features internal current-limiting and thermal shutdown mechanisms. To provide reliable operation across wide V_I ranges, the current-limiting mechanism 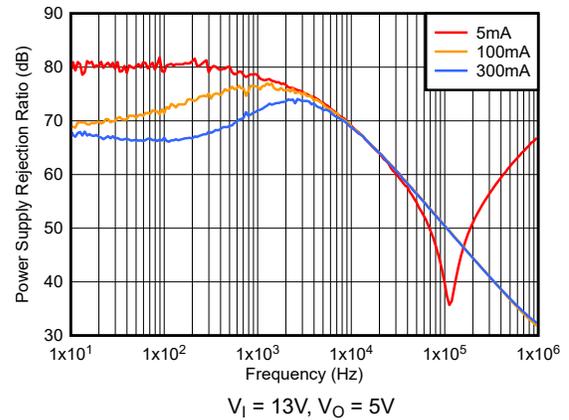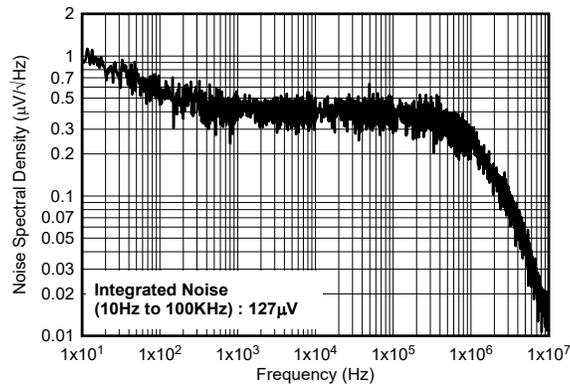modulates the load current capacity both by monitoring the V_O level and the difference between the V_I and V_O voltage levels. The operating ambient temperature range of the device is –40°C to +125°C for all variants.

6.2 Functional Block Diagram
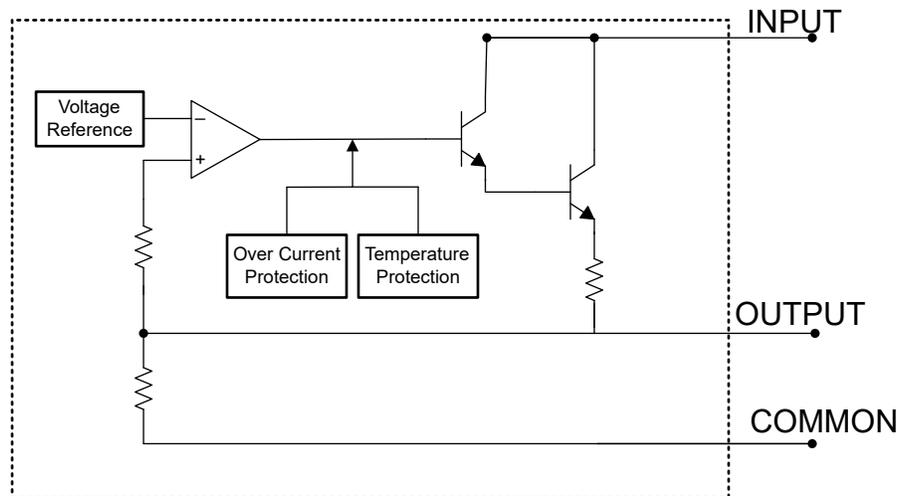
6.3 Feature Description

6.3.1 Current Limit

The device has an internal current-limit circuit that protects the regulator during transient high-load current faults or shorting events. In a high-load current fault, the current limit scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current-limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in current limit, the pass transistor dissipates power [$(V_I – V_O) \times I_{CL}$]. For more information on current limits, see the *Know Your Limits* application note.

Product Folder Links: *UA78M*

To achieve a safe operation across a wide range of Input voltage, the UA78M also has a built-in protection mechanism with current limit. The protection mechanism decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. This protection is designed to provide some output current at all values of input-to-output voltage limits defined in the *Recommended Operating Conditions* table. Figure 6-1 shows the behavior of the current limit variation.
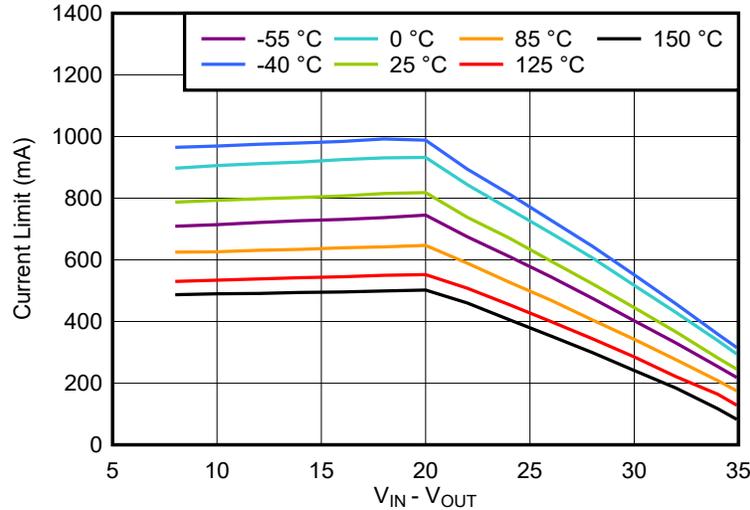

Figure 6-1. Current-Limit vs V$_{Head\text{-}room}$ Behavior (New Chip)

6.3.2 Dropout Voltage (V$_{DO}$)

Dropout voltage (V$_{DO}$) is defined as the input voltage minus the output voltage (V$_I$ – V$_O$) at the rated output current (I$_{RATED}$), where the pass transistor is fully on. I$_{RATED}$ is the maximum I$_O$ listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

6.3.3 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T$_J$) of the pass transistor rises to T$_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis makes sure that the device resets (turns on) when the temperature falls to T$_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start-up can be high from large V$_I$ – V$_O$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start-up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

6.4 Device Functional Modes

Table 6-1 provides a quick comparison between the normal and dropout modes of operation.

Table 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_I	I_O
Normal	$V_I > V_{OUT(nom)} + V_{DO}$	$I_O < I_{CL}$
Dropout	$V_I < V_{OUT(nom)} + V_{DO}$	$I_O < I_{CL}$

6.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_O < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_I < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

Product Folder Links: *UA78M*

7 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The UA78M is designed for use as a linear regulator with only a few external components needed. Use the UA78M to clean power-supply noise by attenuating ripple on the input signal.

7.2 Typical Application

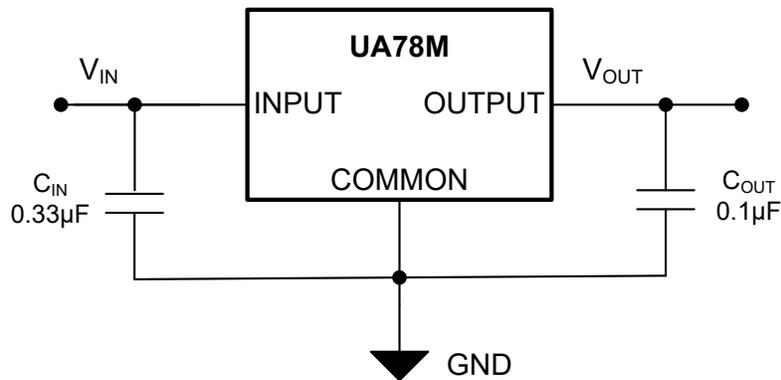The UA78M is typically used as a fixed-output linear regulator, sourcing current up to 500mA into a load.

Figure 7-1. Fixed-Output Regulator

7.2.1 Design Requirements

Tie the COMMON pin to ground to set the OUTPUT pin to the desired fixed output voltage.

Although not required, a 0.33µF bypass capacitor is recommended on the input, and a 0.1µF bypass capacitor is recommend on the output.

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

Although the input and output capacitors are not required for stability, good analog design practice is to connect a capacitor from INPUT to COMMON and from OUTPUT to COMMON. The input capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved by using a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

7.2.2.2 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. Make sure the PCB area around the regulator has few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_I - V_O) \times I_O \tag{1}$$

Note

Power dissipation is minimized, and therefore greater efficiency be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{2}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance. As mentioned in the *An empirical analysis of the impact of board layout on LDO thermal performance* application note, $R_{\theta JA}$ is improved by 35% to 55% compared to the *Thermal Information* table value with the PCB board layout optimization.

7.2.2.3 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{3}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \tag{4}$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

Product Folder Links: *UA78M*

7.2.2.4 External Capacitor Requirements

The UA78M is designed to be stable without any external component. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but use good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

7.2.2.5 Overload Recovery

As the input voltage rises when power is first turned on, the output follows the input, allowing the regulator to start up into very heavy loads. The input-to-output voltage differential is small during start up when the input voltage is rising, allowing the regulator to supply large output currents. With a high input voltage, a problem occurs where removing an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so the behavior is not unique to the UA78M.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately when removing a short circuit after the input voltage is already turned on. The load line for such a load has the possibility to intersect the output current curve at two points. If this condition happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply is potentially cycled down to zero and brought up again to make the output recover to the desired voltage operating point.
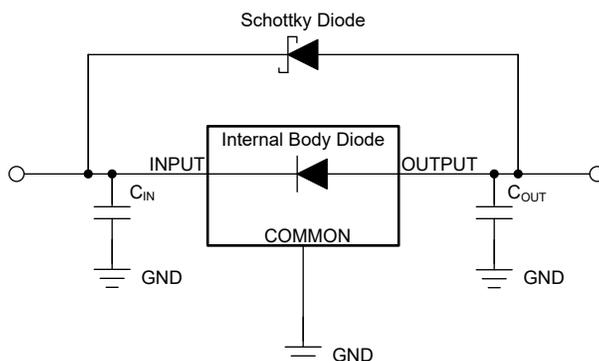
7.2.2.6 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the emitter-base junction of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_O \leq V_I + 7V$. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

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Product Folder Links: *UA78M*

Figure 7-2 shows one approach for protecting the device.

Figure 7-2. Example Circuit for Reverse Current Protection Using a Schottky Diode

7.2.2.7 Polarity Reversal Protection

In many applications, a voltage regulator powers a load that is not connected to ground, but instead, is connected to a voltage source of the opposite polarity (for example, operational amplifiers, level-shifting circuits, and so on). During start-up and short-circuit events, this connection can lead to polarity reversal of the regulator output and can damage the internal components of the regulator.

To avoid polarity reversal on the regulator output, use external protection to protect the device.

Figure 7-3 shows one approach for protecting the device.
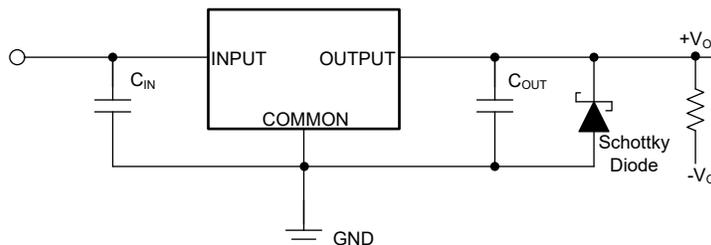
Figure 7-3. Example Circuit for Polarity Reversal Protection Using a Schottky Diode

7.2.3 Application Curves
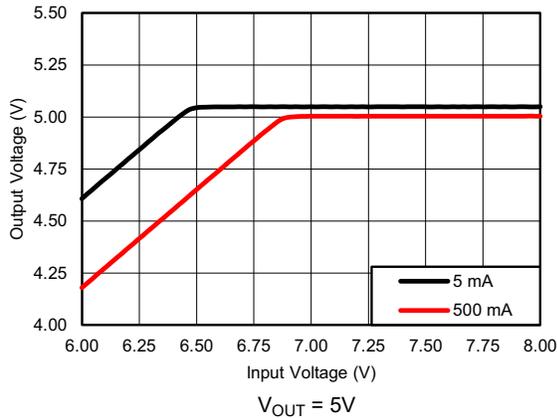
Figure 7-4. V_{IN} vs V_{OUT} at T_J = 25°C (Legacy Chip)

V_{OUT} = 5V
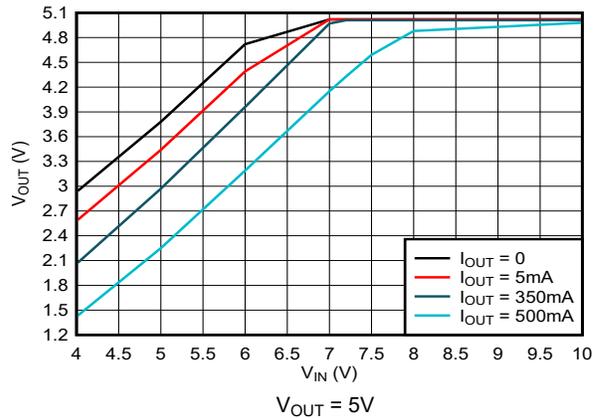
Figure 7-5. V_{IN} vs V_{OUT} at T_J = 25°C (New Chip)

V_{OUT} = 5V
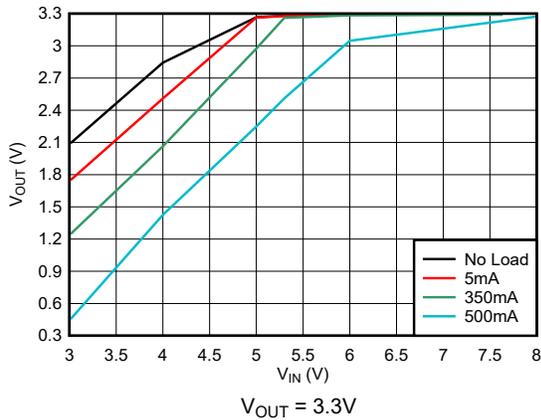
Figure 7-6. V_{IN} vs V_{OUT} at T_J = 25°C (New Chip)

V_{OUT} = 3.3V
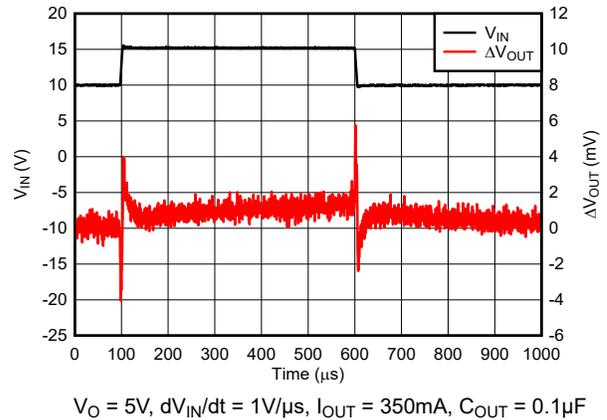
Figure 7-7. Line Transient Behavior (New Chip)

V_O = 5V, dV_{IN}/dt = 1V/µs, I_{OUT} = 350mA, C_{OUT} = 0.1µF
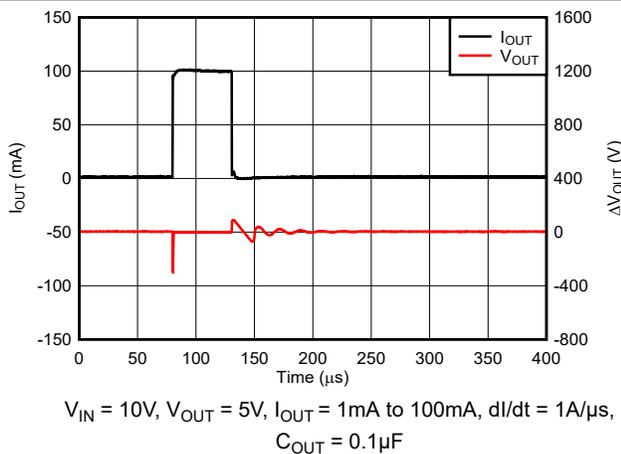
Figure 7-8. Load Transient Behavior (New Chip)

V_{IN} = 10V, V_{OUT} = 5V, I_{OUT} = 1mA to 100mA, dI/dt = 1A/µs, C_{OUT} = 0.1µF
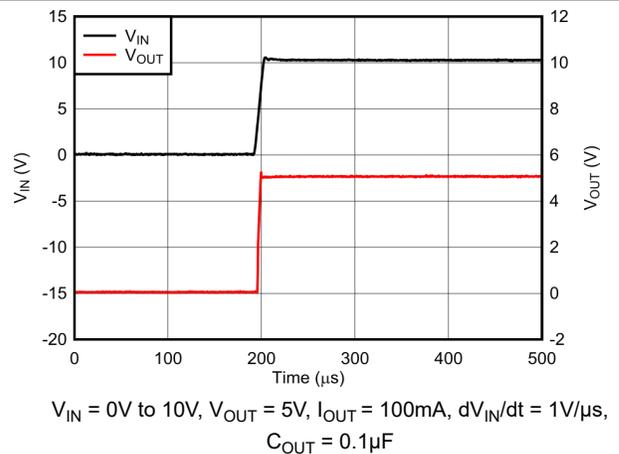
Figure 7-9. Start-Up (New Chip)

V_{IN} = 0V to 10V, V_{OUT} = 5V, I_{OUT} = 100mA, dV_{IN}/dt = 1V/µs, C_{OUT} = 0.1µF

Product Folder Links: *UA78M*

7.3 System Examples

7.3.1 Positive Regulator in Negative Configuration

Figure 7-10 shows the UA78M as a positive regulator used in a negative configuration. Make sure V_I floats in this configuration.
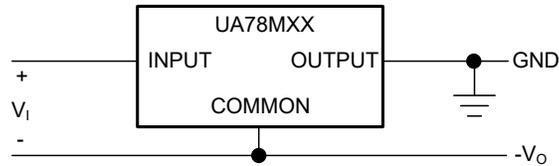
Figure 7-10. Positive Regulator in Negative Configuration

7.3.2 Current Limiter Circuit

Figure 7-11 shows an example of using the UA78M as a current limiter. The output current limit is set by Equation 5,

$$I_O = \left(\frac{V_O}{R1}\right) + I_O \text{ Bias Current}$$

(5)
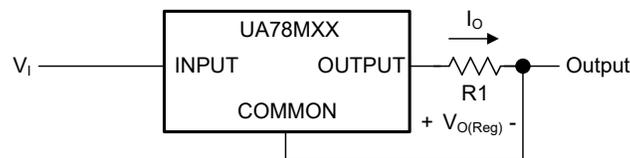
Figure 7-11. Current Limiter Example

7.4 Power Supply Recommendations

See the *Recommended Operating Conditions* for the recommended power supply voltages for each variation of the UA78M. Different orderable part numbers are able to tolerate different levels of voltage. Also, place a decoupling capacitor on the output to limit noise on the input.

7.5 Layout

7.5.1 Layout Guidelines

Keep trace widths large enough to eliminate problematic I×R voltage drops at the input and output pins. Place bypass capacitors as close to the UA78M as possible. Additional copper and vias connected to ground facilitate additional thermal dissipation, preventing the device from reaching thermal overload.

Product Folder Links: *UA78M*

7.5.2 Layout Example
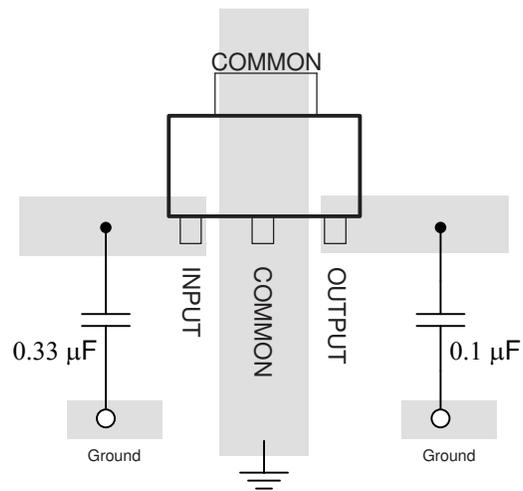
Figure 7-12. Layout Diagram

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the UA78L. The UA78MEVM (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.1.2 Device Nomenclature

Table 8-1. Device Nomenclature

PRODUCT[1]	V$_{OUT}$
UA78M**xxyyyz**	**xx** is the nominal output voltage (for example, 05 = 5.0V, 15 = 15.0V). **yyy** is the package designator. **z** is the package quantity. Devices can ship with the legacy chip (CSO: SFB) or the new chip (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. Device performance for new and legacy chips is denoted throughout the data sheet.

(1)   For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision T (January 2015) to Revision U (May 2024)   **Page**

Changes from Revision S (May 2013) to Revision T (January 2015)   **Page**

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN78MCDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C5	Samples
UA78M05CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C5	Samples
UA78M05CDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C5	Samples
UA78M05CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C5	Samples
UA78M05CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C5	Samples
UA78M05CKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA78M05C	Samples
UA78M05CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA78M05C	Samples
UA78M05CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	78M05C	Samples
UA78M05IDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78M05IDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78M05IDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78M05IDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	J5	Samples
UA78M05IKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	UA78M05I	Samples
UA78M05IKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	-40 to 125	UA78M05I	Samples
UA78M05IKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	78M05I	Samples
UA78M06CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	78M06C	Samples
UA78M08CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C8	Samples
UA78M08CDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C8	Samples
UA78M08CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C8	Samples
UA78M08CKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA78M08C	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA78M08CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA78M08C	Samples
UA78M08CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	78M08C	Samples
UA78M09CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	78M09C	Samples
UA78M10CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	78M10C	Samples
UA78M12CKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA78M12C	Samples
UA78M12CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA78M12C	Samples
UA78M12CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	78M12C	Samples
UA78M33CDCY	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C3	Samples
UA78M33CDCYG3	ACTIVE	SOT-223	DCY	4	80	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C3	Samples
UA78M33CDCYR	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C3	Samples
UA78M33CDCYRG3	ACTIVE	SOT-223	DCY	4	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	0 to 125	C3	Samples
UA78M33CKCS	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA78M33C	Samples
UA78M33CKCSE3	ACTIVE	TO-220	KCS	3	50	RoHS & Green	SN	N / A for Pkg Type	0 to 125	UA78M33C	Samples
UA78M33CKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	78M33C	Samples
UA78M33IKVURG3	ACTIVE	TO-252	KVU	3	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	78M33I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
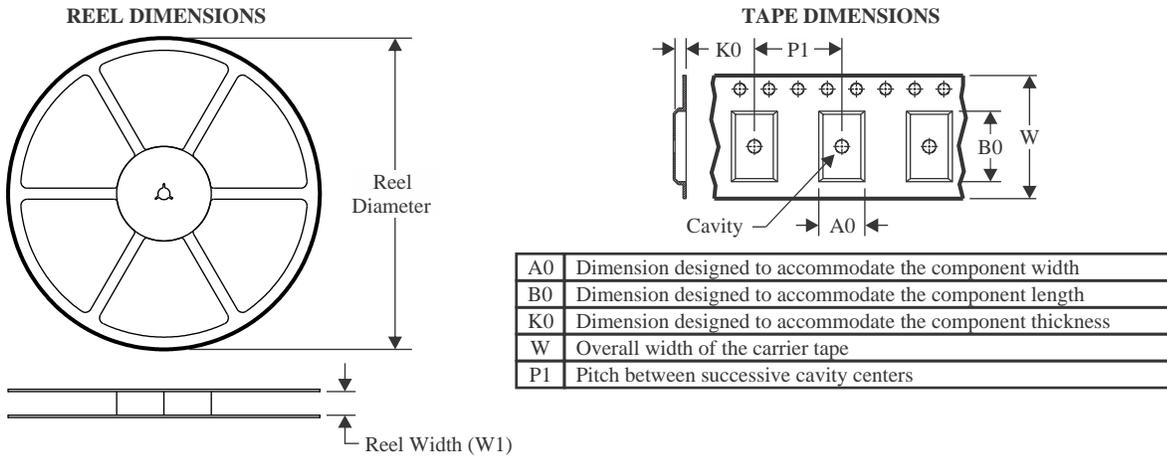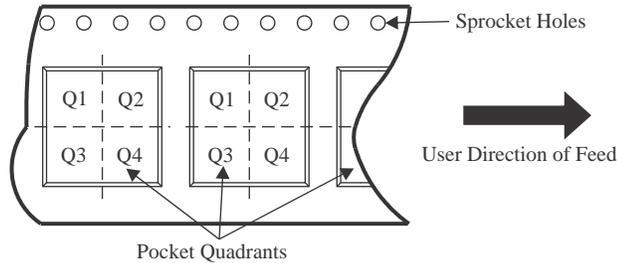
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UA78M :

• Automotive : UA78M-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78M05CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
UA78M05CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
UA78M05CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
UA78M05CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA78M05IDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
UA78M05IDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
UA78M05IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA78M05IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
UA78M06CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA78M08CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
UA78M08CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA78M09CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA78M10CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA78M10CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
UA78M12CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA78M33CDCYR	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3

PACKAGE MATERIALS INFORMATION

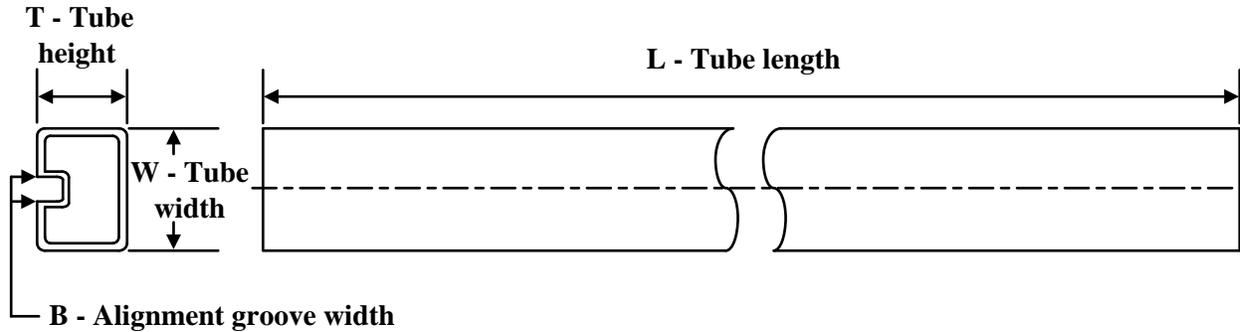| Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA78M33CDCYR	SOT-223	DCY	4	2500	330.0	12.4	6.55	7.25	1.9	8.0	12.0	Q3
UA78M33CKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
UA78M33IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.8	8.0	16.0	Q2
UA78M33IKVURG3	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS
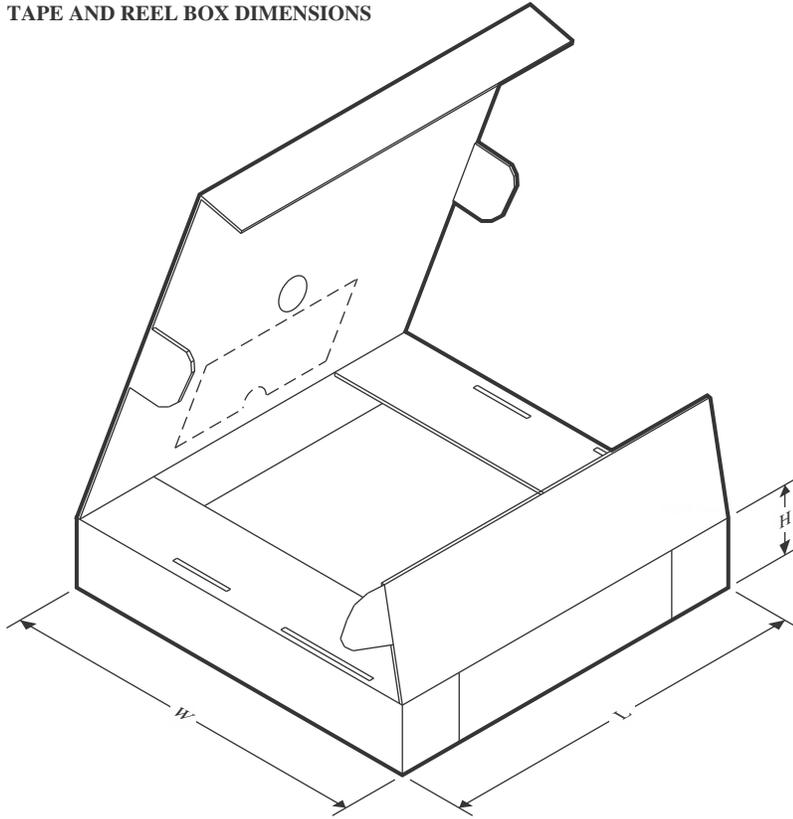
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78M05CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
UA78M05CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
UA78M05CKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
UA78M05CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
UA78M05IDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
UA78M05IDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
UA78M05IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
UA78M05IKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
UA78M06CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
UA78M08CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
UA78M08CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
UA78M09CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
UA78M10CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
UA78M10CKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
UA78M12CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0
UA78M33CDCYR	SOT-223	DCY	4	2500	340.0	340.0	38.0
UA78M33CDCYR	SOT-223	DCY	4	2500	336.0	336.0	48.0
UA78M33CKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA78M33IKVURG3	TO-252	KVU	3	2500	350.0	334.0	47.0
UA78M33IKVURG3	TO-252	KVU	3	2500	340.0	340.0	38.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UA78M05CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
UA78M05CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
UA78M05CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M05CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M05CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M05CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M05IDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
UA78M05IDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
UA78M05IKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M05IKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M05IKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M05IKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M08CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
UA78M08CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
UA78M08CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M08CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M08CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M08CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M12CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M12CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M12CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M12CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M33CDCY	DCY	SOT-223	4	80	559	8.6	500	3.6
UA78M33CDCYG3	DCY	SOT-223	4	80	559	8.6	500	3.6
UA78M33CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M33CKCS	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M33CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6
UA78M33CKCSE3	KCS	TO-220	3	50	532	34.1	700	9.6

DCY (R-PDSO-G4)   **PLASTIC SMALL-OUTLINE**

4202506/B 06/2002
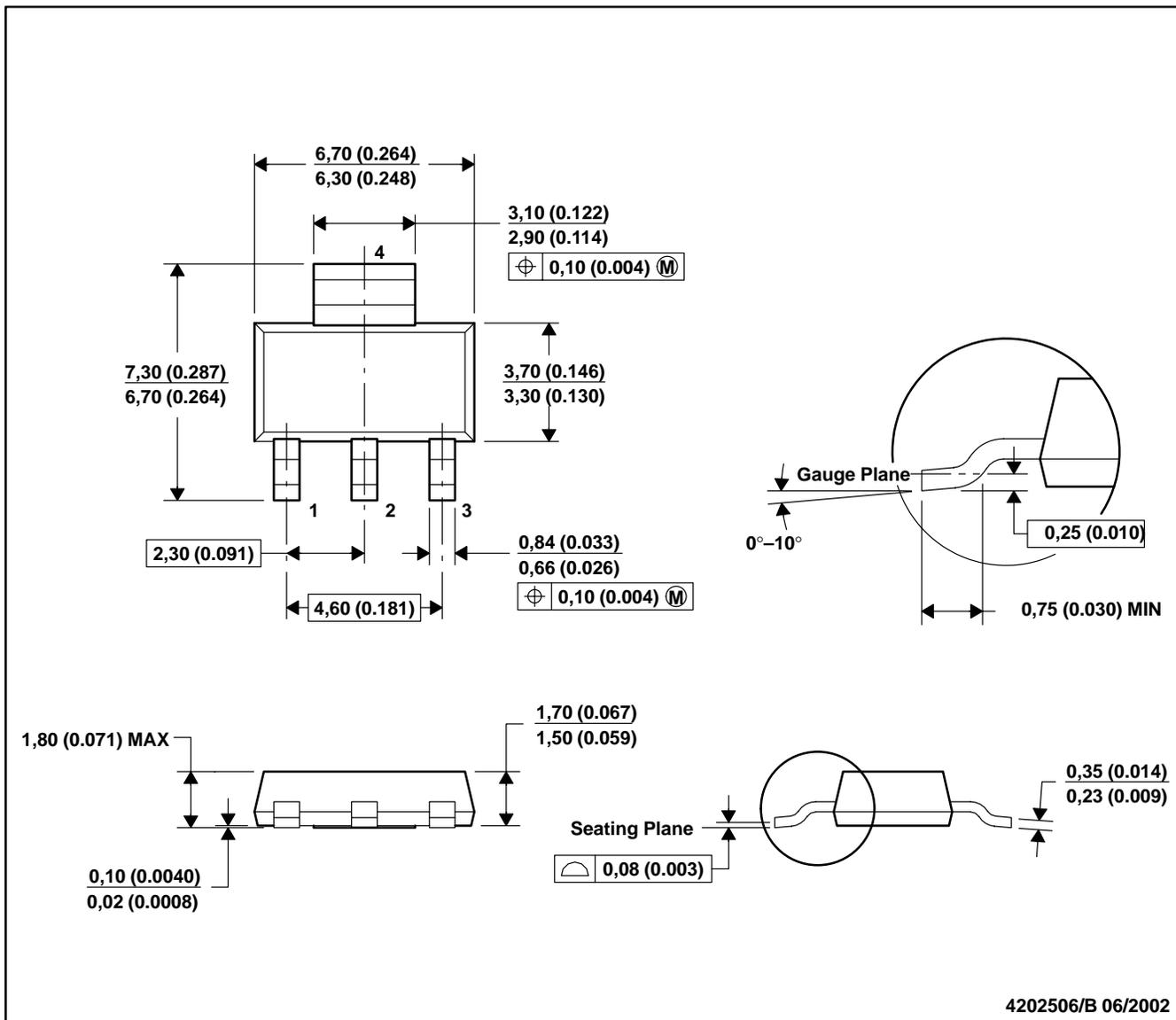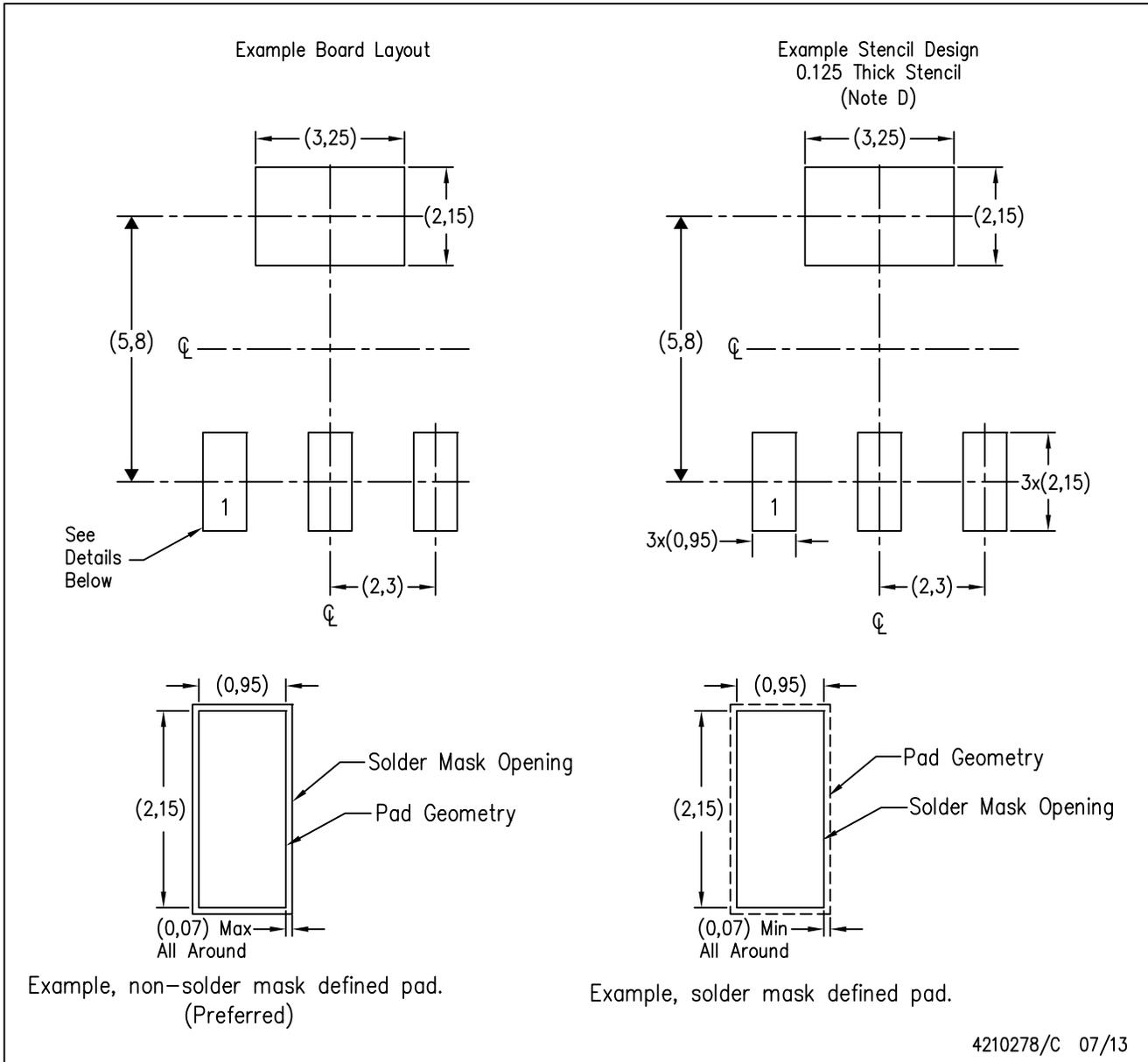
NOTES: A. All linear dimensions are in millimeters (inches).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion.
   D. Falls within JEDEC TO-261 Variation AA.

DCY (R−PDSO−G4)   PLASTIC SMALL OUTLINE

Example Board Layout

(3,25)

(2,15)

(5,8)   ℄

1

See
Details
Below

(2,3)

℄

Example Stencil Design
0.125 Thick Stencil
(Note D)

(3,25)

(2,15)

(5,8)   ℄

1

3x(2,15)

3x(0,95)

(2,3)

℄

(0,95)

Solder Mask Opening

(2,15)

Pad Geometry

(0,07) Max
All Around

Example, non−solder mask defined pad.
(Preferred)

(0,95)

Pad Geometry

(2,15)

Solder Mask Opening

(0,07) Min
All Around

Example, solder mask defined pad.

4210278/C 07/13

NOTES: A.   All linear dimensions are in millimeters.
           B.   This drawing is subject to change without notice.
           C.   Publication IPC−7351 is recommended for alternate designs.
           D.   Laser cutting apertures with trapezoidal walls and also rounding corners will
                offer better paste release. Customers should contact their board assembly
                site for stencil recommendations. Refer to IPC 7525 for stencil design
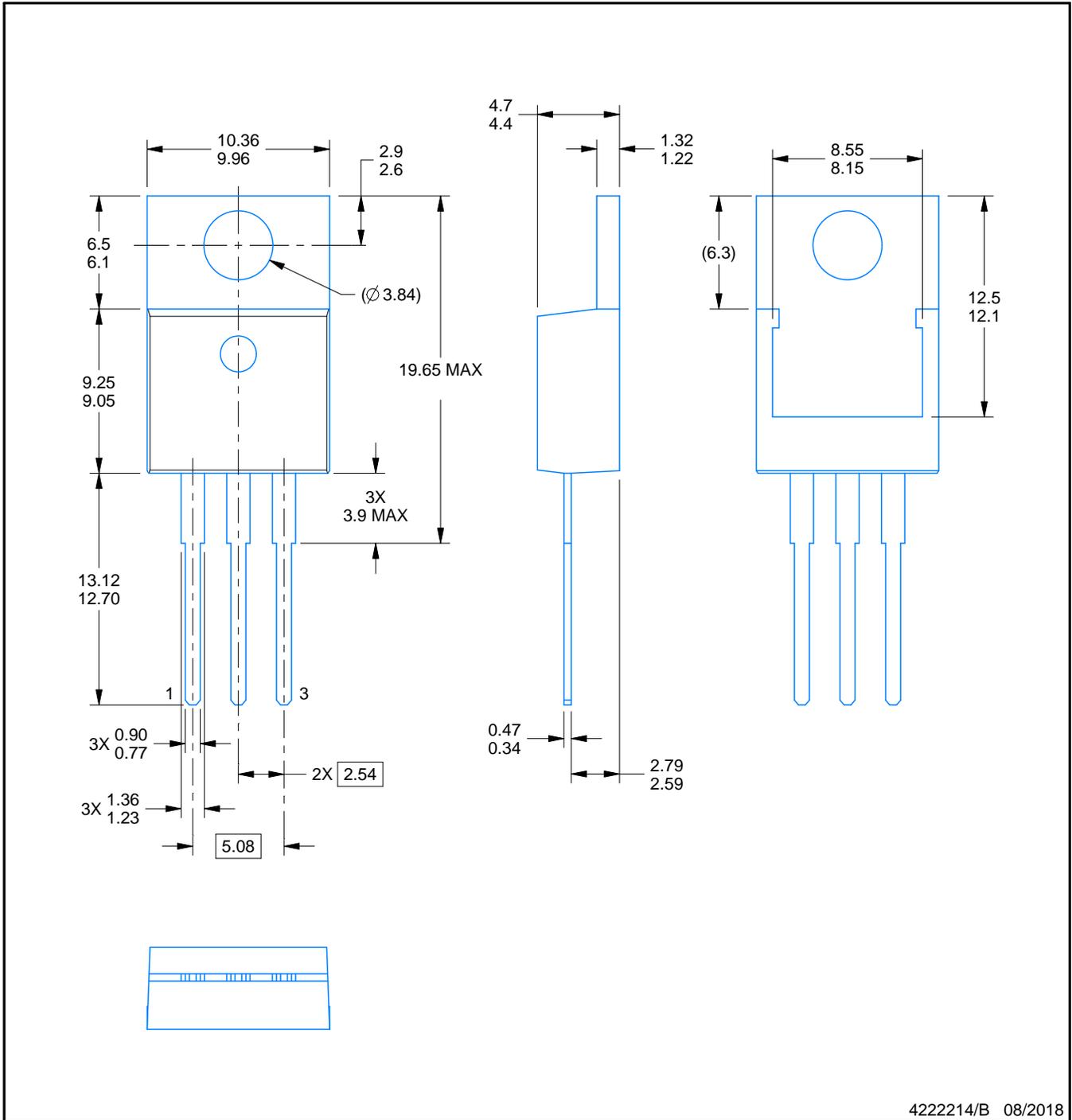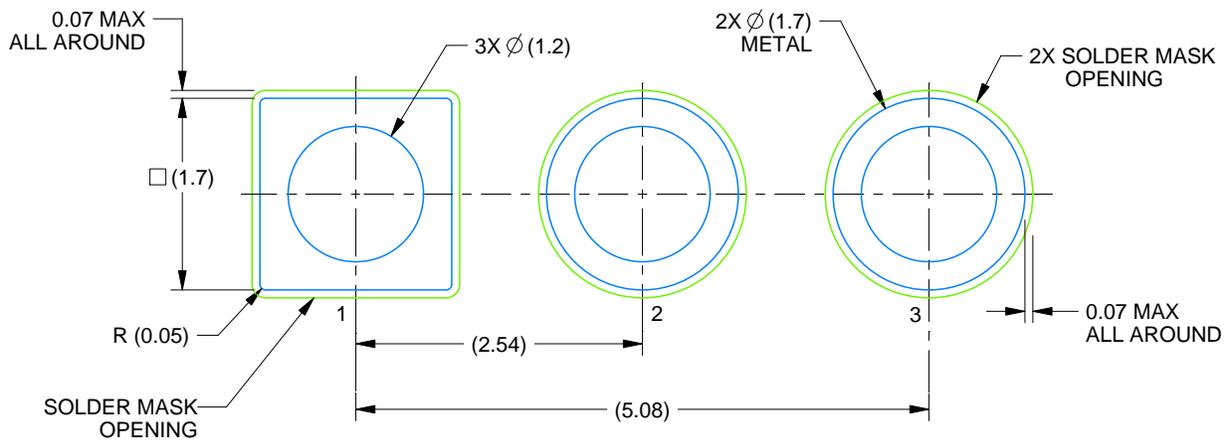   considerations.
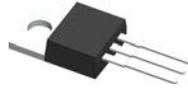
4222214/B   08/2018

NOTES:

1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
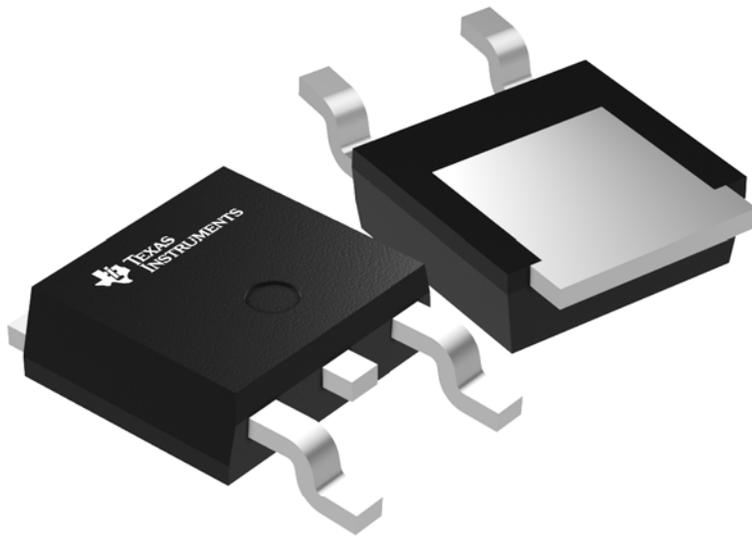3. Reference JEDEC registration TO-220.

0.07 MAX
ALL AROUND

3X ∅ (1.2)

2X ∅ (1.7)
METAL

2X SOLDER MASK
OPENING

□ (1.7)

0.07 MAX
ALL AROUND

R (0.05)

SOLDER MASK
OPENING

1

2

3

(2.54)

(5.08)

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B   08/2018

TRANSISTOR OUTLINE

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

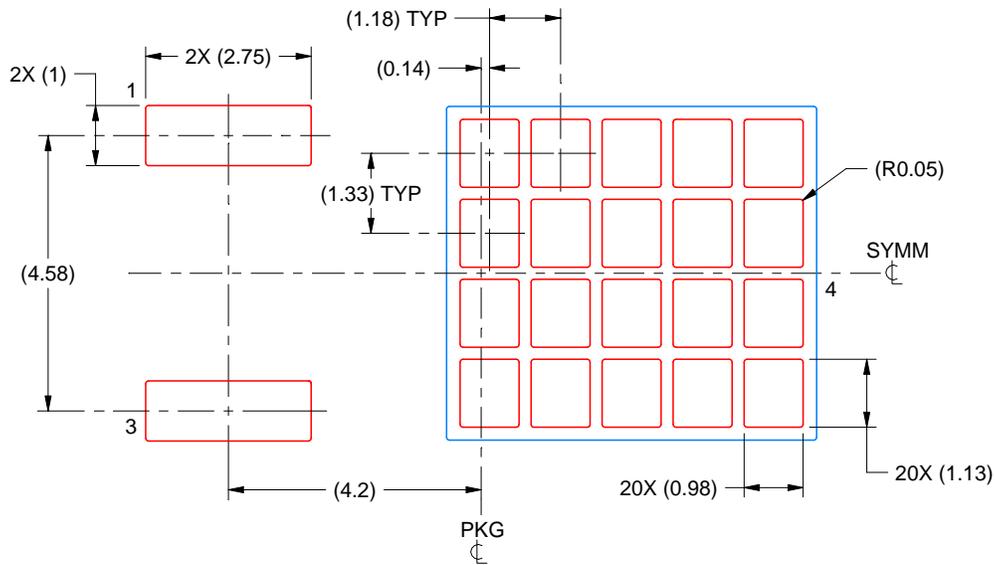4205521-2/E

TEXAS
INSTRUMENTS

10.41
9.40

B 6.22
5.97

1.27
0.89

A

1

2.29

4.58

2

6.70
6.35

5.460
4.953

3

3X 0.890
0.635

1.02
0.61

OPTIONAL

NOTE 3

⌖ 0.25Ⓜ C A B

0.61
0.46

2.52 MAX C

0.61
0.46

SEE DETAIL A

5.21 MIN

3

2

4

4.32
MIN

1

EXPOSED
THERMAL PAD
NOTE 3

0.51

GAGE PLANE

0°-8°

1.78
1.40

0.13
0.00

DETAIL A
TYPICAL

4218915/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Shape may vary per different assembly sites.
4. Reference JEDEC registration TO-252.

2X (2.75)

2X (1)

1

(6.15)

(4.58)

4

SYMM

(5.55)

3

(R0.05) TYP

(4.2)

(2.5)

PKG

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

0.07 MAX
ALL AROUND

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED**

0.07 MIN
ALL AROUND

EXPOSED
METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED**

SOLDER MASK DETAILS
NOT TO SCALE

4218915/A   02/2017

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

2X (1)

1

2X (2.75)

(1.18) TYP

(0.14)

(1.33) TYP

(R0.05)

(4.58)

SYMM

4

3

(4.2)

20X (0.98)

20X (1.13)

PKG

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

4218915/A   02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER