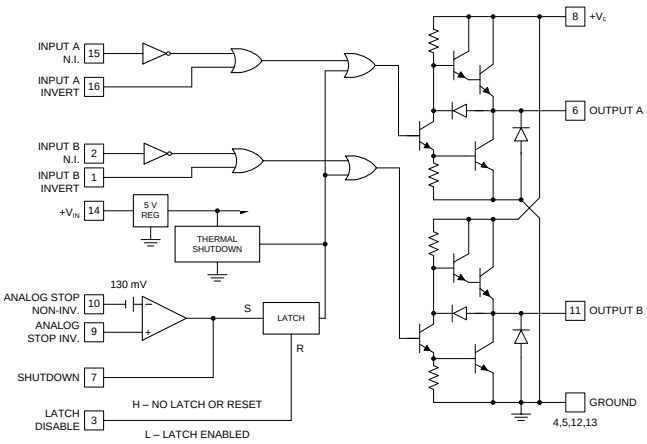
UC1707-SP Dual-Channel Power Driver

1 Features

- Rad-Tolerant: 50 kRad (Si) for 5962-8761903VEA, 5962-8761903VFA (1)
- QML-V Qualified, SMD (5962-8761901VEA, 5962-8761903VEA, 5962-8761903VFA, 5962-8761901V2A)
- Two Independent Drivers
- 1.5-A Totem Pole Outputs
- Inverting and Non-Inverting Inputs
- 40-ns Rise and Fall Into 1000 pF
- High-Speed, Power MOSFET Compatible
- Low Cross-Conduction Current Spike
- Analog Shutdown With Optional Latch
- Low Quiescent Current
- 5-V to 40-V Operation
- Thermal Shutdown Protection
- 16-Pin Dual-In-Line Package

2 Applications

- Switch Mode Power Supply
- DC-DC Converter
- Pulse Transformer Driver



(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/s. Radiation Lot Acceptance Testing is available - contact factory for details.

3 Description

The UC1707-SP power driver is made with a high-speed Schottky process to interface between low-level control functions and high-power switching devices – particularly power MOSFETs. The UC1707-SP contains two independent channels, each of which can be activated by either a high or low input logic level signal. Each output can source or sink up to 1.5 A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, it can be forced low in common through the action either of a digital high signal at the Shutdown terminal or a differential low-level analog signal. The Shutdown command from either source can either be latching or not, depending on the status of the Latch Disable pin.

Supply voltage for both V_{IN} and V_C can independently range from 5 to 40 V.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UC1707-SP	CDIP (16)	6.92 mm × 19.56 mm
	CFP (16)	6.73 mm × 10.30 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Truth Table (Each Channel)(1)

INV.	N.I.	OUT
H	H	L
L	H	H
H	L	L
L	L	L

(1) $\underline{OUT} = \overline{INV}$ and N.I.
$\overline{OUT}$ = INV or N.I.

Table of Contents

4 Revision History

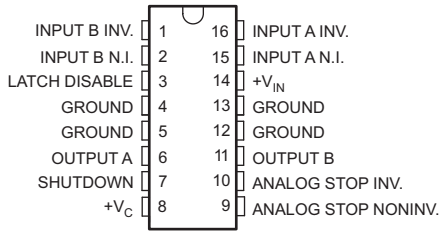
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2011) to Revision A **Page**

- Added *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Corrected typos in *Pin Configuration and Functions* ... 3
- Deleted package thermal impedance in Absolute Maximum Ratings table ... 4
- Added *Community Resources* ... 14

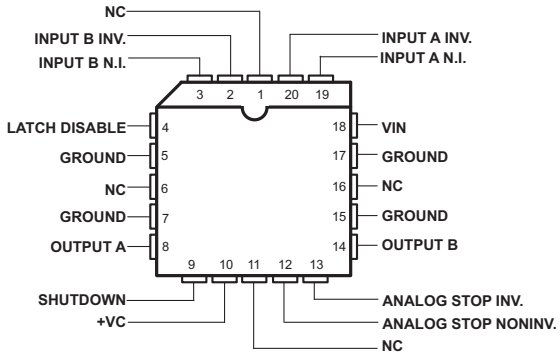
5 Pin Configuration and Functions

J or W Package
16-Pin CDIP or CFP
Top View



All four ground pins must be connected to a common ground.

FK Package
20-Pin LCCC
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	CDIP	LCCC	CFP		
INPUT B INVERTING	1	2	1	I	Inverting TTL compatible input threshold.
INPUT B NONINVERTING	2	3	2	I	Non-Inverting TTL compatible input threshold.
LATCH DISABLE	3	4	3	I	Assuming SHUTDOWN pin is left open, a high on this pin disables the latching functionality of the analog stop shutdown.
GROUND	4	5	4	-	
GROUND	5	7	5	-	
OUTPUT A	6	8	6	O	Output is a 1.5 A totem-pole driver optimized for MOSFET gates.
SHUTDOWN	7	9	7	I	Used as an output of the analog stop circuit. Also used as an input to force shutdown or to force the device out of shutdown.
$+V_C$	8	10	8	I	Collector supply voltage.
ANALOG STOP (+)	9	12	9	I	This pin is normally connected to a reference voltage used for comparison with the sensed power supply output voltage level at the E/A (+) pin.
ANALOG STOP (–)	10	13	10	I	This pin is normally connected to the voltage divider resistors which sense the power supply output level.
OUTPUT B	11	14	11	O	Output is a 1.5 A totem-pole driver optimized for MOSFET gates.
GROUND	12	15	12	-	All voltages are measured with respect to ground (GND).
GROUND	13	17	13	-	All voltages are measured with respect to ground (GND).
$+V_{IN}$	14	18	14	I	Supply voltage.
INPUT A NONINVERTING	15	20	15	I	Non-Inverting TTL compatible input threshold.
INPUT A INVERTING	16	19	16	I	Inverting TTL compatible input threshold.
NC		16			
NC		11			
NC		6			
NC		1			

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{IN}	Supply voltage			40	V
V_C	Collector supply voltage			40	V
	Digital inputs(2)			5.5	V
	Output current (each output, source or sink) steady-state			±500	mA
	Peak transient			±1	A
	Capacitive discharge energy			15	mJ
	Analog stop inputs			V_{IN}	
T_J	Operating virtual-junction temperature			150	°C
	Power dissipation at T_{case} = 25°C(2)	J package		13	W
		W package		15	W
		FK package		13	W
	Lead temperature (soldering, 10 s)			300	°C
	Operating temperature		–55	125	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the four ground pins which must be connected together. All currents are positive into, negative out of the specified terminal. Digital drive can exceed 5.5 V if input current is limited to 10 mA. Consult packaging section of datasheet for thermal limitations and considerations of package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	5	12	38	V
V_C	Supply voltage	5	12	38	V

6.4 Thermal Information

THERMAL METRIC(1)		UC1707-SP			UNIT
		J (CDIP)	FK (LCCC)	W (CFP)	
		16 PINS	20 PINS	16 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36	31.8	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.2	31.3	105	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.5	2.8	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C; V_{IN} = V_C = 20 V. T_A = T_J.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Supply current	V_{IN} = 40 V		12	15	mA

Electrical Characteristics (continued)

Unless otherwise stated, these specifications apply for T_A = –55°C to 125°C; V_{IN} = V_C = 20 V. T_A = T_J.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_C	Supply current	V_C = 40 V, outputs low			5.2	7.5	mA
V_C	Leakage current	V_{IN} = 0, V_C - 30 V, no load			0.05	0.1	mA
	Digital input low level					0.8	V
	Digital input high level			2.2			V
	Input current	V_I = 0			–0.06	–1.0	mA
	Input leakage	V_I = 5 V			0.05	0.1	mA
V_C – V_O	Output high sat	I_O = –50 mA				2.0	V
		I_O = –500 mA				2.5	V
V_O	Output low sat	I_O = –50 mA				0.4	V
		I_O = –500 mA				2.5	V
	Analog threshold	V_{CM} = 0 to 15 V	8761901	100	130	150	mV
			8761903	90	130	150	mV
	Input bias current	V_{CM} = 0			–10	–20	µA
	Thermal shutdown				155		°C
	Shutdown threshold	Pin 7 input		0.4	1.0	2.2	V
	Latch disable threshold	Pin 3 input		0.8	1.2	2.2	V

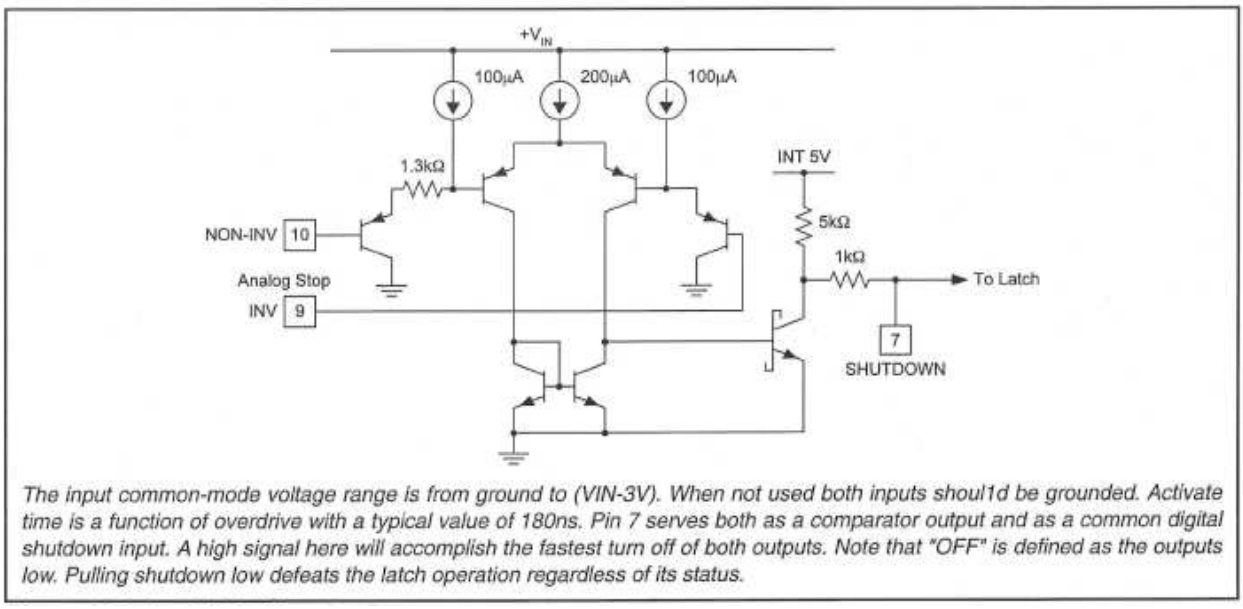
6.6 Typical Switching Characteristics

V_{IN} = V_C = 20 V, T_A = 25°C. Delays measured to 10% output change.

PARAMETER		TEST CONDITIONS	OUTPUT CL =			UNIT
FROM INV. INPUT TO OUTPUT			open	1.0	2.2	nF
	Rise time delay		40	50	60	ns
	10% to 90% rise		25	40	50	ns
	Fall time delay		30	40	50	ns
	90% to 10% fall		25	40	50	ns
FROM N.I. INPUT TO OUTPUT						
	Rise time delay		30	40	50	ns
	10% to 90% rise		25	40	50	ns
	Fall time delay		45	55	65	ns
	90% to 10% fall		25	40	50	ns
V_C	Cross-conduction current spike duration	Output rise	25			ns
		Output fall	0			ns
	Analog shutdown delay	Stop non-Inv. = 0 V	180			ns
		Stop Inv. = 0 to 0.5 V	180			ns
	Digital shutdown delay	2 V input on Pin 7	50			ns

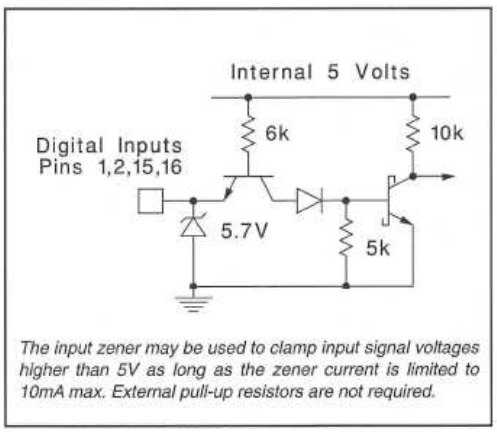
7 Parameter Measurement Information

7.1 Simplified Internal Circuitry



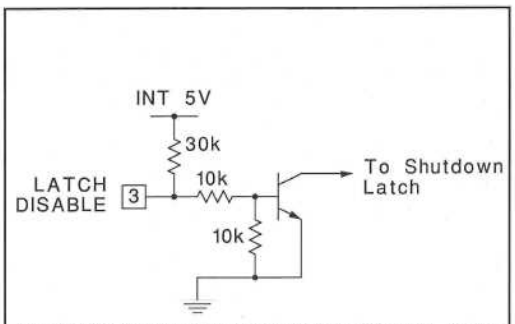
The input common-mode voltage range is from ground to (VIN-3V). When not used both inputs shoul1d be grounded. Activate time is a function of overdrive with a typical value of 180ns. Pin 7 serves both as a comparator output and as a common digital shutdown input. A high signal here will accomplish the fastest turn off of both outputs. Note that "OFF" is defined as the outputs low. Pulling shutdown low defeats the latch operation regardless of its status.

Figure 1. Typical Digital Input Gate



The input zener may be used to clamp input signal voltages higher than 5V as long as the zener current is limited to 10mA max. External pull-up resistors are not required.

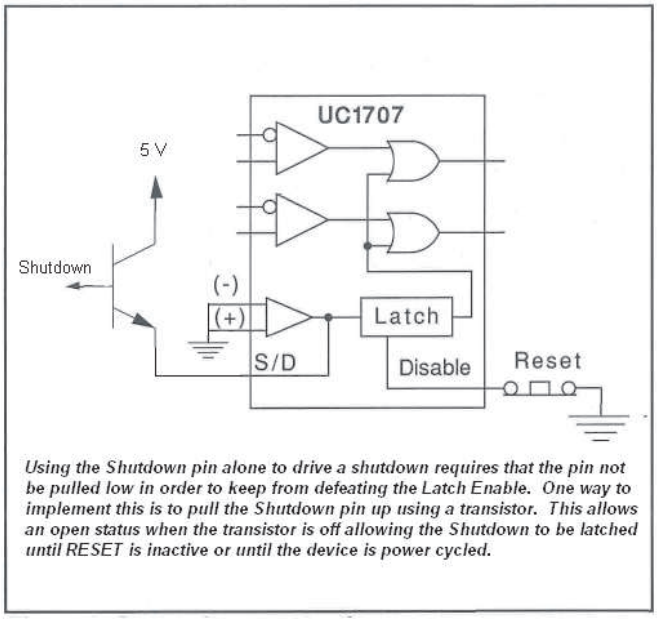
Figure 2. Typical Digital Input Gate



The Shutdown latch is disabled when pin 3 is open. An impedance of 4k or less from pin 3 to ground will allow a shutdown signal to set the latch which can then be reset by either recycling the VIN supply or by momentarily (>200ns) raising pin 3 high.

Figure 3. Latch Disable

Simplified Internal Circuitry (continued)



Using the Shutdown pin alone to drive a shutdown requires that the pin not be pulled low in order to keep from defeating the Latch Enable. One way to implement this is to pull the Shutdown pin up using a transistor. This allows an open status when the transistor is off allowing the Shutdown to be latched until RESET is inactive or until the device is power cycled.

Figure 4. Use of the Shutdown Pin

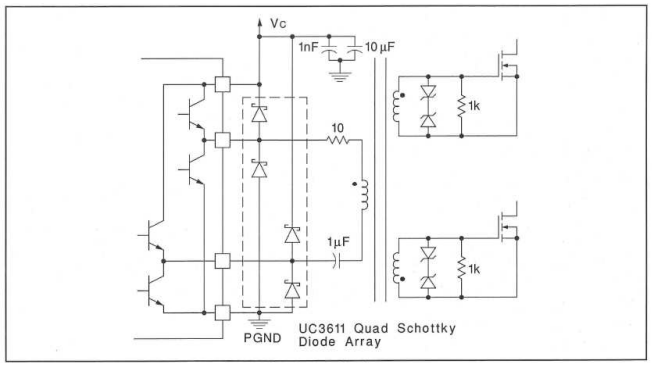
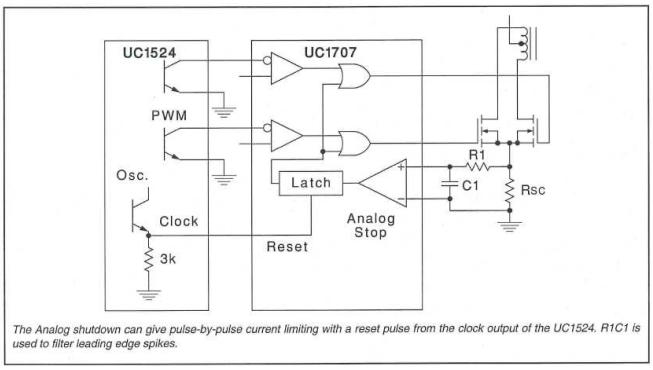


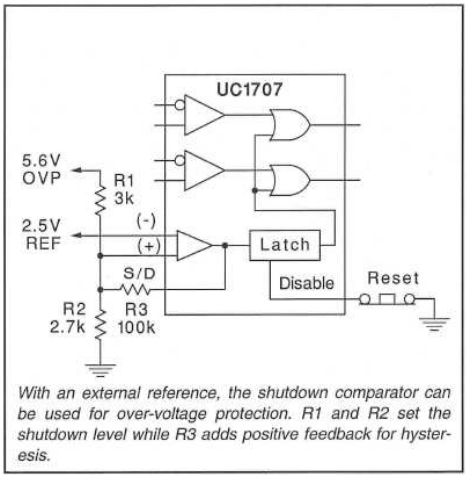
Figure 5. Transformer Coupled Push-Pull MOSFET Drive Circuit



The Analog shutdown can give pulse-by-pulse current limiting with a reset pulse from the clock output of the UC1524. R1C1 is used to filter leading edge spikes.

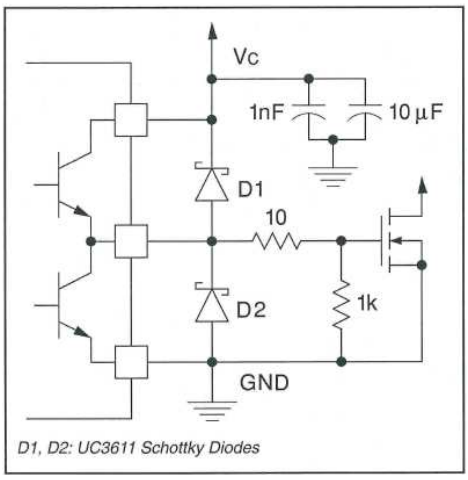
Figure 6. Current Limiting

Simplified Internal Circuitry (continued)



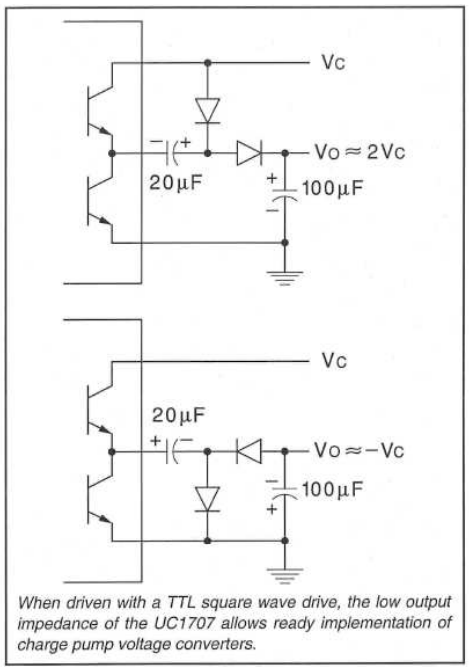
With an external reference, the shutdown comparator can be used for over-voltage protection. R1 and R2 set the shutdown level while R3 adds positive feedback for hysteresis.

Figure 7. Overvoltage Protection



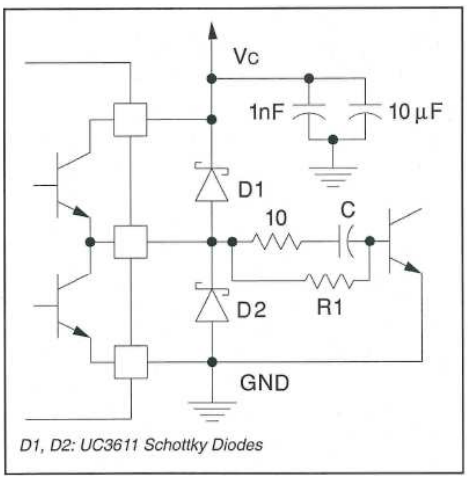
D1, D2: UC3611 Schottky Diodes

Figure 8. Power MOSFET Drive Circuit



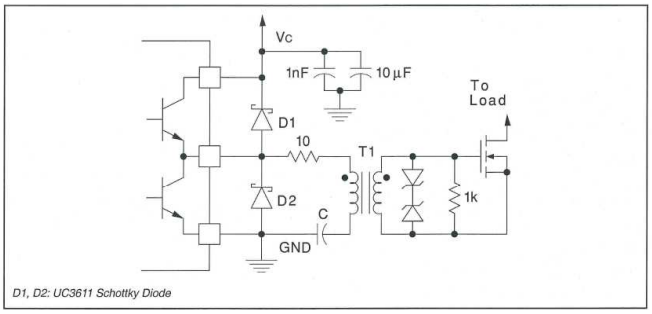
When driven with a TTL square wave drive, the low output impedance of the UC1707 allows ready implementation of charge pump voltage converters.

Figure 9. Charge Pump Circuits



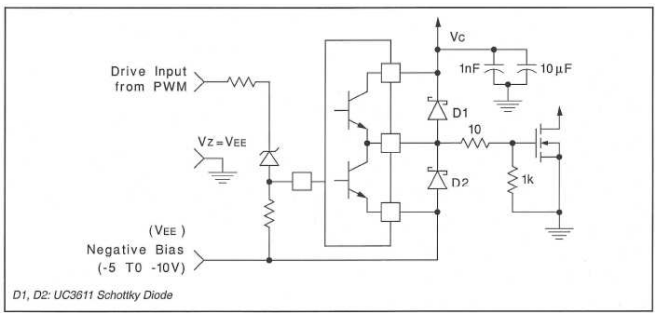
D1, D2: UC3611 Schottky Diodes

Figure 10. Power Bipolar Drive Circuit



D1, D2: UC3611 Schottky Diode

Figure 11. Transformer Coupled MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diode

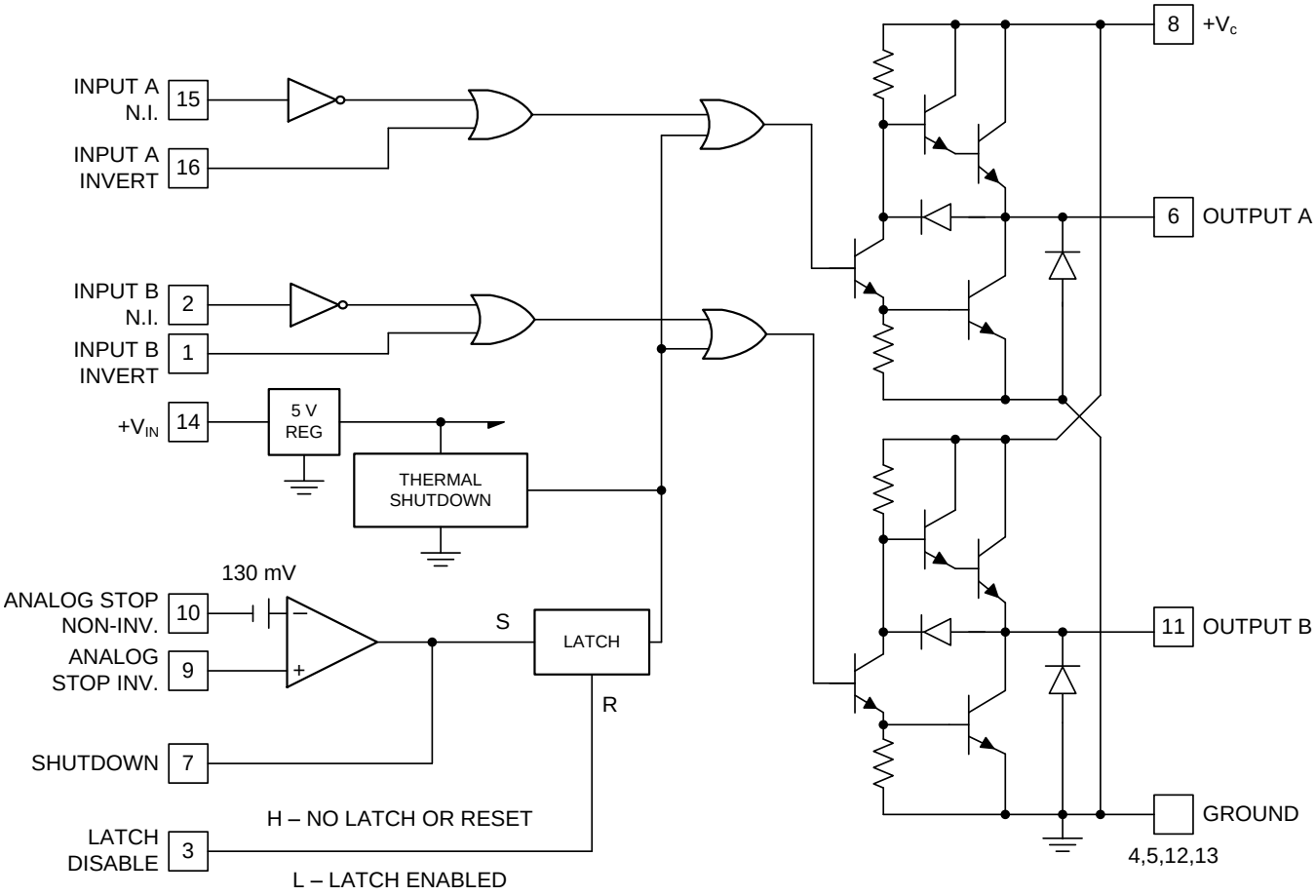
Figure 12. Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Reference PWM

8 Detailed Description

8.1 Overview

UC1707-SP was designed specifically as a power MOSFET driver for switching-mode power supply applications. It is capable of providing fast transitions and high-peak current required by power MOSFETs. One of the most important factors while developing the UC1707-SP was to isolate the high speed switching noise from the low level analog signals at the PWM. Separate supply and return paths at the driver signal inputs and power outputs further enhance noise immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Shutdown Circuit Description

The function of the circuitry is to be able to provide a shutdown of the device. This is defined as functionality that will drive both outputs to the low state. There are three different inputs that govern this shutdown capability.

- Analog Stop Pins — The differential inputs to this comparator provide a way to execute a shutdown.
- Latch Disable Pin — Assuming that the Shutdown pin is left open, a high on this pin disables the latching functionality of the Analog Stop shutdown. A low on this pin enables the latching functionality of the Analog Stop shutdown. If a shutdown occurs through the Analog Stop circuit while Latch Disable is high, then the outputs will go low, but will return to normal operation as soon as the Analog Stop circuit allows it. If a shutdown occurs through the Analog Stop circuit while Latch Disable is low, then the outputs will go low and remain low even if the Analog Stop circuit no longer drives the shutdown. The outputs will remain "latched" low (in shutdown) until the Latch Disable goes high and the Analog Stop circuit allows it to return from shutdown or the VIN voltage is cycled to 0 V and then returned above 5 V.

Feature Description (continued)

- Shutdown Pin — This pin serves two purposes.
  1. It can be used as an output of the Analog Stop circuit.
  2. It can be used as an input to force a shutdown or to force the device out of shutdown. This pin can override both the Analog Stop circuit as well as the Latch Disable Pin. When driving hard logic levels into the Shutdown pin, the Latch Disable functionality will be overridden and the Latch Disable will not function as it does when used in conjunction with the Analog Stop circuit. When the Shutdown pin is high, the outputs will be in the low state (shutdown). When the Shutdown pin is low (hard logic low) the outputs will operate normally, regardless of the state of the Latch Disable pin or the Analog Stop pins.

To use the Shutdown Pin with the Latch Disable functional it is necessary to use either a diode in series with the Shutdown signal or to use an open collector pullup so that the Shutdown pin is not pulled low. This configuration will allow the Latch Disable function to work with the Shutdown pin.

8.4 Device Functional Modes

Table 1. UG1707 Shutdown Truth Table

ANALOG STOP LOGIC	SHUTDOWN	LATCH DISABLE	PREVIOUS STATE OF OUTPUT	OUTPUT
X	0	X	X	Follows Input Logic
X	1	X	X	Low (Shutdown)
1	Open	X	X	Low (Shutdown)
0	Open	0	Shutdown	Latched Shutdown(1)
0	Open	0	Normal	Follows Input Logic
0	Open	1	X	Follows Input Logic

(1) If the output was previously in Shutdown and Latch Disable was low and stays low, then even if the Analog Stop Logic is changed or the Shutdown pin is open, the outputs will remain in Shutdown.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

UC1707-SP MOSFET driver IC is designed to provide fast transition and high peak currents required for the MOSFETs. Each driver features TTL compatible input thresholds, undervoltage lockout, thermal shutdown and low cross conduction, high-speed output circuitry. The peak current of each totem-pole output, whether source or sink is 1.5 A. However, on dual output versions as in UC1707-SP both of the outputs can be paralleled for 3-A peak current.

9.2 Typical Application

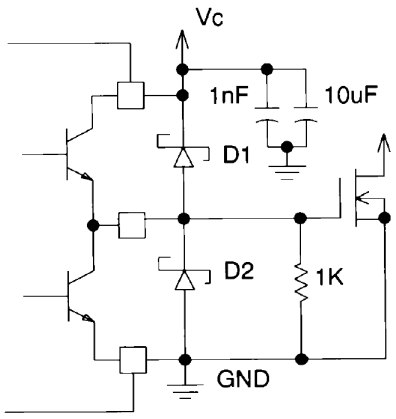


Figure 13. Power MOSFET Drive Circuit

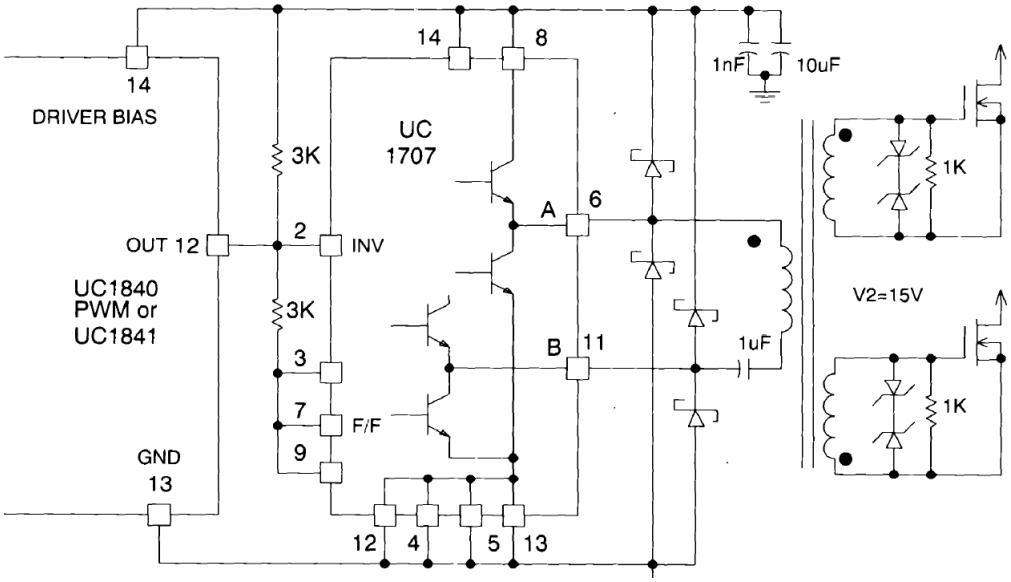


Figure 14. Convert Single Output PWMS High-Current Push-Pull Configuration

Typical Application (continued)

9.2.1 Design Requirements

Push-Pull Transformer coupling – driving MOSFETs with transformer coupled winding.

9.2.2 Detailed Design Procedure

The totem-pole outputs of the UC1707-SP can easily be configured for implementing the balanced transformer drive as shown in Figure 14. Output A and B are alternating now as the internal flip-flop is active and the output frequency is halved. When the UC1707-SP output goes high, the other is held low during the dead time between output pulses. With balanced operation, no coupling capacitor on the primary is necessary since there is no net DC in the primary. Schottky clamp diodes on the primary side and back to back Zener diodes on the secondary are necessary to minimize the overshoot caused by the ringing of the gate capacitance with circuit inductances.

9.2.3 Application Curves

t = 1 µs/DIV.

The following waveforms refer to the application in Figure 14.

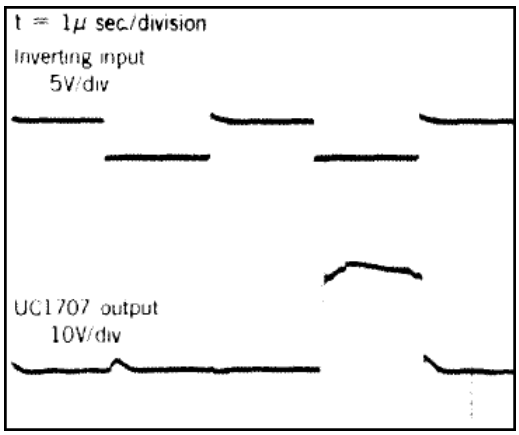


Figure 15. Inverting Input and UC1707 Output

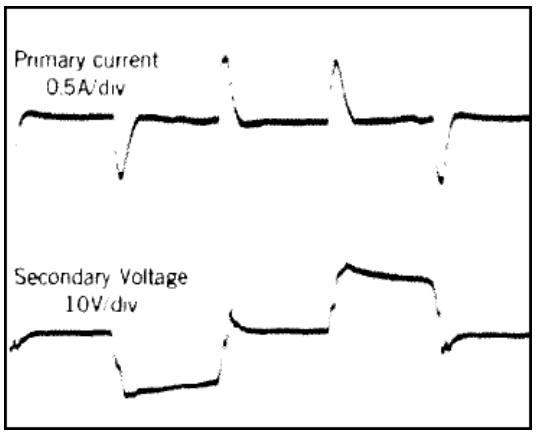


Figure 16. Primary Current and Secondary Voltage

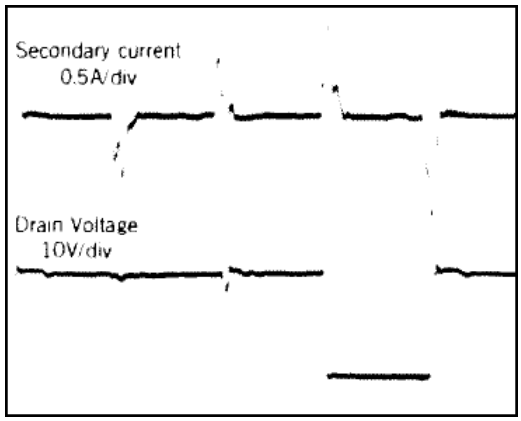


Figure 17. Secondary Current and Drain Voltage

10 Power Supply Recommendations

It is important that the localized capacitors be placed close to the driver V_C/ V_{IN} pins.

Layout is critical to ensure that the driver is placed close to the MOSFETs that are being driven

Adding Schottky diodes prevent the negative transition (below ground) at the derived outputs.

11 Layout

11.1 Layout Guidelines

Directly connecting the MOSFET gate to the output of the driver is straighforward for testing purposes. It does not represent the "real" application which may include several inches of printed circuit board traces. Inductance will sharply degrade the transitions and cause substantial overshoot by ringing with the gate capacitance. This can cause the gate-to-source voltage to overshoot beyond the specified maximum ratings. Additionally, negative transitions (below ground) at the driver output can raise havoc with the internal circuitry, leading to undesirable performance.

Adding Schottky diodes to auxiliary supply rail can help address these concerns.

11.2 Layout Example

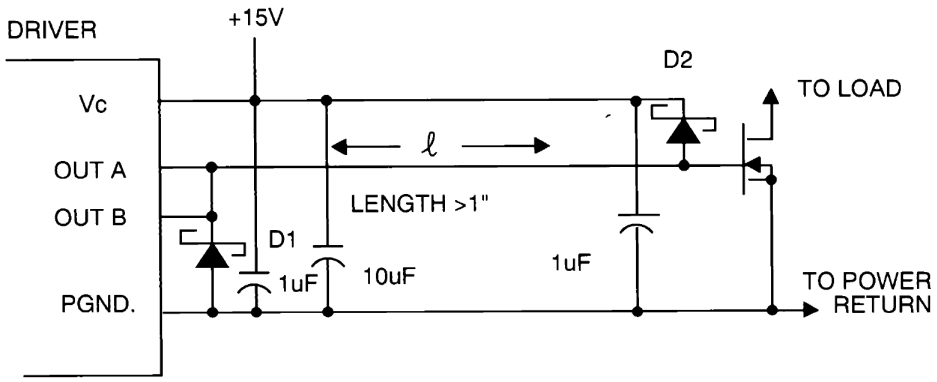


Figure 18. Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8761901V2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8761901V2A UC1707L QMLV	Samples
5962-8761901VEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8761901VEA UC1707JQMLV	Samples
5962-8761903V2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8761903V2A UC1707L-SP	Samples
5962-8761903VEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8761903VEA UC1707J-SP	Samples
5962-8761903VFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8761903VFA UC1707W-SP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

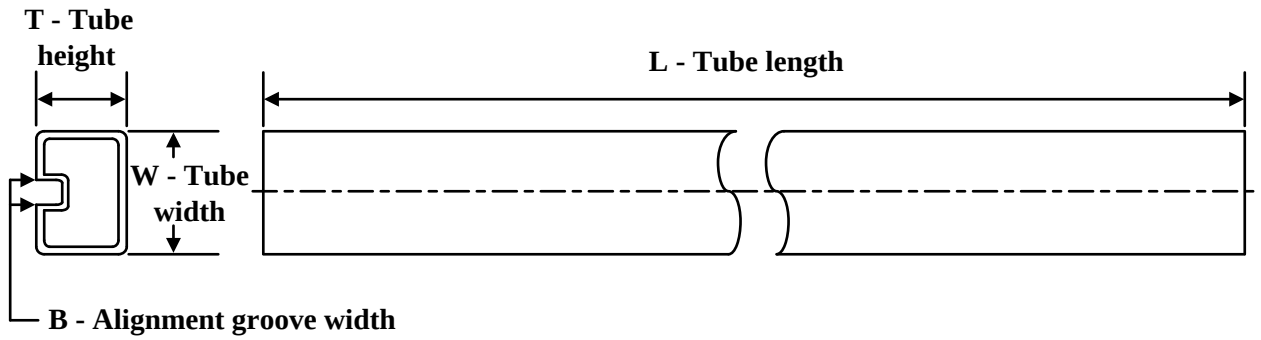
OTHER QUALIFIED VERSIONS OF UC1707-SP :

- Catalog : UC1707

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

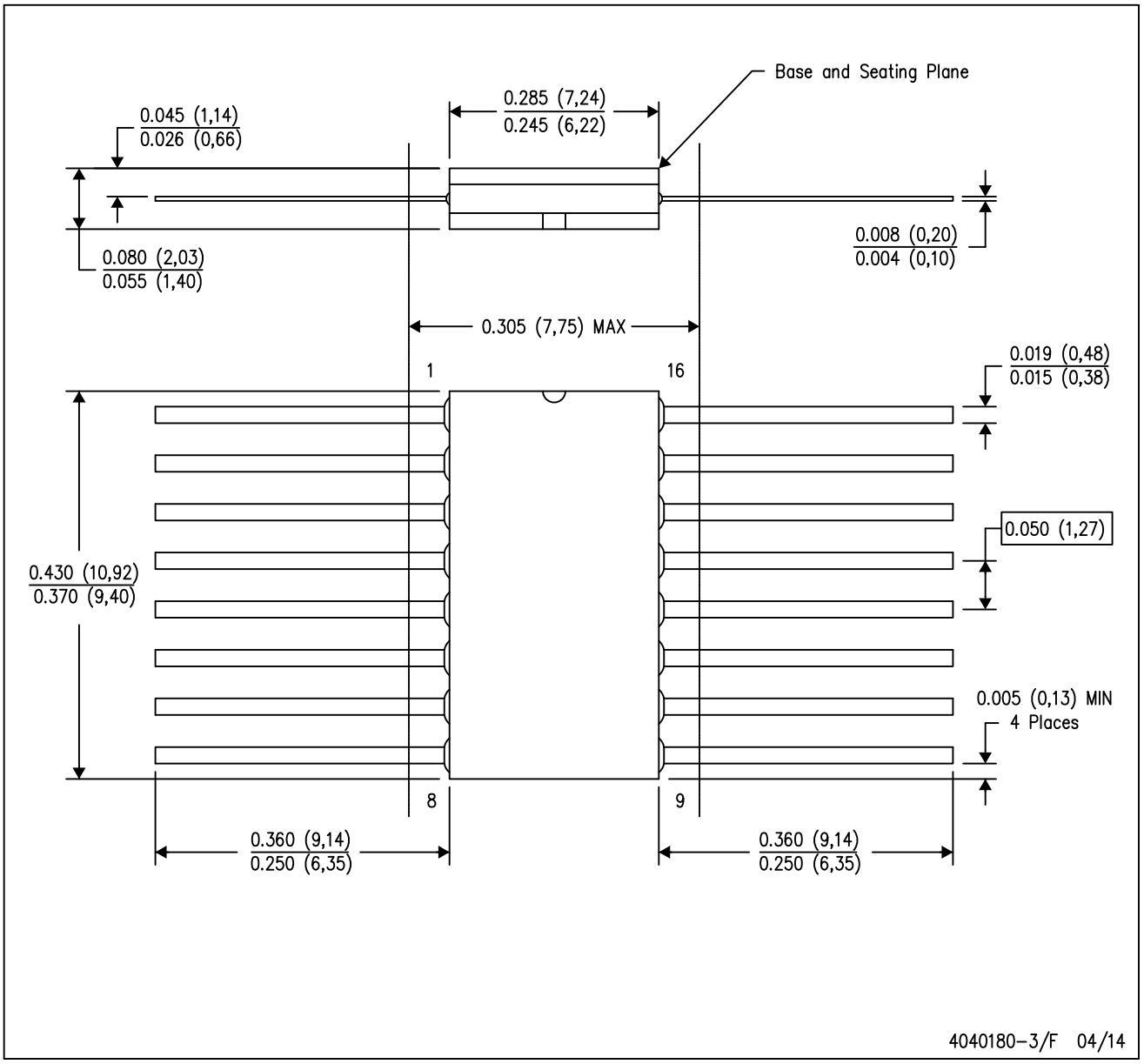
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8761901V2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8761903V2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8761903VEA	J	CDIP	16	25	506.98	15.24	13440	NA
5962-8761903VFA	W	CFP	16	25	506.98	26.16	6220	NA

W (R–GDFP–F16) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

GENERIC PACKAGE VIEW

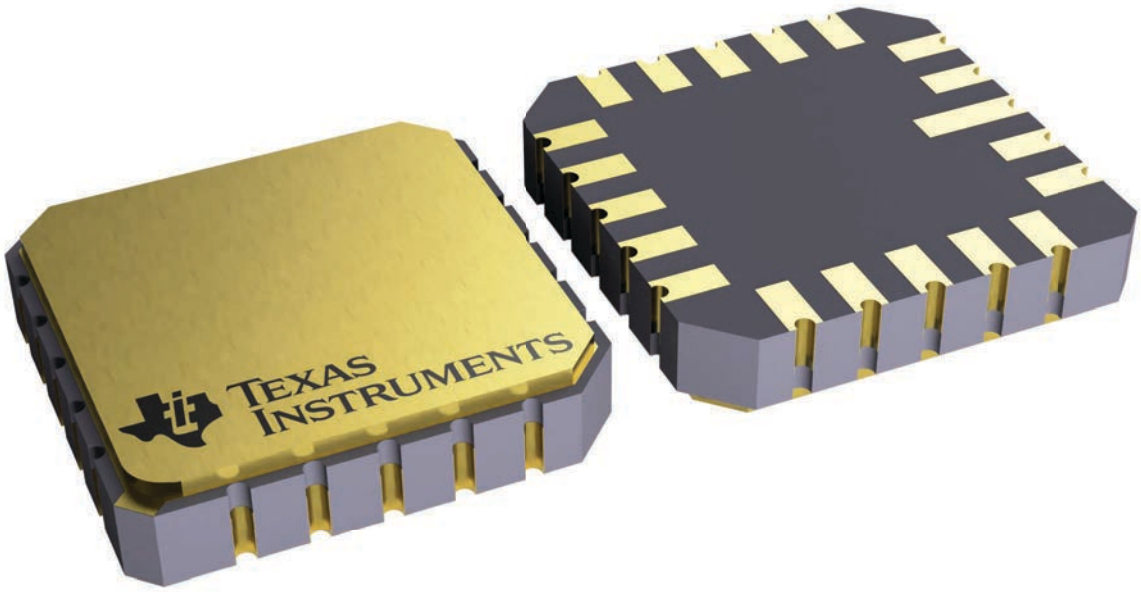
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

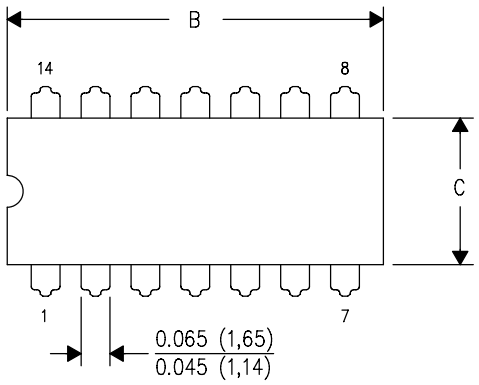


4229370VA\

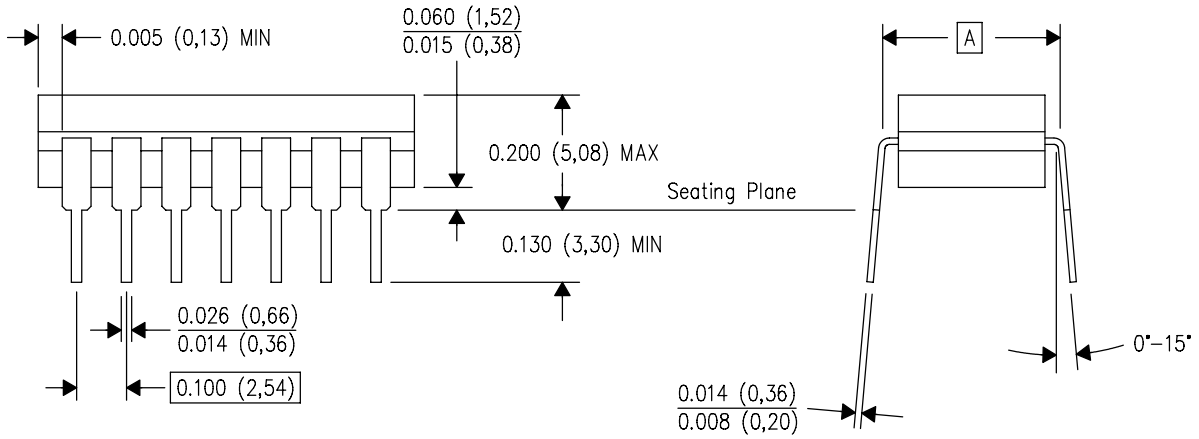
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

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