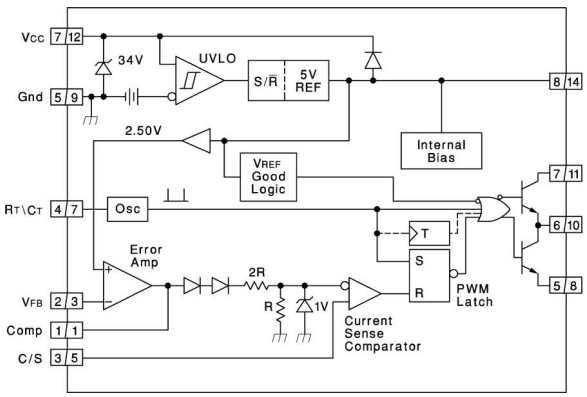
UC2842AQ, UC2843AQ, UC2844AQ, UC2845AQ Current-mode PWM Controller

1 Features

- Extended temperature performance of –40°C to 125°C
- Optimized for off-line and dc to dc converters
- Low start up current (<0.5mA)
- Trimmed oscillator discharge current
- Automatic feed forward compensation
- Pulse-by-pulse current limiting
- Enhanced load response characteristics
- Under-voltage lockout with hysteresis
- Double pulse suppression
- High current totem pole output
- Internally trimmed bandgap reference
- 500kHz operation
- Low r_o error amp

2 Applications

- Switch mode power supplies (SMPS)
- DC-DC converters
- Power modules
- Industrial PSU
- Battery operated PSU



Functional Diagram

3 Description

The UC2842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC2842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is designed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for V_{CC} over 5V.

The difference between members of this family are shown in the table below.

Package Information

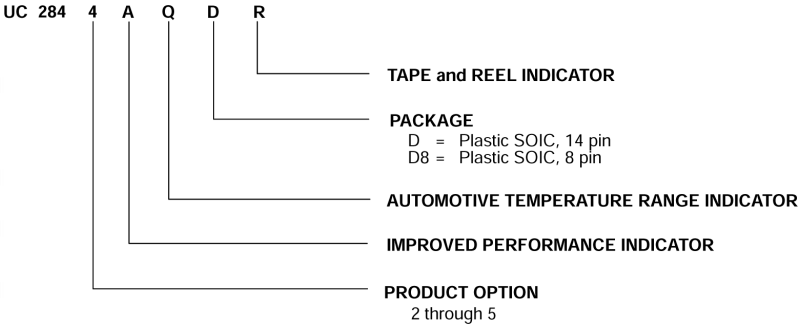
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
UC2842A, UC2843A, UC2844A, UC2845A	D (SOIC, 8)	4.90mm × 6.00mm
	D (SOIC, 14)	8.65mm × 6.00mm

(1) For all available packages, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Device Information

PART NUMBER(1)	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC2842A	16V	10V	<100%
UC2843A	8.5V	7.9V	<100%
UC2844A	16V	10V	<50%
UC2845A	8.5V	7.9V	<50%

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Ordering Information

Table of Contents

4 Pin Configuration and Functions

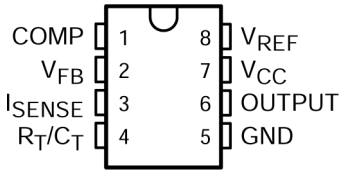


Figure 4-1. D 8-Pin Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
COMP	1	O	Outputs the low impedance 1-MHz internal error amplifier that is also the input to the peak current limit or PWM comparator, with an open-loop gain (AVOL) of 90 dB. This pin is capable of sinking a maximum of 6 mA and is not internally current limited.
V_{FB}	2	I	Input to the error amplifier that can be used to control the power converter voltage feedback loop for stability
I_{SENSE}	3	I	Input to the peak current limit, PWM comparator of the controllers. When used in conjunction with a current sense resistor, the error amplifier output voltage controls the power systems cycle-by-cycle peak current limit. The maximum peak current sense signal is internally clamped to 1 V. See the Functional Block Diagram
R_T/C_T	4	I	Input to the internal oscillator that is programmed with an external timing resistor (RT) and timing capacitor (CT). See Oscillator for information on properly selecting these timing components. TI recommends using capacitance values from 470 pF to 4.7 nF. TI also recommends that the timing resistor values chosen be from 5 kΩ to 100 kΩ.
GND	5	GND	Controller signal ground.
OUTPUT	6	O	Output of 1-A totem pole gate driver. This pin can sink and source up to 1 A of gate driver current. A gate driver resistor must be used to limit the gate driver current.
V_{CC}	7	I	Analog controller bias input that provides power to the device. Total VCC current is the sum of the quiescent VCC current and the average OUTPUT current. Knowing the switching frequency and the MOSFET gate charge, Qg, the average OUTPUT current can be calculated from: IOUTPUT = Qg × fSW A bypass capacitor, typically 0.1 µF, connected directly to GROUND with minimal trace length, is required on this pin. An additional bypass capacitor at least 10 times greater than the gate capacitance of the main switching FET used in the design is also required on VCC.
V_{REF}	8	O	Bias input to the gate driver. This pin must have a biasing capacitor that is at least 10 times greater than the gate capacitance of the main switching FET used in the design.

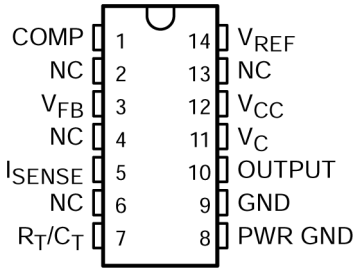


Figure 4-2. D 14-Pin Package (Top View)

Table 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
COMP	1	I/O	Error amplifier compensation pin
NC	2	-	Do not connect
VFB	3	I	Error amplifier input
NC	4	-	Do not connect
ISENSE	5	I	Current sense comparator input
NC	6	-	Do not connect
RT/CT	7	I/O	Oscillator RC input
PWR GND	8	GND	Output PWM ground terminal
GND	9	GND	Device power supply ground terminal
OUTPUT	10	O	PWM Output
V_S	11	-	Output PWM positive voltage supply
V_{CC}	12	-	Device positive voltage supply
NC	13	-	Do not connect
V_{REF}	14	O	Oscillator voltage reference

(1) I = Input, O = Output, I/O = Input or Output, GND = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

	MIN	MAX	UNIT
V_{CC} voltage (low impedance source)		30	V
V_{CC} voltage (I_{CC} mA)	self limiting		
Output current I_O		±1	A
Output energy (capacitive load)		5	µJ
Analog Inputs (pins 3, 5)	–0.3	6.3	V
Error Amp Output Sink current		10	mA
Power Dissipation at T_A < +25°C (D package)		1	W
Package thermal impedance: D (8-pin) package θ_{JA} (see (3)):	Typical 117.4		°C/W
Storage temperature range T_{stg}	–65	150	°C
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds		300	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.
(3) Long term high–temperature storage and/or extended use at maximum recommended operating conditions can result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Electrical Characteristics

T_A = –40°C to 125°C, V_{CC} = 15 V ([1]), R_T = 10 kΩ, C_T = 3.3 nF, and T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reference Section					
Output voltage	T_J = 25°C, I_O = 1 mA	4.95	5.0	5.05	V
Line regulation voltage	V_{IN} = 12 V to 25 V		6	20	mV
Load regulation voltage	I_O = 1 mA to 20 mA		6	25	mV
Temperature stability	See Notes 2 and 3		0.2	0.4	mV/°C
Total output variation voltage	Line, Load, Temp.	4.9		5.1	V
Output noise voltage	f = 10 Hz to 10 kHz, [2]T_J = 25 C		50		μV
Long term stability	1000 hours, [2] T_A=125°C		5	25	mV
Output short-circuit current		-30	-100	-180	mA
Oscillator Section					
Initial accuracy	See [4] T_J = 25 C	47	52	57	kHz
Voltage stability	V_{CC} = 12 V to 25 V		0.2	1	%
Temperature stability	T_A = MIN to MAX, [2]		5		%
Amplitude peak-to-peak	V pin 7, [2]		1.7		V
Discharge current	T_J = 25 C	7.8	8.3	8.8	
	V pin 7 = 2 V,[3] T_J = Full range	7.5		8.8	mA
Error Amplifier Section					
Input voltage	COMP = 2.5 V	2.45	2.5	2.55	V
Input bias current			-0.3	-1	μA
Open loop voltage gain (A_{VOL})	V_O = 2 V to 4 V	65	90		dB
Unity gain bandwidth	T_J = 25°C[2]	0.7	1		MHz
PSRR	V_{CC} = 12 V to 25 V	60	70		dB
Output sink current	FB = 2.7 V, COMP = 1.1 V	2	6		mA
Output source current	FB = 2.3 V, COMP = 5 V	-0.5	-0.8		mA
VOUT high	FB = 2.3 V, R_L = 15 kΩ to GND	5	6		V
VOUT low	FB = 2.7 V, R_L = 15 kΩ to V_{REF}		0.7	1.1	V
Current Sense Section					
Gain	[3] and [4]	2.85	3	3.15	V/V
Maximum input signal	COMP = 5 V, [3]	0.9	1	1.1	V
PSRR	V_{CC} = 12 V to 25 V, [3]		70		dB
Input bias current			—2	—10	μA
Delay to output	I_{SENSE} = 0 V to 2 V, [2]		150	300	ns
Output Section (OUT)					
Low-level output voltage	I_{OUT} = 20 mA		0.1	0.4	V
	I_{OUT} = 200 mA		1.5	2.2	
High-level output voltage	I_{OUT} = -20 mA	13	13.5		V
	I_{OUT} = -200 mA	12	13.5		
Rise time	C_L = 1 nF, [2]T_J = 25 C		25	150	ns
Fall time	C_L = 1 nF, [2]T_J = 25 C		25	150	ns
UVLO saturation	V_{CC} = 5 V, I_{OUT} = 10 mA		0.7	1.2	V
Undervoltage Lockout Section					
Start threshold	UC2842A, UC2844A	15	16	17	V
	UC2843A, UC2845A	7.8	8.4	9	

T_A = –40°C to 125°C, V_{CC} = 15 V ([1]), R_T = 10 kΩ, C_T = 3.3 nF, and T_A = T_J (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Minimum operation voltage after turn on	UC2842A, UC2844A	9	10	11	V
	UC2843A, UC2845A	7	7.6	8.2	
PWM Section					
Maximum duty cycle	UC2842A, UC2843A	92	96	100	%
	UC2844A, UC2845A	46	48	50	
Minimum duty cycle				0	%
Total Standby Current					
Start-up current			0.3	0.5	mA
Operating supply current	FB = 0 V, SENSE = 0 V		11	17	mA
V_{CC} internal Zener voltage	ICC = 25 mA	30	39		V

(1) Adjust V_{CC} above the start threshold before setting at 15 V.
(2) Not production tested.
(3) Parameter measured at trip point of latch with V_{FB} at 0 V.
(4) Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}}$; 0 v VSENSE v 0.8 V.

5.4 Typical Characteristics

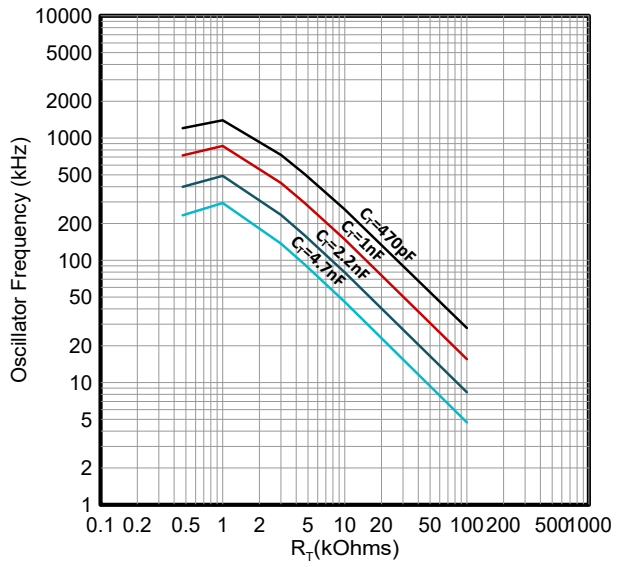


Figure 5-1. Oscillator Frequency vs Timing Resistance

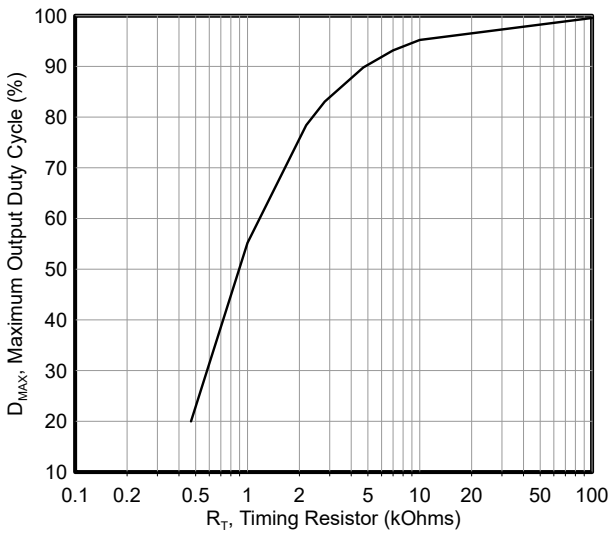


Figure 5-2. Maximum Duty vs Timing Resistance

6 Parameter Measurement Information

Error Amp can source and sink up to 0.5 mA, and sink up to 2 mA.

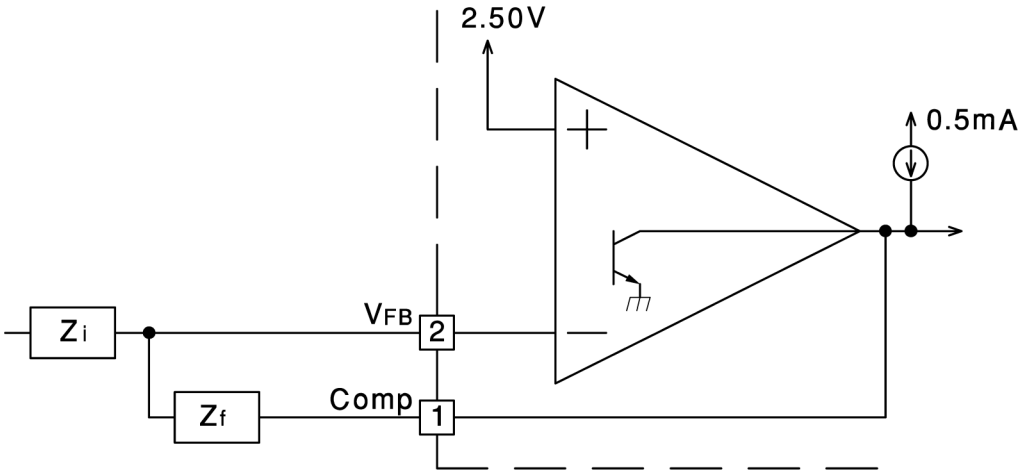
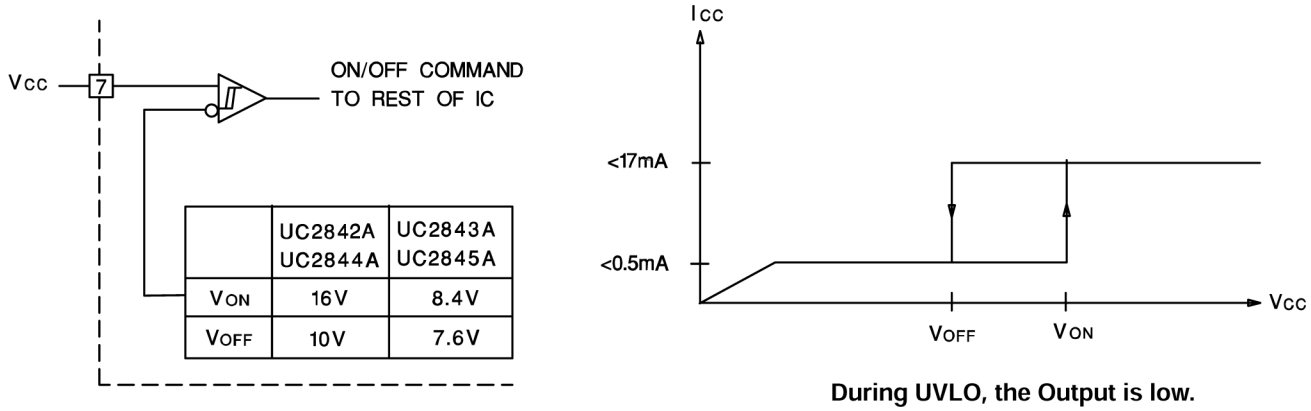


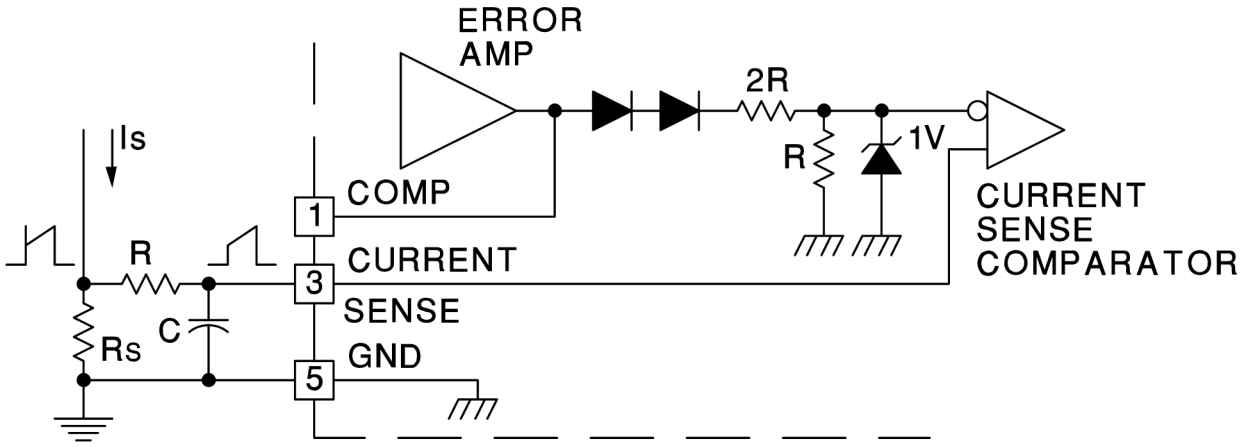
Figure 6-1. Error Amp Configuration



	UC2842A UC2844A	UC2843A UC2845A
VON	16V	8.4V
VOFF	10V	7.6V

During UVLO, the Output is low.

Figure 6-2. Under Voltage Lockout



Peak Current (Is) is Determined By The Formula:

$$Ismax' \frac{1.0V}{RS}$$

A small RC filter may be required to supress switch transients.

Figure 6-3. Current Sense Circuit

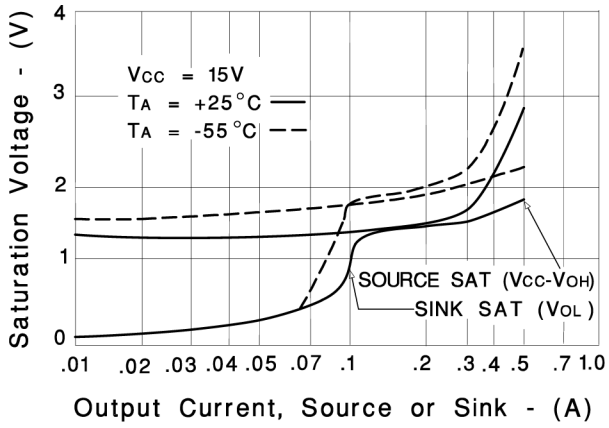


Figure 6-4. Output Saturation Characteristics

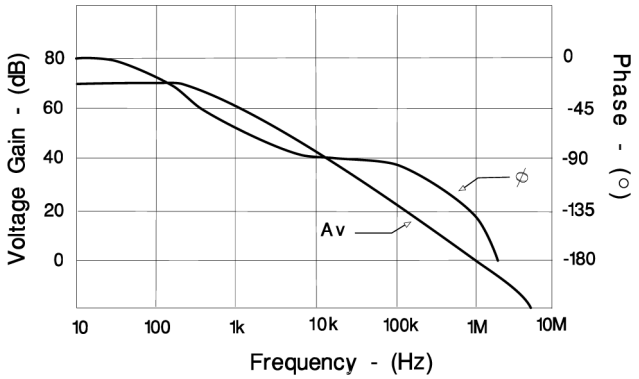
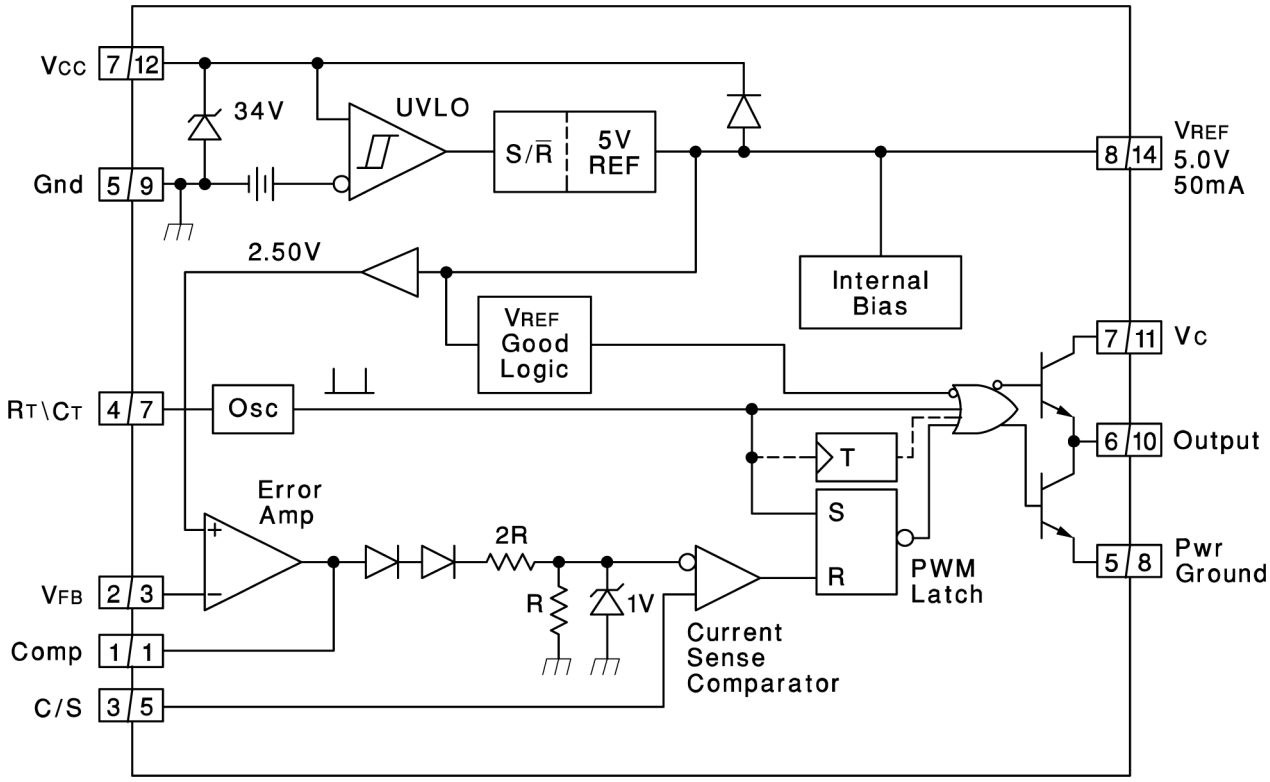


Figure 6-5. Error Amplifier Open-Loop Frequency Response

7 Detailed Description

7.1 Functional Block Diagram



Note

A = DIL-8 Pin Number. B = SO-14 Pin Number.

Toggle flip flop used only in 2844A and 2845A.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

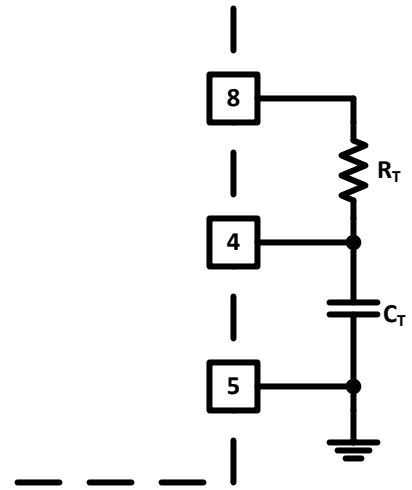


Figure 8-1. Oscillator

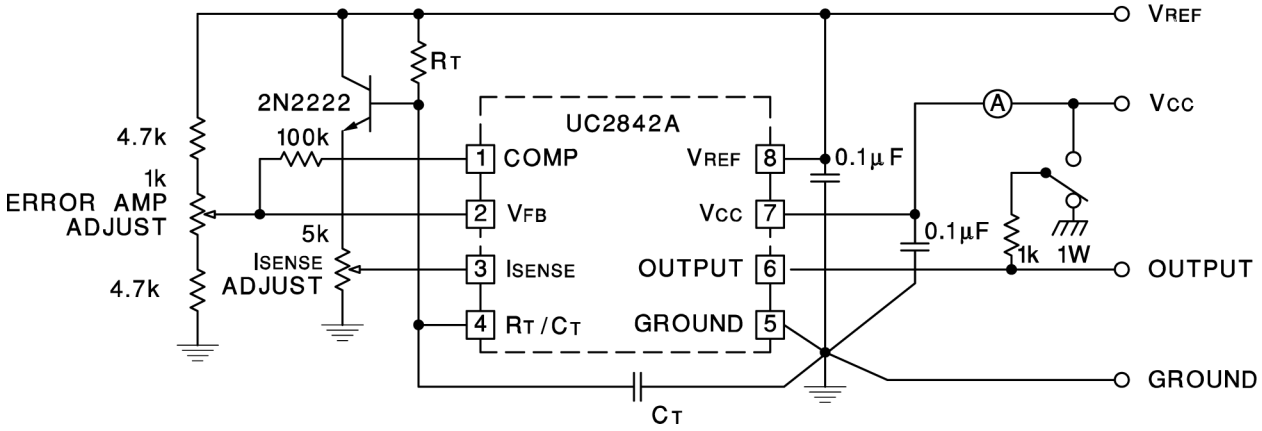


Figure 8-2. Open-Loop Laboratory Text Fixture

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors must be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

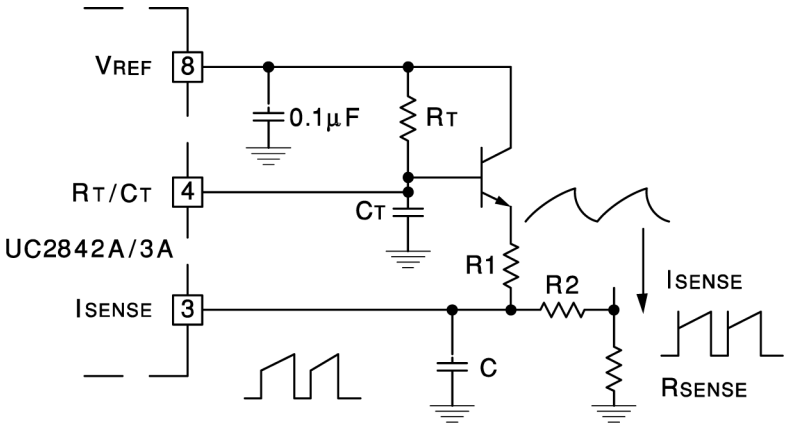


Figure 8-3. Slope Compression

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%. Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

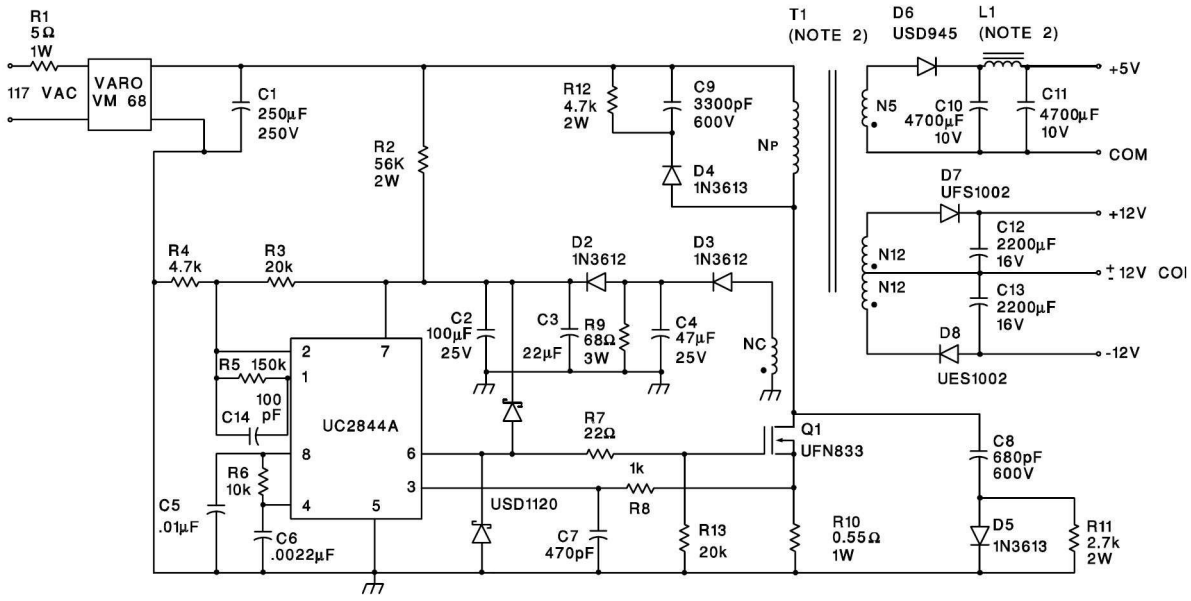


Figure 8-4. Off-Line Flyback Regulator

1. Input Voltage: 95 VAC to 130 VAC (50Hz/60Hz)
2. Line Isolation: 3750V
3. Switching Frequency 40 kHz
4. Efficiency, Full Load: 70%
5. Output Voltage:
   a. +5V, ±5%; 1A to 4A Load
   b. +12V, ±3%; 0.1A to 0.3A Load Ripple voltage: 100 mV P-P Max
   c. –12V, ±3%; 0.1A to 0.3A Load Ripple voltage: 100 mV P-P Max

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2003) to Revision A (October 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed in Absolute Maximum ratings: Lead temperature soldering, 10s from 260°C to 300°C	5
• Added ESD Ratings table, HBM = ±2000V; CDM = ±1500V	5
• Changed in Electrical Characteristics table, OUTPUT SECTION: Rise and fall time, typical value from 50ns to 25ns	6
• Changed in Electrical Char. table, PWM SECTION: maximum duty cycle of UC2842/3A, minimum value from 94% to 92%	6
• Changed in Electrical Char. table, PWM SECTION: maximum duty cycle of UC2844/5A, minimum value from 47% to 46%	6
• Changed Electrical Char. table, TOTAL STANDBY CURRENT, VCC Zener voltage, typical value from 34V to 39V	6
• Added Typical Characteristics section	7
• Updated the Frequency vs Rt and Maximum Duty Cycle vs Rt graphs in the Typical Characteristics section	7

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2842AQD8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	(2842AQ, UC2842AQ)	
UC2842AQD8R	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2842AQ, UC2842AQ)	Samples
UC2842AQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2842AQ, UC2842AQ)	Samples
UC2843AQD8	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2843AQ, UC2843AQ)	Samples
UC2843AQD8R	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2843AQ, UC2843AQ)	Samples
UC2843AQDR	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	(2843AQ, UC2843AQ)	
UC2845AQD8	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	(2845AQ, UC2845AQ)	
UC2845AQD8R	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2845AQ, UC2845AQ)	Samples
UC2845AQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2845AQ, UC2845AQ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

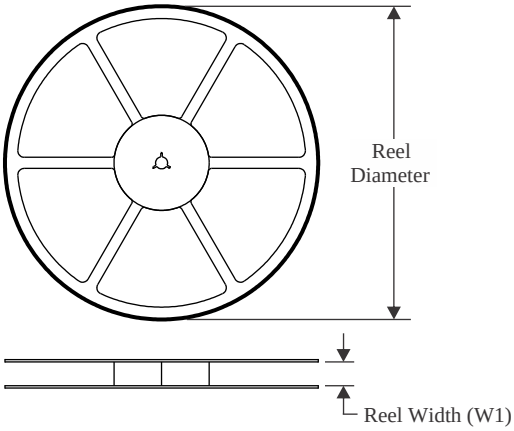
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

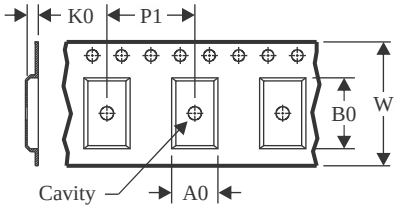
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

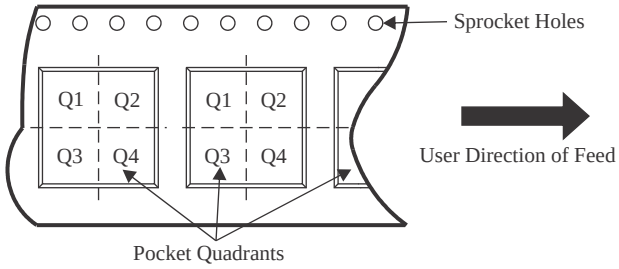


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

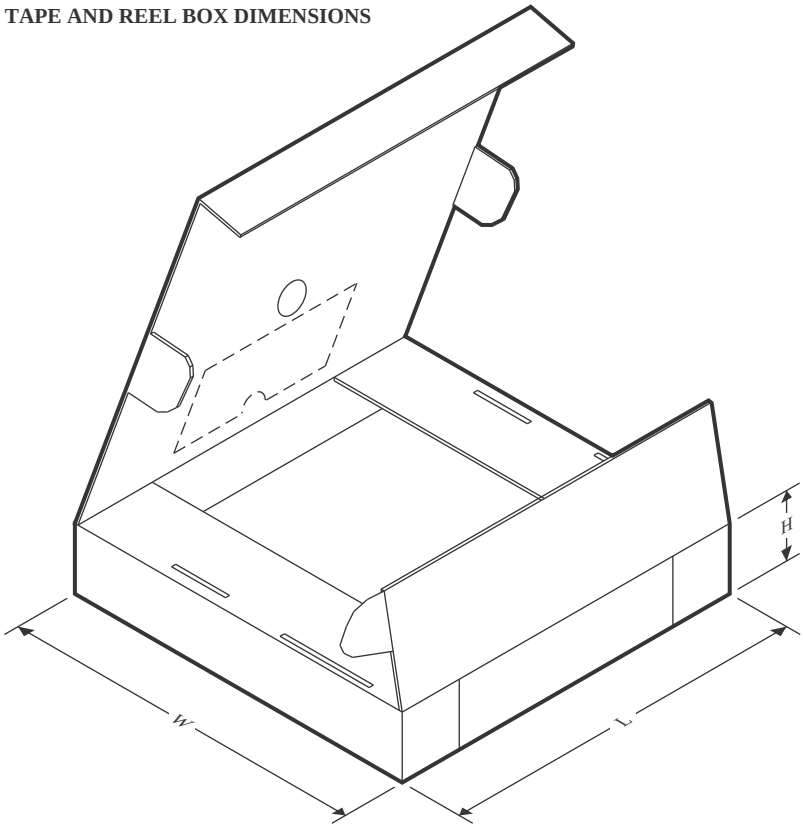
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2842AQD8R	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2843AQD8R	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845AQD8R	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845AQDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

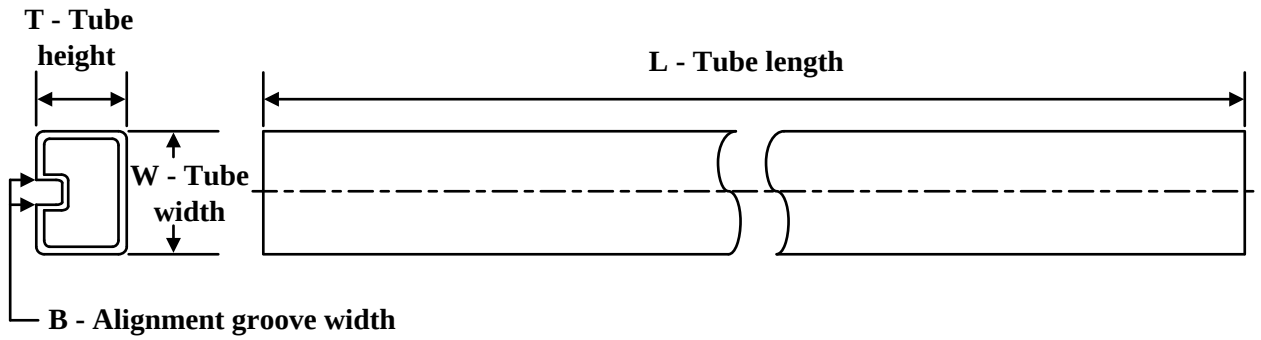
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

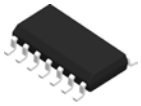
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2842AQD8R	SOIC	D	8	2500	356.0	356.0	35.0
UC2842AQDR	SOIC	D	14	2500	356.0	356.0	35.0
UC2843AQD8R	SOIC	D	8	2500	356.0	356.0	35.0
UC2845AQD8R	SOIC	D	8	2500	356.0	356.0	35.0
UC2845AQDR	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UC2843AQD8	D	SOIC	8	75	506.6	8	3940	4.32

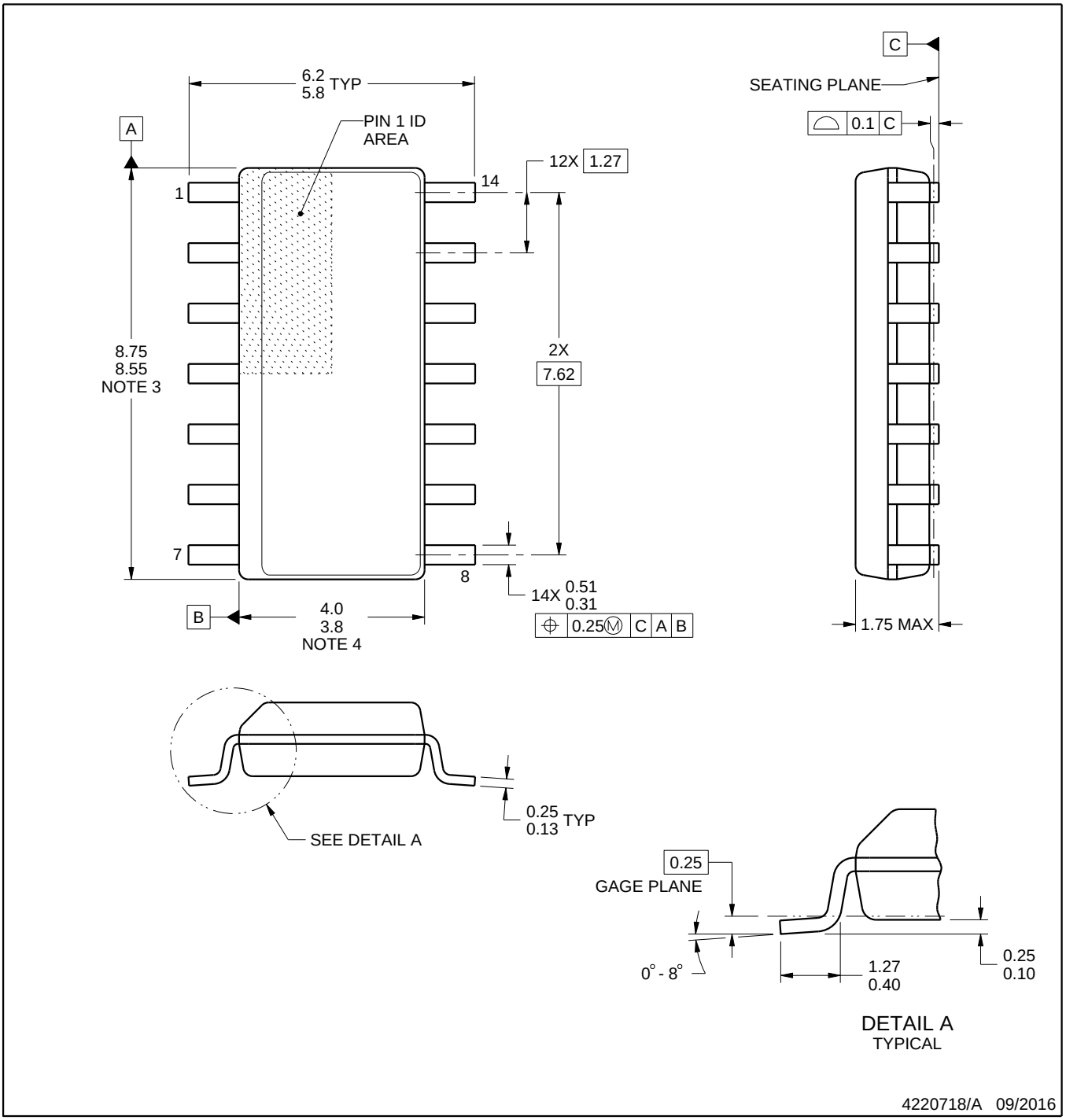


PACKAGE OUTLINE

D0014A

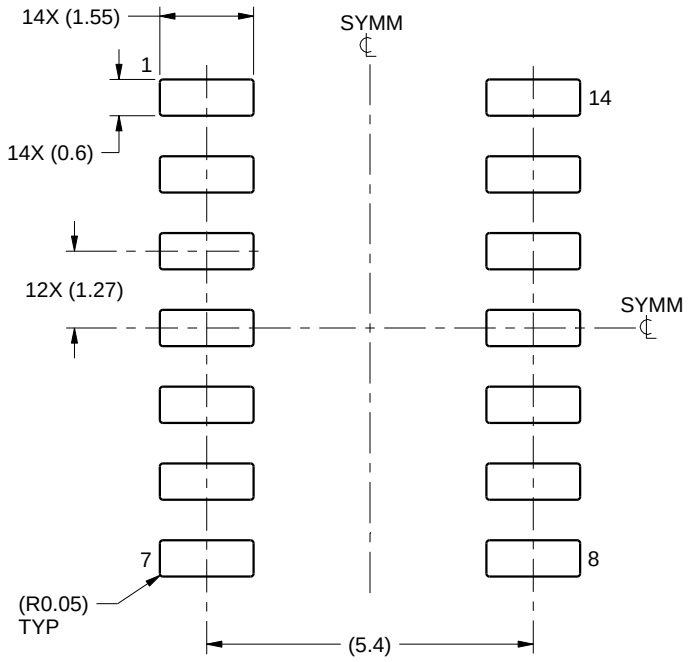
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

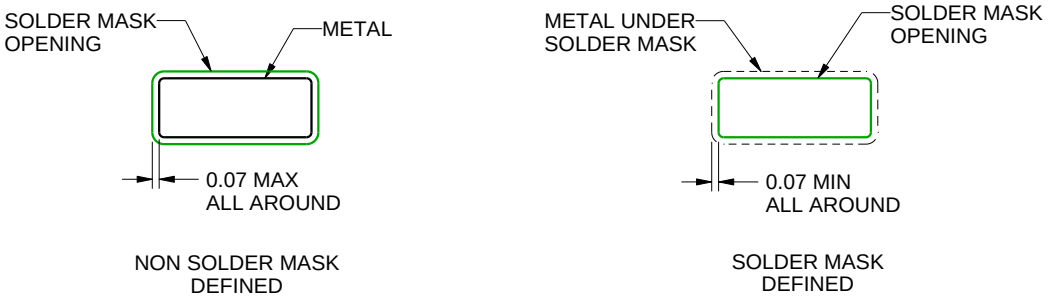


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

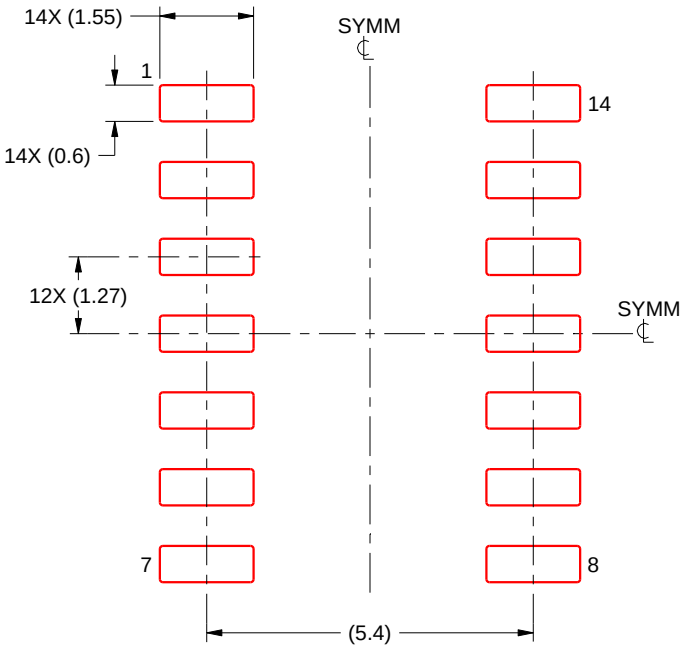
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

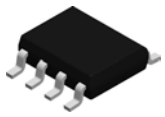


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

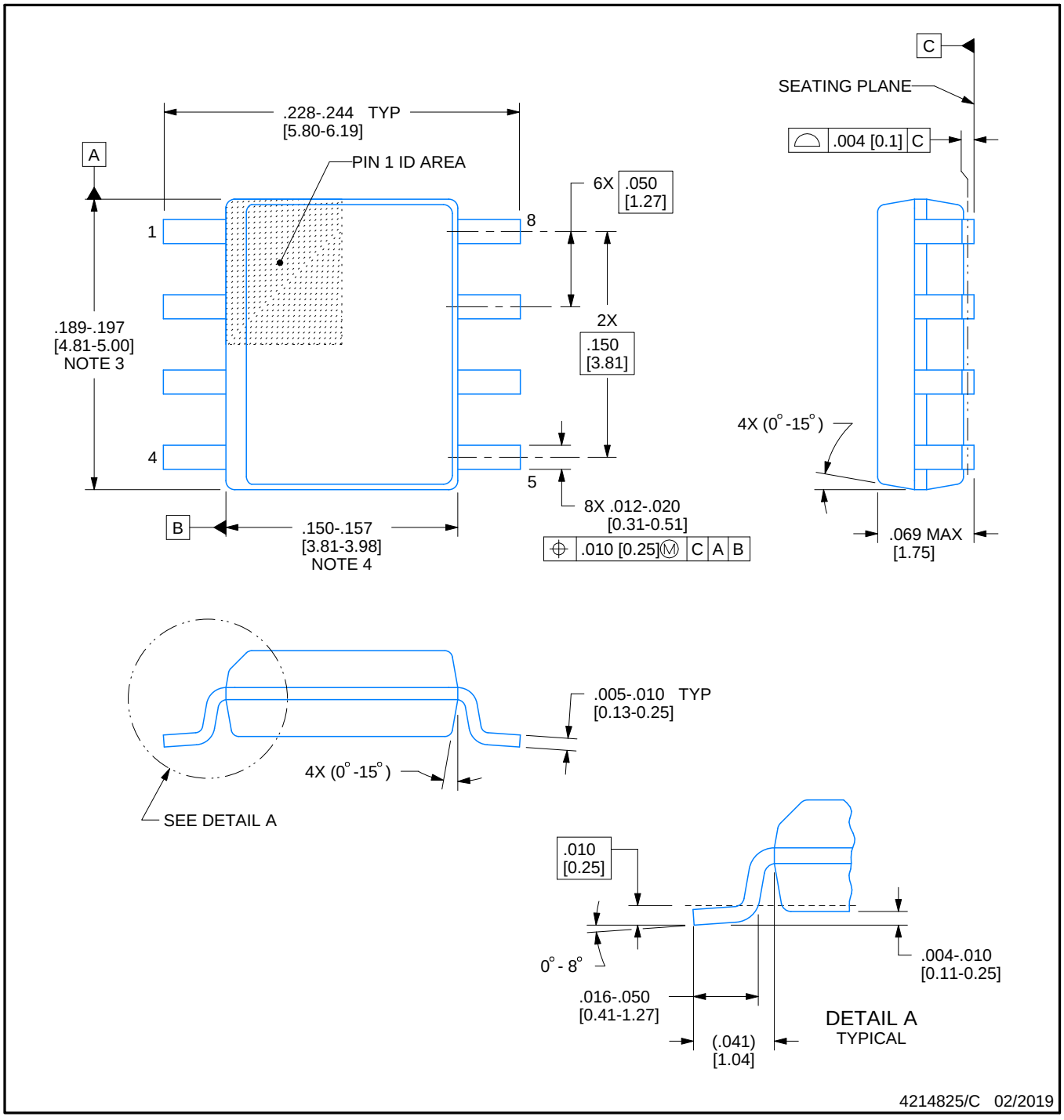


PACKAGE OUTLINE

D0008A

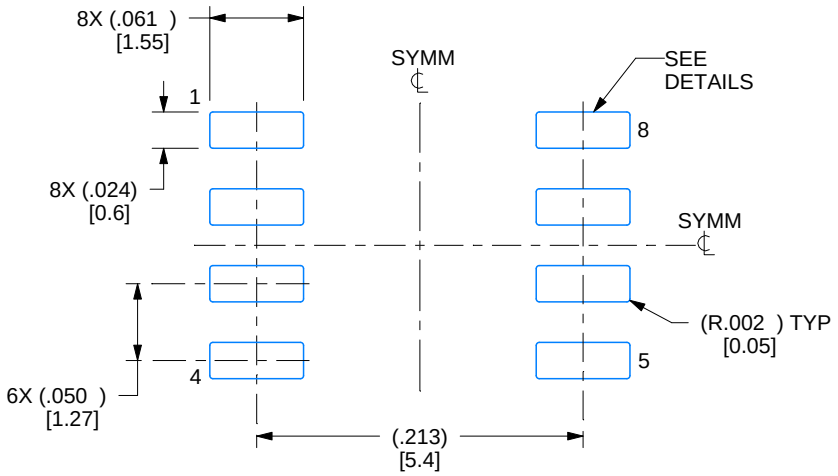
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

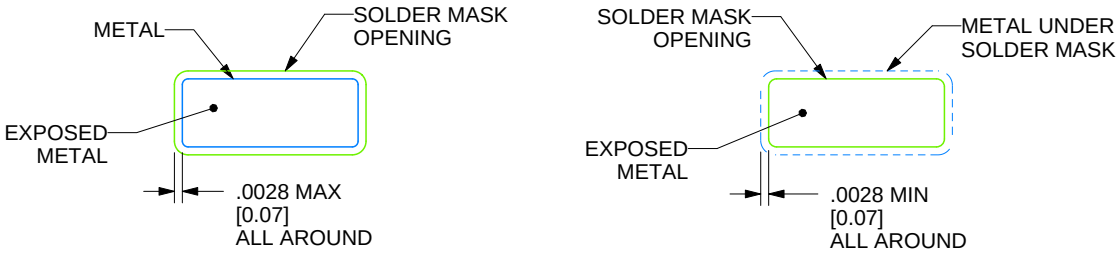


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

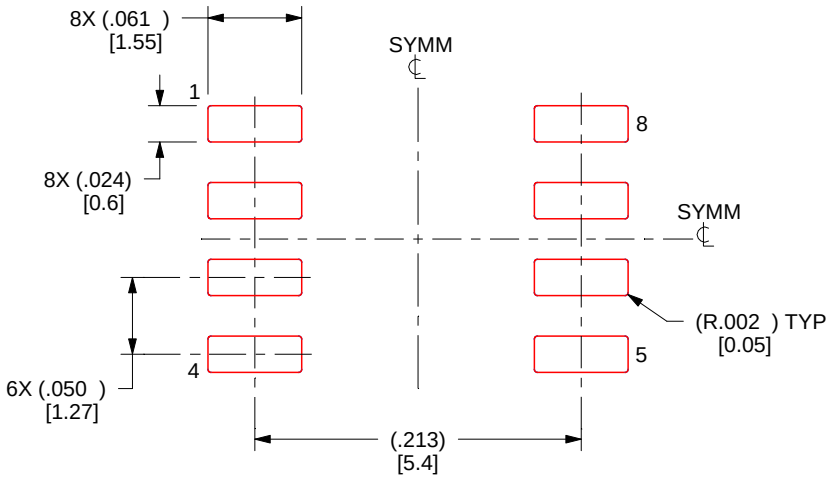
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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