8-Pin Continuous Conduction Mode (CCM) PFC Controller

FEATURES

- **8-pin Solution Without Sensing Line Voltage Reduces External Components**
- **Wide-Range Universal AC Input Voltage**
- **Fixed 65-kHz Operating Frequency**
- **Maximum Duty Cycle of 97%**
- **Output Over/Under-Voltage Protection**
- **Input Brown-Out Protection**
- **Cycle-by-Cycle Peak Current Limiting**
- **Open Loop Detection**
- **Low-Power User Controlled Standby Mode**

APPLICATIONS

- **CCM Boost Power Factor Correction Power Converters in the 100 W to >2 kW Range**
- **Server and Desktop Power Supplies**
- **Telecom Rectifiers**
- **Industrial Electronics**
- **Home Electronics**

CONTENTS

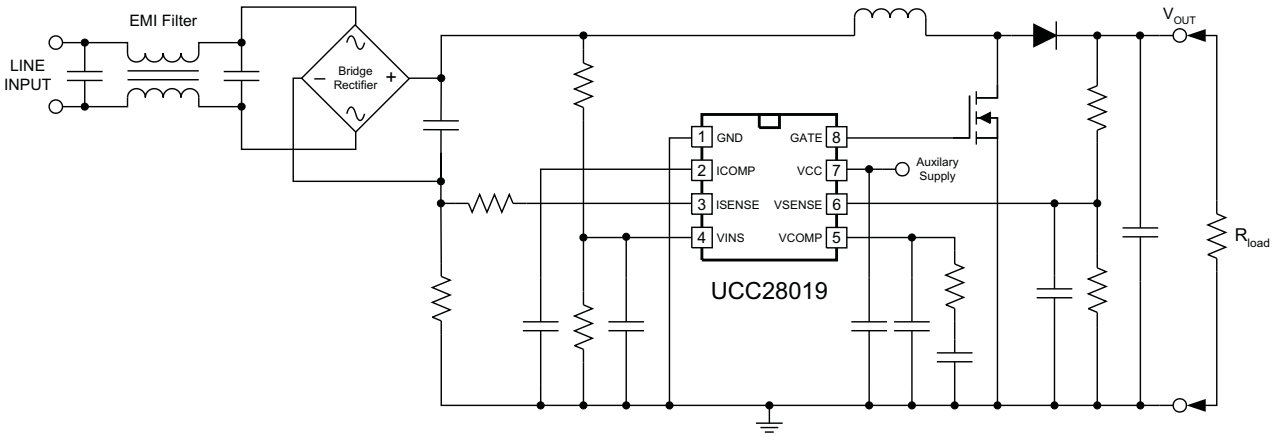
DESCRIPTION

The UCC28019 8-pin active Power Factor Correction (PFC) controller uses the boost topology operating in Continuous Conduction Mode (CCM). The controller is suitable for systems in the 100 W to >2 kW range over a wide-range universal ac line input. Startup current during under-voltage lockout is less than 200 µA. The user can control low power standby mode by pulling the VSENSE pin below 0.77 V.

Low-distortion wave-shaping of the input current using average current mode control is achieved without input line sensing, reducing the Bill of Materials component count. Simple external networks allow for flexible compensation of the current and voltage control loops. The switching frequency is internally fixed and trimmed to better than 5% accuracy at 25°C. Fast 1.5-A gate peak current drives the external switch.

Numerous system-level protection features include peak current limit, soft over-current detection, open-loop detection, input brown-out detection, output over-voltage protection/under-voltage detection, a no-power discharge path on VCOMP, and overload protection on ICOMP. Soft-Start limits boost current during start-up. A trimmed internal reference provides accurate protection thresholds and regulation set-point. An internal clamp limits the gate drive voltage to 12.5 V.

TYPICAL APPLICATION DIAGRAM



ORDERING INFORMATION

PART NUMBER	PACKAGE(1)	OPERATING TEMPERATURE RANGE, T_A
UCC28019D	SOIC 8-Pin (D) ead (Pb)-Free/Green	–40°C to 125°C
UCC28019P	Plastic DIP 8 Pin (P) Lead (Pb)-Free/Green	

(1) SOIC (D) package is available taped and reeled by adding "R" suffix the the above part number, reeled quantities are 2500 devices per reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input voltage range	VCC	–0.3 to 22	V
	GATE	–0.3 to 16	
	VINS, VSENSE, VCOMP, ICOMP	–0.3 to 7	
	ISENSE	–24 to 7	
Input current range	VSENSE, ISENSE	–1 to 1	mA
Junction temperature, T_J	Operating	–55 to 150	°C
	Storage	–65 to 150	
Lead temperature, T_{SOL}	Soldering, 10s	300°	

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

DISSIPATION RATINGS(1)

PACKAGE	THERMAL IMPEDANCE JUNCTION TO AMBIENT (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 85°C POWER RATING (W)
SOIC-8 (D)	160	0.65	0.25
PDIP-8 (P)	110	1	0.36

(1) Tested per JEDEC EIA/JESD 51-1. Thermal resistance is a strong function of board construction and layout. Air flow reduces thermal resistance. This number is only a general guide. See TI document SPRA953 Thermal Metrics.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
	VCC input voltage from a low-impedance source	$VCC_{OFF(max)}$ + 1 V	21	V
T_J	Operating junction temperature	–40	125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER	RATING	UNIT
Human Body Model (HBM)	2	kV
Charged Device Model (CDM)	500	V

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VCC = 15 V_{DC}, 0.1 µF from VCC to GND, -40°C ≤ T_J = T_A ≤ 125°C. All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC Bias Supply						
$I_{VCC(start)}$	Pre-start current	VCC = VCC_{ON} – 0.1 V	25	100	200	µA
$I_{VCC(stby)}$	Standby current	VSENSE = 0.5 V	1.0	2.1	2.9	mA
$I_{VCC(on\_load)}$	Operating current	VSENSE = 4.5 V, C_{GATE} = 4.7 nF	4	7	10	mA
Under Voltage Lockout (UVLO)						
VCC_{ON}	Turn on threshold		10.0	10.5	11.0	V
VCC_{OFF}	Turn off threshold		9	9.5	10	V
UVLO	Hysteresis		0.8	1.0	1.2	V
Oscillator						
f_{SW}	Switching frequency,	T_A = 25°C	61.7	65.0	68.3	kHz
		–40°C ≤ T_A ≤ 125°C	59	65	71	kHz
PWM						
D_{MIN}	Minimum duty cycle	VCOMP = 0 V, VSENSE = 5 V, ICOMP = 6.4 V			0%	
D_{MAX}	Maximum duty cycle	VSENSE = 4.95 V	94%	97%	99.3%	
$t_{OFF(min)}$	Minimum off time	VSENSE = 3 V, ICOMP = 1 V	100	250	600	ns
System Protection						
V_{SOC}	ISENSE threshold, soft over current (SOC) ,		-0.66	-0.73	-0.79	V
V_{PCL}	ISENSE threshold, peak current Limit (PCL) ,		-1.00	-1.08	-1.15	V
V_{OLP}	VSENSE threshold, open loop protection (OLP),	ICOMP = 1 V, ISENSE = 0 V, VCOMP = 1 V	0.77	0.82	0.86	V
	Open loop protection (OLP) internal pull-down current	VSENSE = 0.5 V		100	250	nA
V_{UVD}	VSENSE threshold, output under-voltage detection (UVD),		4.63	4.75	4.87	V
V_{OVP}	VSENSE threshold, output over-voltage protection (OVP),	ISENSE = -0.2 V	5.12	5.25	5.38	V
$VINS_{BROWNOUT\_th}$	Input brown-out detection (IBOP) high-to-low threshold		0.76	0.82	0.88	V
$VINS_{ENABLE\_th}$	Input brown-out Detection (IBOP) low-to-high threshold		1.4	1.5	1.6	V
$I_{VINS\_0\ V}$	VINS bias current	VINS = 0 V		0	±0.1	µA
	ICOMP threshold, external overload protection			0.6		V

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, VCC = 15 V_{DC}, 0.1 µF from VCC to GND, -40°C ≤ T_J = T_A ≤ 125°C. All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Loop						
gmi	Transconductance gain	T_A = 25°C	0.75	0.95	1.15	mS
	Output linear range			50		µA
	ICOMP voltage during OLP	VSENSE = 0.5 V	3.7	4.0	4.3	V
Voltage Loop						
V_{REF}	Reference voltage	-40°C ≤ T_A ≤ 125°C	4.90	5.00	5.10	V
gmv	Transconductance gain		31.5	42	52.5	µS
	Maximum sink current under normal operation	VSENSE = 6 V, VCOMP = 4 V	21	30	38	µA
	Source current under soft start	VSENSE = 4 V, VCOMP = 0 V	–21	-30	-38	
	Maximum source current under EDR operation	VSENSE = 4 V, VCOMP = 0 V	–100	–170	–250	
		VSENSE = 4 V, VCOMP = 4 V	–60	–100	–140	
	Enhanced dynamic response, V_{SENSE} low threshold, falling		4.63	4.75	4.87	V
	V_{SENSE} input bias current	1 V ≤ VSENSE ≤ 5 V		100	250	nA
	V_{COMP} voltage during OLP	VSENSE = 0.5 V, I_{VCOMP} = 0.5 mA	0	0.2	0.4	V
GATE Driver						
	GATE current, peak, sinking(1)	C_{GATE} = 4.7 nF		2.0		A
	GATE current, peak, sourcing(1)	C_{GATE} = 4.7 nF		–1.5		
	GATE rise time	C_{GATE} = 4.7 nF, GATE = 2 V to 8 V		40	60	ns
	GATE fall time	C_{GATE} = 4.7 nF, GATE = 8 V to 2 V		25	40	
	GATE low voltage, no load	GATE = 0 A		0	0.05	V
	GATE low voltage, sinking	GATE = 20 mA		0.3	0.8	
	GATE low voltage, sourcing	GATE = -20 mA		–0.3	–0.8	
	GATE low voltage, sinking	VCC = 5 V, GATE = 5 mA	0.2	0.75	1.2	
	GATE low voltage, sinking	VCC = 5 V, GATE = 20 mA	0.2	0.9	1.5	
	GATE high voltage	VCC = 20 V, C_{GATE} = 4.7 nF	11	12.5	14	
	GATE high voltage	VCC = 11 V, C_{GATE} = 4.7 nF	9.5	10.5	11.0	
	GATE high voltage	VCC = VCC_{OFF} + 0.2 V, C_{GATE} = 4.7 nF	8.0	9.0	10.2	

(1) Not tested. Characterized by design.

TYPICAL CHARACTERISTICS

Unless otherwise noted, VCC = 15 V_{DC}, 0.1 µF from VCC to GND, $T_J = T_A = 25°C$. All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

UVLO THRESHOLDS vs TEMPERATURE

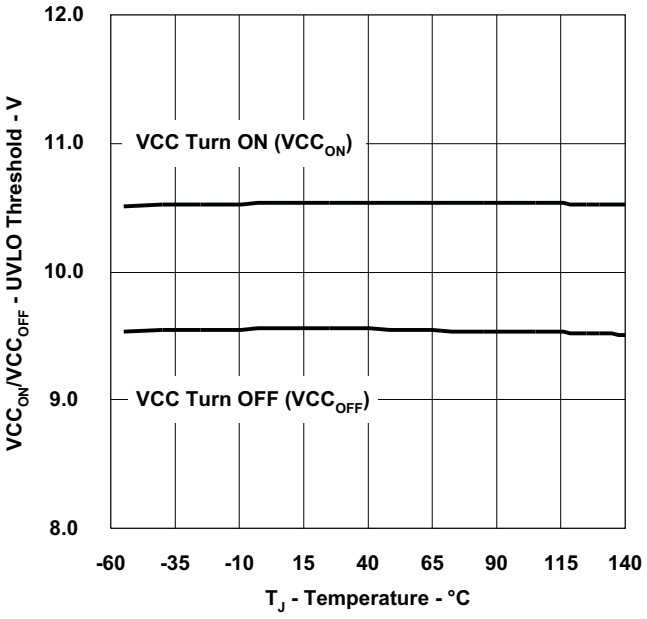


Figure 1.

SUPPLY CURRENT vs BIAS SUPPLY VOLTAGE

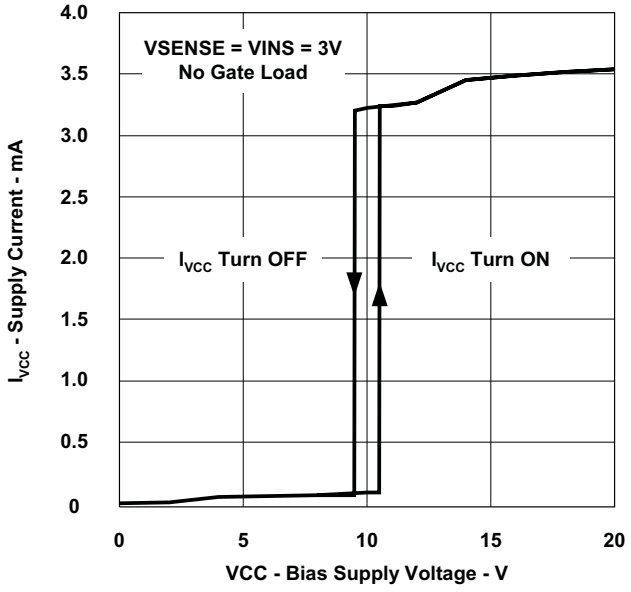


Figure 2.

SUPPLY CURRENT vs TEMPERATURE

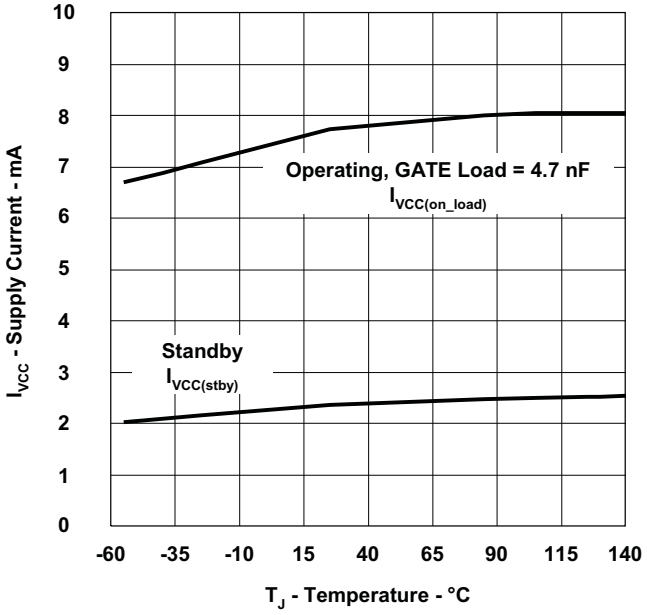


Figure 3.

SUPPLY CURRENT vs TEMPERATURE

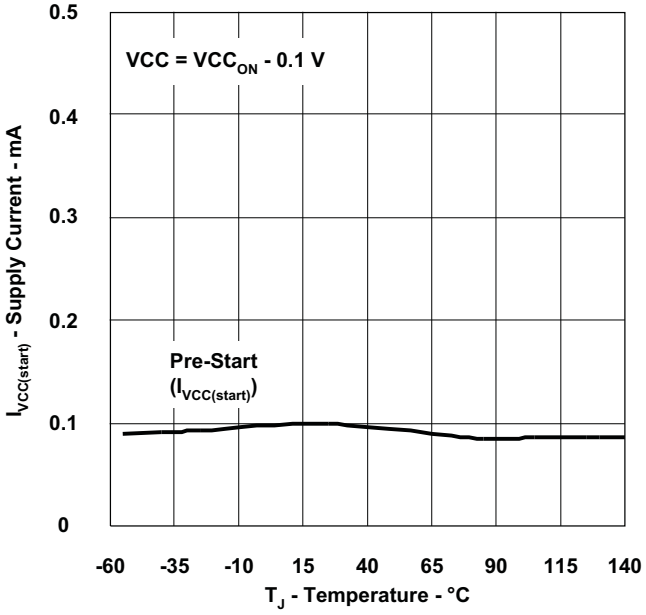


Figure 4.

TYPICAL CHARACTERISTICS (continued)

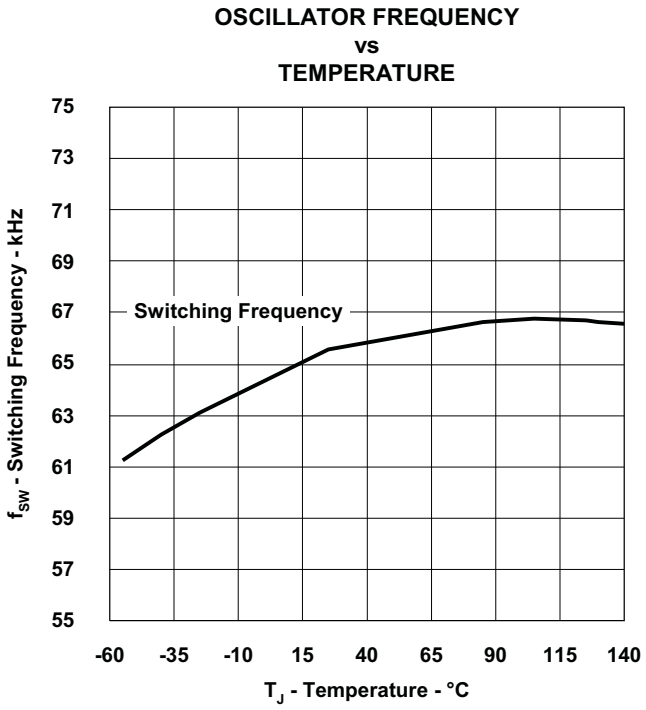


Figure 5.

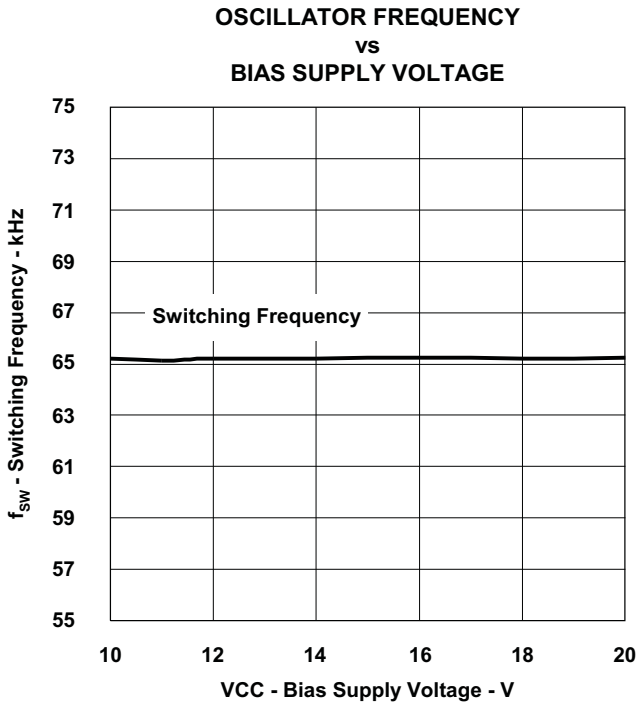


Figure 6.

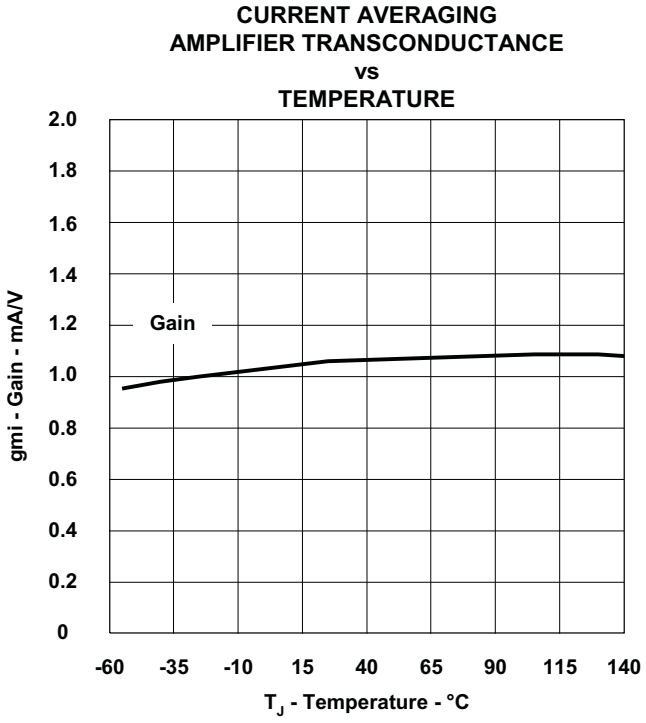


Figure 7.

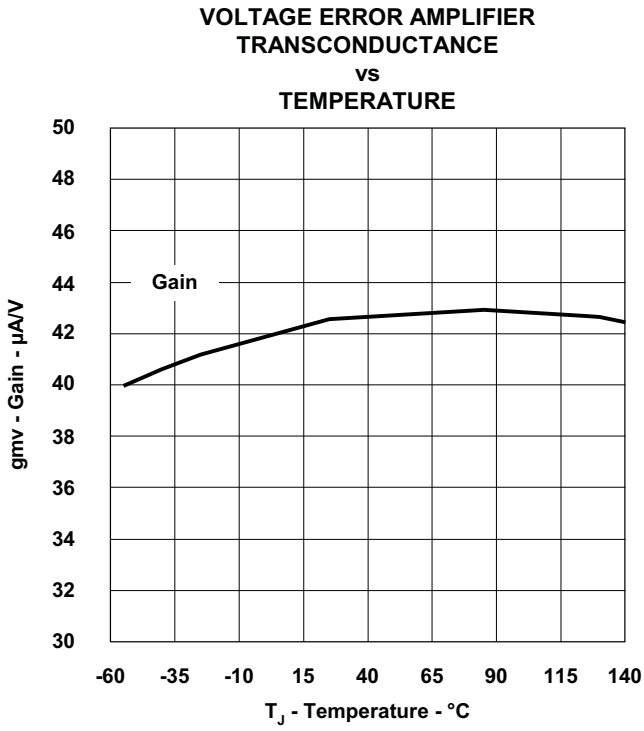


Figure 8.

TYPICAL CHARACTERISTICS (continued)

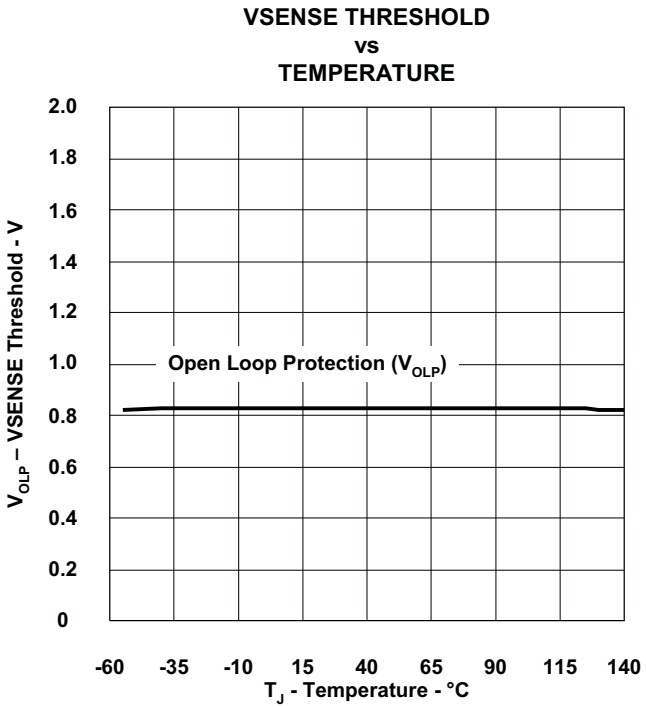


Figure 9.

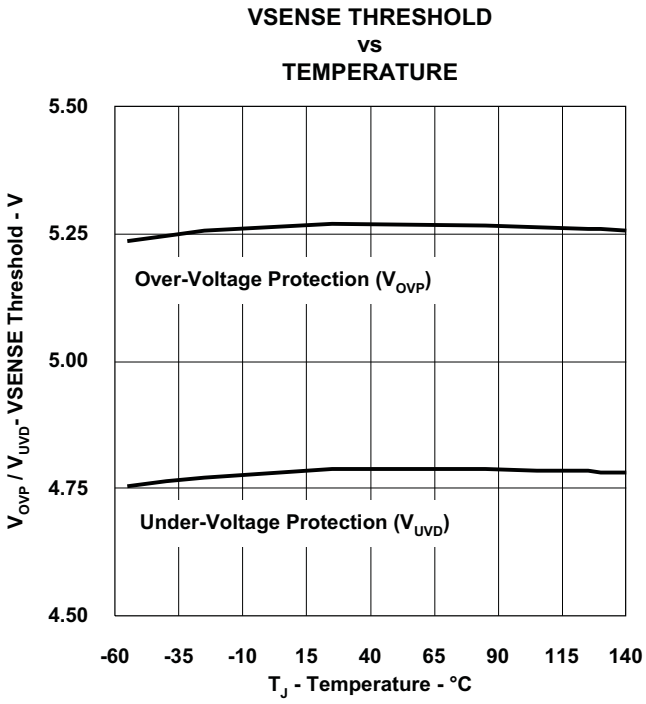


Figure 10.

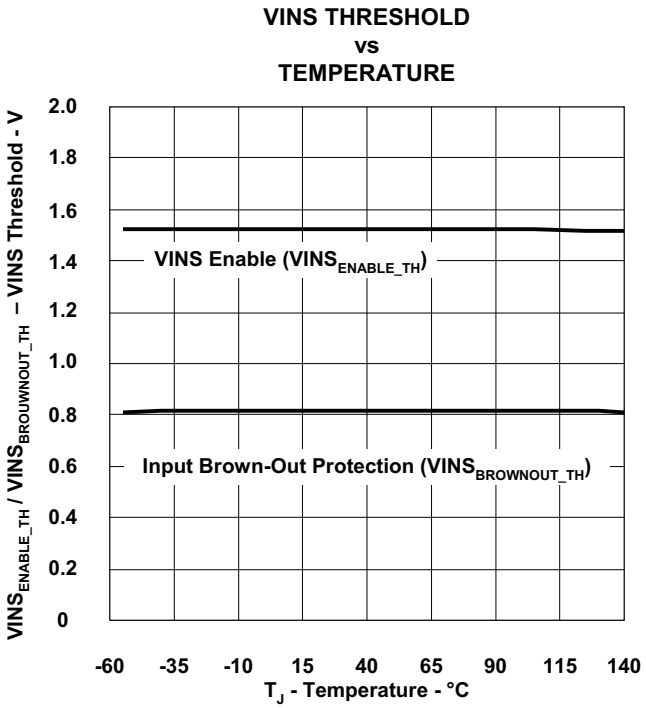


Figure 11.

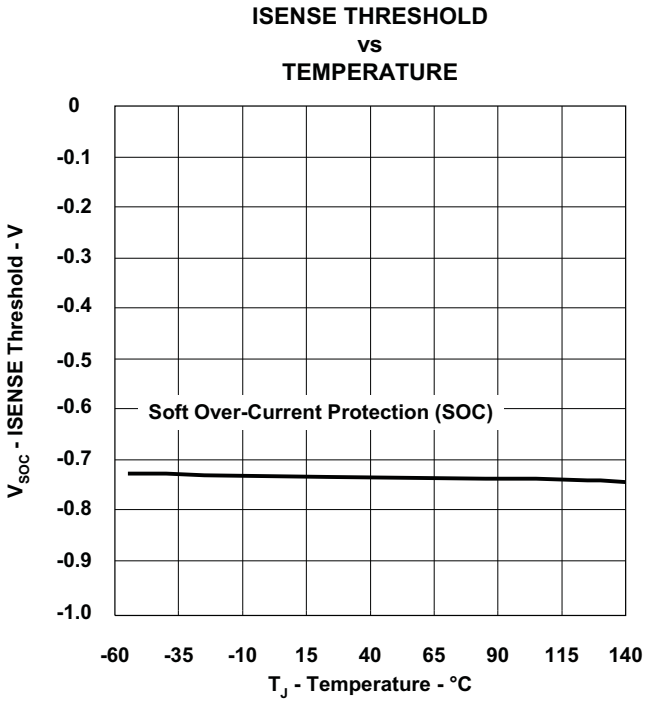


Figure 12.

TYPICAL CHARACTERISTICS (continued)

MINIMUM OFF TIME
vs
TEMPERATURE

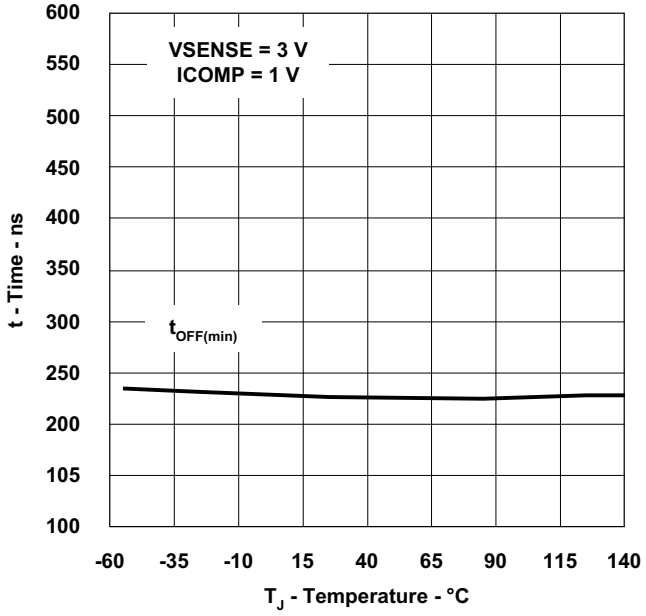


Figure 13.

GATE DRIVE SWITCHING
vs
TEMPERATURE

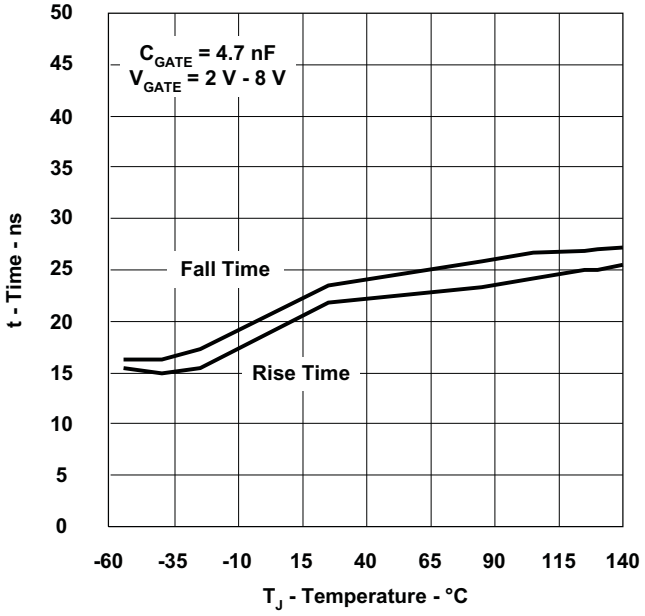


Figure 14.

GATE DRIVE SWITCHING
vs
BIAS SUPPLY VOLTAGE

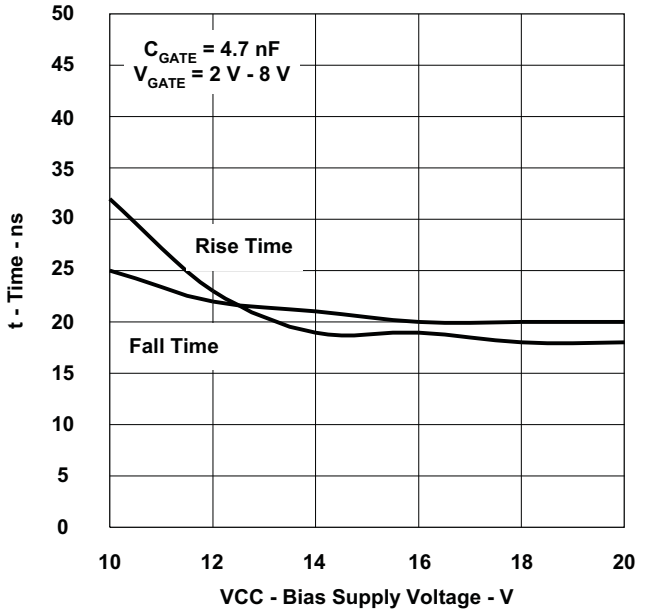


Figure 15.

GATE LOW VOLTAGE
WITH DEVICE OFF
vs
TEMPERATURE

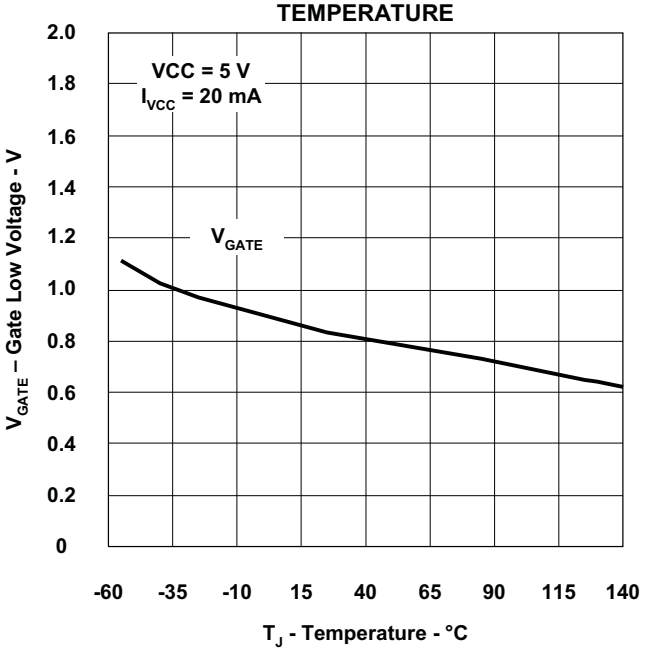


Figure 16.

TYPICAL CHARACTERISTICS (continued)

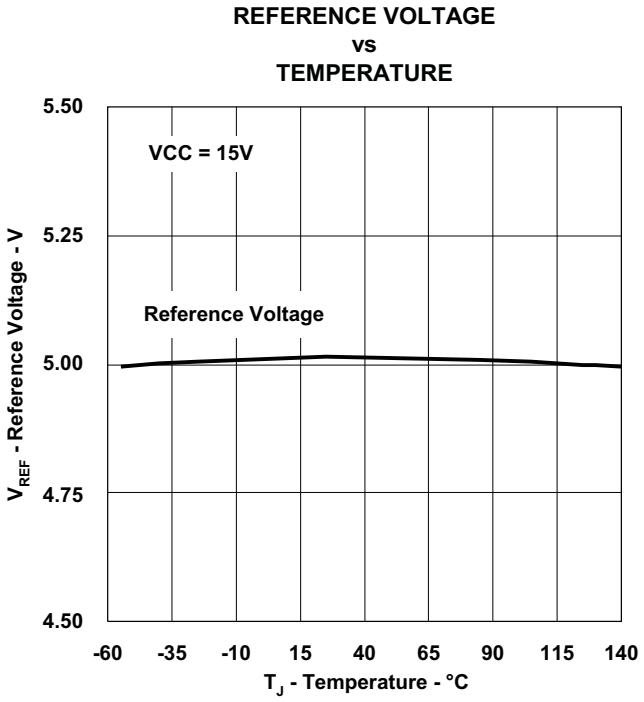
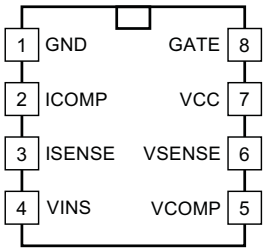


Figure 17.

DEVICE INFORMATION

Connection Diagram

UCC28019 Top View (SOIC-8, PDIP-8)



Pin Descriptions

Terminal Functions

TERMINAL		I/O	FUNCTION
NAME	#		
GATE	8	O	**Gate drive:** Integrated push-pull gate driver for one or more external power MOSFETs. 2.0-A sink and 1.5-A source capability. Output voltage is clamped at 12.5 V.
GND	1		**Ground:** Device ground reference.
ICOMP	2	O	**Current loop compensation:** Transconductance current amplifier output. A capacitor connected to GND provides compensation and averaging of the current sense signal in the current control loop. The controller is disabled if the voltage on ICOMP is less than 0.6 V.
ISENSE	3	I	**Inductor current sense:** An input for the voltage across the external current sense resistor, which represents the instantaneous current through the PFC boost inductor. This voltage is averaged to eliminate the effects of noise and ripple. Soft Over Current (SOC) limits the average inductor current. Cycle-by-cycle peak current limit (PCL) immediately shuts off the GATE drive if the peak-limit voltage is exceeded. Use a 220-Ω resistor between this pin and the current sense resistor to limit inrush-surge currents into this pin.
VCC	7		**Device supply:** External bias supply input. Under Voltage Lock Out (UVLO) disables the controller until VCC exceeds a turn-on threshold of 10.5 V. Operation continues until VCC falls below the turn-off (UVLO) threshold of 9.5 V. A ceramic by-pass capacitor of 0.1 µF minimum value should be connected from VCC to GND as close to the device as possible for high frequency filtering of the VCC voltage.
VCOMP	5	O	**Voltage loop compensation:** Transconductance voltage error amplifier output. A resistor-capacitor network connected from this pin to GND provides compensation. VCOMP is held at GND until VCC, VINS, and VSENSE all exceed their threshold voltages. Once these conditions are satisfied, VCOMP is charged until the VSENSE voltage reaches 95% of its nominal regulation level. When the Enhanced Dynamic Response (EDR) is engaged, additional current is applied to VCOMP to reduce the charge time. EDR additional current is inhibited during soft-start. Soft-start is programmed by the capacitance on this pin.
VINS	4	I	**Input ac voltage sense:** Input Brown Out Protection (IBOP) detects when the system ac-input voltage is above a user-defined normal operating level, or below a user-defined “brown-out” level. A filtered resistor-divider network connects from this pin to the rectified-mains node. At startup the controller is disabled until the VINS voltage exceeds a threshold of 1.5 V, initiating a soft-start. The controller is also disabled if VINS drops below the brown-out threshold of 0.8 V. Operation will not resume until both VINS and VSENSE voltages exceed their enable thresholds, initiating another soft-start.
VSENSE	6	I	**Output voltage sense:** An external resistor-divider network connected from this pin to the PFC output voltage provides feedback sensing for output voltage regulation. A small capacitor from this pin to GND filters high-frequency noise. Standby disables the controller and discharges VCOMP when the voltage at VSENSE drops below the enable threshold of 0.8V. An internal 100nA current source pulls VSENSE to GND for Open-Loop Protection (OLP), including pin disconnection. Output over-voltage protection (OVP) disables the GATE output when VSENSE exceeds 105% of the reference voltage. Enhanced Dynamic Response (EDR) rapidly returns the output voltage to its normal regulation level when a system line or load step causes VSENSE to fall below 95% of the reference voltage.

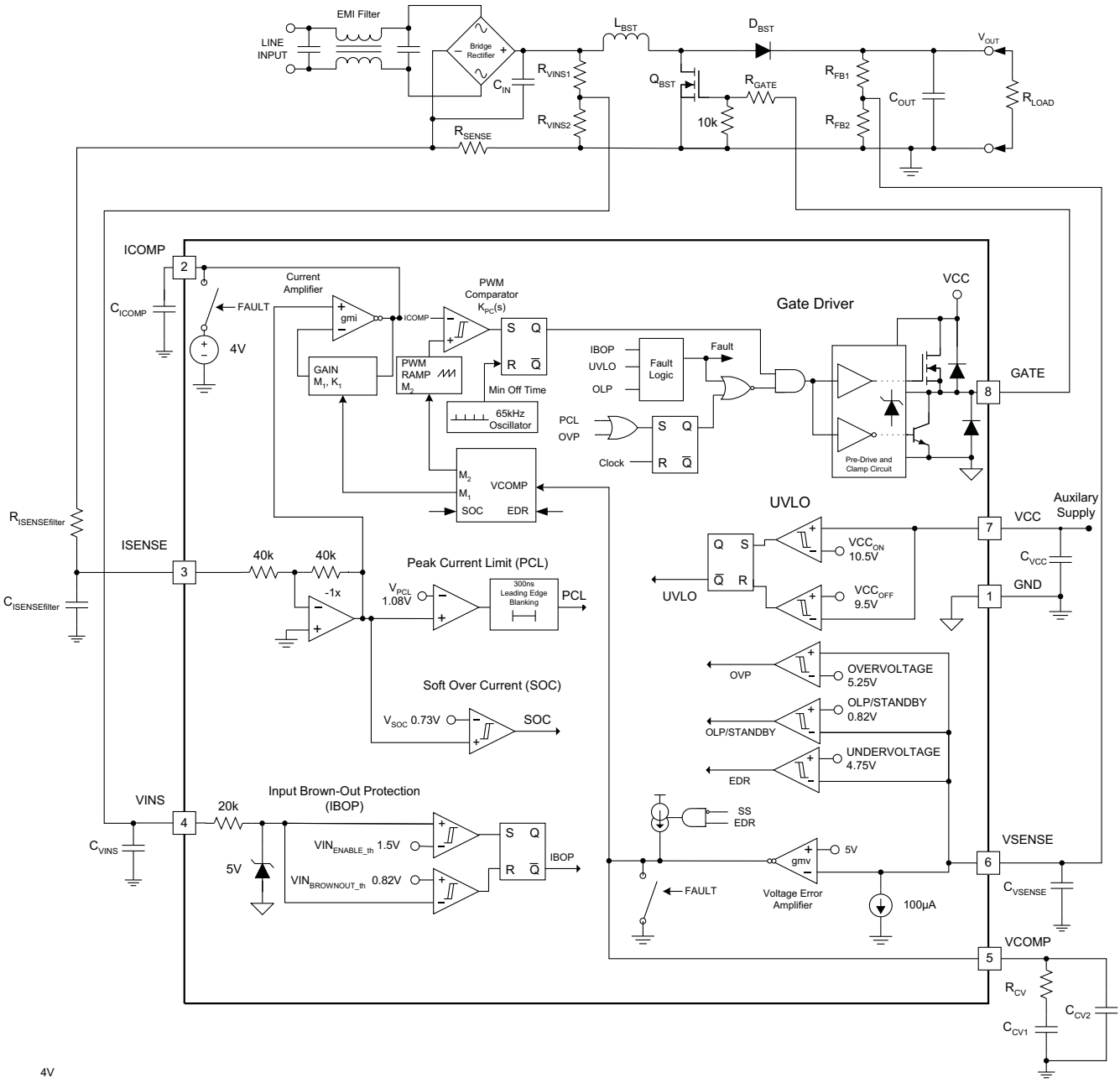


Figure 18. Block Diagram

APPLICATION INFORMATION

UCC28019 Operation

The UCC28019 is a switch-mode controller used in boost converters for power factor correction operating at a fixed frequency in continuous conduction mode. The UCC28019 requires few external components to operate as an active PFC pre-regulator. Its trimmed oscillator provides a nominal fixed switching frequency of 65 kHz, ensuring that both the fundamental and second harmonic components of the conducted-EMI noise spectrum are below the EN55022 conducted-band 150-kHz measurement limit.

Its tightly-trimmed internal 5-V reference voltage provides for accurate output voltage regulation over the typical world-wide 85 V_{AC} to 265 V_{AC} mains input range from zero to full output load. The usable system load ranges from 100 W to 2 kW and may be extended in special situations.

Regulation is accomplished in two loops. The inner current loop shapes the average input current to match the sinusoidal input voltage under continuous inductor current conditions. Under extremely light load conditions, depending on the boost inductor value, the inductor current may go discontinuous but still meet Class-D requirements of IEC 1000-3-2 despite the higher harmonics. The outer voltage loop regulates the output voltage on VCOMP (dependent upon the line and load conditions) which determines the internal gain parameters for maintaining a low-distortion steady-state input current waveshape.

Power Supply

The UCC28019 operates from an external bias supply. It is recommended that the device be powered from a regulated auxiliary supply. This device is not intended to be used from a bootstrap bias supply. A bootstrap bias supply is fed from the input high voltage through a resistor with sufficient capacitance on VCC to hold up the voltage on VCC until current can be supplied from a bias winding on the boost inductor. The minimal hysteresis on VCC would require an unreasonable value of hold-up capacitance.

During normal operation, when the output is regulated, current drawn by the device includes the nominal run current plus the current supplied to the gate of the external boost switch. Decoupling of the bias supply must take switching current into account in order to keep ripple voltage on VCC to a minimum. A ceramic capacitor with a minimum value of 0.1 µF is recommended from VCC to GND with short, wide traces.

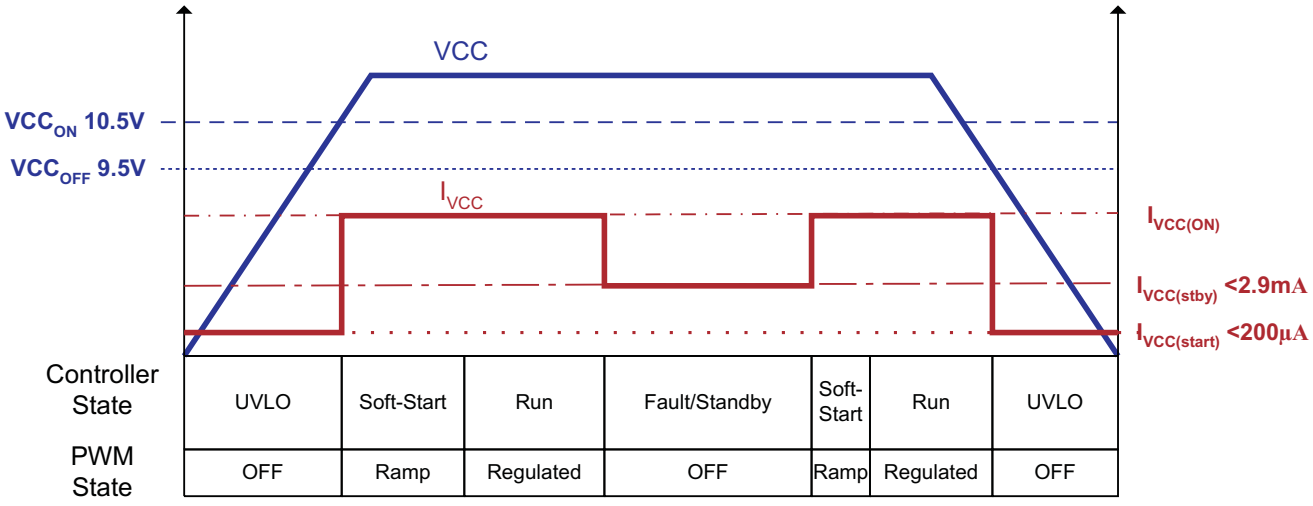


Figure 19. Device Supply States

The device bias operates in several states. During startup, VCC Under-Voltage LockOut (UVLO) sets the minimum operational dc input voltage of the PFC controller. There are two UVLO thresholds. When the UVLO turn-on threshold is exceeded, the controller turns ON. If VCC falls below the UVLO lower turn-off threshold, the controller turns OFF. During UVLO, current drawn by the device is minimal. After the device turns on, Soft Start (SS) is initiated and the output is ramped up in a controlled manner to reduce the stress on the external components and prevents output voltage overshoot. During soft start and after the output is in regulation, the device draws its normal run current. If any of several fault conditions is encountered or if the device is put in Standby with an external signal, the device draws a reduced standby current.

Soft Start

VCOMP, the output of the voltage loop transconductance amplifier, is pulled low during UVLO, IBOP, and OLP(Open-Loop Protection)/STANDBY. After the fault condition is released, soft start controls the rate of rise of VCOMP in order to obtain a linear control of the increasing duty cycle as a function of time. During soft start a constant 30 μA of current is sourced into the compensation components causing the voltage on this pin to ramp linearly until the output voltage reaches 85% of its final value. At this point, the sourcing current begins to decrease until the output voltage reaches 95% of its final rated voltage. The soft-start time is controlled by the voltage error amplifier compensation components selected, and is user-programmable based on desired loop crossover frequency. Once V_{OUT} exceeds 95% of rate voltage, EDR is no longer inhibited.

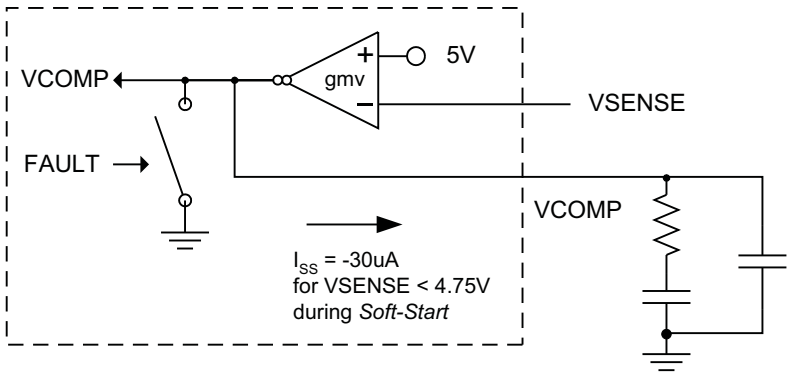


Figure 20. Soft Start

System Protection

System level protection features keep the system in safe operating limits:

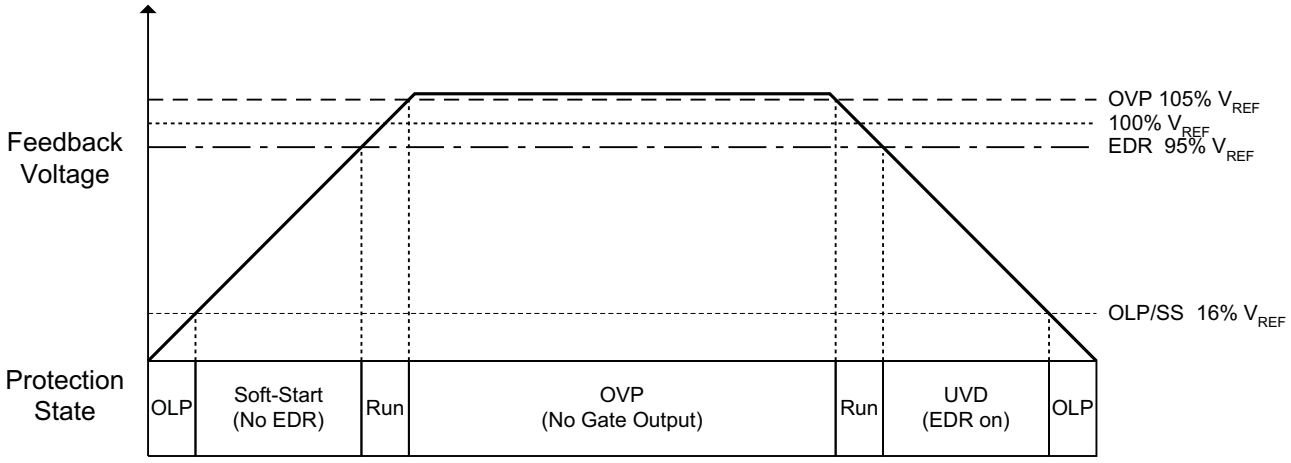


Figure 21. Output Protection States

VCC Under-Voltage Lockout (UVLO)

During startup, UVLO keeps the device in the off state until VCC rises above the 10.5-V enable threshold, VCC_{ON}. With a typical 1 V of hysteresis on UVLO to eliminate noise, the device turns off when VCC drops to the 9.5-V disable threshold, VCC_{OFF}.

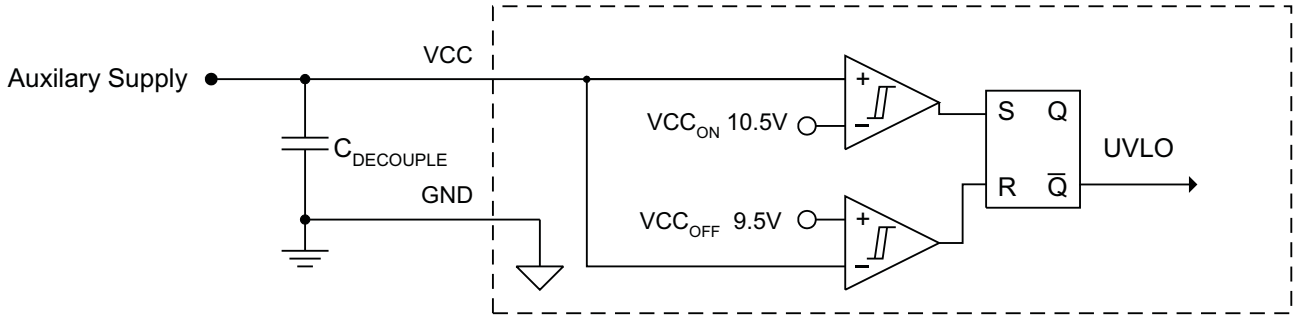


Figure 22. UVLO

Input Brown-Out Protection (IBOP)

The VINS, (sensed input line voltage), input provides a means for the designer to set the desired mains RMS voltage level at which the PFC pre-regulator should start-up, $V_{AC(turnon)}$, as well as the desired mains RMS level at which it should shut down, $V_{AC(turnoff)}$. This prevents unwanted sustained system operation at or below a "brown-out" voltage, where excessive line current could overheat components. In addition, because VCC bias is not derived directly from the line voltage, IBOP protects the circuit from low line conditions that may not trigger the VCC UVLO turn-off.

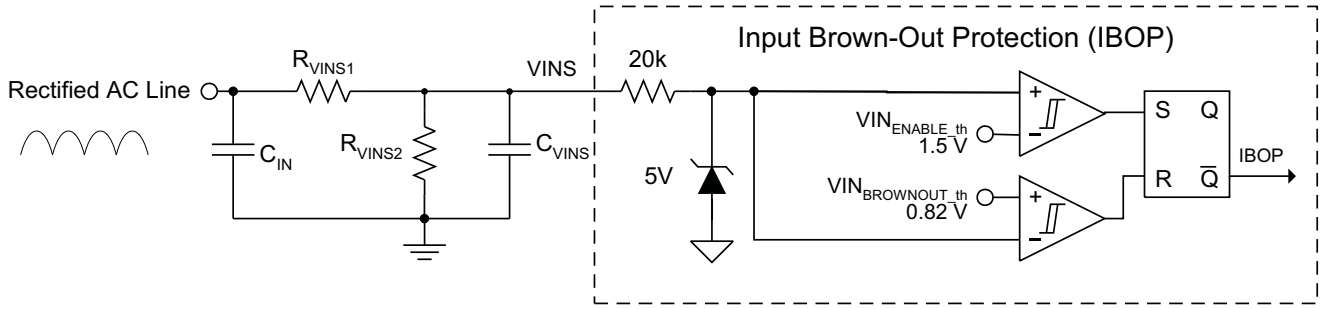


Figure 23. Input Brown-Out Protection (IBOP)

Input line voltage is sensed directly from the rectified ac mains voltage through a resistor divider filter network providing a scaled and filtered value at the VINS input. IBOP puts the device in standby mode when VINS falls (high-to-low) below 0.8 V, $VINS_{BROWNOUT\_th}$. The device comes out of standby when VINS rises (low-to-high) above 1.5 V, $VINS_{ENABLE\_th}$. $I_{VINS\_0\ V}$, bias current sourced from VINS, is less than 0.1 µA. With a bias current this low, there is little concern for any set-point error caused by this current flowing through the sensing network. The highest reasonable value resistance for this network should be chosen to minimize power dissipation, especially in applications requiring low standby power. Be aware that higher resistance values are more susceptible to noise pickup, but low noise PCB layout techniques can help mitigate this. Also, depending on the resistor type used and its voltage rating, R_{VINS1} should be implemented with multiple resistors in series to reduce voltage stresses.

First, select R_{VINS1} based on the the highest reasonable resistance value available for typical applications.

Then select R_{VINS2} based on this value:

$$R_{VINS2} = R_{VINS1} \frac{VINS_{ENABLE\_th(max)}}{\sqrt{2}V_{AC(on)} - VINS_{ENABLE\_th(max)} - V_{F\_BRIDGE}}$$

Where V_{F_Bridge} is the forward voltage drop across the ac rectifier bridge.

Power dissipated in the resistor network is:

$$P_{VINS} = \frac{V_{IN\_RMS}^{2}}{R_{VINS1} + R_{VINS2}}$$

The filter capacitor, C_{VINS}, has two functions. First, to attenuate the voltage ripple to levels between the enable and brown-out thresholds which will prevent the ripple on VINS from falsely triggering IBOP when the converter is operating at low line. Second, C_{VINS} delays the brown-out protection operation for a desired number of line half-cycle periods while still having a good response to an actual brown-out event.

The capacitor is chosen so that it will discharge to the $VINS_{BROWNOUT\_th}$ level after N number of half line cycles of delay to accommodate line dropouts.

$$C_{VINS} = \frac{-t_{CVIN\_dschg}}{R_{VINS2}\ell n\left[\frac{VINS_{BROWNOUT\_th(min)}}{0.9V_{IN\_RMS(min)}\left(\frac{R_{VINS2}}{R_{VINS1} + R_{VINS2}}\right)}\right]}$$

Where:

$$t_{CVINS\_dschrg} = \frac{N_{half\_cycles}}{2f_{LINE(min)}}$$

and $V_{IN\_RMS(min)}$ is the lowest normal operating RMS input voltage.

Output Over-Voltage Protection (OVP)

$V_{OUT(OVP)}$ is the output voltage exceeding 5% of the rated value, causing VSENSE to exceed a 5.25-V threshold (5-V reference voltage + 5%), V_{OVP}. The normal voltage control loop is bypassed and the GATE output is disabled until VSENSE falls below 5.25 V. For example, $V_{OUT(OVP)}$ is 420 V in a system with a 400-V rated output.

Open Loop Protection/Standby (OLP/Standby)

If the output voltage feedback components were to fail and disconnect (open loop) the signal from the VSENSE input, then it is likely that the voltage error amp would increase the GATE output to maximum duty cycle. To prevent this, an internal pull-down forces VSENSE low. If the output voltage falls below 16% of its rated voltage, causing VSENSE to fall below 0.8 V, the device is put in Standby, a state where the PWM switching is halted and the device is still on but draws standby current below 3 mA. This shutdown feature also gives the designer the option of pulling VSENSE low with an external switch.

Output Under-Voltage Detection (UVD) / Enhanced Dynamic Response (EDR)

During large changes in load, Enhanced Dynamic Response (EDR) acts to speed up the slow response of the low-bandwidth voltage loop.

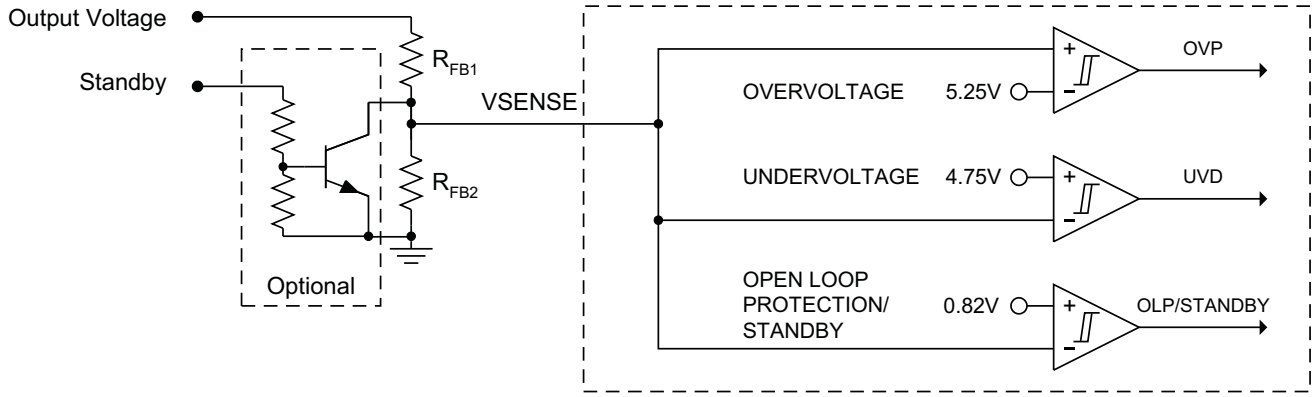


Figure 24. Over Voltage Protection, Open Loop Protection/Standby

Overcurrent Protection

Inductor current is sensed by R_{SENSE}, a low value resistor in the return path of input rectifier. The other side of the resistor is tied to the system ground. The voltage is sensed on the rectifier side of the sense resistor and is always negative. There are two over-current protection features; Peak Current Limit (PCL) protects against inductor saturation and Soft Over Current (SOC) protects against an overload on the output.

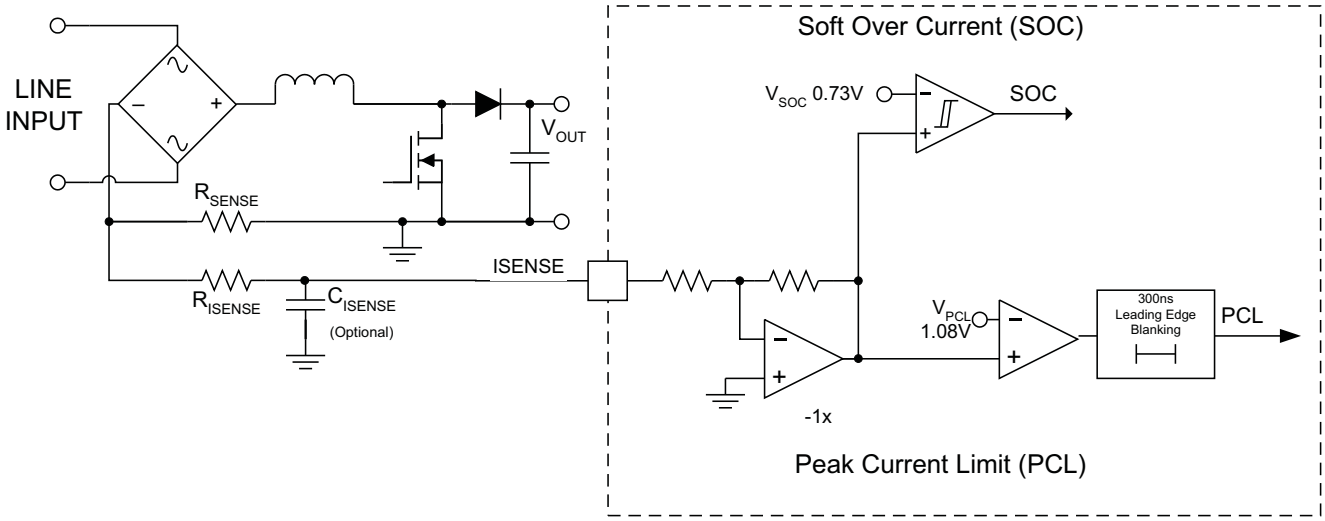


Figure 25. Soft Over Current (SOC) / Peak Current Limit (PCL)

Soft Over-Current (SOC)

SOC limits the input current. SOC is activated when the current sense voltage on ISENSE reaches -0.73 V, affecting the internal VCOMP level, and the control loop is adjusted to reduce the PWM duty cycle.

Peak Current Limit (PCL)

Peak current limit operates on a cycle-by-cycle basis. When the current sense voltage on ISENSE reaches -1.08 V, PCL is activated terminating the active switch cycle. The voltage at ISENSE is amplified by a fixed gain of -1.0 and then leading-edge blanked to improve noise immunity against false triggering.

Current Sense Resistor, R_{SENSE}

The current sense resistor, R_{SENSE}, is sized using the minimum threshold value of Soft Over Current (SOC), $V_{SOC(min)}$ = 0.66 V. To avoid triggering this threshold during normal operation, taking into account the gain of the internal non-linear power limit, resulting in a decreased duty cycle, the resistor is typically sized for an overload current of 25% more than the peak inductor peak current.

$$R_{SENSE} \le \frac{V_{SOC(min)}}{1.25\, I_{L\_PEAK(max)}}$$

Since R_{SENSE} sees the average input current, worst-case power dissipation occurs at input low line when input line current is at its maximum. Power dissipated by the sense resistor is:

$$P_{RSENSE} = (I_{IN\_RMS(max)})^2 R_{SENSE}$$

Peak Current Limit (PCL) protection turns off the output driver when the voltage across the sense resistor reaches the PCL threshold, V_{PCL}. The absolute maximum peak current, I_{PCL}, is given as:

$$I_{PCL} = \frac{V_{PCL}}{R_{SENSE}}$$

Gate Driver

The GATE output is designed with a current-optimized structure to directly drive large values of total MOSFET gate capacitance at high turn-on and turn-off speeds. An internal clamp limits voltage on the MOSFET gate to 12.5 V. An external gate drive resistor, R_{GATE}, limits the rise time and dampens ringing caused by parasitic inductances and capacitances of the gate drive circuit thus reducing EMI. The final value of the resistor depends upon the parasitic elements associated with the layout and other considerations. A 10-kΩ resistor close to the gate of the MOSFET, between the gate and ground, discharges stray gate capacitance and protects against inadvertent dv/dt-triggered turn-on.

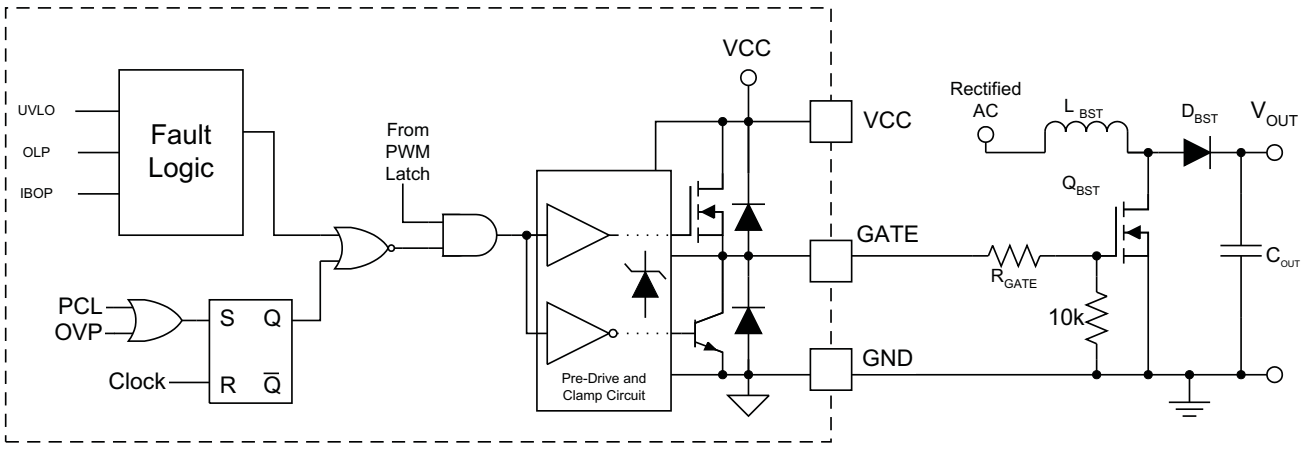


Figure 26. Gate Driver

Current Loop

The overall system current loop consists of the current averaging amplifier stage, the pulse width modulator (PWM) stage, the external boost inductor stage, and the external current sensing resistor.

ISENSE and ICOMP Functions

The negative polarity signal from the current sense resistor is buffered and inverted at the ISENSE input. The internal positive signal is then averaged by the current amplifier (gmi), whose output is the ICOMP pin. The voltage on ICOMP is proportional to the average inductor current. An external capacitor to GND is applied to the ICOMP pin for current loop compensation and current ripple filtering. The gain of the averaging amplifier is determined by the internal VCOMP voltage. This gain is non-linear to accommodate the world-wide ac-line voltage range. ICOMP is connected to 4 V internally whenever the device is in a Fault or Standby condition.

Pulse Width Modulator

The PWM stage compares the ICOMP signal with a periodic ramp to generate a leading-edge-modulated output signal which is high whenever the ramp voltage exceeds the ICOMP voltage. The slope of the ramp is defined by a non-linear function of the internal VCOMP voltage.

The PWM output signal always starts low at the beginning of the cycle, triggered by the internal clock. The output stays low for a minimum off-time, $t_{OFF(min)}$, after which the ramp rises linearly to intersect the ICOMP voltage. The ramp-I_{COMP} intersection determines t_{OFF}, and hence D_{OFF}. Since $D_{OFF} = V_{IN}/V_{OUT}$ by the boost-topology equation, and since V_{IN} is sinusoidal in wave-shape, and since ICOMP is proportional to the inductor current, it follows that the control loop forces the inductor current to follow the input voltage wave-shape to maintain boost regulation. Therefore, the average input current is also sinusoidal in wave-shape.

Control Logic

The output of the PWM comparator stage is conveyed to the GATE drive stage, subject to control by various protection functions incorporated into the IC. The GATE output duty-cycle may be as high as 99%, but will always have a minimum off-time $t_{OFF(min)}$. Normal duty-cycle operation can be interrupted directly by OVP and PCL on a cycle-by-cycle basis. UVLO, IBOP and OLP/Standby also terminate the GATE output pulse, and further inhibit output until the SS operation can begin.

Voltage Loop

The outer control loop of the PFC controller is the voltage loop. This loop consists of the PFC output sensing stage, the voltage error amplifier stage, and the non-linear gain generation.

Output Sensing

A resistor-divider network from the PFC output voltage to GND forms the sensing block for the voltage control loop. The resistor ratio is determined by the desired output voltage and the internal 5-V regulation reference voltage.

Like the VINS input, the very low bias current at the VSENSE input allows the choice of the highest practicable resistor values for lowest power dissipation and standby current. A small capacitor from VSENSE to GND serves to filter the signal in a high-noise environment. This filter time constant should generally be less than 100 µs.

Voltage Error Amplifier

The transconductance error amplifier (gmv) generates an output current proportional to the difference between the voltage feedback signal at VSENSE and the internal 5-V reference. This output current charges or discharges the compensation network capacitors on the VCOMP pin to establish the proper VCOMP voltage for the system operating conditions. Proper selection of the compensation network components leads to a stable PFC pre-regulator over the entire ac-line range and 0-100% load range. The total capacitance also determines the rate-of-rise of the VCOMP voltage at soft start, as discussed earlier.

The amplifier output VCOMP is pulled to GND during any Fault or Standby condition to discharge the compensation capacitors to an initial zero state. Usually, the large capacitor has a series resistor which delays complete discharge by their respective time constant (which may be several hundred milliseconds). If VCC bias voltage is quickly removed after UVLO, the normal discharge transistor on VCOMP loses drive and the large capacitor could be left with substantial voltage on it, negating the benefit of a subsequent Soft-Start. The UCC28019 incorporates a parallel discharge path which operates without VCC bias, to further discharge the compensation network after VCC is removed.

When output voltage perturbations greater than 5% appear at the VSENSE input, the amplifier moves out of linear operation. On an over-voltage, the OVP function acts directly to shut off the GATE output until VSENSE returns within 5% of regulation. On an under-voltage, the UVD function invokes EDR which immediately increases the internal VCOMP voltage by 2 V and increases the external VCOMP charging current typically to 100 μA to 170 μA. This higher current facilitates faster charging of the compensation capacitors to the new operating level, improving transient response time.

Non-linear Gain Generation

The voltage at VCOMP is used to set the current amplifier gain and the PWM ramp slope. This voltage is buffered internally and is then subject to modification by the EDR function and the SOC function, as discussed earlier.

Together the current gain and the PWM slope adjust to the different system operating conditions (set by the ac-line voltage and output load level) as VCOMP changes, to provide a low-distortion, high-power-factor input current wave-shape following that of the input voltage.

Layout Guidelines

As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. The pinout of the UCC28019 is ideally suited for separating the high di/dt induced noise on the power ground from the low current quiet signal ground required for adequate noise immunity. A star point ground connection at the GND pin of the device can be achieved with a simple cut out in the ground plane of the printed circuit board. As shown in Figure 27, the capacitors on ISENSE, VINS, VCOMP, and VSENSE (C11, C12, C15, C17, and C16, respectively) must all be returned directly to the quiet portion of the ground plane, indicated by Signal GND, and not the high current return path of the converter, shown as the Power GND. Because the example circuit in Figure 27 uses surface mount components, the ICOMP capacitor, C10, has its own dedicated return to the GND pin.

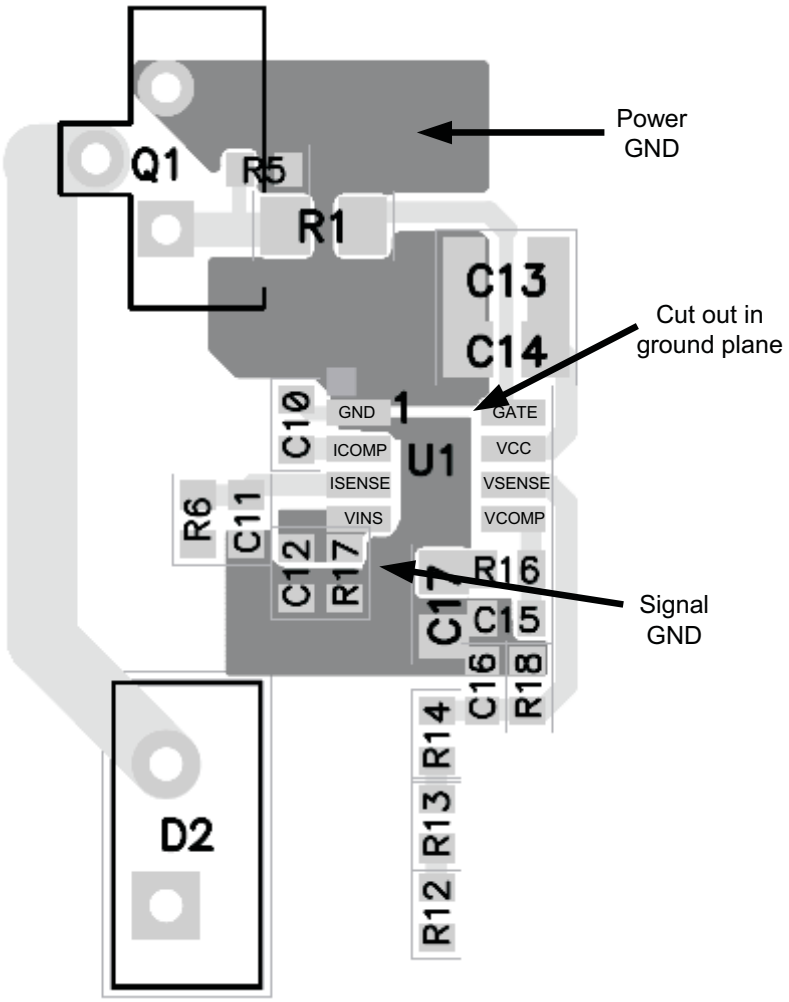


Figure 27. Recommended Layout for the UCC28019

DESIGN EXAMPLE

350-W, Universal Input, 390-V_{DC} Output, PFC Converter

Design Goals

This example illustrates the design process and component selection for a continuous conduction mode power factor correction boost converter utilizing the UCC28019. The target design is a universal input, 350-W PFC designed for an ATX supply application. This design process is directly tied to the UCC28019 Design Calculator spreadsheet that can be found in the Tools section of the UCC28019 product folder on the Texas Instruments website.

Table 1. Design Goal Parameters

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Input characteristics					
Input voltage	V_{IN}	85	115	265	VAC
Input frequency	f_{LINE}	47		63	Hz
Brown out voltage	$V_{AC(on)}$ I_{OUT} = 0.9 A		75		VAC
	$V_{AC(off)}$ I_{OUT} = 0.9 A		65		
Output characteristics					
Output voltage	V_{OUT} 85 VAC ≤ V_{IN} ≤ 265 VAC 47 Hz ≤ f_{LINE} ≤ 63 Hz 0 A ≤ I_{OUT} ≤ 0.9 A	370	390	410	VDC
Line regulation	85 VAC ≤ V_{IN} ≤ 65VAC I_{OUT} = 0.440 A			5%	
Load regulation	V_{IN} = 115 VAC, f_{LINE} = 60 Hz 0 A ≤ I_{OUT} ≤ 0.9 A			5%	
	V_{IN} = 230 VAC, f_{LINE} = 50 Hz 0 A ≤ I_{OUT} ≤ 0.9 A			5%	
High frequency output voltage ripple	$V_{RIPPLE(SW)}$ V_{IN} = 115 VAC, f_{LINE} = 60 Hz I_{OUT} = 0.9 A			3.9	Vpp
	$V_{RIPPLE(SW)}$ V_{IN} = 230 VAC , f_{LINE} = 50 Hz I_{OUT} = 0.9 A			3.9	
Line frequency output voltage ripple	$V_{RIPPLE(f\_LINE)}$ V_{IN} = 115 VAC, f_{LINE} = 60 Hz, I_{OUT} = 0.9 A			19.5	
	$V_{RIPPLE(f\_LINE)}$ V_{IN} = 230 VAC, f_{LINE} = 50 Hz I_{OUT} = 0.9 A			19.5	
Output load current	I_{OUT} 85 VAC ≤ V_{IN} ≤ 265 VAC 47 Hz ≤ f_{LINE} ≤ 63 Hz			0.9	A
Output power	P_{OUT}			350	W
Output over voltage protection	$V_{OUT(OVP)}$		410		V
Output under voltage protection	$V_{OUT(UVP)}$		370		

Table 1. Design Goal Parameters (continued)

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Control loop characteristics					
Switching frequency	f_{SW}, T_J = 25°C	61.7	65	68.3	kHz
Control loop bandwidth	$f_{(CO)}$ V_{IN} = 162 VDC, I_{OUT} = 0.45 A		10		Hz
Phase margin	V_{IN} = 162 VDC, I_{OUT} = 0.45 A		70		degrees
Power factor	PF V_{IN} = 115 VAC, I_{OUT} = 0.9 A		0.99		
Total harmonic distortion	THD V_{IN} = 115 VAC, f_{LINE} = 60 Hz I_{OUT} = 0.9 A		4.13%	10%	
	THD V_{IN} = 230 VAC, f_{LINE} = 50 Hz I_{OUT} = 0.9 A		6.67%	10%	
Full load efficiency	η V_{IN} = 115 VAC, f_{LINE} = 60 Hz, I_{OUT} = 0.9 A	0.92			
Ambient temperature	T_{AMB}			50	°C

The following procedure refers to the schematic shown in Figure 28.

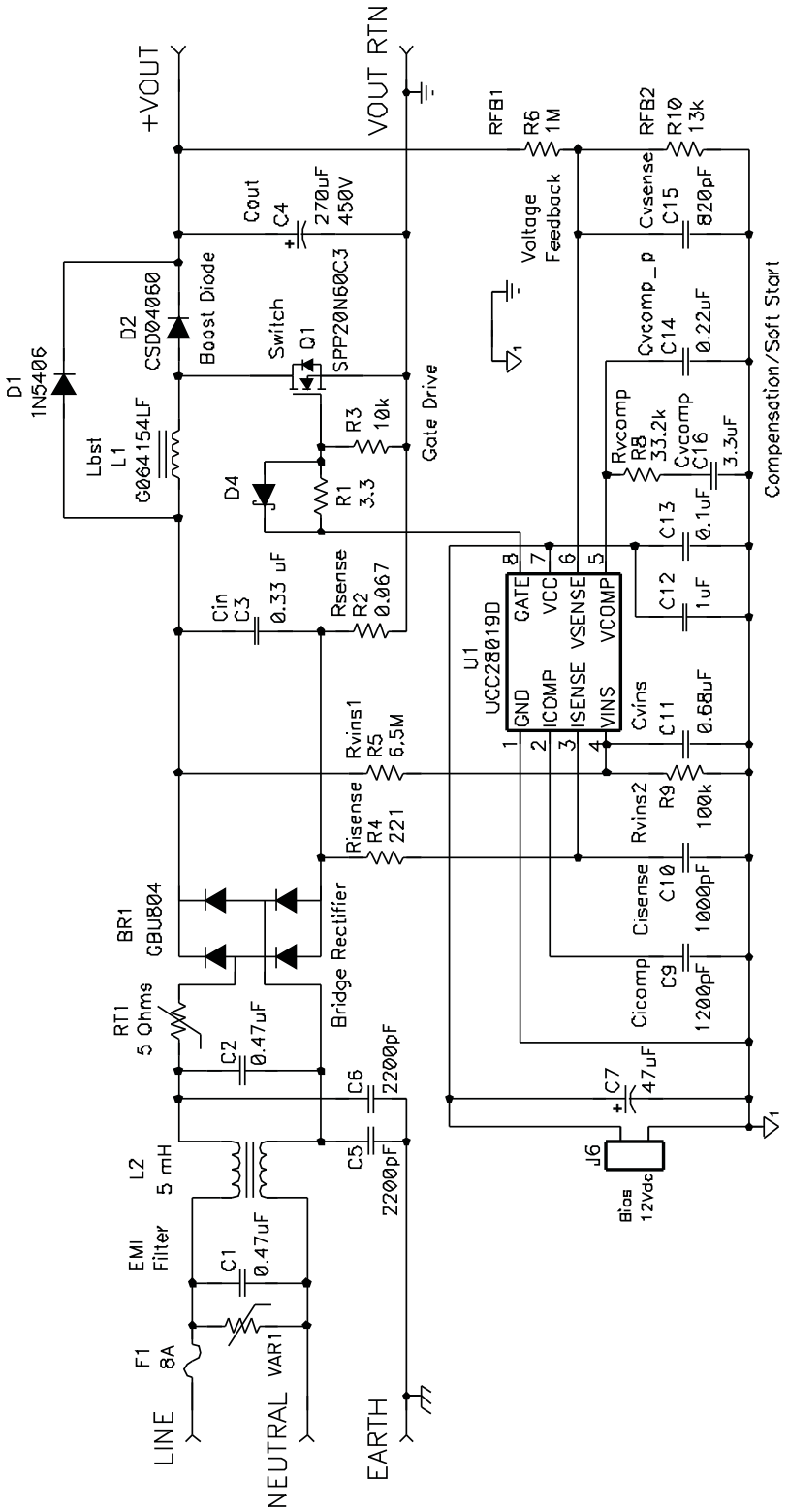


Figure 28. Design Example Schematic

Current Calculations

First, determine the maximum average output current, $I_{OUT(max)}$:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}}$$

$$I_{OUT(max)} = \frac{350W}{390V} \cong 0.9A$$

The maximum input RMS line current, $I_{IN\_RMS(max)}$, is calculated using the parameters from Table 1 and the efficiency and power factor initial assumptions:

$$I_{IN\_RMS(max)} = \frac{P_{OUT(max)}}{\eta V_{IN(min)} PF}$$

$$I_{IN\_RMS(max)} = \frac{350W}{0.92 \times 85V \times 0.99} = 4.52A$$

Based upon the calculated RMS value, the maximum peak input current, $I_{IN\_PEAK(max)}$, and the maximum average input current, $I_{IN\_AVG(max)}$, assuming the waveform is sinusoidal, can be determined.

$$I_{IN\_PEAK(max)} = \sqrt{2} I_{IN\_RMS(max)}$$

$$I_{IN\_PEAK(max)} = \sqrt{2} \times 4.52A = 6.39A$$

$$I_{IN\_AVG(max)} = \frac{2 I_{IN\_PEAK(max)}}{\pi}$$

$$I_{IN\_AVG(max)} = \frac{2 \times 6.39A}{\pi} = 4.07A$$

Bridge Rectifier

Assuming a forward voltage drop, V_{F_BRIDGE}, of 0.95 V across the rectifier diodes, BR1, the power loss in the input bridge, P_{BRIDGE}, can be calculated:

$$P_{BRIDGE} = 2 V_{F\_BRIDGE} I_{IN\_AVG(max)}$$

$$P_{BRIDGE} = 2 \times 0.95V \times 4.07A = 7.73W$$

Input Capacitor

Note that the UCC28019 is a continuous conduction mode controller and as such the inductor ripple current should be sized accordingly. Allowing an inductor ripple current, I_{RIPPLE}, of 20% and a high frequency voltage ripple factor, V_{RIPPLE_IN}, of 6%, the maximum input capacitor value, C_{IN}, is calculated by first determining the input ripple current, I_{RIPPLE}, and the input voltage ripple, $V_{IN\_RIPPLE(max)}$:

$$I_{RIPPLE} = \Delta I_{RIPPLE} I_{IN\_PEAK(max)}$$

$$\Delta I_{RIPPLE} = 0.2$$

$$I_{RIPPLE} = 0.2 \times 6.39A = 1.28A$$

$$V_{IN\_RIPPLE(max)} = \Delta V_{RIPPLE\_IN} V_{IN\_RECTIFIED(min)}$$

$$\Delta V_{RIPPLE\_IN} = 0.06$$

$$V_{IN\_RECTIFIED} = \sqrt{2} V_{IN}$$

$$V_{IN\_RECTIFIED(min)} = \sqrt{2} \times 85V = 120.2V$$

$$V_{IN\_RIPPLE(max)} = 0.06 \times 120.2V = 7.21V$$

The value for the input x-capacitor can now be calculated:

$$C_{IN} = \frac{I_{RIPPLE}}{8 f_{SW} V_{IN\_RIPPLE(max)}}$$

$$C_{IN} = \frac{1.28A}{8 \times 65kHz \times 7.21V} = 0.341\mu F$$

Boost Inductor

The boost inductor, L_{BST}, is selected after determining the maximum inductor peak current, $I_{L\_PEAK(max)}$:

$$I_{L\_PEAK(max)} = I_{IN\_PEAK(max)} + \frac{I_{RIPPLE}}{2}$$

$$I_{L\_PEAK(max)} = 6.39A + \frac{1.28A}{2} = 7.03A$$

The minimum value of the boost inductor is calculated based upon a worst case duty cycle of 0.5:

$$L_{BST(min)} \geq \frac{V_{OUT} D(1-D)}{f_{SW(typ)} I_{RIPPLE}}$$

$$L_{BST(min)} \geq \frac{390V \times 0.5(1-0.5)}{65kHz \times 1.28A} \geq 1.17mH$$

The actual value of the boost inductor that will be used is 1.25 mH.

The maximum duty cycle, $DUTY_{(max)}$, can be calculated and will occur at the minimum input voltage:

$$DUTY_{(max)} = \frac{V_{OUT} - V_{IN\_RECTIFIED(min)}}{V_{OUT}}$$

$$V_{IN\_RECTIFIED(min)} = \sqrt{2} \times 85V = 120V$$

$$DUTY_{(max)} = \frac{390V - 120V}{390V} = 0.692$$

Boost Diode

The diode losses are estimated based upon the forward voltage drop, V_F, at 125°C and the reverse recovery charge, Q_{RR}, of the diode. Using a silicone carbide diode, although more expensive, will essentially eliminate the reverse recovery losses:

$$P_{DIODE} = V_{F\_125C} I_{OUT(max)} + 0.5 f_{SW(typ)} V_{OUT} Q_{RR}$$

$$V_{F\_125C} = 1.5V$$

$$Q_{RR} = 0nC$$

$$P_{DIODE} = 1.5V \times 0.897A + 0.5 \times 65kHz \times 390V \times 0nC = 1.35W$$

Switching Element

The conduction losses of the switch are estimated using the $R_{DS(on)}$ of the FET at 125°C , found in the FET data sheet, and the calculated drain to source RMS current, I_{DS_RMS}:

$$P_{COND} = I_{DS\_RMS}^2 R_{DSon(125C)}$$

$$R_{DSon(125C)} = 0.35\Omega$$

$$I_{DS\_RMS} = \frac{P_{OUT(max)}}{V_{IN\_RECTIFIED(min)}} \sqrt{2 - \frac{16 V_{IN\_RECTIFIED(min)}}{3\pi V_{OUT}}}$$

$$I_{DS\_RMS} = \frac{350W}{120V} \sqrt{2 - \frac{16 \times 120V}{3\pi \times 390V}} = 3.54A$$

$$P_{COND} = 3.54A^2 \times 0.35\Omega = 4.38W$$

The switching losses are estimated using the rise time of the gate, t_r, and the output capacitance losses.

For the selected device:

$$t_r = 4.5ns$$

$$C_{OSS} = 780pF$$

$$P_{SW} = f_{SW(typ)}(t_r V_{OUT} I_{IN\_PEAK(max)} + 0.5 C_{OSS} V_{OUT}^2)$$

$$P_{SW} = 65kHz(4.5ns \times 390V \times 6.39A + 0.5 \times 780pF \times 390V^2) = 4.59W$$

Total FET losses:

$$P_{COND} + P_{SW} = 4.38W + 4.59W = 8.97W$$

Sense Resistor

To accommodate the gain of the internal non-linear power limit, R_{SENSE}, is sized such that it will trigger the soft over-current at 25% higher than the maximum peak inductor current using the minimum SOC threshold, V_{SOC}, of ISENSE.

$$R_{SENSE} = \frac{V_{SOC}}{I_{L\_PEAK(max)} \times 1.25}$$

$$R_{SENSE} = \frac{0.66V}{7.03A \times 1.25} = 0.075\Omega$$

Using a parallel combination of available standard value resistors, the sense resistor is chosen.

$$R_{SENSE} = 0.067\Omega$$

The power dissipated across the sense resistor, P_{Rsense}, must be calculated:

$$P_{Rsense} = I^2_{IN\_RMS(\max)} R_{SENSE}$$

$$P_{Rsense} = (4.52A)^2 \times 0.067\Omega = 1.36W$$

The peak current limit, PCL, protection feature will be triggered when current through the sense resistor results in the voltage across R_{SENSE} to be equal to the V_{PCL} threshold. For a worst case analysis, the maximum V_{PCL} threshold is used:

$$I_{PCL} = \frac{V_{PCL}}{R_{SENSE}}$$

$$I_{PCL} = \frac{1.15V}{0.067\Omega} = 17.16A$$

To protect the device from inrush current, a standard 220-Ω resistor, R_{ISENSE}, is placed in series with the ISENSE pin. A 1000-pF capacitor is placed close to the device to improve noise immunity on the ISENSE pin.

Output Capacitor

The output capacitor, C_{OUT}, is sized to meet holdup requirements of the converter. Assuming the downstream converters require the output of the PFC stage to never fall below 300 V, $V_{OUT\_HOLDUP(min)}$, during one line cycle, $t_{HOLDUP} = 1/f_{LINE(min)}$, the minimum calculated value for the capacitor is:

$$C_{OUT(min)} \geq \frac{2P_{OUT}t_{HOLDUP}}{V_{OUT}^2 - V_{OUT\_HOLDUP(min)}^2}$$

$$C_{OUT(min)} \geq \frac{2 \times 350W \times 21.28ms}{390V^2 - 300V^2} \geq 240\mu F$$

It is advisable to de-rate this capacitor value by 20%; the actual capacitor used is 270 µF.

Setting the maximum peak-to-peak output ripple voltage to be less than 5% of the output voltage will ensure that the ripple voltage will not trigger the output over-voltage or output under-voltage protection features of the controller. The maximum peak-to-peak ripple voltage, occurring at twice the line frequency, and the ripple current of the output capacitor are calculated:

$$V_{OUT\_RIPPLE(pp)} < 0.05V_{OUT}$$

$$V_{OUT\_RIPPLE(pp)} < 0.05 \times 390V < 19.5V_{PP}$$

$$V_{OUT\_RIPPLE(pp)} = \frac{I_{OUT}}{\pi(2f_{LINE(min)})C_{OUT}}$$

$$V_{OUT\_RIPPLE(pp)} = \frac{0.9A}{\pi(2 \times 47Hz) \times 270\mu F} = 11.26V$$

The required ripple current rating at twice the line frequency is equal to:

$$I_{Cout\_2fline} = \frac{I_{OUT(max)}}{\sqrt{2}}$$

$$I_{Cout\_2fline} = \frac{0.9A}{\sqrt{2}} = 0.635A$$

There will also be a high frequency ripple current through the output capacitor:

$$I_{Cout\_HF} = I_{OUT(max)}\sqrt{\frac{16V_{OUT}}{3\pi V_{IN\_RECTIFIED(min)}} - 1.5}$$

$$I_{Cout\_HF} = 0.9A\sqrt{\frac{16 \times 390V}{3\pi \times 120V} - 1.5} = 1.8A$$

The total ripple current in the output capacitor is the combination of both and the output capacitor must be selected accordingly:

$$I_{Cout\_RMS(total)} = \sqrt{I_{Cout\_2fline}^2 + I_{Cout\_HF}^2}$$

$$I_{Cout\_RMS(total)} = \sqrt{0.635A^2 + 1.8A^2} = 1.9A$$

Output Voltage Set Point

For low power dissipation and minimal contribution to the voltage set point error, it is recommended to use 1 MΩ for the top voltage feedback divider resistor, R_{FB1}. Multiple resistors in series are used due to the maximum allowable voltage across each. Using the internal 5-V reference, V_{REF}, select the bottom divider resistor, R_{FB2}, to meet the output voltage design goals.

$$R_{FB2} = \frac{V_{REF} R_{FB1}}{V_{OUT} - V_{REF}}$$

$$R_{FB2} = \frac{5V \times 1M\Omega}{390V - 5V} = 13.04k\Omega$$

Using 13 kΩ for R_{FB2} results in a nominal output voltage set point of 391 V.

The over-voltage protection, OVD, will be triggered when the output voltage exceeds 5% of its nominal set-point:

$$V_{OUT(OVP)} = VSENSE_{OVP}\left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}}\right)$$

$$V_{OUT(OVP)} = 5.25V \times \left(\frac{1M\Omega + 13k\Omega}{13k\Omega}\right) = 410.7V$$

The under-voltage detection, UVD, will be triggered when the output voltage falls below 5% of its nominal set-point:

$$V_{OUT(UVD)} = VSENSE_{UVD}\left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}}\right)$$

$$V_{OUT(UVD)} = 4.75V \times \left(\frac{1M\Omega + 13k\Omega}{13k\Omega}\right) = 371.6V$$

A small capacitor on VSENSE must be added to filter out noise that would trigger the enhanced dynamic response in a no-load high-line configuration. Limit the value of the filter capacitor such that the RC time constant is less than 0.1 ms so as not to significantly reduce the control response time to output voltage deviations.

Loop Compensation

The selection of compensation components, for both the current loop and the voltage loop, is made easier by using the UCC28019 Design Calculator spreadsheet that can be found in the Tools section of the UCC28019 product folder on the Texas Instruments website. The current loop is compensated first by determining the product of the internal loop variables, M_1M_2, using the internal controller constants K_1 and K_{FQ}:

$$M_1M_2 = \frac{I_{OUT(max)} V_{OUT}^2 R_{SENSE} K_1}{\eta^2 V_{IN\_RMS}^2 K_{FQ}}$$

$$K_{FQ} = \frac{1}{f_{SW(typ)}}$$

$$K_{FQ} = \frac{1}{65kHz} = 15.385\mu s$$

$$K_1 = 7$$

$$M_1M_2 = \frac{0.9A \times 390V^2 \times 0.067\Omega \times 7}{0.92^2 \times 115V^2 \times 15.385\mu s} = 0.372\frac{V}{\mu s}$$

The VCOMP operating point is found on Figure 29. The Design Calculator spreadsheet enables the user to iteratively select the appropriate VCOMP value.

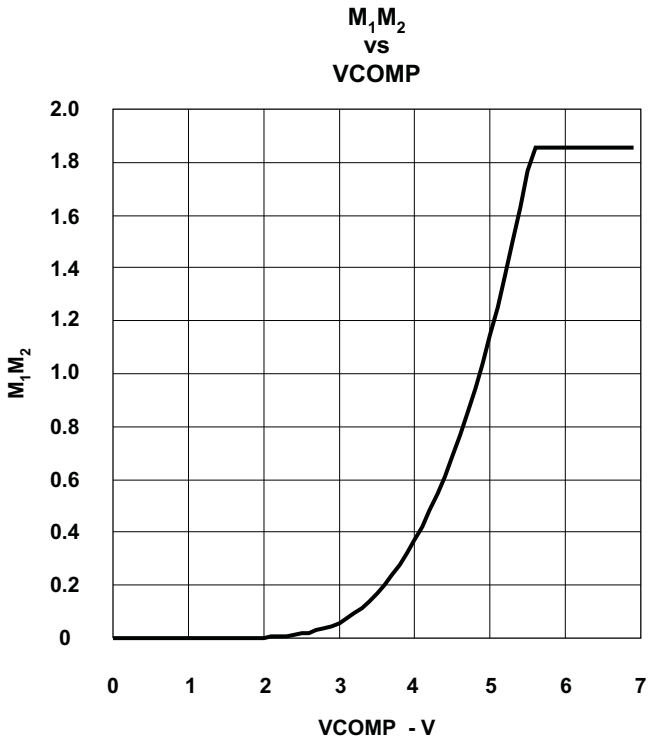


Figure 29. M_1M_2 vs. VCOMP

For the given M_1M_2 of 0.372 V/µs, the VCOMP, approximately equal to 4, as shown in Figure 29.

The individual loop factors, M_1 which is the current loop gain factor, and M_2 which is the voltage loop PWM ramp slope, are calculated using the following conditions:

The M_1 current loop gain factor:

$$if: 0 < VCOMP < 2$$

$$then: M_1 = 0.064$$

$$if: 2 \le VCOMP < 3$$

$$then: M_1 = 0.139 \times VCOMP - 0.214$$

$$if: 3 \le VCOMP < 5.5$$

$$then: M_1 = 0.279 \times VCOMP - 0.632$$

$$if: 5.5 \le VCOMP < 7$$

$$then: M_1 = 0.903$$

$$VCOMP = 4$$

$$M_1 = 0.279 \times 4 - 0.632 = 0.484$$

The M_2 PWM ramp slope:

$$if: 0 < VCOMP < 1.5$$

$$then: M_2 = 0 \frac{V}{\mu s}$$

$$if: 1.5 \le VCOMP < 5.6$$

$$then: M_2 = 0.1223 \times (VCOMP - 1.5)^2 \frac{V}{\mu s}$$

$$if: 5.6 \le VCOMP < 7$$

$$then: M_2 = 2.056 \frac{V}{\mu s}$$

$$VCOMP = 4$$

$$M_2 = 0.1223 \times (4 - 1.5)^2 \frac{V}{\mu s} = 0.764 \frac{V}{\mu s}$$

Verify that the product of the individual gain factors is approximately equal to the M_1M_2 factor determined above, if not, reselect VCOMP and recalculate M_1M_2.

$$M_1 \times M_2 = 0.484 \times 0.764 \frac{V}{\mu s} = 0.37 \frac{V}{\mu s}$$

$$0.37 \frac{V}{\mu s} \cong M_1 M_2 = 0.372 \frac{V}{\mu s}$$

The non-linear gain variable, M_3, can now be calculated:

$$if: 0 < VCOMP < 3$$

$$then: M_3 = 0.0510 \times VCOMP^2 - 0.1543 \times VCOMP - 0.1167$$

$$if: 3 \le VCOMP < 7$$

$$then: M_3 = 0.1026 \times VCOMP^2 - 0.3596 \times VCOMP + 0.3085$$

$$VCOMP = 4$$

$$M_3 = 0.1026 \times 4^2 - 0.3596 \times 4 + 0.3085 = 0.512$$

The frequency of the current averaging pole, f_{IAVG}, is chosen to be at 9.5 kHz. The required capacitor on ICOMP, C_{ICOMP}, for this is determined using the transconductance gain, gmi, of the internal current amplifier:

$$C_{ICOMP} = \frac{gmiM_1}{K_1 2\pi f_{IAVG}}$$

$$C_{ICOMP} = \frac{0.95mS \times 0.484}{7 \times 2 \times \pi \times 9.5kHz} = 1100pF$$

The transfer function of the current loop can be plotted:

$$G_{CL}(f) = \frac{K_1 R_{SENSE} V_{OUT}}{K_{FQ} M_1 M_2 L_{BST}} \times \frac{1}{s(f) + \frac{s(f)^2 K_1 C_{ICOMP}}{gmi M_1}}$$

$$G_{CLdB}(f) = 20 \log\left(\left|G_{CL}(f)\right|\right)$$

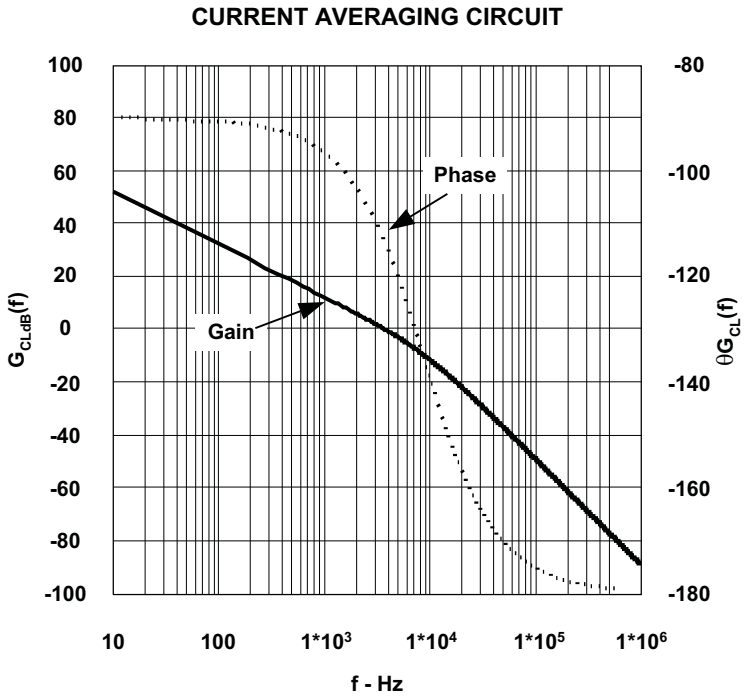


Figure 30. Bode Plot of the Current Averaging Circuit.

The open loop of the voltage transfer function, $G_{VL}(f)$ contains the product of the voltage feedback gain, G_{FB}, and the gain from the pulse width modulator to the power stage, G_{PWM_PS}, which includes the pulse width modulator to power stage pole, f_{PWM_PS}. The plotted result is shown in Figure 31.

$$G_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$

$$G_{FB} = \frac{13k\Omega}{1M\Omega + 13k\Omega} = 0.013$$

$$f_{PWM\_PS} = \frac{1}{2\pi \frac{K_1 R_{SENSE} V_{OUT}^3 C_{OUT}}{K_{FQ} M_1 M_2 V_{IN(typ)}^2}}$$

$$f_{PWM\_PS} = \frac{1}{2\pi \frac{7 \times 0.067\Omega \times 390V^3 \times 270\mu F}{15.385\mu s \times 0.484 \times 0.764 \frac{V}{\mu s} \times 115V^2}} = 1.589Hz$$

$$G_{PWM\_PS}(f) = \frac{\frac{M_3 V_{OUT}}{M_1 M_2 \times 1\mu s}}{1 + \frac{s(f)}{2\pi f_{PWM\_PS}}}$$

$$G_{VL}(f) = G_{FB} G_{PWM\_PS}(f)$$

$$G_{VLdB}(f) = 20 log\left(\left|G_{VL}(f)\right|\right)$$

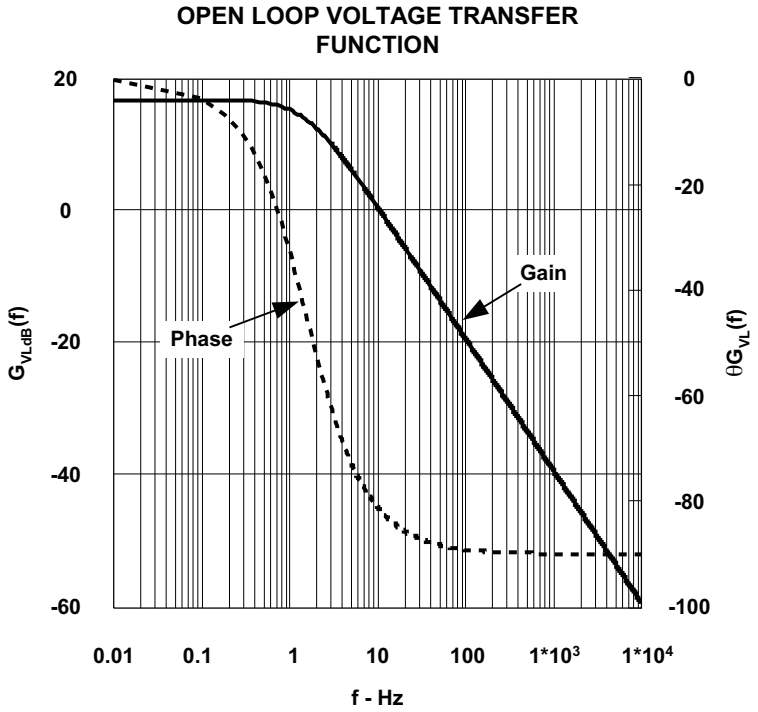


Figure 31. Bode Plot of the Open Loop Voltage Transfer Function

The voltage error amplifier is compensated with a zero, f_{ZERO}, at the f_{PWM_PS} pole and a pole, f_{POLE}, placed at 20 Hz to reject high frequency noise and roll off the gain amplitude. The overall voltage loop crossover, f_V, is desired to be at 10 Hz. The compensation components of the voltage error amplifier are selected accordingly.

$$f_{ZERO} = \frac{1}{2\pi R_{VCOMP} C_{VCOMP}}$$

$$f_{POLE} = \frac{1}{2\pi \frac{R_{VCOMP} C_{VCOMP} C_{VCOMP\_P}}{C_{VCOMP} + C_{VCOMP\_P}}}$$

$$G_{EA}(f) = gmv \left[\frac{1 + s(f) R_{VCOMP} C_{VCOMP}}{\left(C_{VCOMP} + C_{VCOMP\_P}\right) s(f) \left[1 + s(f) \left(\frac{R_{VCOMP} C_{VCOMP} C_{VCOMP\_P}}{C_{VCOMP} + C_{VCOMP\_P}} \right) \right]} \right]$$

$$f_V = 10Hz$$

From Figure 31, and the Design Calculator spreadsheet, the open loop gain of the voltage transfer function at 10 Hz is approximately 0.709 dB. Estimating that the parallel capacitor, C_{VCOMP_P}, is much smaller than the series capacitor, C_{VCOMP}, the unity gain will be at f_V, and the zero will be at f_{PWM_PS}, the series compensation capacitor is determined:

$$C_{VCOMP} = \frac{gmv \frac{f_V}{f_{PWM\_PS}}}{10^{\frac{G_{VLdB}(f)}{20}} \times 2\pi f_V}$$

$$C_{VCOMP} = \frac{42\mu S \times \frac{10Hz}{1.589Hz}}{10^{\frac{0.709\,dB}{20}} \times 2 \times \pi \times 10Hz} = 3.88\mu F$$

A 3.3-µF capacitor is used for C_{VCOMP}.

$$R_{VCOMP} = \frac{1}{2\pi f_{ZERO} C_{VCOMP}}$$

$$R_{VCOMP} = \frac{1}{2 \times \pi \times 1.589Hz \times 3.3\mu F} = 30.36k\Omega$$

A 33-kΩ resistor is used for R_{VCOMP}.

$$C_{VCOMP\_P} = \frac{C_{VCOMP}}{2\pi f_{POLE} R_{VCOMP} C_{VCOMP} - 1}$$

$$C_{VCOMP\_P} = \frac{3.3\mu F}{2 \times \pi \times 20Hz \times 33k\Omega \times 3.3\mu F - 1} = 0.258\mu F$$

A 0.22-µF capacitor is used for C_{VCOMP_P}.

The total closed loop transfer function, G_{VL_total}, contains the combined stages and is plotted in Figure 32.

$$G_{VL\_total}(f) = G_{FB}(f)G_{PWM\_PS}(f)G_{EA}(f)$$

$$G_{VL\_totaldB}(f) = 20\,log\left(\left|G_{VL\_total}(f)\right|\right)$$

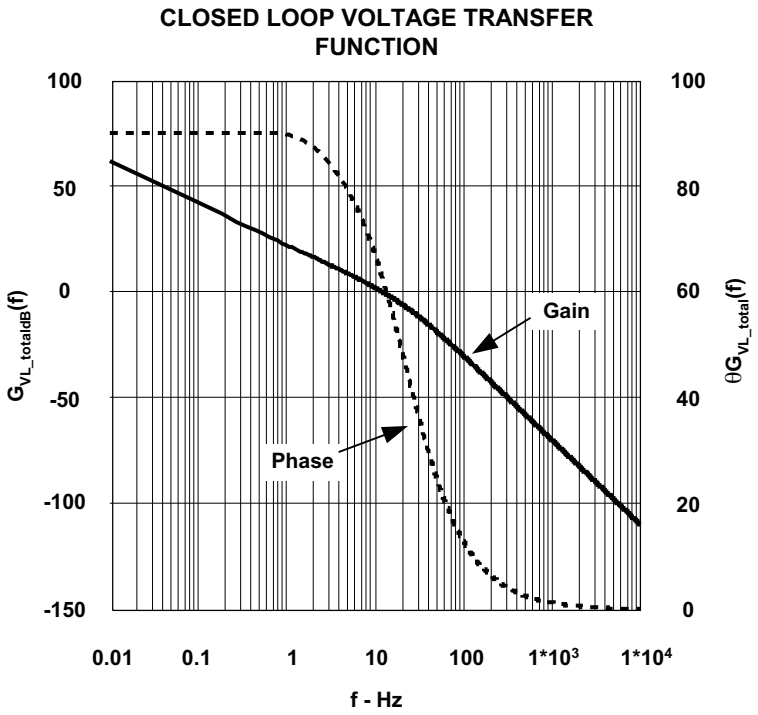


Figure 32. Closed Loop Voltage Bode Plot

Brown Out Protection

Select the top divider resistor into the VINS pin so as not to contribute excessive power loss. The extremely low bias current into VINS means the value of R_{VINS1} could be hundreds of megaohms. For practical purposes, a value less than 10 MΩ is usually chosen. Assuming approximately 150 times the input bias current through the resistor dividers will result in an R_{VINS1} that is less than 10 MΩ , so as to not contribute excessive noise, and still maintain minimal power loss. The brown out protection will turn off the gate drive when the input falls below the user programmable minimum voltage, $V_{AC(off)}$, and turn on when the input rises above $V_{AC(on)}$.

$$I_{VINS} = 150 \times I_{VINS\_0V}$$

$$I_{VINS} = 150 \times 0.1\mu A = 15\mu A$$

$$V_{AC(on)} = 75V$$

$$V_{AC(off)} = 65V$$

$$R_{VINS1} = \frac{\sqrt{2} \times V_{AC(on)} - V_{F\_BRIDGE} - VINS_{ENABLE\_th(max)}}{I_{VINS}}$$

$$R_{VINS1} = \frac{\sqrt{2} \times 75V - 0.95V - 1.6V}{15\mu A} = 6.9M\Omega$$

A 6.5-M resistance is chosen.

$$R_{VINS2} = \frac{VINS_{ENABLE\_th(max)} \times R_{VINS1}}{\sqrt{2} \times V_{AC(on)} - VINS_{ENABLE\_th(max)} - V_{F\_BRIDGE}}$$

$$R_{VINS2} = \frac{1.6V \times 6.5M\Omega}{\sqrt{2} \times 75V - 1.6V - 0.95V} = 100k\Omega$$

The capacitor on VINS, C_{VINS}, is selected so that it's discharge time is greater than the output capacitor hold up time. C_{OUT} was chosen to meet one-cycle hold-up time so C_{VINS} will be chosen to meet 2.5 half-line cycles.

$$t_{CVINS\_dischrg} = \frac{N_{HALF\_CYCLES}}{2 \times f_{LINE(min)}}$$

$$t_{CVINS\_dischrg} = \frac{2.5}{2 \times 47Hz} = 25.6ms$$

$$C_{VINS} = \frac{-t_{CVINS\_dischrg}}{R_{VINS2} \times ln\left[\frac{VINS_{BROWNOUT\_th(min)}}{0.9 \times V_{IN\_RMS(min)} \times \left(\frac{R_{VINS2}}{R_{VINS1} + R_{VINS2}}\right)}\right]}$$

$$C_{VINS} = \frac{-25.6ms}{100k\Omega \times ln\left[\frac{0.76V}{0.9 \times 85V \times \left(\frac{100k\Omega}{6.5M\Omega + 100k\Omega}\right)}\right]} = 0.63\mu F$$

REFERENCES

These references, additional design tools, and links to additional references, including design software and models may be found on the web at http://www.power.ti.com under Technical Documents.

Evaluation Module, 350-W Universal Input, 390-V_{DC} Output PFC Converter, Texas Instruments Literature No. SLUA272

Design Spreadsheet, UCC28019 Design Calculator, Texas Instruments

RELATED PRODUCTS

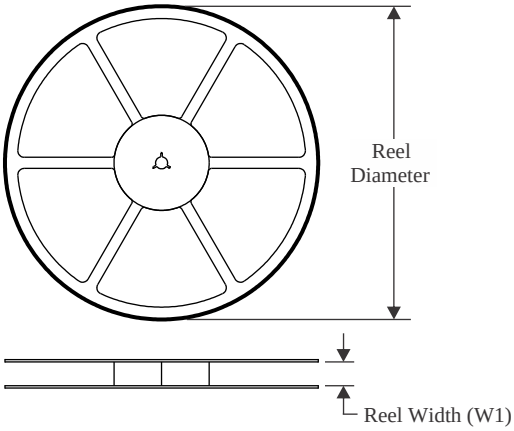
The following parts have characteristics similar to the UCC28019 and may be of interest.

Related Products

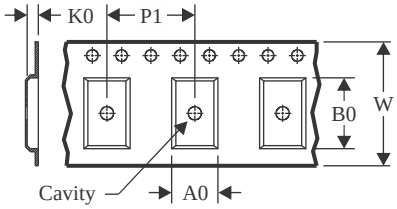
DEVICE	DESCRIPTION
UCC3817/18	Full-Feature PFC Controller
UC2853A	8-Pin CCM PFC Controller

TAPE AND REEL INFORMATION

REEL DIMENSIONS

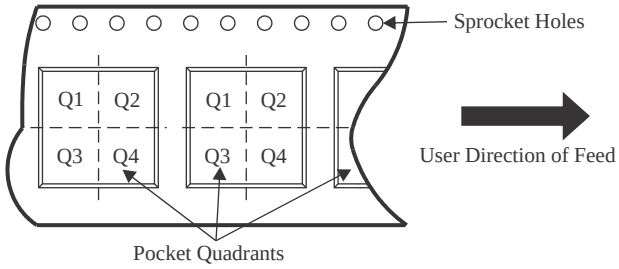


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

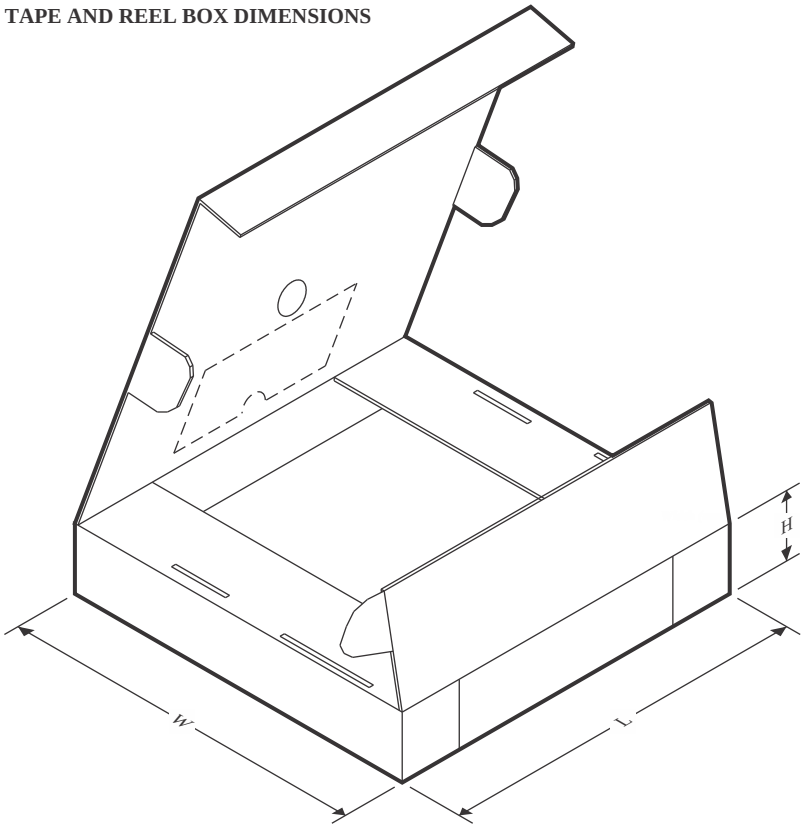
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28019DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

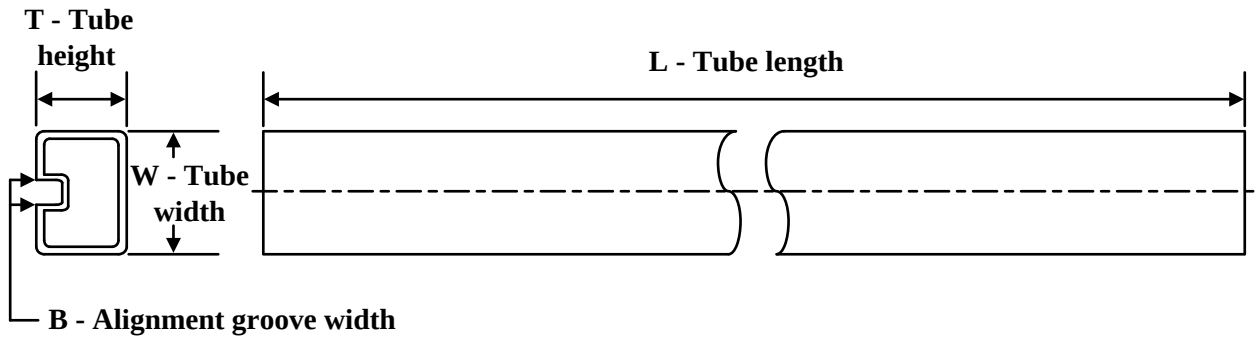
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

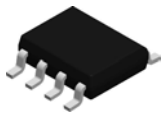
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28019DR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28019D	D	SOIC	8	75	507	8	3940	4.32

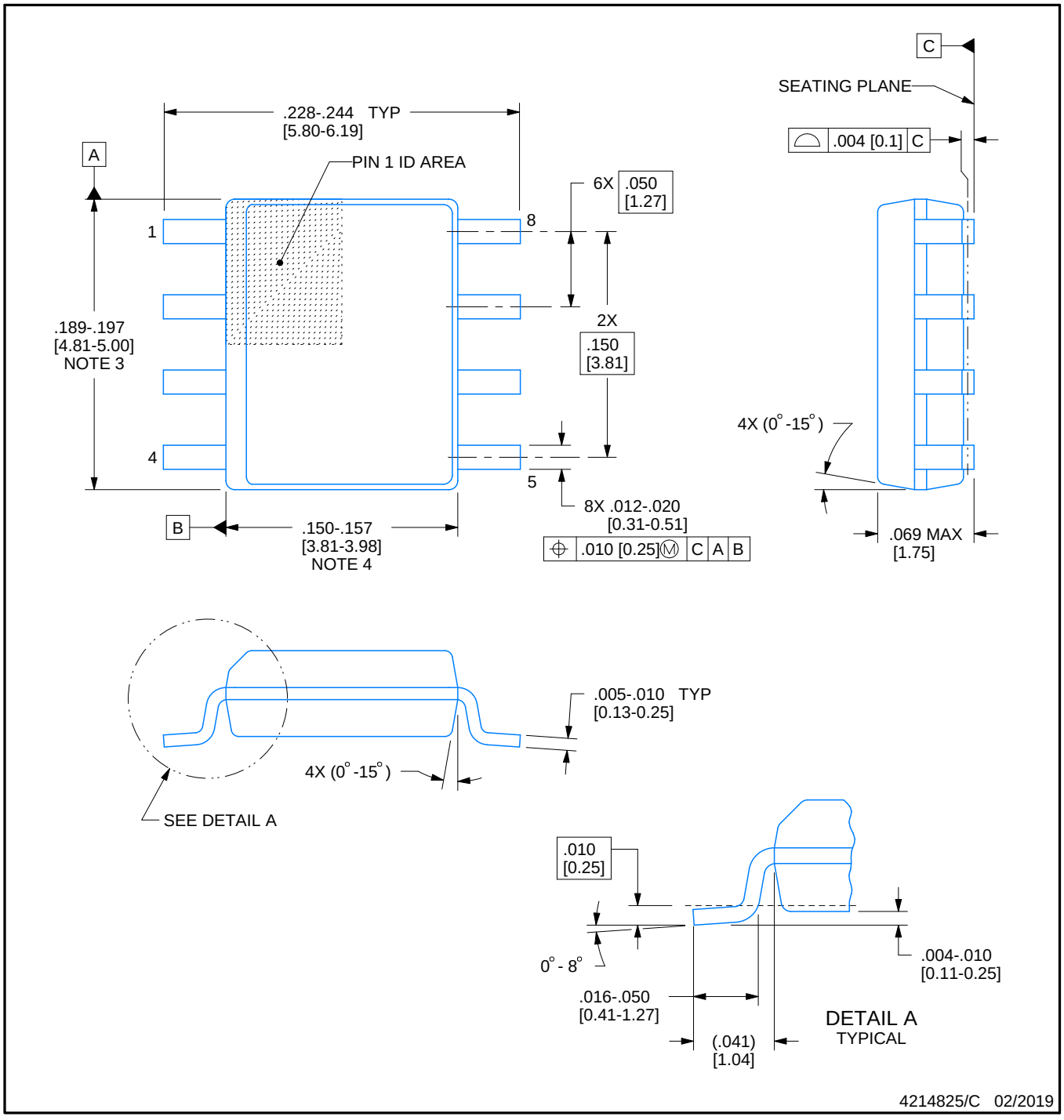


PACKAGE OUTLINE

D0008A

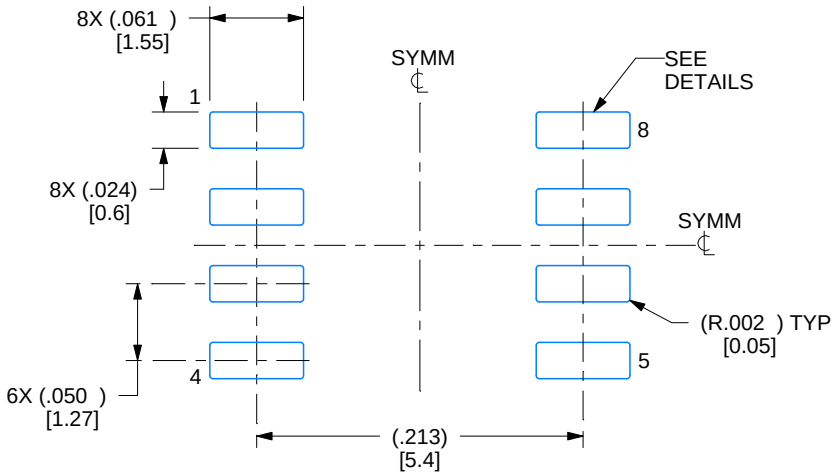
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

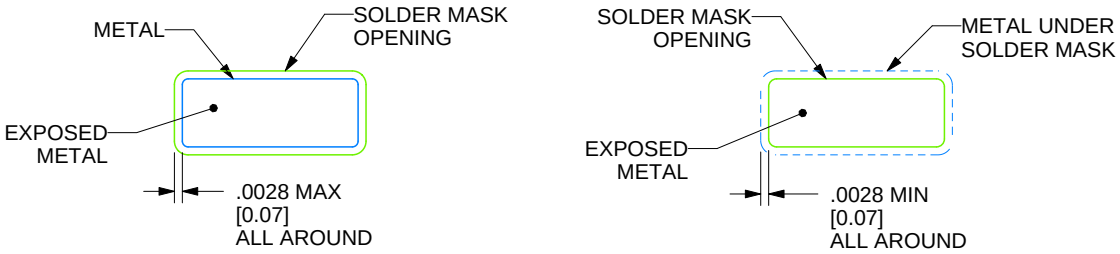


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

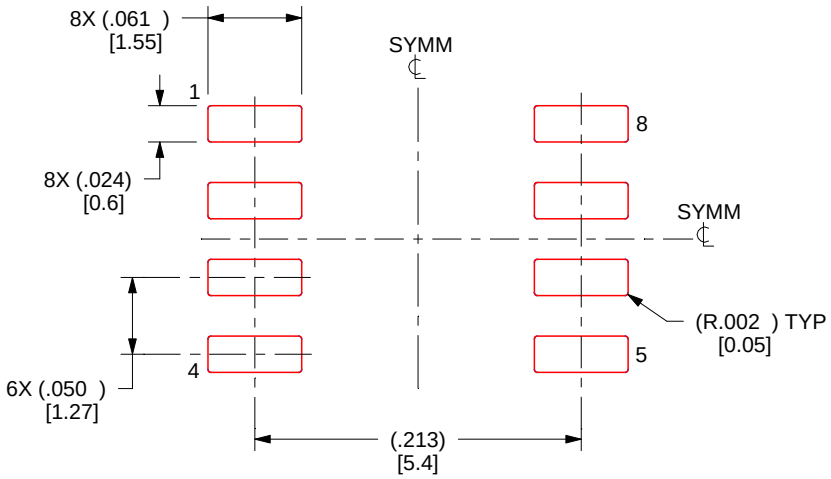
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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