# ADC3908Dx and ADC3908Sx 8-bit, 25 to 125MSPS Low Latency, Low Power, Small, Single and Dual Channel ADC with Integrated Input Buffers

## 1 Features

- Sampling rate up to 125MSPS
- Latency: 1 clock cycle
- Low power (2 channel):
  - 90mW at 125MSPS
  - 56mW at 25MSPS
  - 3mW in PD mode
- Small footprint: 32-VQFN (4mm x 4mm)
- Single or dual channel ADC
- Internal reference
- No missing codes, ±0.25 LSB INL
- Buffered, differential or single ended inputs
- Input bandwidth: 150MHz (3dB)
- Single 1.8V supply
  - Optional 3.3$V_{IO}$ capability
- Industrial temperature range: -40°C to 105°C
- Parallel (SDR, DDR) CMOS interface
- Spectral performance ($FS_{CLK}$ = 125MSPS, $f_{IN}$ = 5 MHz):
  - SNR: 49.8dBFS
  - SFDR: 60dBFS

## 2 Applications

- Low latency control loops
- Laser scanners
- Displacement sensors
- Detection equipment

## 3 Description

The ADC3908Dx and ADC3908Sx are a family of ultra-low power 8-bit 125MSPS high-speed dual and single channel analog-to-digital converters. High-speed control loops benefit from the short latency of only 1 clock cycle. The ADC consumes only 90mW at 125MSPS with a power consumption that scales with lower sampling rates.

The ADC3908Dx and ADC3908Sx uses parallel DDR or SDR CMOS interface to output the data, and can be driven at +1.8V or +3.3V to accommodate various receiver requirements. The analog input and output interface can be easily configured via pin control (Interface Configuration Table). The device is a pin-to-pin compatible family of ADCs with 8 and 10-bit resolution and different speed grades. The device is available in a 32-pin VQFN package, and supports industrial temperature range from -40 to +105°C.

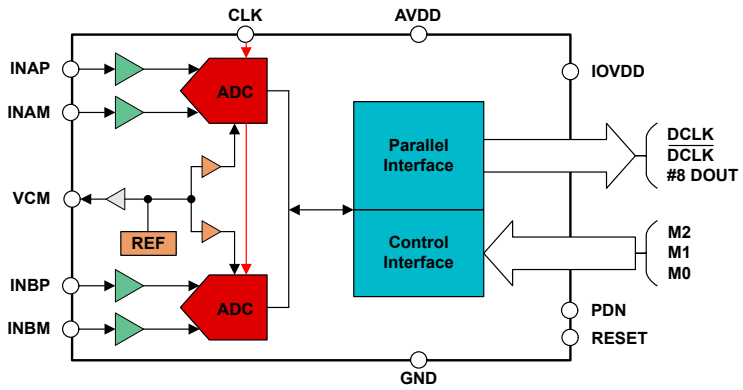
**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| ADC3908D025, 'D065, 'D125 ADC3908S025,'S065, 'S125 | VQFN (32) | 4mm × 4mm |

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

**Device Information**

| PART NUMBER (c= #CH; sss= MSPS) | RESOLUTION | SAMPLING RATE MSPS |
|---|---|---|
| ADC3910csss | 10-Bit | 25, 65, 125 |
| ADC3908csss | 8-Bit | 25, 65, 125 |




**Block Diagram**

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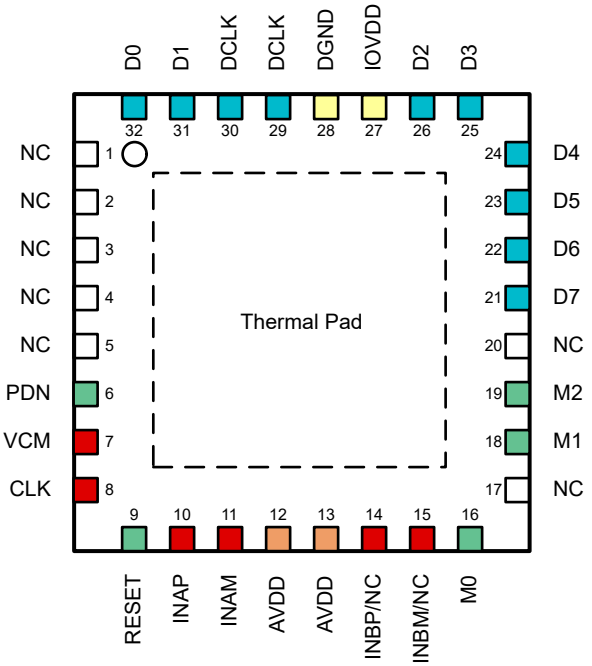
## 4 Device Comparison

**Table 4-1. Device Comparison Table**

| Device | Resolution (Bits) | Channels | Sample Rate (MSPS) | Control Interface | Digital Features |
|---|---|---|---|---|---|
| ADC3910D125 | 10 | 2 | 125 | SPI Control | Full Features |
| ADC3910S125 | 10 | 1 | 125 | SPI Control | Full Features |
| ADC3910D065 | 10 | 2 | 65 | SPI Control | Full Features |
| ADC3910S065 | 10 | 1 | 65 | SPI Control | Full Features |
| ADC3910D025 | 10 | 2 | 25 | SPI Control | Full Features |
| ADC3910S025 | 10 | 1 | 25 | SPI Control | Full Features |
| ADC3908D125 | 8 | 2 | 125 | Pin Control | Not available |
| ADC3908S125 | 8 | 1 | 125 | Pin Control | Not available |
| ADC3908D065 | 8 | 2 | 65 | Pin Control | Not available |
| ADC3908S065 | 8 | 1 | 65 | Pin Control | Not available |
| ADC3908D025 | 8 | 2 | 25 | Pin Control | Not available |
| ADC3908S025 | 8 | 1 | 25 | Pin Control | Not available |

# 5 Pin Configuration and Functions




A. AGND is soldered to the thermal pad

**Figure 5-1. RSM (VQFN) Package, 32-Pin (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **INPUT or REFERENCE** | | | |
| INAP | 10 | I | Positive analog input, channel A |
| INAM | 11 | I | Negative analog input, channel A |
| INBP/NC | 14 | I | Positive analog input, channel B (NC on single channel device) |
| INBM/NC | 15 | I | Negative analog input, channel B (NC on single channel device) |
| VCM | 7 | O | Common-mode voltage output for the analog inputs, 1.25 V |
| **CLOCK** | | | |
| CLK | 8 | I | Sampling clock input for the ADC |
| **CONFIGURATION** | | | |
| RESET | 9 | I | Hardware reset. Active high. This pin has an internal 60 kΩ pull-down resistor. |
| M0 | 16 | I | Default, internal 40 kΩ pull-down resistor.<br>Tie to GND for dual channel devices or AVDD for single channel devices.<br>This pin is used to configure default operating conditions. Interface configuration table |
| M1 | 18 | I | Default, internal 40 kΩ pull-down resistor.<br>This pin is used to configure default operating conditions. Interface configuration table |
| M2 | 19 | I | Default, internal 40 kΩ pull-down resistor.<br>This pin is used to configure default operating conditions. Interface configuration table |
| **DIGITAL INTERFACE** | | | |

**Table 5-1. Pin Functions (continued)**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| D0 | 32 | O | Parallel CMOS digital lane output data. |
| D1 | 31 | O | |
| D2 | 26 | O | |
| D3 | 25 | O | |
| D4 | 24 | O | |
| D5 | 23 | O | |
| D6 | 22 | O | |
| D7 | 21 | O | |
| DCLK | 30 | O | CMOS output for data bit clock. |
| $\overline{\text{DCLK}}$ | 29 | O | Inverse data bit clock for CMOS output data. |
| PDN | 6 | I | Default, pin has 60 kΩ pull-down. When PDN is pulled high device is put in a powerdown state. |
| **POWER SUPPLY** | | | |
| AVDD | 12, 13 | I | Analog 1.8 V power supply |
| GND | PowerPAD™ | I | Analog Ground, 0 V |
| IOVDD | 27 | I | 1.8 V power supply for digital interface |
| DGND | 5, 28 | I | Ground, 0 V for digital interface |
| **OTHER** | | | |
| NC | 1, 2, 3, 4, 5, 17, 20 | - | No connection. Connect to ground. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range 1.8 V, AVDD | | –0.3 | 2.1 | V |
| Supply voltage range 1.8 V to 3.3 V, IOVDD | | –0.3 | 3.6 | |
| Supply voltage range, GND, DGND | | –0.3 | 0.3 | |
| Voltage applied to input pins | INAP/M, INBP/M, CLK | –0.3 | 2.1 | |
| | RESET, PDN, M0 , M1, M2 | –0.3 | 2.1 | |
| Junction temperature, $T_J$ | | | 125 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | 1000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2) | 500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage range | Supply voltage range 1.8v | AVDD(1) | 1.7 | 1.8 | 1.9 | V |
| Supply voltage range | | IOVDD(1) | 1.7 | 1.8 | 1.9 | V |
| Supply voltage range | Supply voltage range 3.3v | IOVDD(1) | 3.2 | 3.3 | 3.4 | V |
| $T_A$ | Operating free-air temperature | | –40 | | 105 | °C |
| $T_J$ | Operating junction temperature | | | | 115(2) | °C |

(1) Measured to GND.
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | ADC39xx RSM (QFN) 32 Pins | UNIT |
|---|---|---|---|
| $R_{\Theta JA}$ | Junction-to-ambient thermal resistance | 38.1 | °C/W |
| $R_{\Theta JC(top)}$ | Junction-to-case (top) thermal resistance | 37.2 | °C/W |
| $R_{\Theta JB}$ | Junction-to-board thermal resistance | 17.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 17.9 | °C/W |
| $R_{\Theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 7.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics - Power Consumption

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at TA = 25°C, AVDD = IOVDD = 1.8 V, $F_{IN}$ = 5MHz, $A_{IN}$ = -1dBFS, Internal 1.2 V reference, 5 pF output load, and 50% clock duty cycle, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ADC3908D025** | | | | | | |
| $I_{AVDD}$ | Analog supply current | $F_s$ = 25MSPS, dual channel, DDR CMOS | | 28 | 31 | mA |
| $I_{IOVDD}$ | Digital supply current | | | 3 | 9 | mA |
| $P_{DIS}$ | Power dissipation | | | 56 | | mW |
| **ADC3908S025** | | | | | | |
| $I_{AVDD}$ | Analog supply current | $F_s$ = 25MSPS, single channel, SDR CMOS | | 19 | 22 | mA |
| $I_{IOVDD}$ | Digital supply current | | | 3 | 8 | mA |
| $P_{DIS}$ | Power dissipation | | | 40 | | mW |
| **ADC3908D065** | | | | | | |
| $I_{AVDD}$ | Analog supply current | $F_s$ = 65MSPS, dual channel, DDR CMOS | | 32 | 34 | mA |
| $I_{IOVDD}$ | Digital supply current | | | 7 | 14 | mA |
| $P_{DIS}$ | Power dissipation | | | 70 | | mW |
| **ADC3908S065** | | | | | | |
| $I_{AVDD}$ | Analog supply current | $F_s$ = 65MSPS, single channel, SDR CMOS | | 21 | 24 | mA |
| $I_{IOVDD}$ | Digital supply current | | | 6 | 13 | mA |
| $P_{DIS}$ | Power dissipation | | | 49 | | mW |
| **ADC3908D125** | | | | | | |
| $I_{AVDD}$ | Analog supply current | $F_s$ = 125MSPS, dual channel, DDR CMOS | | 38 | 40 | mA |
| $I_{IOVDD}$ | Digital supply current | | | 12 | 21 | mA |
| $P_{DIS}$ | Power dissipation | | | 90 | | mW |
| **ADC3908S125** | | | | | | |
| $I_{AVDD}$ | Analog supply current | $F_s$ = 125MSPS, single channel, SDR CMOS | | 24 | 27 | mA |
| $I_{IOVDD}$ | Digital supply current | | | 10 | 18 | mA |
| $P_{DIS}$ | Power dissipation | | | 61 | | mW |
| **Power down** | | | | | | |
| $P_{DIS}$ | Power consumption in power down | | | 3 | | mW |

## 6.6 Electrical Characteristics - DC Specifications

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, Internal 1.2 V reference, and –1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC ACCURACY (25 MSPS)** | | | | | | |
| No missing codes | | | 8 | | | bits |
| DNL | Differential nonlinearity | | -0.35 | ±0.15 | +0.35 | LSB |
| INL | Integral nonlinearity | | -0.6 | ±0.25 | +0.6 | LSB |
| $V_{OS\_ERR}$ | Offset error | | -2.75 | ±1 | +2.75 | LSB |
| $V_{OS\_DRIFT}$ | Offset drift over temperature | | | 0.001 | | LSB/ºC |
| $GAIN_{ERR}$ | Gain error | Internal Reference | | ±0.8 | | %FSR |
| $GAIN_{DRIFT}$ | Gain drift over temperature | Internal Reference | | -102 | | ppm/ºC |
| **DC ACCURACY (65 MSPS)** | | | | | | |
| No missing codes | | | 8 | | | bits |

## 6.6 Electrical Characteristics - DC Specifications (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, Internal 1.2 V reference, and –1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| DNL | Differential nonlinearity | | -0.35 | ±0.15 | +0.35 | LSB |
| INL | Integral nonlinearity | | -0.6 | ±0.25 | +0.6 | LSB |
| $V_{OS\_ERR}$ | Offset error | | -2.75 | ±1 | -2.75 | LSB |
| $V_{OS\_DRIFT}$ | Offset drift over temperature | | | 0.001 | | LSB/ºC |
| $GAIN_{ERR}$ | Gain error | Internal Reference | | ±0.8 | | %FSR |
| $GAIN_{DRIFT}$ | Gain drift over temperature | Internal Reference | | -102 | | ppm/ºC |
| **DC ACCURACY (125 MSPS)** | | | | | | |
| No missing codes | | | 8 | | | bits |
| DNL | Differential nonlinearity | | -0.35 | ±0.15 | +0.35 | LSB |
| INL | Integral nonlinearity | | -0.6 | ±0.25 | +0.6 | LSB |
| $V_{OS\_ERR}$ | Offset error | | -2.75 | ±1 | 2.75 | LSB |
| $V_{OS\_DRIFT}$ | Offset drift over temperature | | | 0.001 | | LSB/ºC |
| $GAIN_{ERR}$ | Gain error | Internal Reference | | ±0.8 | | %FSR |
| $GAIN_{DRIFT}$ | Gain drift over temperature | Internal Reference | | -102 | | ppm/ºC |
| **ADC ANALOG INPUT (INAP/M, INBP/M)** | | | | | | |
| FS | Input full scale | Differential | | 1.9 | | Vpp |
| | | Single-ended | | 0.95 | | Vpp |
| $C_{IN}$ | Differential input Capacitance | $F_{IN}$ = 100 kHz | | 7 | | pF |
| $V_{CM}$ | Input common mode voltage | | $V_{OCM}$ - 50mV | 1.275 | $V_{OCM}$ + 50mV | V |
| $V_{OCM}$ | Output common mode voltage | | | 1.25 | | V |
| BW | Analog Input Bandwidth (-3dB) | | | 150 | | MHz |
| **CLOCK INPUT** | | | | | | |
| Input clock frequency | | ADC3908D125, ADC3908S125 | 5 | | 125 | MHz |
| | | ADC3908D065, ADC3908S065 | 5 | | 65 | MHz |
| | | ADC3908D025, ADC3908S025 | 5 | | 25 | MHz |
| $V_{IH}$ | High level input voltage | | AVDD - 0.3 | 1.8 | | Vpp |
| $V_{IL}$ | Low level input voltage | | | 0 | AVSS + 0.3 | V |
| $C_{IN}$ | Input capacitance | | | 0.5 | | pF |
| Clock duty cycle | | | 45 | 50 | 55 | % |
| **DIGITAL INPUTS (RESET, PDN, M0, M1, M2)** | | | | | | |
| $V_{IH}$ | High level input voltage | | 1.4 | | | V |
| $V_{IL}$ | Low level input voltage | | | | 0.4 | V |
| $I_{IH}$ | High level input current | | | 90 | 150 | uA |
| $I_{IL}$ | Low level input current | | -150 | -90 | | uA |
| $C_I$ | Input capacitance | | | 1.5 | | pF |
| **DIGITAL CMOS OUTPUTS (D0:D07)** | | | | | | |
| Output data rate | | per CMOS output pin | | | 250 | Mbps |
| $V_{OH}$ | High level output voltage | $I_{LOAD}$ = -400 uA | IOVDD - 0.1 | IOVDD | | V |
| $V_{OL}$ | Low level output voltage | $I_{LOAD}$ = 400 uA | | | 0.1 | V |

## 6.7 Electrical Characteristics - AC Specifications (25 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, AVDD = IOVDD = 1.8 V, $FS_{CLK}$ = 25 MSPS, $F_{IN}$ = 5MHz, $A_{IN}$ = -1dBFS, Internal 1.2 V reference , and 50% clock duty cycle, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| NSD | Noise Spectral Density | $f_{IN}$ = 10 MHz, $A_{IN}$ = -20 dBFS | | -120.8 | | dBFS/Hz |
| SNR | Signal to noise ratio, excluding DC, HD2 to HD5 | $f_{IN}$ = 1.1 MHz | | 49.9 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 48 | 49.9 | | |
| | | $f_{IN}$ = 10 MHz | | 49.9 | | |
| | | $f_{IN}$ = 20 MHz | | 49.9 | | |
| SINAD | Signal to noise and distortion ratio, excluding DC offset | $f_{IN}$ = 1.1 MHz | | 49.6 | | dBFS |
| | | $f_{IN}$ = 5 MHz | | 49.7 | | |
| | | $f_{IN}$ = 10 MHz | | 49.7 | | |
| | | $f_{IN}$ = 20 MHz | | 49.7 | | |
| ENOB | Effective number of bits, excluding DC offset | $f_{IN}$ = 1.1 MHz | | 8.0 | | Bit |
| | | $f_{IN}$ = 5 MHz | | 8.0 | | |
| | | $f_{IN}$ = 10 MHz | | 8.0 | | |
| | | $f_{IN}$ = 20 MHz | | 8.0 | | |
| THD | Total Harmonic Distortion (First five harmonics) | $f_{IN}$ = 1.1 MHz | | -61 | | dBc |
| | | $f_{IN}$ = 5 MHz | | -63 | | |
| | | $f_{IN}$ = 10 MHz | | -63 | | |
| | | $f_{IN}$ = 20 MHz | | -64 | | |
| SFDR | Spur free dynamic range including second and third harmonic | $f_{IN}$ = 1.1 MHz | | 63 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 60 | 65 | | |
| | | $f_{IN}$ = 10 MHz | | 64 | | |
| | | $f_{IN}$ = 20 MHz | | 64 | | |
| SPUR | Spur free dynamic range (excluding DC, HD2, HD3) | $f_{IN}$ = 1.1 MHz | | 67 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 63 | 68 | | |
| | | $f_{IN}$ = 10 MHz | | 68 | | |
| | | $f_{IN}$ = 20 MHz | | 68 | | |
| IMD3 | Two tone inter-modulation distortion | $f_{IN}$ = 8/10 MHz, $A_{IN}$ = -7 dBFS/tone | | -91 | | dBc |
| XTALK | Channel-to-channel crosstalk | Aggressor = 1.1 MHz | | 107 | | dBFS |
| | | Aggressor = 10 MHz | | 97 | | |
| | | Aggressor = 20 MHz | | 93 | | |

## 6.8 Electrical Characteristics - AC Specifications (65 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, AVDD = IOVDD = 1.8 V, $FS_{CLK}$ = 65 MSPS, $F_{IN}$ = 5MHz, $A_{IN}$ = -1dBFS, Internal 1.2 V reference , and 50% clock duty cycle, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| NSD | Noise Spectral Density | $f_{IN}$ = 10 MHz, $A_{IN}$ = -20 dBFS | | -125.0 | | dBFS/Hz |
| SNR | Signal to noise ratio, excluding DC, HD2 to HD5 | $f_{IN}$ = 1.1 MHz | | 49.8 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 47 | 49.8 | | |
| | | $f_{IN}$ = 10 MHz | | 49.8 | | |
| | | $f_{IN}$ = 20 MHz | | 49.8 | | |
| | | $f_{IN}$ = 40 MHz | | 49.8 | | |
| | | $f_{IN}$ = 70 MHz | | 49.8 | | |
| SINAD | Signal to noise and distortion ratio, excluding DC offset | $f_{IN}$ = 1.1 MHz | | 49.6 | | dBFS |
| | | $f_{IN}$ = 5 MHz | | 49.7 | | |
| | | $f_{IN}$ = 10 MHz | | 49.7 | | |
| | | $f_{IN}$ = 20 MHz | | 49.7 | | |
| | | $f_{IN}$ = 40 MHz | | 49.6 | | |
| | | $f_{IN}$ = 70 MHz | | 49.6 | | |
| ENOB | Effective number of bits, excluding DC offset | $f_{IN}$ = 1.1 MHz | | 8.0 | | Bit |
| | | $f_{IN}$ = 5 MHz | | 8.0 | | |
| | | $f_{IN}$ = 10 MHz | | 8.0 | | |
| | | $f_{IN}$ = 20 MHz | | 8.0 | | |
| | | $f_{IN}$ = 40 MHz | | 8.0 | | |
| | | $f_{IN}$ = 70 MHz | | 8.0 | | |
| THD | Total Harmonic Distortion (First five harmonics) | $f_{IN}$ = 1.1 MHz | | -61 | | dBc |
| | | $f_{IN}$ = 5 MHz | | -63 | | |
| | | $f_{IN}$ = 10 MHz | | -63 | | |
| | | $f_{IN}$ = 20 MHz | | -64 | | |
| | | $f_{IN}$ = 40 MHz | | -62 | | |
| | | $f_{IN}$ = 70 MHz | | -61 | | |
| SFDR | Spur free dynamic range including second and third harmonic | $f_{IN}$ = 1.1 MHz | | 62 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 60 | 64 | | |
| | | $f_{IN}$ = 10 MHz | | 64 | | |
| | | $f_{IN}$ = 20 MHz | | 65 | | |
| | | $f_{IN}$ = 40 MHz | | 63 | | |
| | | $f_{IN}$ = 70 MHz | | 62 | | |
| SPUR | Spur free dynamic range (excluding DC, HD2, HD3) | $f_{IN}$ = 1.1 MHz | | 68 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 61 | 68 | | |
| | | $f_{IN}$ = 10 MHz | | 68 | | |
| | | $f_{IN}$ = 20 MHz | | 68 | | |
| | | $f_{IN}$ = 40 MHz | | 68 | | |
| | | $f_{IN}$ = 70 MHz | | 68 | | |
| IMD3 | Two tone inter-modulation distortion | $f_{IN}$ = 8/10 MHz, $A_{IN}$ = -7 dBFS/tone | | -91 | | dBc |
| XTALK | Channel-to-channel crosstalk | Aggressor = 1.1 MHz | | 106 | | dBFS |
| | | Aggressor = 10 MHz | | 102 | | |
| | | Aggressor = 20 MHz | | 97 | | |

## 6.9 Electrical Characteristics - AC Specifications (125 MSPS)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, AVDD = IOVDD = 1.8 V, $FS_{CLK}$ = 125 MSPS, $F_{IN}$ = 5MHz, $A_{IN}$ = -1dBFS, Internal 1.2 V reference , and 50% clock duty cycle, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| NSD | Noise Spectral Density | $f_{IN}$ = 10 MHz, $A_{IN}$ = -20 dBFS | | -127.8 | | dBFS/Hz |
| SNR | Signal to noise ratio, excluding DC, HD2 to HD5 | $f_{IN}$ = 1.1 MHz | | 49.8 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 48 | 49.8 | | |
| | | $f_{IN}$ = 10 MHz | | 49.8 | | |
| | | $f_{IN}$ = 20 MHz | | 49.8 | | |
| | | $f_{IN}$ = 40 MHz | | 49.8 | | |
| | | $f_{IN}$ = 70 MHz | | 49.8 | | |
| SINAD | Signal to noise and distortion ratio, excluding DC offset | $f_{IN}$ = 1.1 MHz | | 49.6 | | dBFS |
| | | $f_{IN}$ = 5 MHz | | 49.5 | | |
| | | $f_{IN}$ = 10 MHz | | 49.5 | | |
| | | $f_{IN}$ = 20 MHz | | 49.6 | | |
| | | $f_{IN}$ = 40 MHz | | 49.7 | | |
| | | $f_{IN}$ = 70 MHz | | 49.4 | | |
| ENOB | Effective number of bits, excluding DC offset | $f_{IN}$ = 1.1 MHz | | 8.0 | | Bit |
| | | $f_{IN}$ = 5 MHz | | 8.0 | | |
| | | $f_{IN}$ = 10 MHz | | 8.0 | | |
| | | $f_{IN}$ = 20 MHz | | 8.0 | | |
| | | $f_{IN}$ = 40 MHz | | 8.0 | | |
| | | $f_{IN}$ = 70 MHz | | 8.0 | | |
| THD | Total Harmonic Distortion (First five harmonics) | $f_{IN}$ = 1.1 MHz | | -61 | | dBc |
| | | $f_{IN}$ = 5 MHz | | -59 | | |
| | | $f_{IN}$ = 10 MHz | | -60 | | |
| | | $f_{IN}$ = 20 MHz | | -61 | | |
| | | $f_{IN}$ = 40 MHz | | -64 | | |
| | | $f_{IN}$ = 70 MHz | | -59 | | |
| SFDR | Spur free dynamic range including second and third harmonic | $f_{IN}$ = 1.1 MHz | | 62 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 56 | 60 | | |
| | | $f_{IN}$ = 10 MHz | | 61 | | |
| | | $f_{IN}$ = 20 MHz | | 63 | | |
| | | $f_{IN}$ = 40 MHz | | 65 | | |
| | | $f_{IN}$ = 70 MHz | | 60 | | |
| SPUR | Spur free dynamic range (excluding DC, HD2, HD3) | $f_{IN}$ = 1.1 MHz | | 68 | | dBFS |
| | | $f_{IN}$ = 5 MHz | 61 | 68 | | |
| | | $f_{IN}$ = 10 MHz | | 68 | | |
| | | $f_{IN}$ = 20 MHz | | 68 | | |
| | | $f_{IN}$ = 40 MHz | | 68 | | |
| | | $f_{IN}$ = 70 MHz | | 68 | | |
| IMD3 | Two tone inter-modulation distortion | $f_{IN}$ = 8/10 MHz, $A_{IN}$ = -7 dBFS/tone | | -86 | | dBc |
| XTALK | Channel-to-channel crosstalk | Aggressor = 1.1 MHz | | 102 | | dBFS |
| | | Aggressor = 10 MHz | | 90 | | |
| | | Aggressor = 20 MHz | | 98 | | |

## 6.10 Timing Requirements

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8 V, Internal 1.2 V reference, 5 pF output load, and –1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ADC TIMING SPECIFICATIONS** | | | | | | |
| $t_{AD}$ | Aperture Delay | | | 0.5 | | ns |
| $t_A$ | Aperture Jitter | square wave clock with fast edges | | 250 | | fs |
| $t_{ACQ}$ | Signal acquisition period, referenced to sampling clock falling edge | | | $-T_S/5$ | | Sampling Clock Period |
| $t_{CONV}$ | Signal conversion period, referenced to sampling clock falling edge | Fs = 25 MSPS | | 5.5 | | ns |
| | | Fs = 65 MSPS | | 5.5 | | ns |
| | | Fs = 125 MSPS | | 5.5 | | ns |
| Wake up time | Time to valid data after coming out of power down. Internal reference. | | | 30 | | us |
| ADC Latency | Signal input to data output | DDR | | 1 | | ADC clock cycles |
| | | SDR | | 1 | | |
| **INTERFACE TIMING - DDR CMOS** | | | | | | |
| $t_{PD}$ | Propagation delay: sampling clock falling edge to DCLK rising edge | | | $T_S/4 + 3$ | | ns |
| $t_{DE}$ | DCLK edge to previous data transition | Fs = 25 MSPS | | -10 | -9 | ns |
| | | Fs = 65 MSPS | | -3.8 | -3.4 | |
| | | Fs = 125 MSPS | | -2 | -1.8 | |
| $t_{DL}$ | DCLK edge to next data transition | Fs = 25 MSPS | 9 | 10 | | |
| | | Fs = 65 MSPS | 3.4 | 3.8 | | |
| | | Fs = 125 MSPS | 1.8 | 2 | | |
| **INTERFACE TIMING - SDR CMOS** | | | | | | |
| $t_{PD}$ | Propagation delay: sampling clock falling edge to DCLK rising edge | | | $T_S/4 + 3$ | | ns |
| $t_{DE}$ | DCLK edge to previous data transition | Fs = 25 MSPS | | -20 | -18 | ns |
| | | Fs = 65 MSPS | | -7.6 | -6.9 | |
| | | Fs = 125 MSPS | | -4 | -3.6 | |
| $t_{DV}$ | DCLK edge to next data transition | Fs = 25 MSPS | 18 | 20 | | |
| | | Fs = 65 MSPS | 6.9 | 7.7 | | |
| | | Fs = 125 MSPS | 3.6 | 4 | | |

## 6.11 Output Interface Timing Diagram

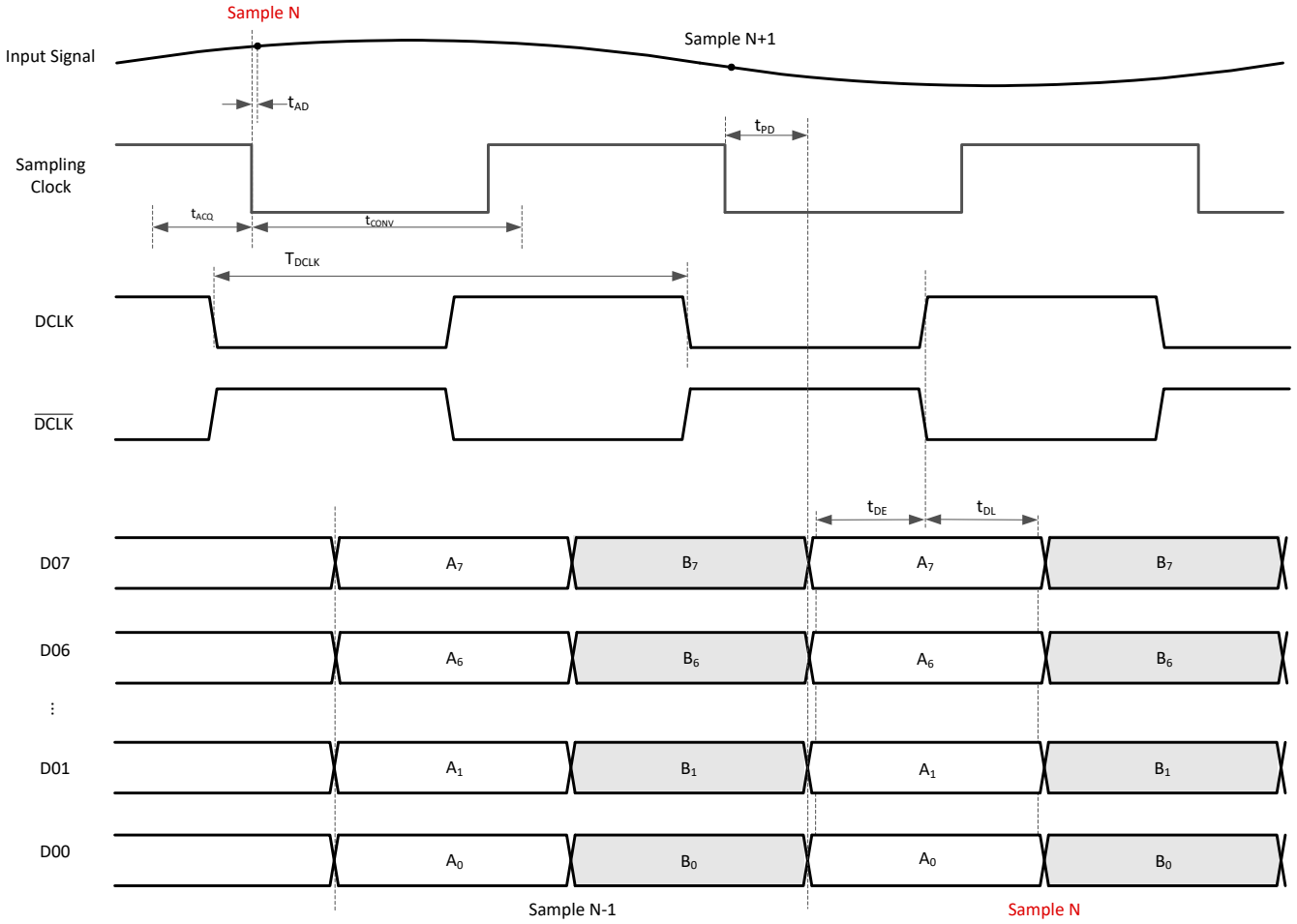



**Figure 6-1. Timing Diagram: Dual CH, DDR (Default: 8 Lanes)**

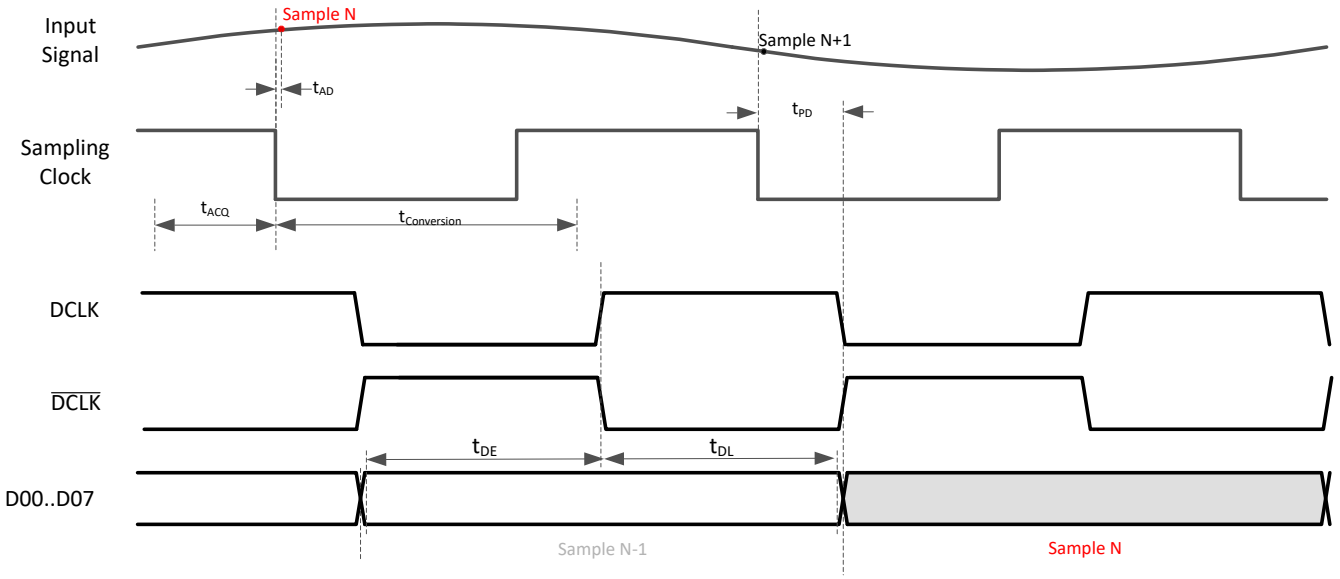
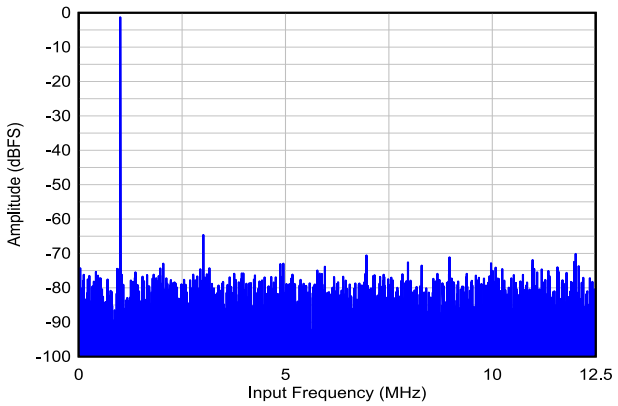



**Figure 6-2. Timing Diagram: Single CH (CHA), SDR (Default: 8 Lanes)**

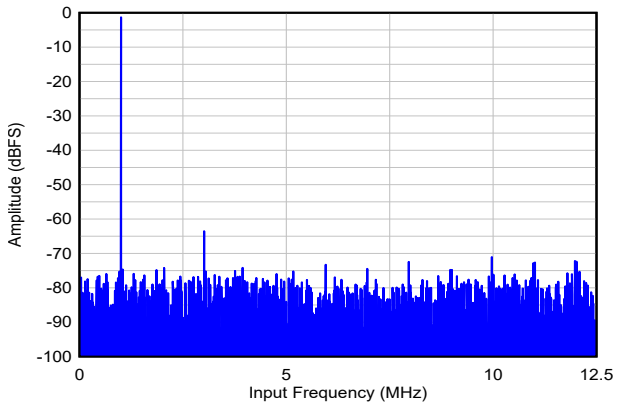
## 6.12 Typical Characteristics: 25MSPS

Typical values at $T_A$ = 25°C, ADC sampling rate = 25MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.



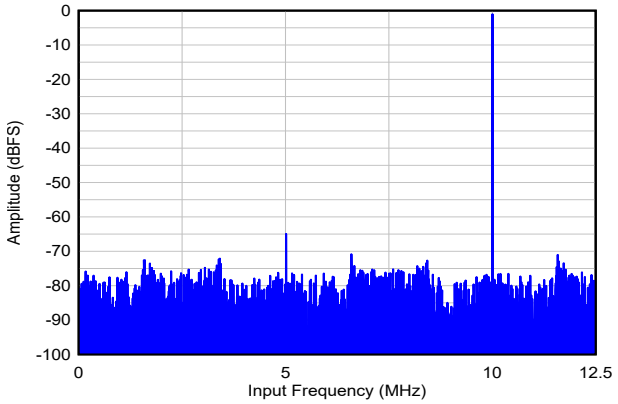

SNR = 49.8dBFS, SFDR = 63dBc, Non HD23 = 69dBFS

**Figure 6-3. Single Tone FFT at $F_{IN}$ = 1MHz**



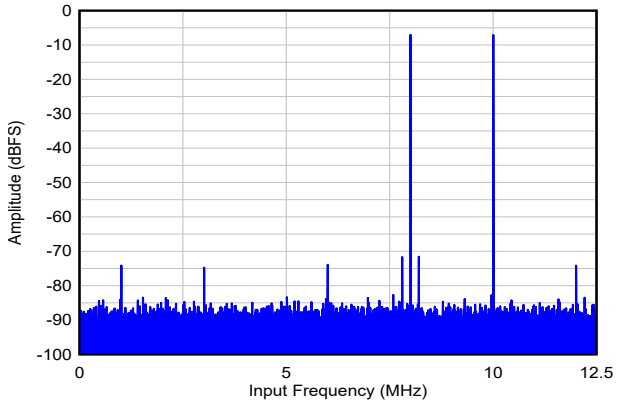

SNR = 49.7dBFS, SFDR = 62dBc, Non HD23 = 70dBFS

**Figure 6-4. Single Tone FFT at $F_{IN}$ = 1MHz, Single-ended Input**




SNR = 49.7dBFS, SFDR = 64dBc, Non HD23 = 70dBFS

**Figure 6-5. Single Tone FFT at $F_{IN}$ = 10MHz**




$A_{IN}$ = -7dBFS/tone, IMD3 = -95dBc

**Figure 6-6. Two Tone FFT at $F_{IN}$ = 8/10MHz**

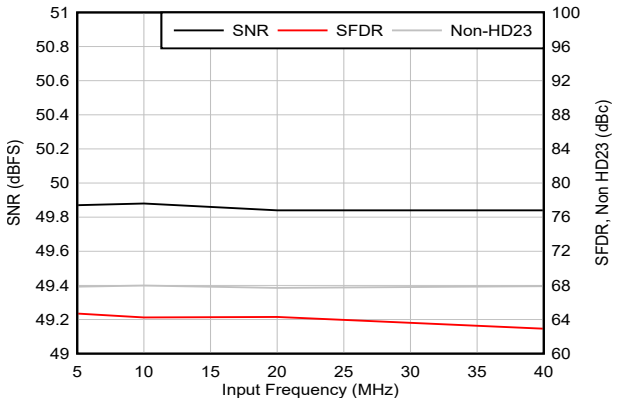
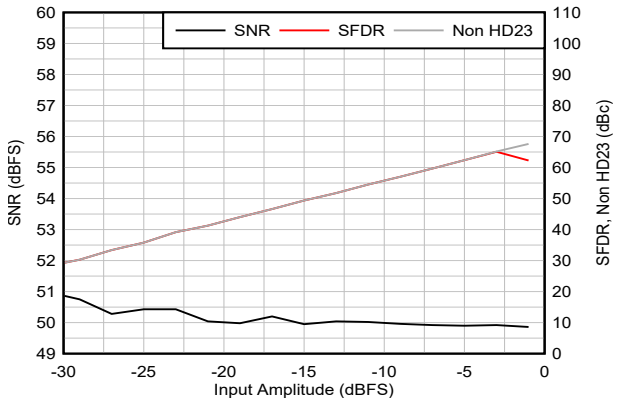



**Figure 6-7. AC Performance vs Input Frequency**

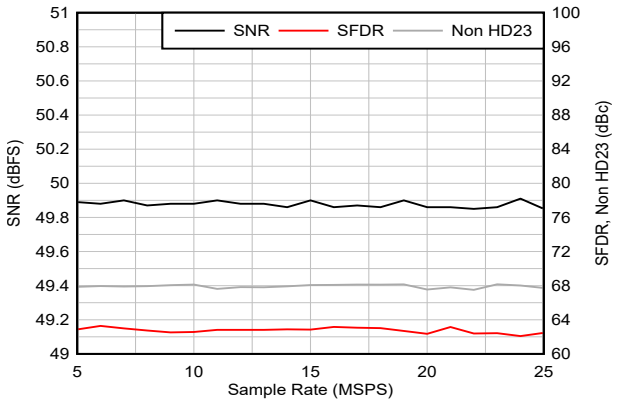



$F_{IN}$ = 1MHz

**Figure 6-8. AC Performance vs Input Amplitude**

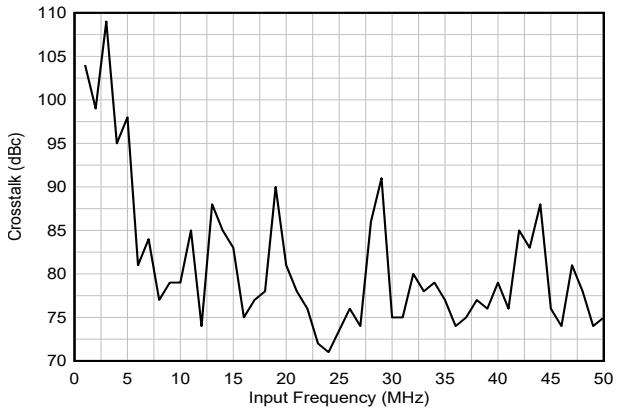
## 6.12 Typical Characteristics: 25MSPS (continued)

Typical values at $T_A$ = 25°C, ADC sampling rate = 25MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.



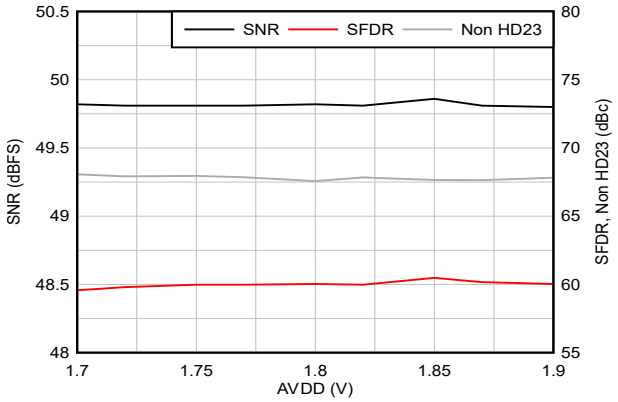

$F_{IN}$ = 1MHz

**Figure 6-9. AC Performance vs Sampling Rate**



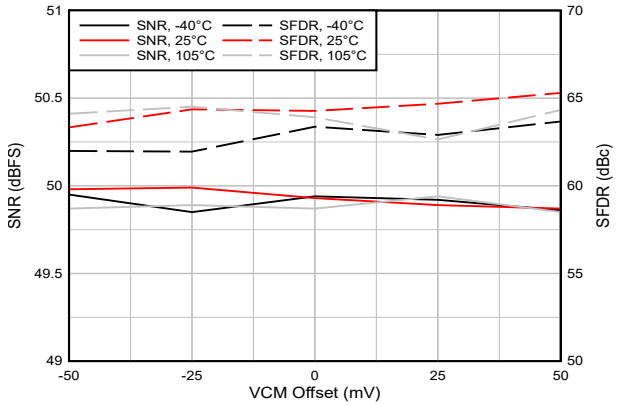

$A_{IN}$ = -1dBFS on aggressor channel

**Figure 6-10. Crosstalk vs Input Frequency**



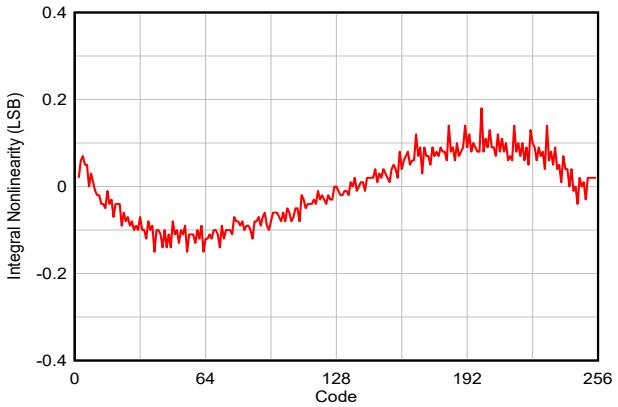

$F_{IN}$ = 1MHz

**Figure 6-11. AC Performance vs AVDD**



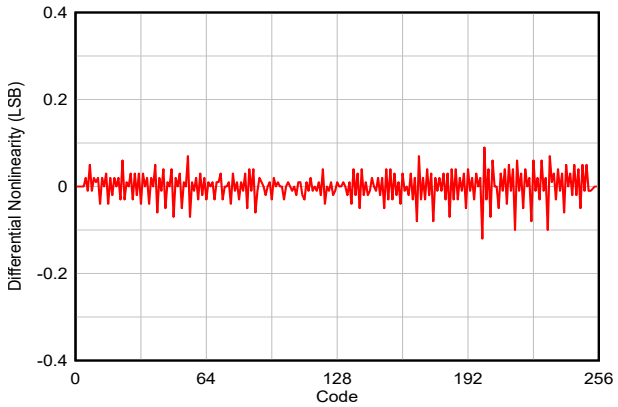

$F_{IN}$ = 1MHz

**Figure 6-12. AC Performance vs VCM vs Temperature**




$F_{IN}$ = 5MHz

**Figure 6-13. INL vs ADC Code**

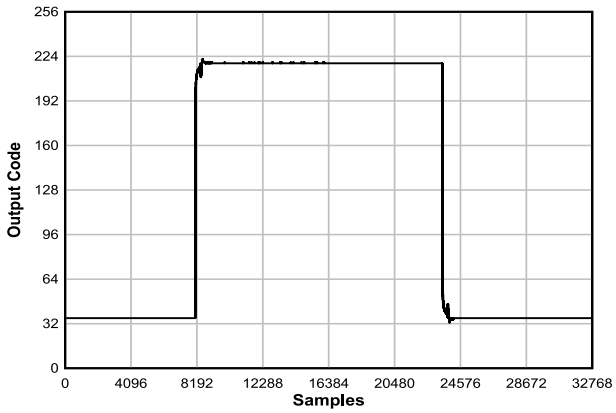



$F_{IN}$ = 5MHz

**Figure 6-14. DNL vs ADC Code**

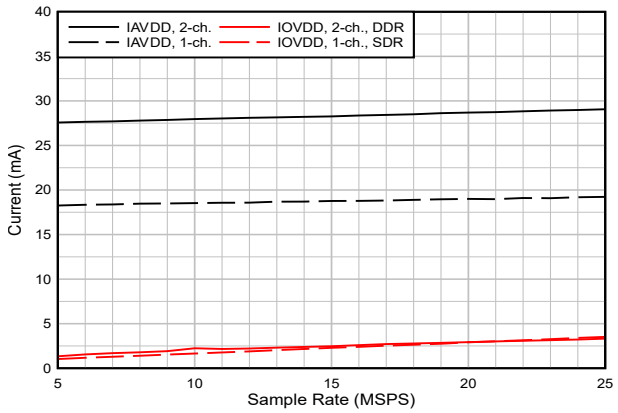
## 6.12 Typical Characteristics: 25MSPS (continued)

Typical values at $T_A$ = 25°C, ADC sampling rate = 25MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.



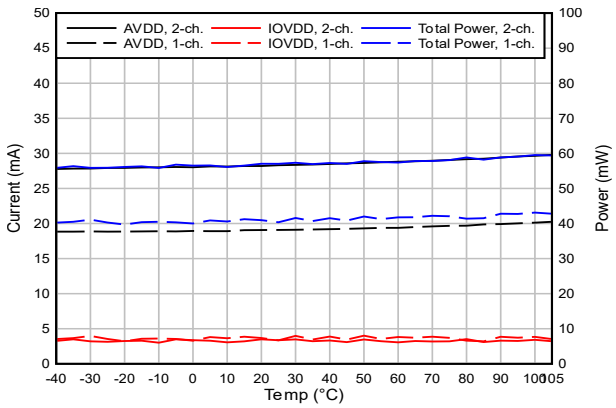

Pulse Input = 1MHz

**Figure 6-15. Pulse Response**



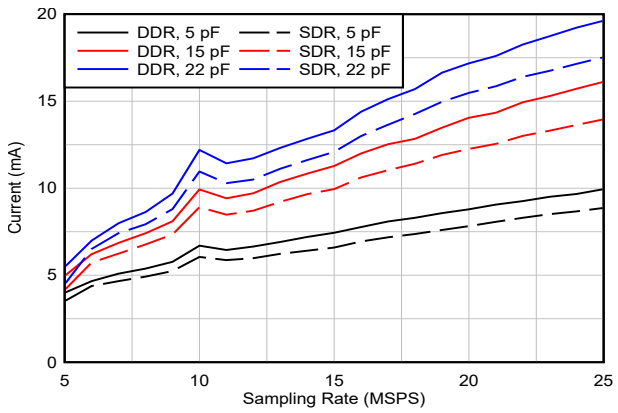

$F_{IN}$ = 5MHz

**Figure 6-16. Current vs Sampling Rate**




$F_{IN}$ = 5MHz

**Figure 6-17. Current vs Temperature**

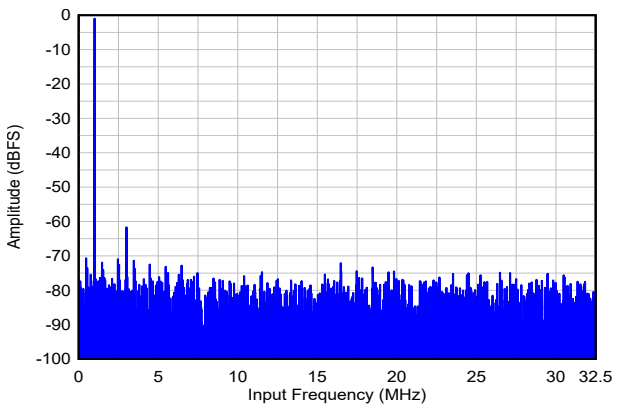



$F_{IN}$ = 5MHz

**Figure 6-18. $I_{IOVDD}$ Current vs Load Capacitance**

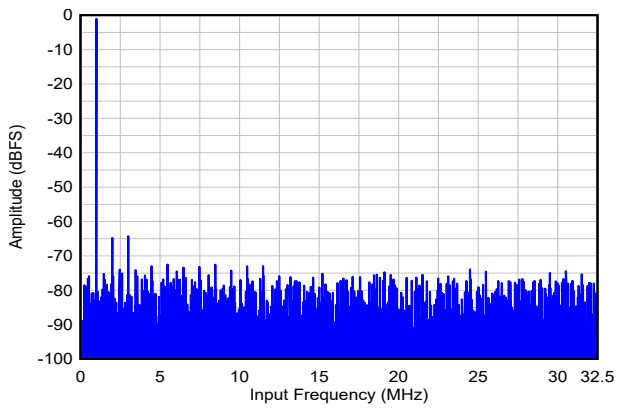
## 6.13 Typical Characteristics - 65MSPS

Typical values at $T_A$ = 25°C, ADC sampling rate = 65 MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.



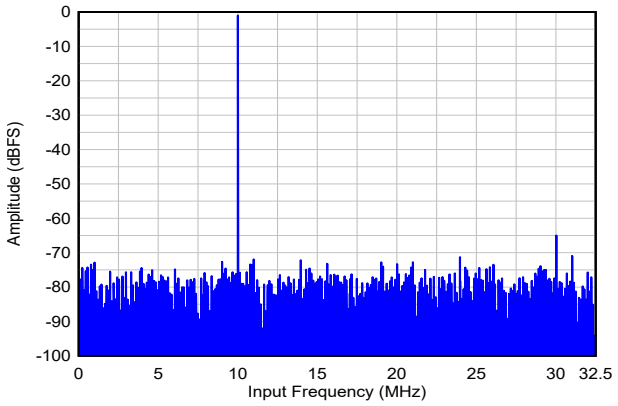

SNR = 49.7dBFS, SFDR = 61dBc, Non-HD23 = 70dBFS

**Figure 6-19. Single Tone FFT at $F_{IN}$ = 1MHz**



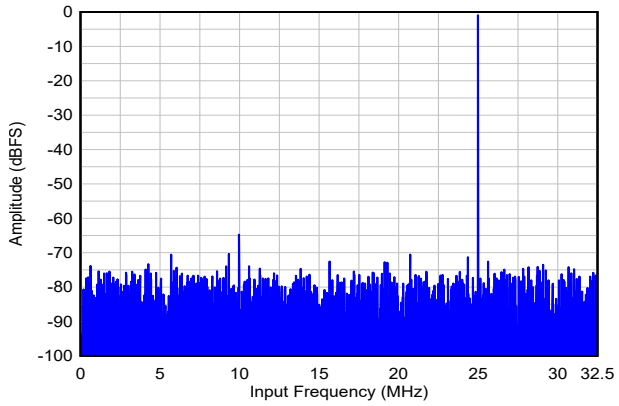

SNR = 49.6dBFS, SFDR = 63dBc, Non-HD23 = 72dBFS

**Figure 6-20. Single Tone FFT at $F_{IN}$ = 1MHz, Single-ended input**



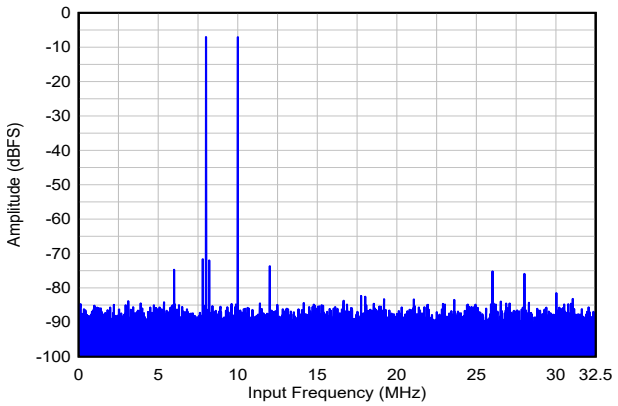

SNR = 49.8dBFS, SFDR = 64dBc, Non-HD23 = 70dBFS

**Figure 6-21. Single Tone FFT at $F_{IN}$ = 10MHz**




SNR = 49.9dBFS, SFDR = 64dBc, Non-HD23 = 69dBFS

**Figure 6-22. Single Tone FFT at $F_{IN}$ = 40MHz**




$A_{IN}$ = -7dBFS/tone, IMD3 = -93dBc

**Figure 6-23. Two Tone FFT at $F_{IN}$ = 8/10MHz**

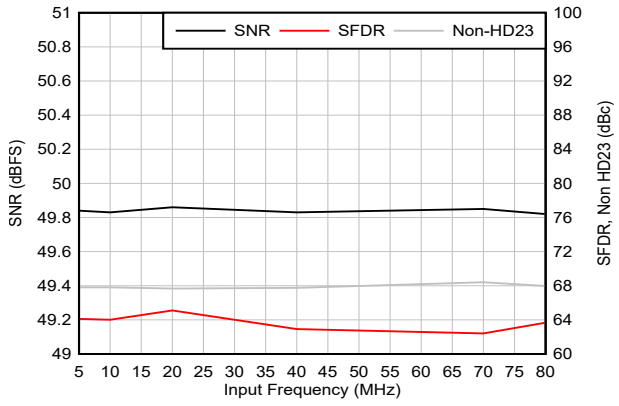
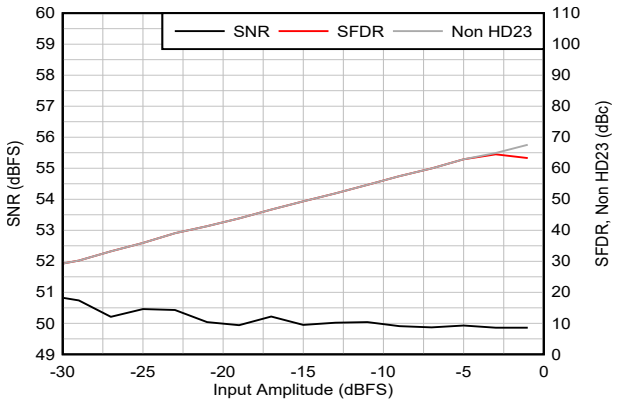



**Figure 6-24. AC Performance vs Input Frequency**

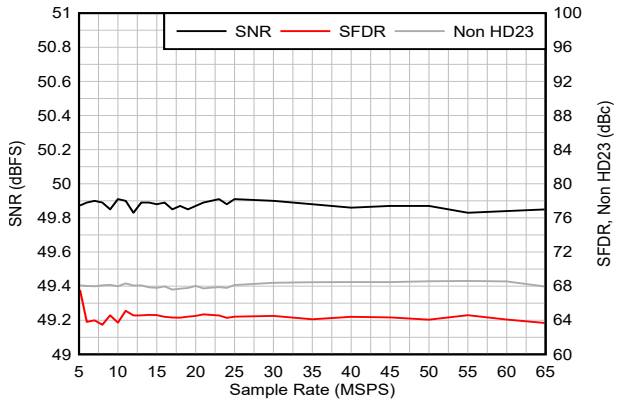
## 6.13 Typical Characteristics - 65MSPS (continued)

Typical values at $T_A$ = 25°C, ADC sampling rate = 65 MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.



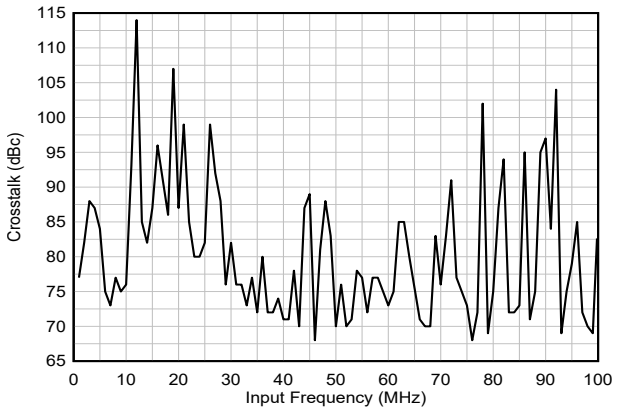

$F_{IN}$ = 5MHz

**Figure 6-25. AC Performance vs Input Amplitude**



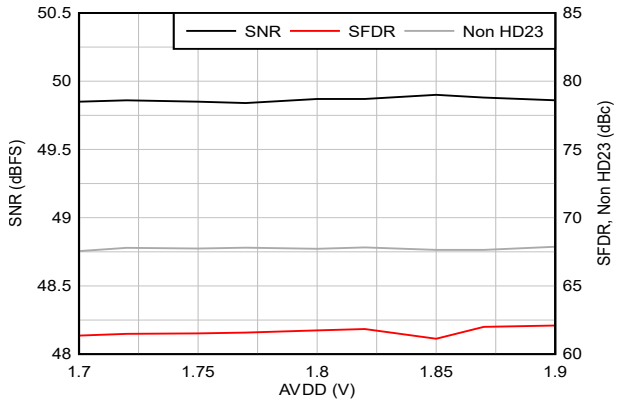

$F_{IN}$ = 5MHz

**Figure 6-26. AC Performance vs Sampling Rate**



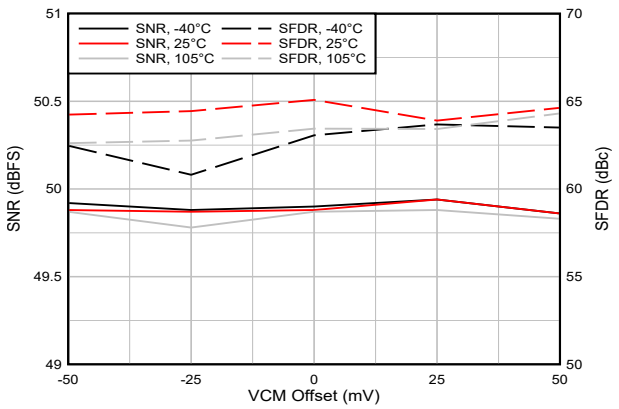

$A_{IN}$ = -1dBFS on aggressor channel

**Figure 6-27. Crosstalk vs Input Frequency**



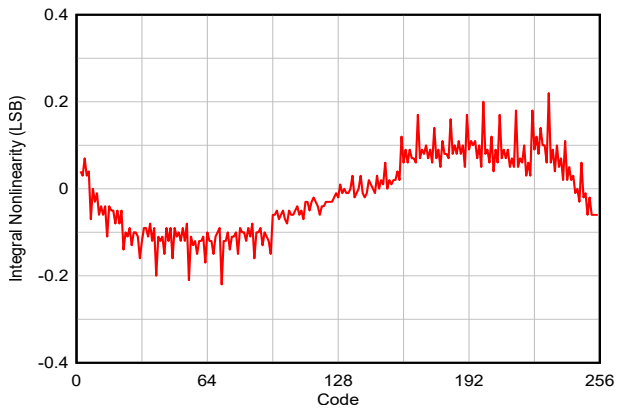

$F_{IN}$ = 5MHz

**Figure 6-28. AC Performance vs AVDD**




$F_{IN}$ = 5MHz

**Figure 6-29. AC Performance vs VCM vs Temperature**

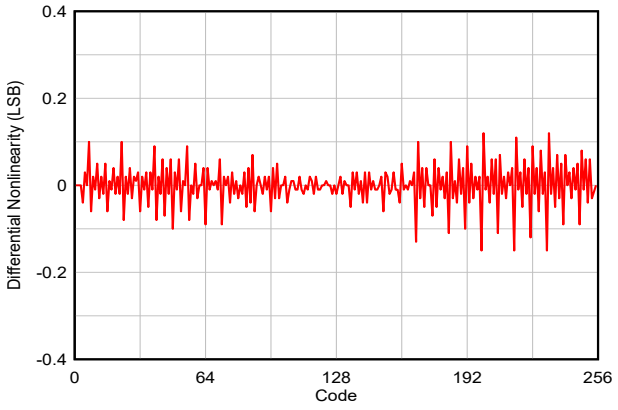



$F_{IN}$ = 5MHz

**Figure 6-30. INL vs ADC Code**

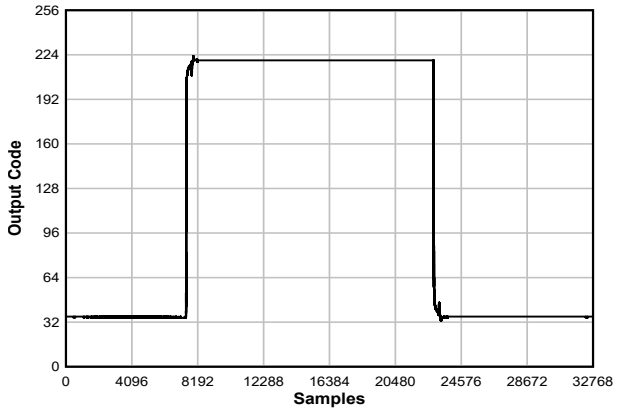
## 6.13 Typical Characteristics - 65MSPS (continued)

Typical values at $T_A$ = 25°C, ADC sampling rate = 65 MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.



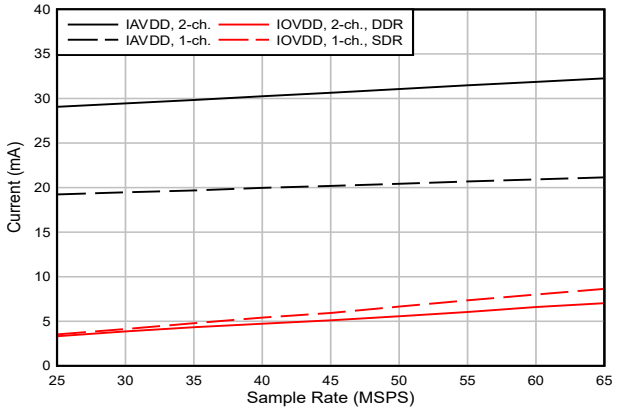

$F_{IN}$ = 5MHz

**Figure 6-31. DNL vs ADC Code**



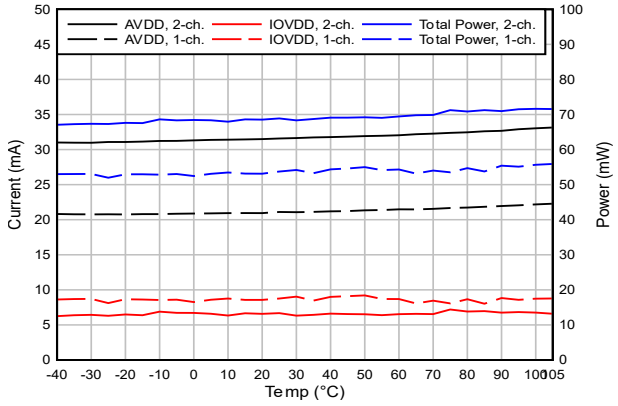

Pulse Input = 1MHz

**Figure 6-32. Pulse Response**



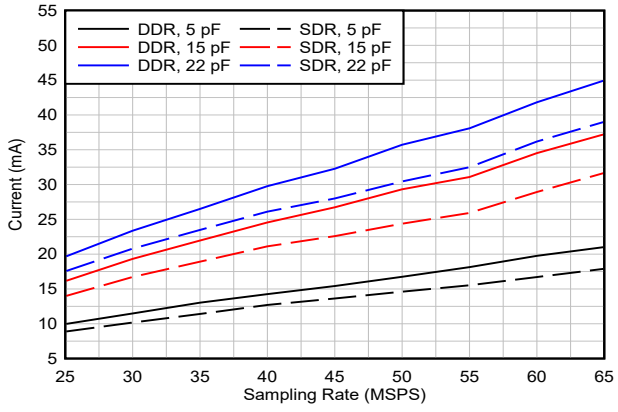

$F_{IN}$ = 5MHz

**Figure 6-33. Current vs Sampling Rate**




$F_{IN}$ = 5MHz

**Figure 6-34. Current vs Temperature**

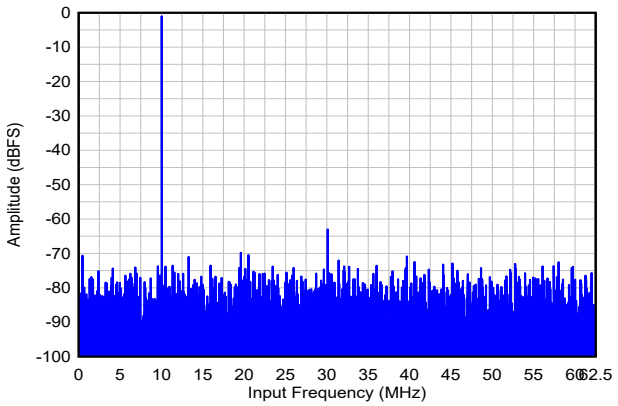



$F_{IN}$ = 5MHz

**Figure 6-35. $I_{IOVDD}$ Current vs Load Capacitance**

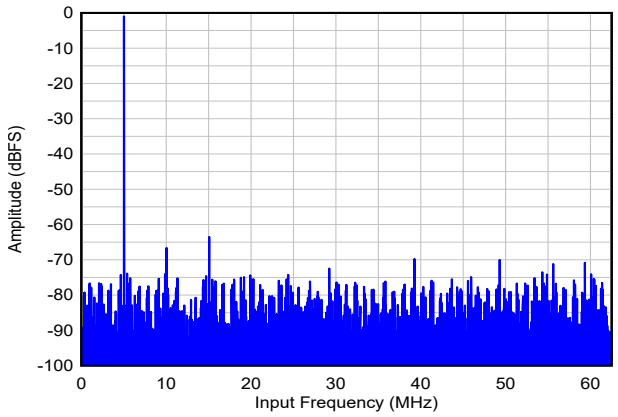
## 6.14 Typical Characteristics - 125MSPS

Typical values at $T_A$ = 25°C, ADC sampling rate = 125MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.



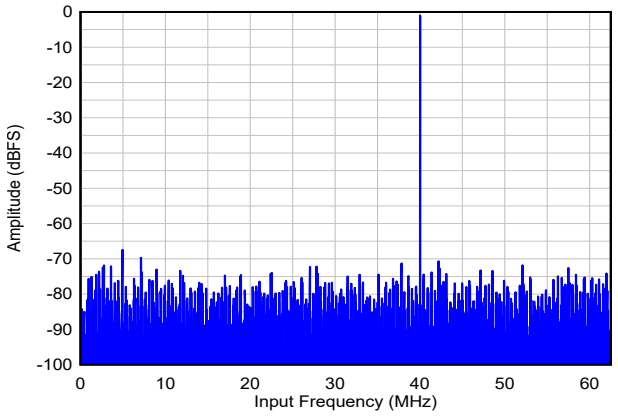

SNR = 49.8dBFS, SFDR = 62dBc, Non-HD23 = 69dBFS

**Figure 6-36. Single Tone FFT at $F_{IN}$ = 10MHz**



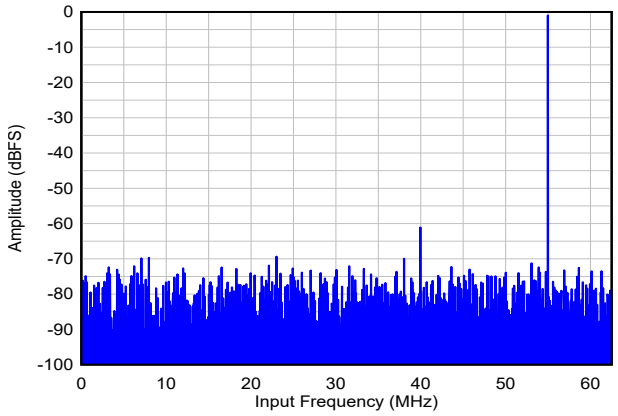

SNR = 49.5dBFS, SFDR = 63dBc, Non-HD23 = 69dBFS

**Figure 6-37. Single Tone FFT at $F_{IN}$ = 5MHz, Single-ended input**



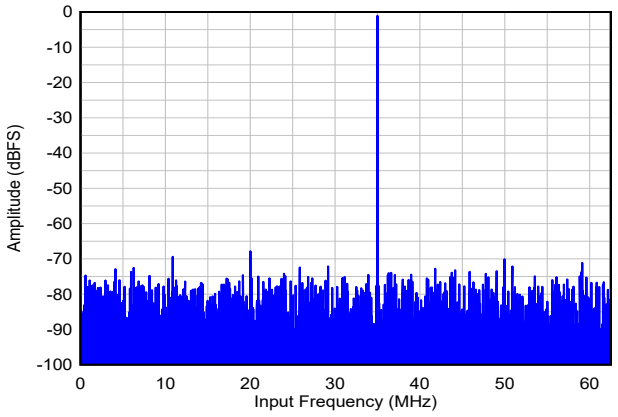

SNR = 49.8dBFS, SFDR = 66dBc, Non-HD23 = 69dBFS

**Figure 6-38. Single Tone FFT at $F_{IN}$ = 40MHz**



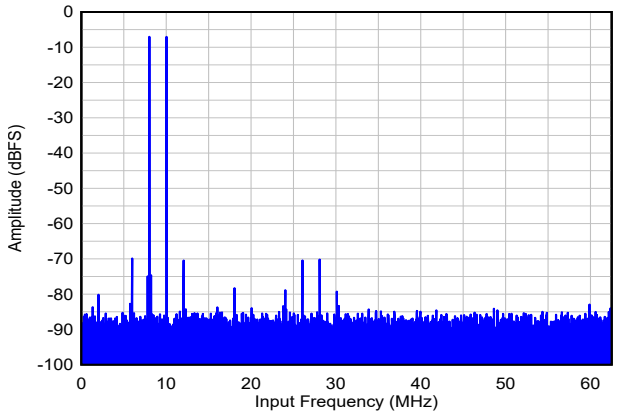

SNR = 49.8dBFS, SFDR = 60dBc, Non-HD23 = 68dBFS

**Figure 6-39. Single Tone FFT at $F_{IN}$ = 70MHz**




SNR = 49.8dBFS, SFDR = 67dBc, Non-HD23 = 68dBFS

**Figure 6-40. Single Tone FFT at $F_{IN}$ = 90MHz**

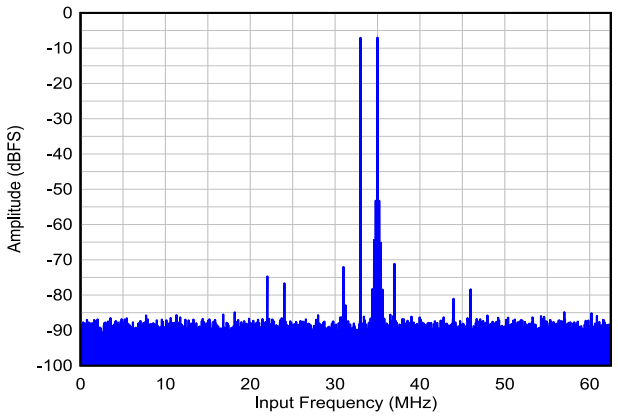



$A_{IN}$ = -7dBFS/tone, IMD3 = -87dBc

**Figure 6-41. Two Tone FFT at $F_{IN}$ = 8/10MHz**

## 6.14 Typical Characteristics - 125MSPS (continued)

Typical values at $T_A$ = 25°C, ADC sampling rate = 125MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.




$A_{IN}$ = -7dBFS/tone, IMD3 = -87dBc

**Figure 6-42. Two Tone FFT at $F_{IN}$ = 90/92MHz**

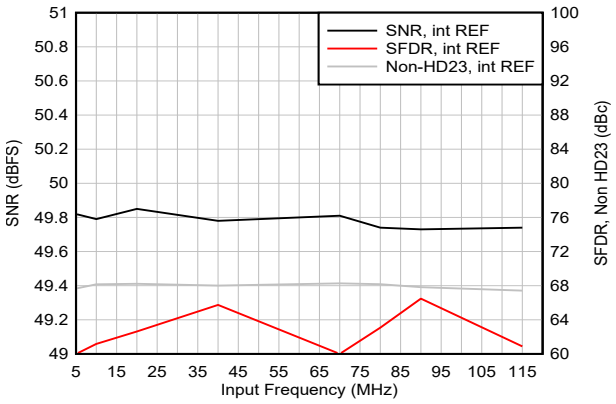
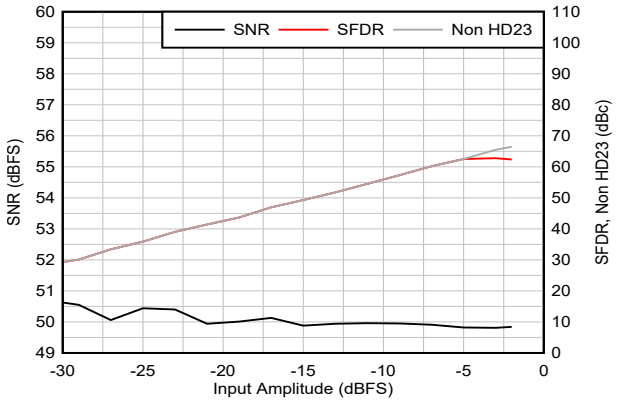
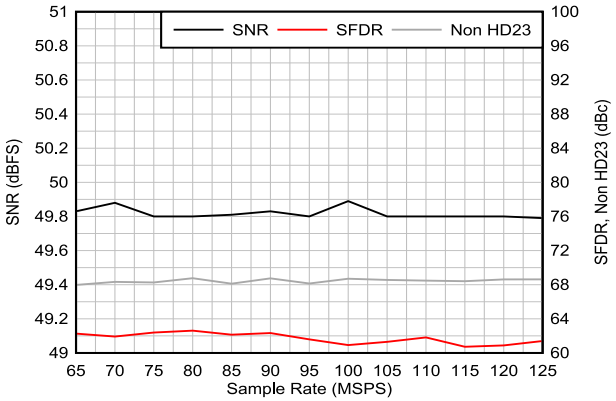



**Figure 6-43. AC Performance vs Input Frequency**



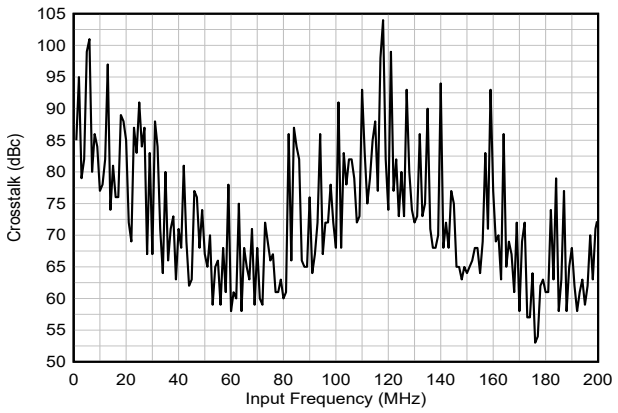

$F_{IN}$ = 5MHz

**Figure 6-44. AC Performance vs Input Amplitude**



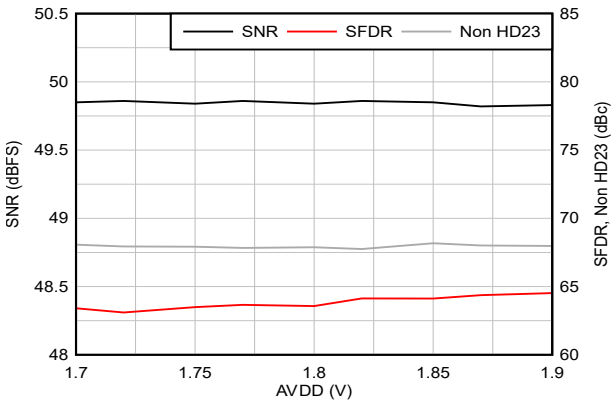

$F_{IN}$ = 10MHz

**Figure 6-45. AC Performance vs Sampling Rate**




$A_{IN}$ = -1dBFS on aggressor channel

**Figure 6-46. Crosstalk vs Input Frequency**

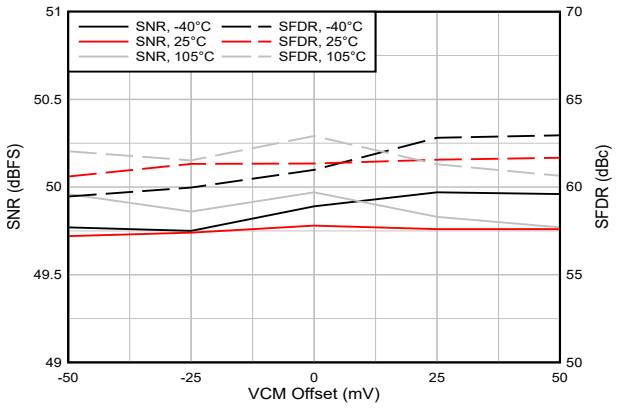



$F_{IN}$ = 5MHz

**Figure 6-47. AC Performance vs AVDD**

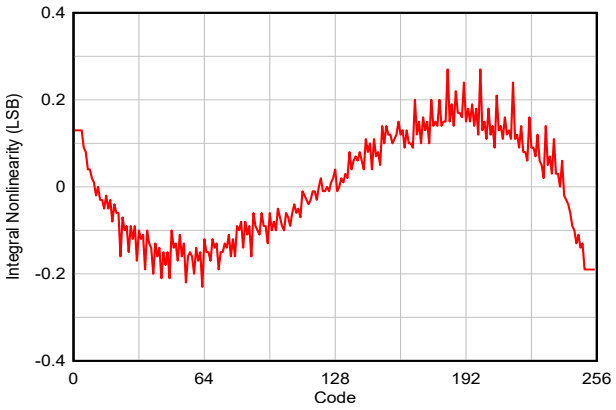
## 6.14 Typical Characteristics - 125MSPS (continued)

Typical values at $T_A$ = 25°C, ADC sampling rate = 125MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.



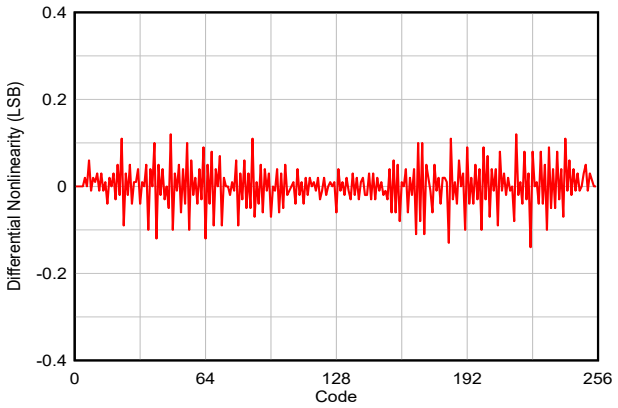

$F_{IN}$ = 10MHz

**Figure 6-48. AC Performance vs VCM vs Temperature**



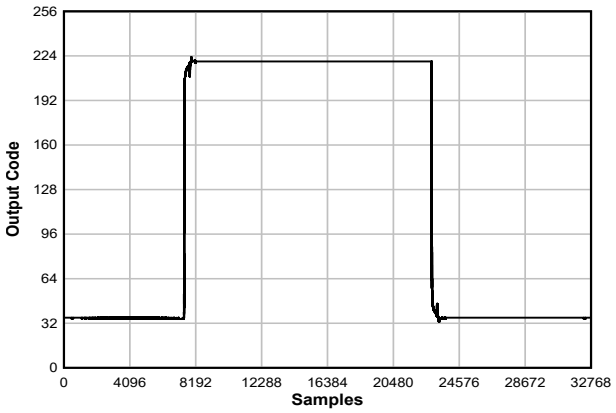

$F_{IN}$ = 5MHz

**Figure 6-49. INL vs ADC Code**



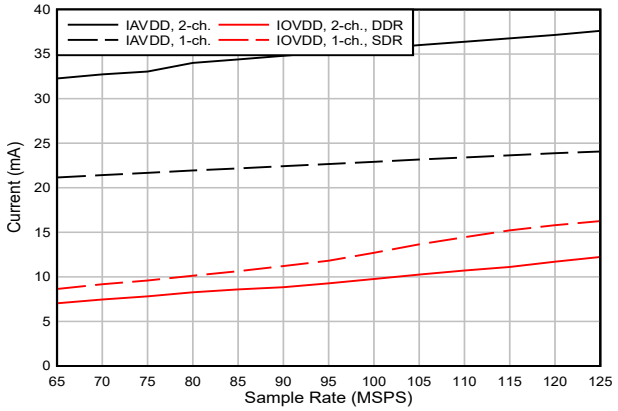

$F_{IN}$ = 5MHz

**Figure 6-50. DNL vs ADC Code**



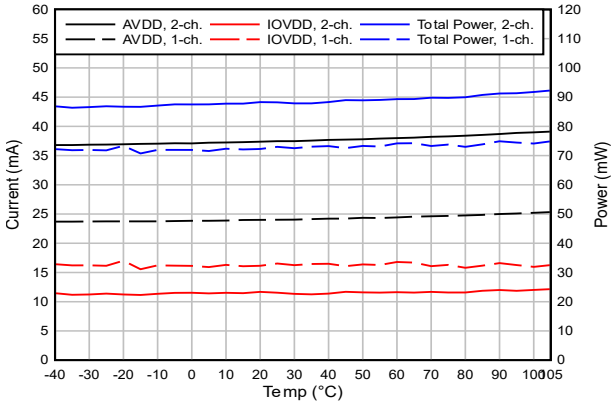

Pulse Input = 1MHz

**Figure 6-51. Pulse Response**




$F_{IN}$ = 5MHz

**Figure 6-52. Current vs Sampling Rate**

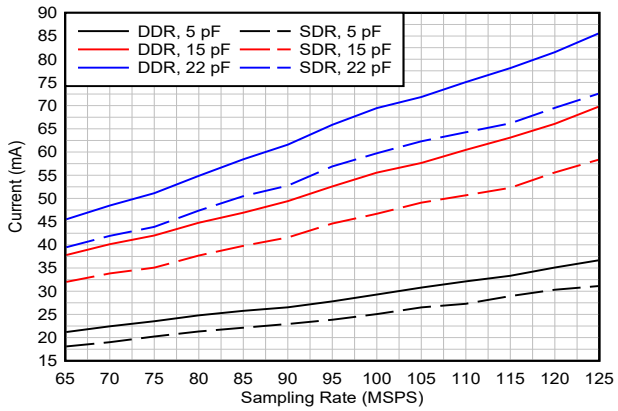



$F_{IN}$ = 5MHz

**Figure 6-53. Current vs Temperature**

## 6.14 Typical Characteristics - 125MSPS (continued)

Typical values at $T_A$ = 25°C, ADC sampling rate = 125MSPS, $A_{IN}$ = –1dBFS, differential input, AVDD = IOVDD = 1.8V, internal 1.2V voltage reference, unless otherwise noted.




$F_{IN}$ = 5MHz

**Figure 6-54. $I_{IOVDD}$ Current vs Load Capacitance**

# 7 Detailed Description

## 7.1 Overview

The ADC3908Dx and ADC3908Sx is a low noise, ultra-low power 8-bit high-speed single and dual channel ADC family supporting sampling rates up to 125MSPS. With the inherent low latency architecture, the digital output result is available after only one clock cycle. The ADC has buffered analog inputs which eases design by isolating the input from the ADC sampling operation. The ADC3908Dx and ADC3908Sx is equipped with an on-chip internal reference buffer and supports either single ended or differential input signaling.

The CMOS output data interface is configured as parallel DDR for dual channel devices and SDR for single channel devices with the option of 1.8V or 3.3V logic. The device supports 2's Complement or Offset Binary format options. The ADC3908Dx and ADC3908Sx offers $\overline{\text{DCLK}}$ as an alternate data clock for receivers that can not capture on the DCLK falling edge when using DDR interface. Table 7-1 shows the pin mapping to supply.

**Table 7-1. Device Pin to Supply Mapping**

| Power Supply | Device Pins |
|---|---|
| AVDD | CLK, INxP\|M, RESET, M0, M1, M2, PDN |
| IOVDD | D0-D7, DCLK, $\overline{\text{DCLK}}$ |

## 7.2 Functional Block Diagram

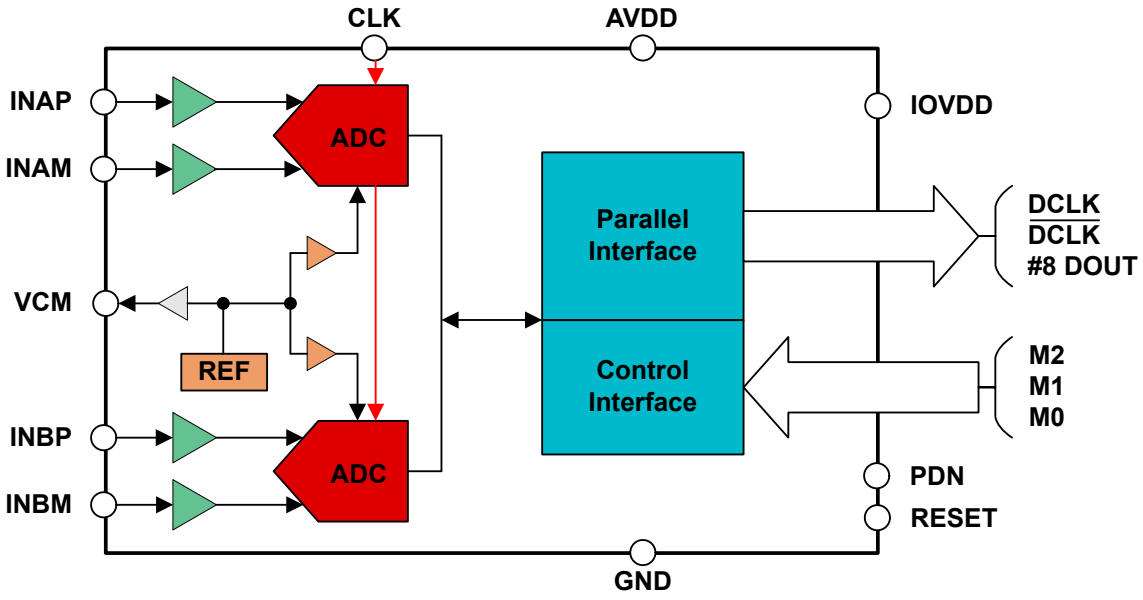



**Figure 7-1. Dual Channel Device**

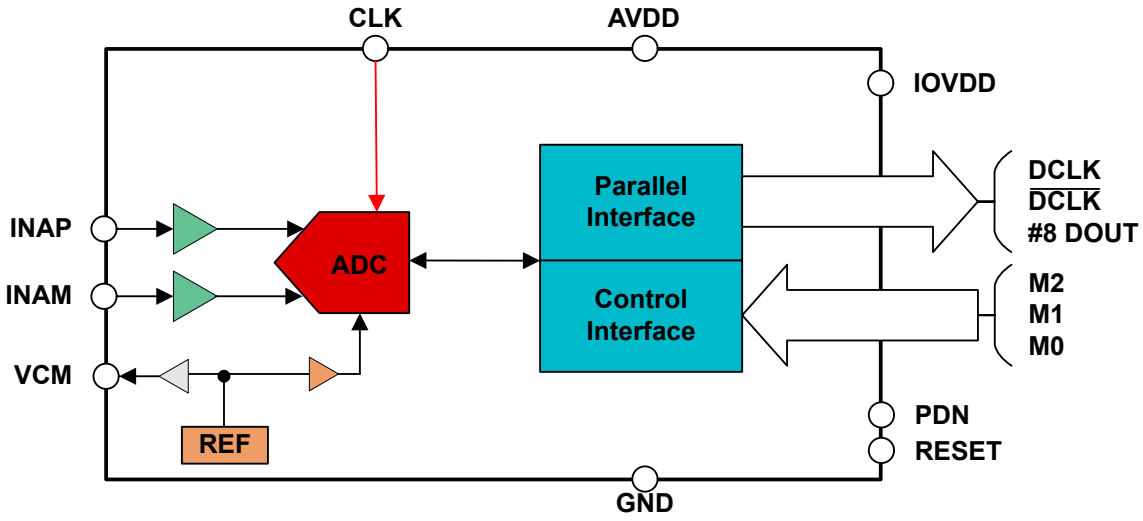



**Figure 7-2. Single Channel Device**

## 7.3 Feature Description

### *7.3.1 Analog Input*

The analog inputs of ADC3908Dx and ADC3908Sx supports differential and single-ended configuration, with support for AC coupling and DC coupling. Analog inputs are designed for an input common mode voltage of 1.25V which must be provided externally on each input pin. DC-coupled input signals must have a common mode voltage that meets the device input common mode voltage range.

The ADC3908Dx and ADC3908Sx has buffered analog inputs which eases design by isolating the input from the ADC sampling operation.

#### 7.3.1.1 Single Ended Input

The ADC3908Dx and ADC3908Sx can be configured to operate in single ended mode using just the positive signal input. This operating mode must be enabled via pin control (Interface configuration table). The single ended signal is connected to the positive input of the ADC and negative input must be biased to VCM as shown in Figure 7-3.

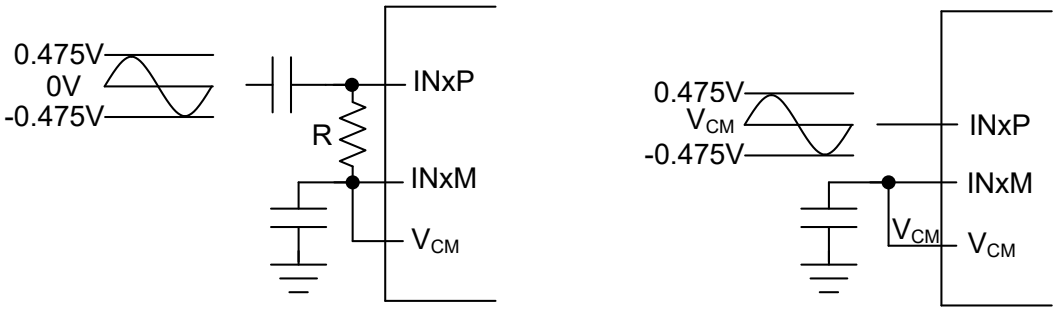



**Figure 7-3. Single ended analog input: AC coupled (left) and DC coupled (right)**

#### 7.3.1.2 Differential Input

The ADC3908Dx and ADC3908Sx supports differential mode with a swing of $1.9V_{PP}$ as shown in Figure 7-4. This operating mode must be enabled via pin control (Interface configuration table).

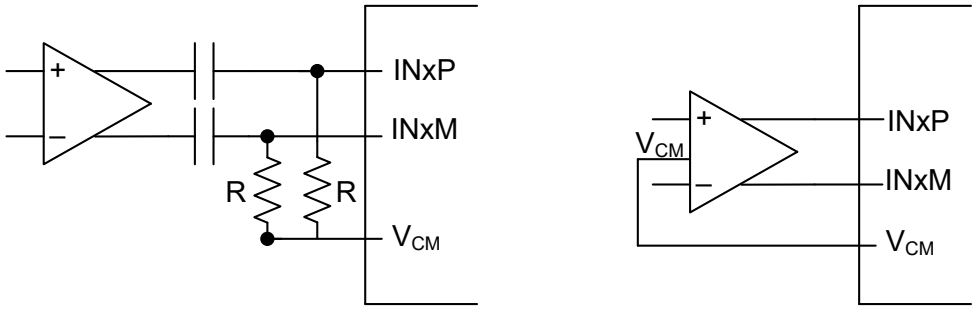



**Figure 7-4. Differential analog input: AC coupled (left) and DC coupled (right)**

#### 7.3.1.3 Analog Input Bandwidth

Figure 7-5 shows the analog full power input bandwidth. The -3dB bandwidth is approximately 150MHz.

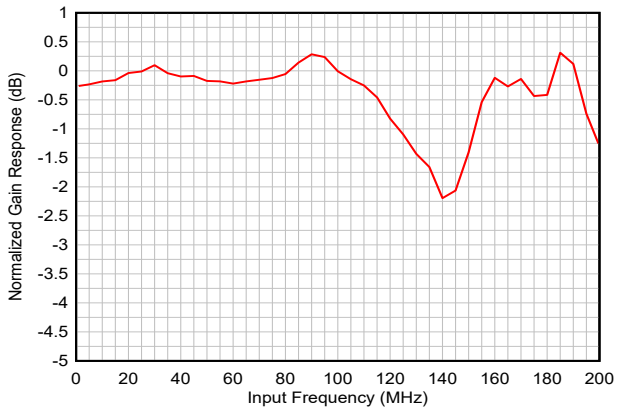



**Figure 7-5. ADC Analog Input Bandwidth Response**

### *7.3.2 Sampling Clock Input*

The ADC3908Dx and ADC3908Sx has a single-ended sampling clock input. To maximize the ADC SNR performance, the external sampling clock should have low jitter with a high slew rate. The ADC3908Dx and ADC3908Sx can be AC or DC coupled externally. When AC coupling, sampling clock needs to have a resistor divider such that the center voltage is around 0.9V and when DC coupling the sampling clock, center voltage needs to be around 0.9V as shown in Figure 7-6.

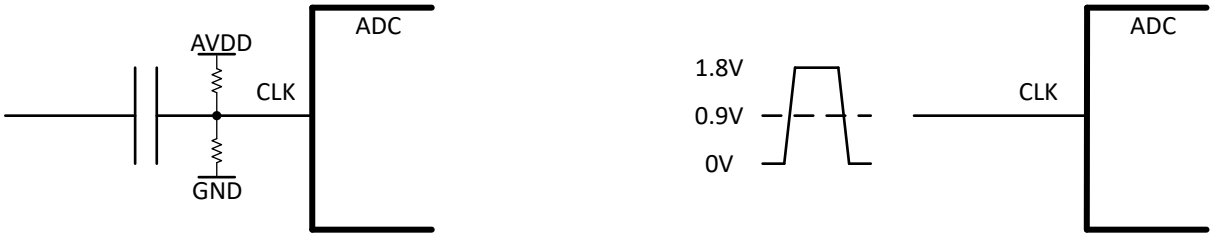



**Figure 7-6. Sampling clock configuration: AC coupled (left) and DC coupled (right)**

### 7.3.3 Digital Interface

The ADC3908Dx and ADC3908Sx family supports parallel CMOS output modes - DDR (double data rate) and SDR (single data rate) output formats for dual and single channel devices, respectively. The output data can be configured to 2's complement (default) or offset binary via pin control (Interface configuration table). The device generates an output data clock and inverse data clock. For receivers that cannot use falling edge of data clock, inverse data clock can be used to clock data.

#### 7.3.3.1 Test Pattern

The ADC3908Dx and ADC3908Sx has a static test pattern that can be enabled via pin control (see Interface Configuration Table). The test pattern splits each channel data into two groups, upper (D7:D4) and lower (D3:D0) bits. Each group has a value of all zeros or a value of all 1s. Figure 7-7 shows how test pattern is implemented for dual channel. Figure 7-8 shows how test pattern is implemented for single channel.

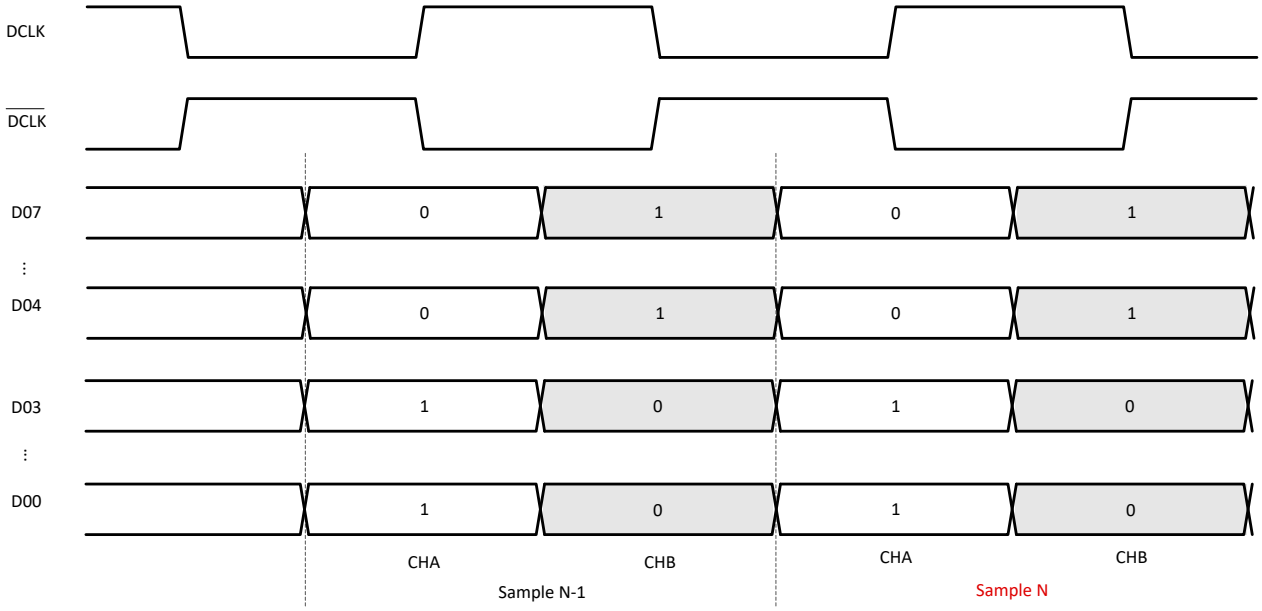



**Figure 7-7. Dual Channel, Test Pattern**

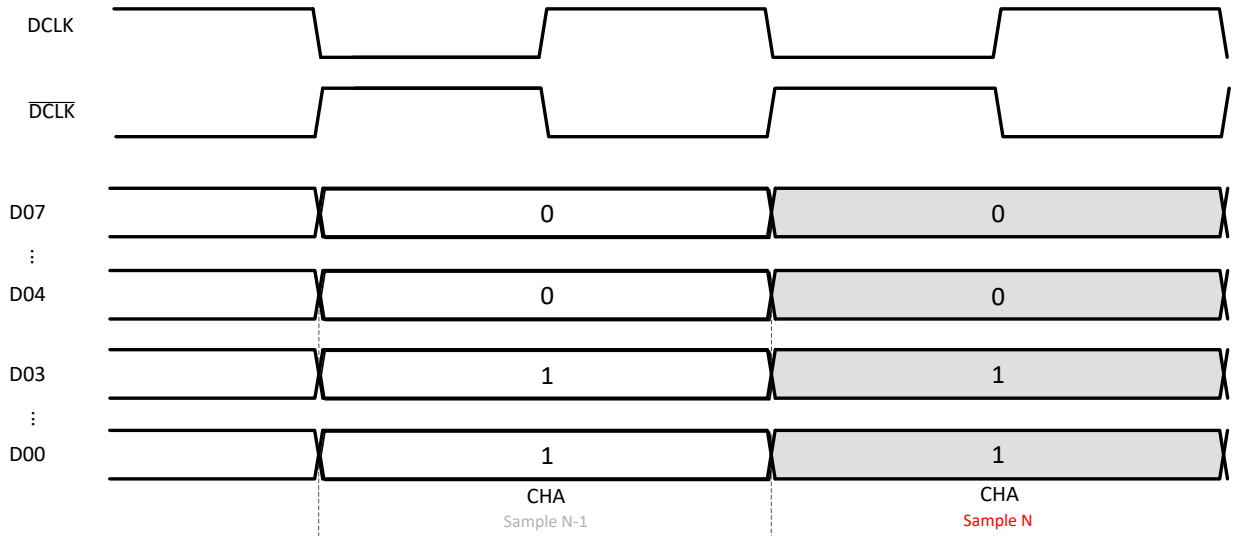



**Figure 7-8. Single Channel, Test Pattern**

#### 7.3.3.2 Interface Configuration using Pin Control

The ADC3908Dx and ADC3908Sx analog input and output interface is configured via pin control only. Pins M0, M1, and M2 can either be pulled high to AVDD, pulled low to GND or intermediate voltages in between. Interface Configuration Table shows configuration options.

**Table 7-2. Interface Configuration**

| Pin Name | Description | GND | 0.5V | 1V | AVDD |
|---|---|---|---|---|---|
| M0 | CMOS interface | DDR (dual channel only) | | | SDR (single channel only) |
| M1 | Output data | ADC data | | | Test Pattern |
| M2 | Analog input | Differential input | | Single-ended input | |
| | Output data format | 2's Complement | Offset binary | 2's Complement | Offset binary |

## 7.4 Device Functional Modes

### *7.4.1 Normal Operation*

In normal operating mode, the entire ADC full scale range gets converted to a digital output with 8-bit resolution. The output is available in as little as 1 clock cycle on the digital CMOS outputs.

### *7.4.2 Power Down*

The ADC3908Dx and ADC3908Sx can be put into power down mode when PDN pin is pulled high.

# 8 Application Information Disclaimer

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Typical Application

A digitizer is a typical time domain application for the ADC3908D125. The front end circuitry is similar to several other systems such as oscilloscopes, distance meters, laser scanners or other hand held test equipment.

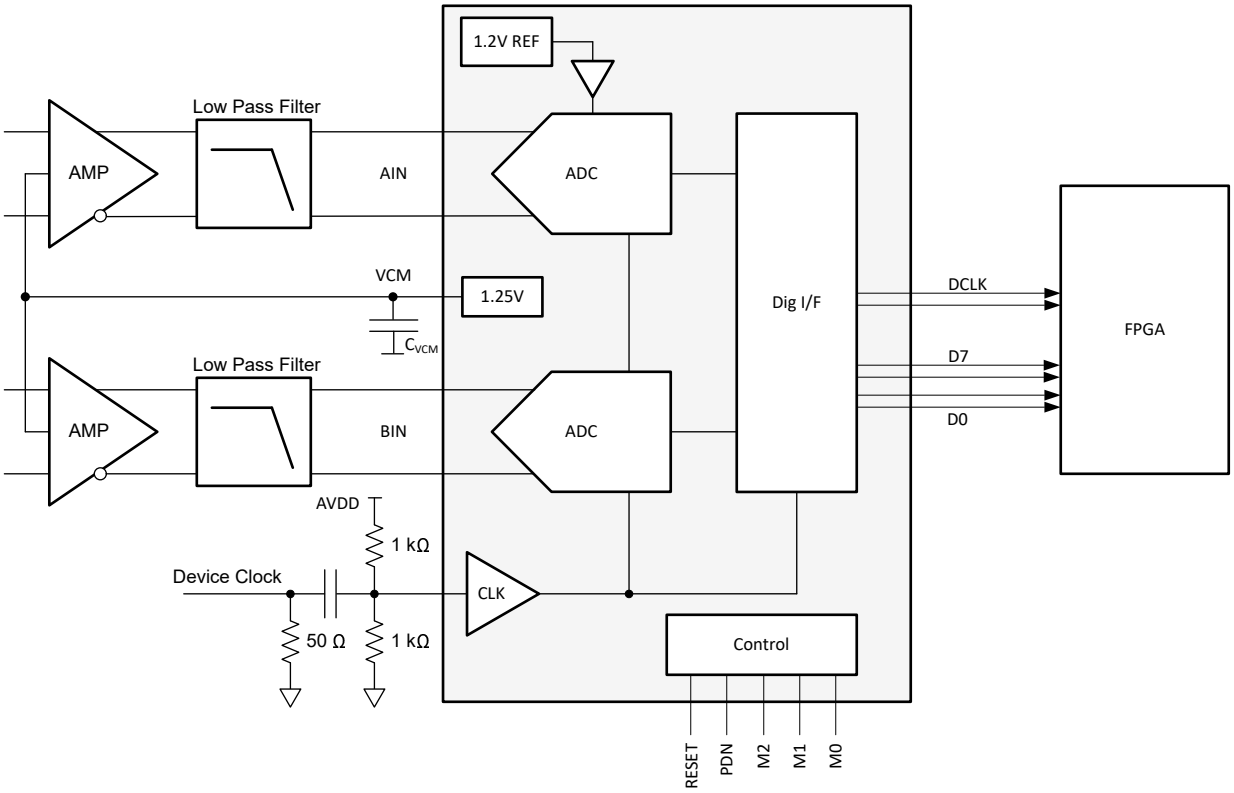



**Figure 8-1. Typical configuration for a time domain digitizer**

### *8.1.1 Design Requirements*

Time domain applications cover a wide range of frequencies from low input frequencies at or near DC in the 1st Nyquist zone. If a low input frequency is supported, then the input has to be DC coupled and the ADC driven by a fully differential amplifier (FDA).

The ADC performance is highly dependent on the quality of the external clock source. A higher ADC sampling rate is desirable to relax the external anti-aliasing filter. For optimum performance, the analog inputs must be driven differentially.

**Table 8-1. Design key care abouts**

| FEATURE | DESCRIPTION |
|---|---|
| Signal Bandwidth | DC to 30MHz |
| Input Driver | Single ended to differential signal conversion and DC coupling |
| Clock Source | External clock with low jitter |

When designing the amplifier/filter driving circuit, the ADC input full-scale voltage needs to be taken into consideration. For example, the ADC3908D125 input full-scale is 1.9 $V_{PP}$. When factoring in approximately 1dB for insertion loss of the filter, then the amplifier needs to deliver close to 2.1 $V_{PP}$. The amplifier distortion performance degrades with a larger output swing and considering the ADC common mode input voltage the amplifier may not be able to deliver the full swing. The deviceADC3908D125 provides an output common mode voltage of 1.25V and the THS4541 for example can only swing within 250mV of its negative supply. A unipolar 3.3V amplifier power supply limits the maximum voltage swing to approximately 2.8$V_{PP}$. Hence, if a larger output swing is required (factoring in filter insertion loss) then a negative supply for the amplifier is needed to eliminate that limitation. Additionally, input voltage protection diodes may be needed to protect the ADC from over-voltage events.

**Table 8-2. Output voltage swing of THS4541 vs power supply**

| DEVICE | MIN OUTPUT VOLTAGE | MAX SWING WITH 3.3V/ 0V SUPPLY |
|---|---|---|
| THS4541 | VS- + 250mV | 2.8$V_{PP}$ |

### *8.1.2 Detailed Design Procedure*

#### 8.1.2.1 Input Signal Path

The THS4541 provides a good low power option to drive the ADC inputs. Table 8-3 provides an overview of the THS4541 with power consumption and usable frequency.

**Table 8-3. Fully Differential Amplifier Options**

| DEVICE | CURRENT (IQ) PER CHANNEL | USABLE FREQUENCY RANGE |
|---|---|---|
| THS4541 | 10mA | < 70MHz |

The low pass filter design (topology, filter order) is driven by the application. However, when designing the low pass filter, the optimum load impedance for the amplifier must also be taken into consideration.

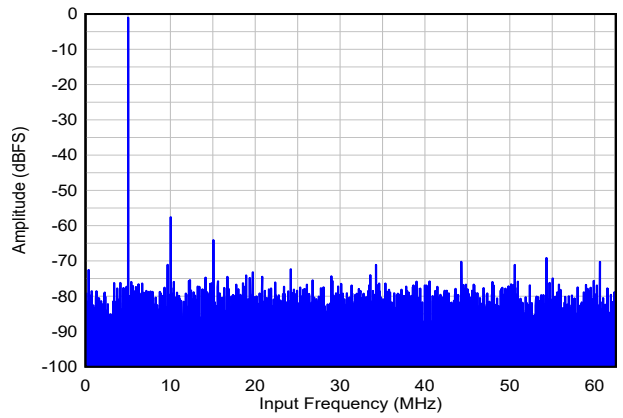
#### 8.1.2.2 Sampling Clock

Applications operating with low input frequencies (such as DC to 20MHz) typically are less sensitive to performance degradation due to clock jitter. The internal ADC aperture jitter improves with faster rise and fall times (that is, square wave vs sine wave).

Termination of the clock input needs to be considered for long clock traces.

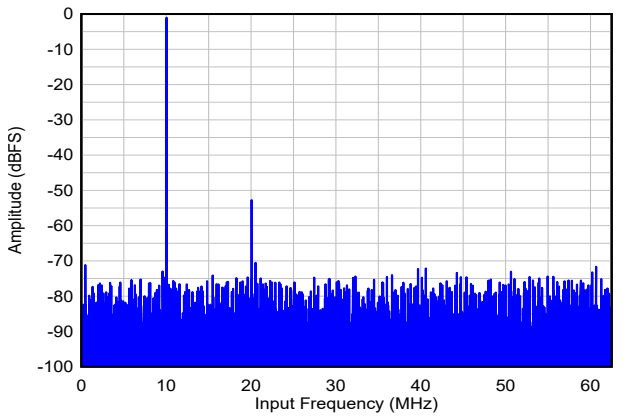
### 8.1.3 Application Curves

The following FFT plots show the performance of THS4541 driving the ADC3908D125 operated at 125MSPS with a full-scale input at -1dBFS.




$A_{IN}$ = - 1dBFS, SNR = 49.8 dBFS, SFDR = 57 dBFS

**Figure 8-2. 5MHz FFT (THS4541 FDA)**




$A_{IN}$ = - 1dBFS, SNR = 49.7 dBFS, SFDR = 52 dBFS

**Figure 8-3. 10MHz FFT (THS4541 FDA)**

## 8.2 Initialization Set Up

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin.

1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied the internal band gap reference powers up and settle out in approximately 2ms.
2. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses and the internal power up calibration is initiated. The calibration takes approximately 2,000 clock cycles.
3. Begin programming using the device control pins.

## 8.3 Power Supply Recommendations

The ADC requires two different power-supplies. The AVDD rail provides power for the internal analog and digital circuits and the ADC itself while the IOVDD rail powers the digital interface. Power sequencing is not required.

The AVDD power supply must be low noise to achieve data sheet performance. In applications operating near DC, the 1/f noise contribution of the power supply also needs to be considered. The ADC is designed for very good PSRR which aids with the power supply filter design.

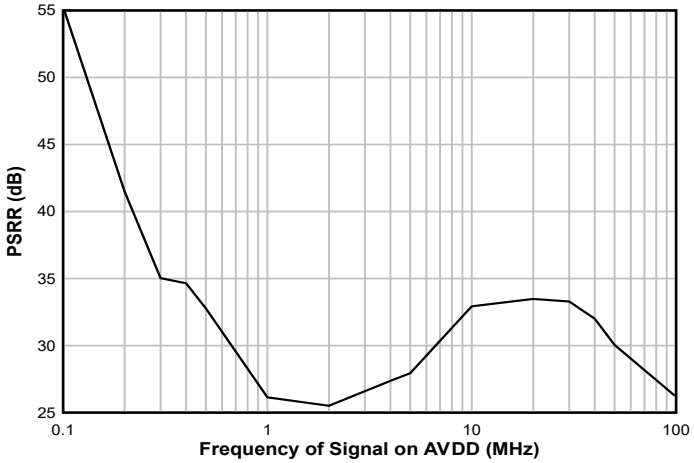



**Figure 8-4. Power supply rejection ratio (PSRR) vs frequency**

There are two recommended power-supply architectures:

1. Step down using high-efficiency switching converters, followed by a second stage of regulation using a low noise LDO to provide switching noise reduction and improved voltage accuracy.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken to make sure switching noise is minimized to prevent degraded ADC performance.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include the TPS62821, and similar devices.

Recommended low dropout (LDO) linear regulators include the TPS7A4701, TPS7A90, LP5901, and similar devices.

For the switch regulator only approach, the ripple filter must be designed with a notch frequency that aligns with the switching ripple frequency of the DC/DC converter. Note the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. Figure 8-5 and Figure 8-6 illustrate the two approaches.

AVDD and IOVDD supply voltages should not be shared to prevent digital switching noise from coupling into the analog signal chain.

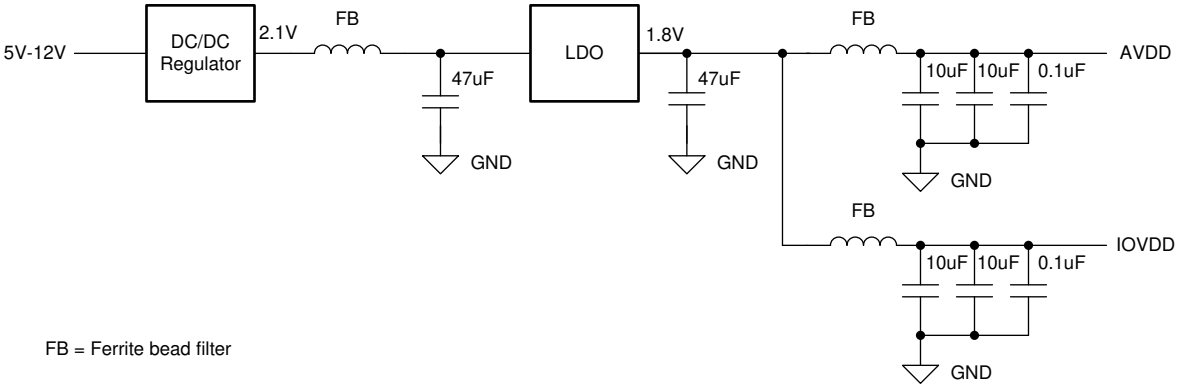



**Figure 8-5. Example: LDO Linear Regulator Approach**

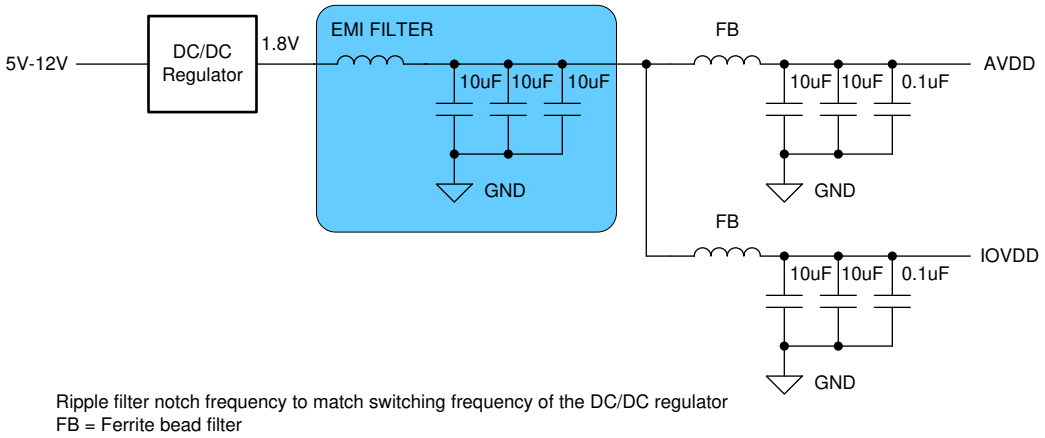



**Figure 8-6. Example: Switcher-Only Approach**

## 8.4 Layout

### *8.4.1 Layout Guidelines*

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
   - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
2. Digital output interface
   - Traces should be as short as possible to reduce capacitive load seen by the CMOS outputs.
   - Series resistance should be used to reduce instantaneous current demand and improve signal integrity.
3. Power and ground connections
   - Provide low resistance connection paths to all power and ground pins.
   - Use power and ground planes instead of traces.
   - Avoid narrow, isolated paths which increase the connection resistance.
   - Use a signal/ground/power circuit board stackup to maximize coupling between the ground and power plane.

### *8.4.2 Layout Example*

The following screen shot shows the top layer of the ADC3910D125EVM.

- Signal inputs are routed as different signal and along with clock input on the top layer avoiding vias.
- Serial CMOS output interface lanes with isolation resistor.
- Bypass caps are close to the VREF pin on the top layer avoiding vias.

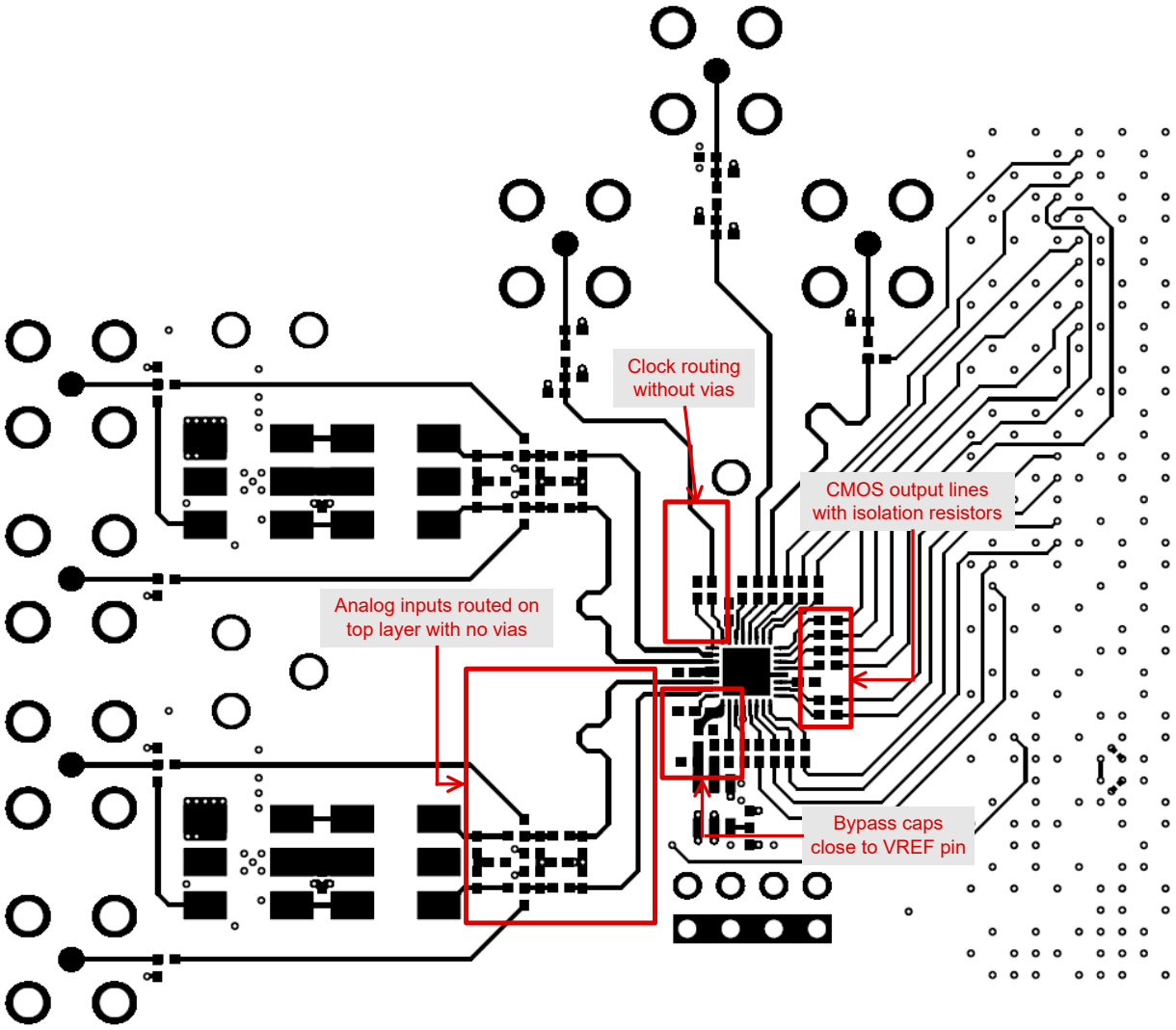



**Figure 8-7. Layout Example: top layer of ADC3910D125EVM**

# 9 Device and Documentation Support

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| October 2024 | * | Initial Release |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC3908D025IRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398D1 | Samples |
| ADC3908D025IRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398D1 | Samples |
| ADC3908D065IRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398D2 | Samples |
| ADC3908D065IRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398D2 | Samples |
| ADC3908D125IRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398D3 | Samples |
| ADC3908D125IRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398D3 | Samples |
| ADC3908S025IRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398S1 | Samples |
| ADC3908S025IRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398S1 | Samples |
| ADC3908S065IRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398S2 | Samples |
| ADC3908S065IRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398S2 | Samples |
| ADC3908S125IRSMR | ACTIVE | VQFN | RSM | 32 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398S3 | Samples |
| ADC3908S125IRSMT | ACTIVE | VQFN | RSM | 32 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 105 | AZ398S3 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

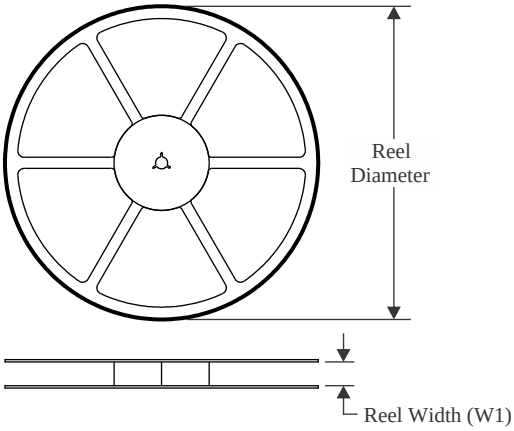
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

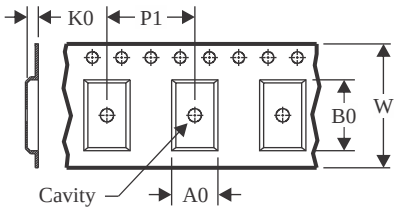
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

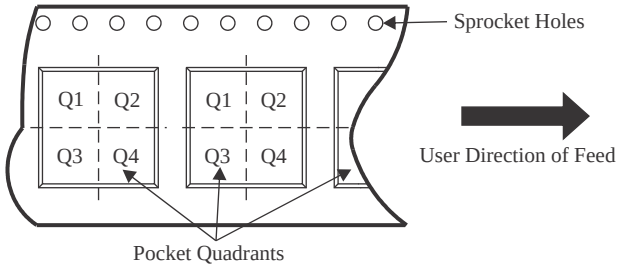



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

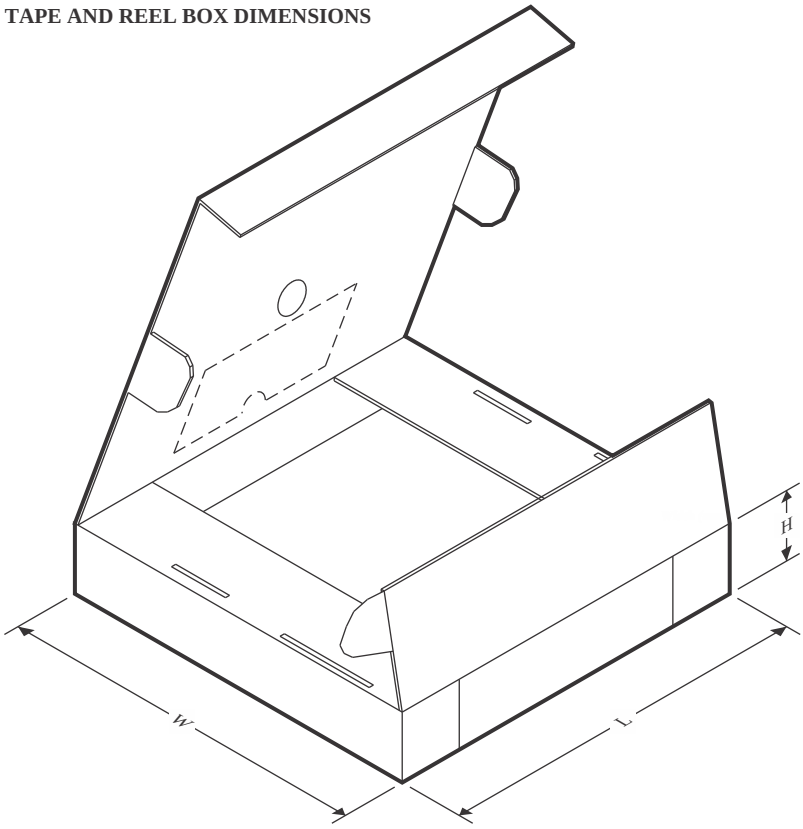
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC3908D025IRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908D025IRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908D065IRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908D065IRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908D125IRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908D125IRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908S025IRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908S025IRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908S065IRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908S065IRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908S125IRSMR | VQFN | RSM | 32 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |
| ADC3908S125IRSMT | VQFN | RSM | 32 | 250 | 180.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADC3908D025IRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| ADC3908D025IRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |
| ADC3908D065IRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| ADC3908D065IRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |
| ADC3908D125IRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| ADC3908D125IRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |
| ADC3908S025IRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| ADC3908S025IRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |
| ADC3908S065IRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| ADC3908S065IRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |
| ADC3908S125IRSMR | VQFN | RSM | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| ADC3908S125IRSMT | VQFN | RSM | 32 | 250 | 210.0 | 185.0 | 35.0 |

# GENERIC PACKAGE VIEW

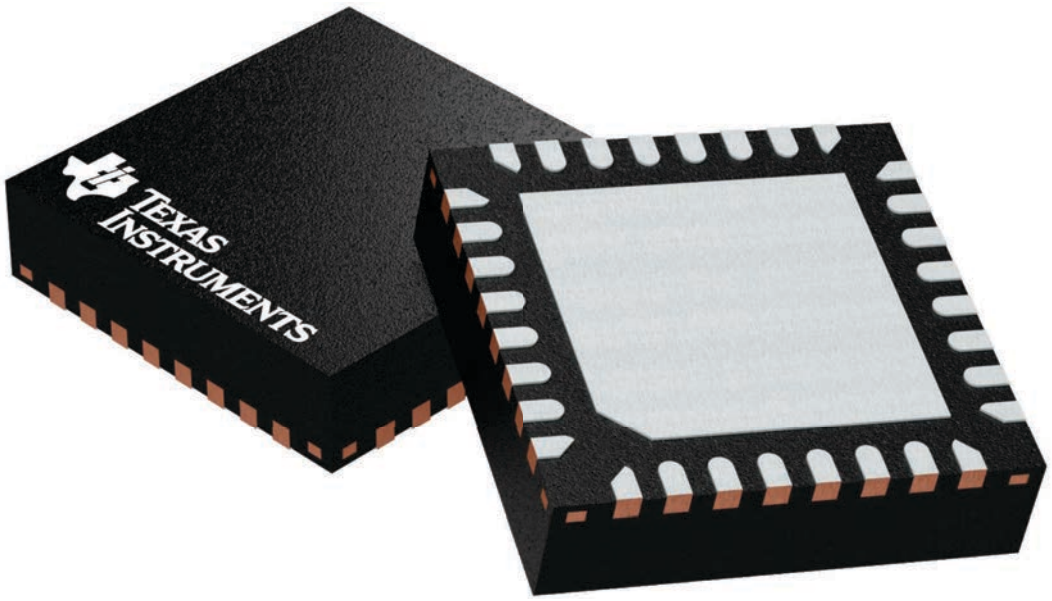
## RSM 32

## VQFN - 1 mm max height

**4 x 4, 0.4 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



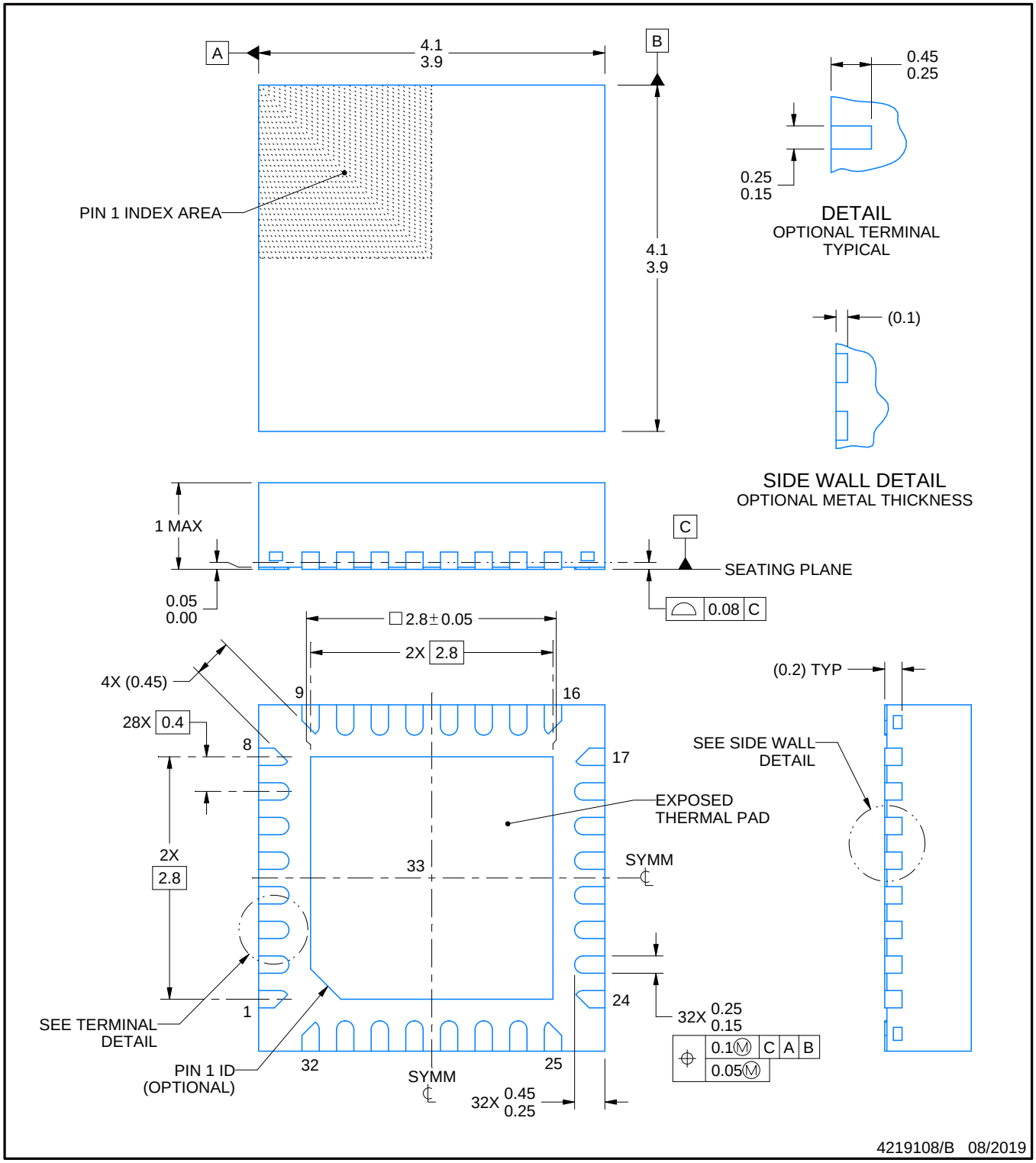

4224982/A

# PACKAGE OUTLINE

## RSM0032B

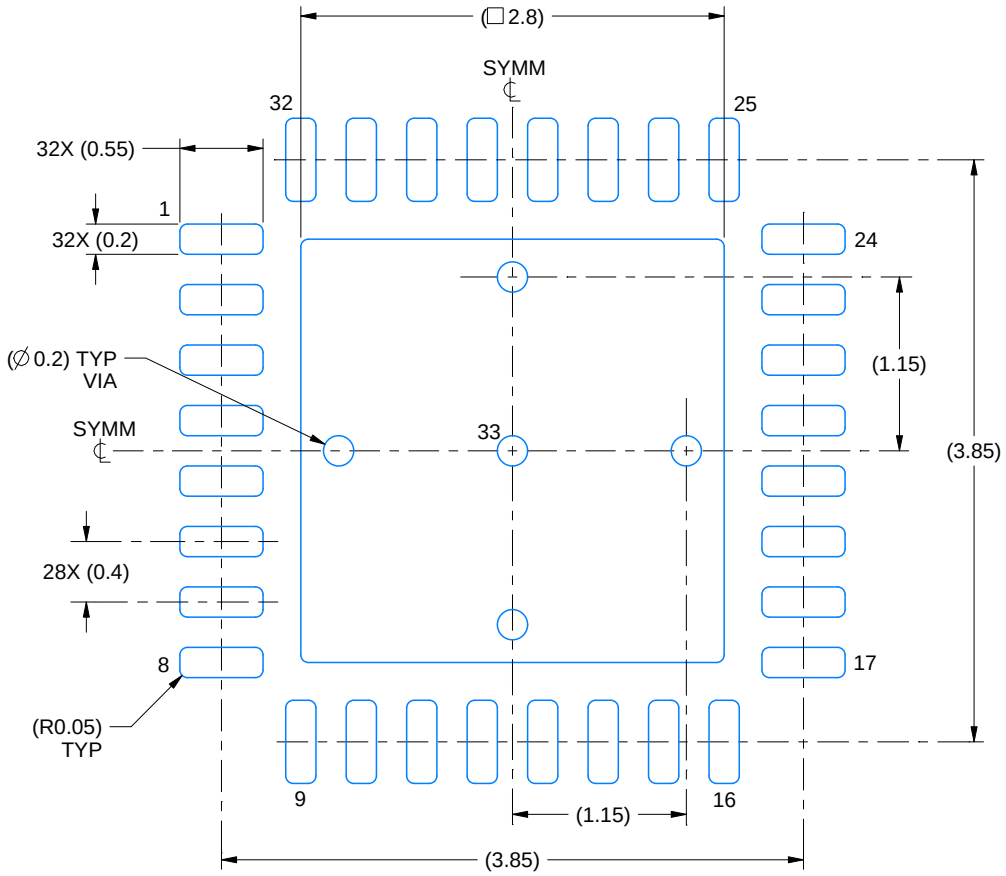
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

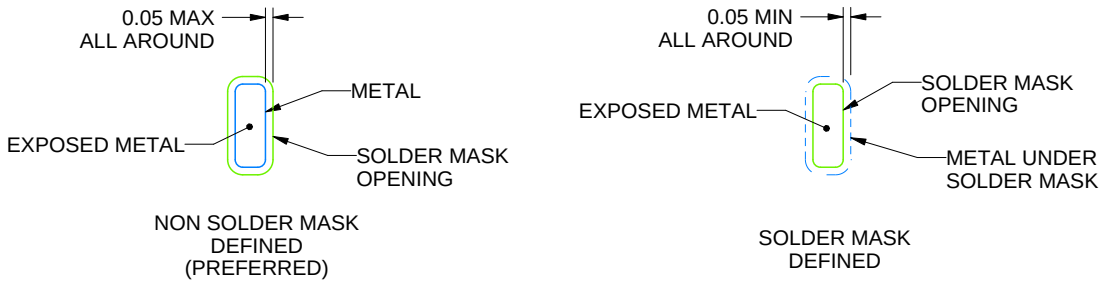



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

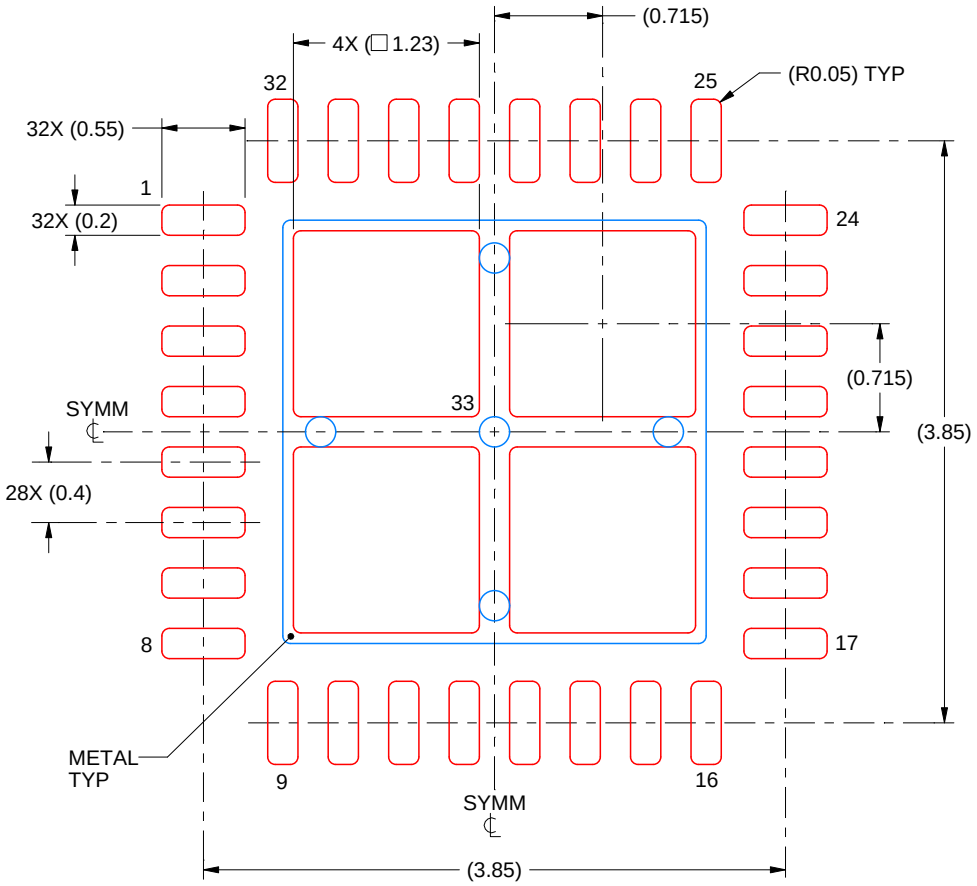



SOLDER MASK DETAILS

4219108/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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