500kHz, 12-Bit, 6-Channel Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **6 Simultaneous Sampling Channels**
- **Fully Differential Inputs**
- **2µs Total Throughput per Channel**
- **No Missing Codes**
- **Parallel Interface**
- **1MHz Effective Sampling Rate**
- **Low Power: 50mW**
- **6X FIFO**

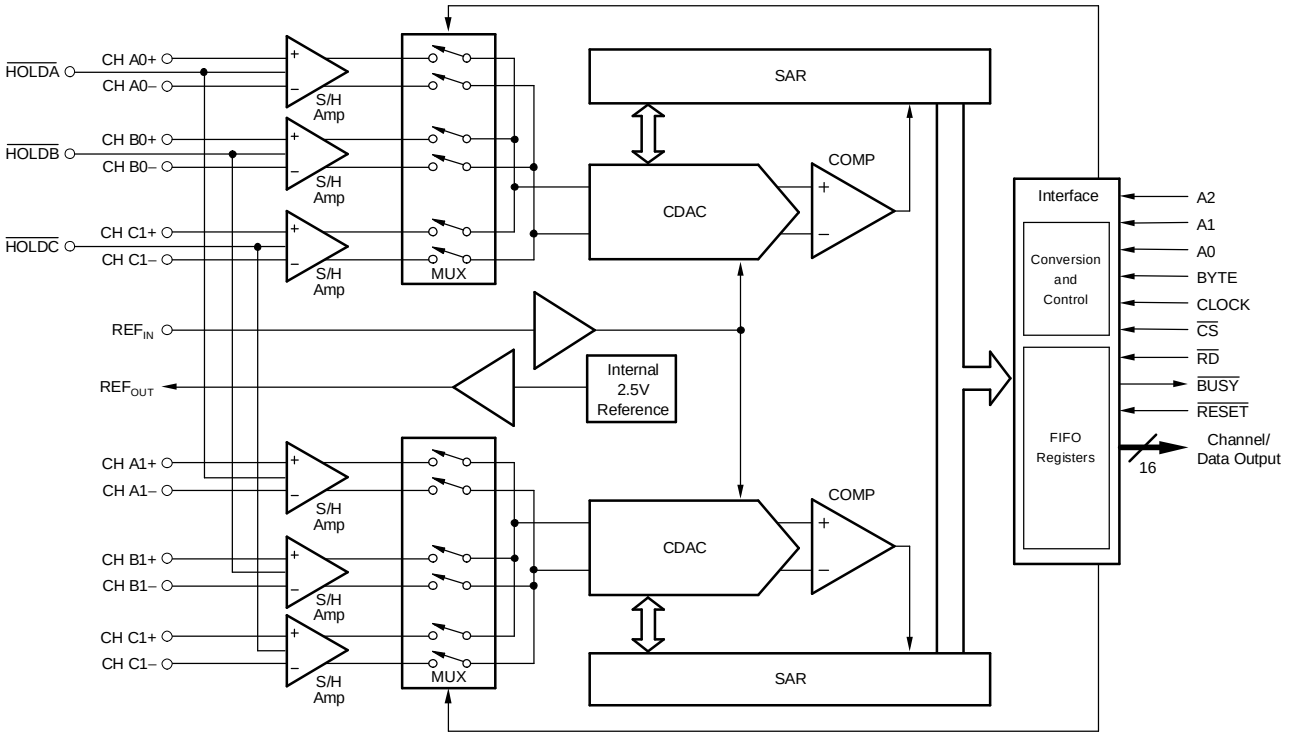
APPLICATIONS

- **Motor Control**
- **Multi-Axis Positioning Systems**
- **3-Phase Power Control**

DESCRIPTION

The ADS7864 is a dual 12-bit, 500kHz analog-to-digital (A/D) converter with 6 fully differential input channels grouped into three pairs for high speed simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differential to the input of the A/D converter. This provides excellent common-mode rejection of 80dB at 50kHz which is important in high noise environments.

The ADS7864 offers a parallel interface and control inputs to minimize software overhead. The output data for each channel is available as a 16-bit word (address and data). The ADS7864 is offered in a TQFP-48 package and is fully specified over the –40°C to +85°C operating range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (%)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7864Y	±2	±0.75	TQFP-48	PFB	–40°C to +85°C	ADS7864Y	Tape and Reel, 250
						ADS7864Y	Tape and Reel, 2000
ADS7864YB	±1	±0.5	TQFP-48	PFB	–40°C to +85°C	ADS7864YB	Tape and Reel, 250
						ADS7864YB	Tape and Reel, 2000

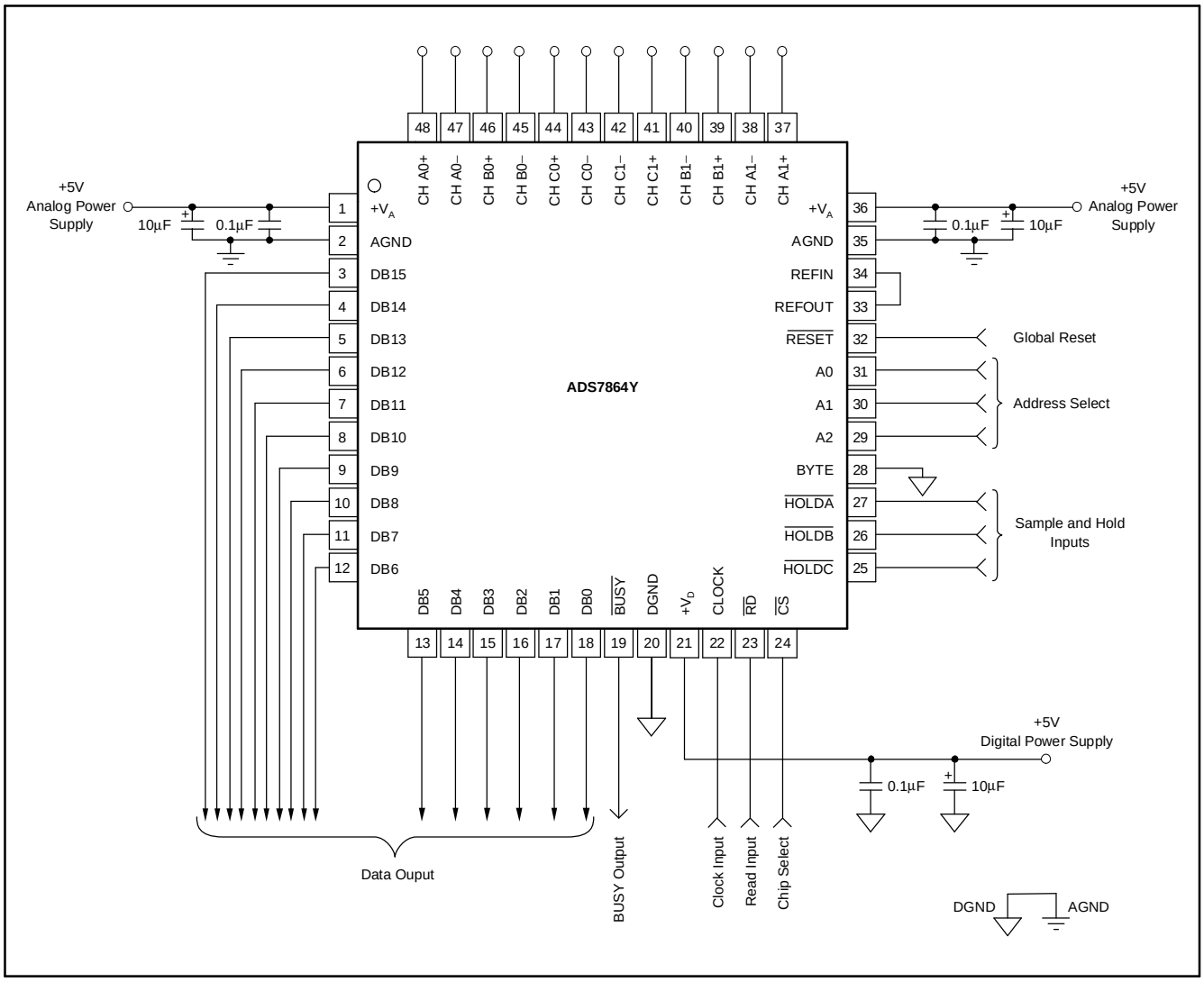
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

	ADS7864	UNIT
Analog Inputs to AGND: Any Channel Input	–0.3 to ($+V_D$ + 0.3)	V
Analog Inputs to AGND: REF_{IN}	–0.3 to ($+V_D$ + 0.3)	V
Digital Inputs to DGND	–0.3 to ($+V_D$ + 0.3)	V
Ground Voltage Differences: AGND, DGND	±0.3	V
Ground Voltage Differences: $+V_D$ to AGND	–0.3 to +6	V
Power Supply Difference: $+V_A$, $+V_D$	±0.3	V
Power Dissipation	325	mW
Maximum Junction Temperature	+150	°C
Operating Temperature Range	–40 to +85	°C
Storage Temperature Range	–65 to +150	°C
Lead Temperature (soldering, 10s)	+300	°C

BASIC OPERATION



ELECTRICAL CHARACTERISTICS

All specifications T_{MIN} to T_{MAX}, $+V_A = +V_D = +5V$, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz (unless otherwise noted).

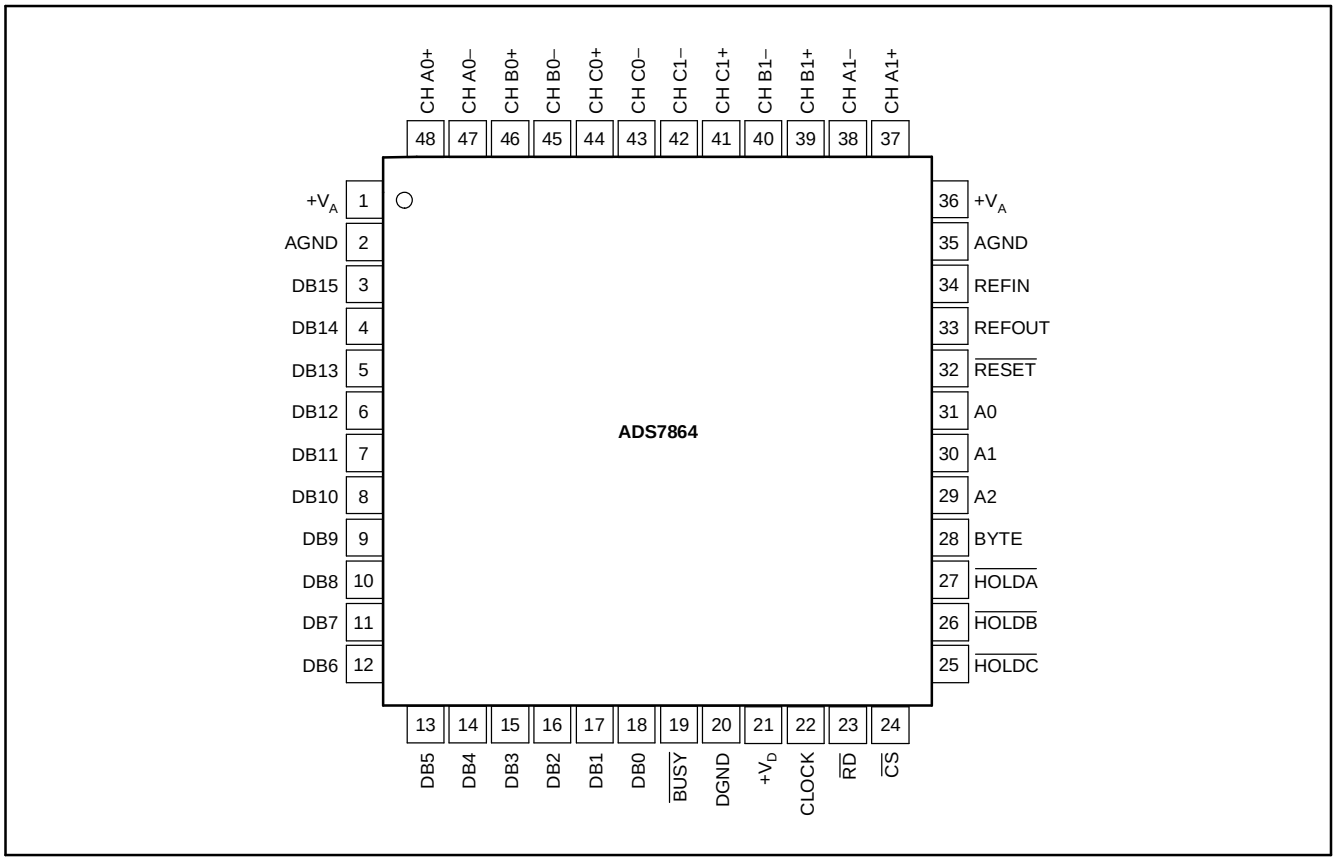
PARAMETER	TEST CONDITIONS	ADS7864Y			ADS7864YB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				12			12	Bits
Analog Input								
Input Voltage Range-Bipolar	V_{CENTER} = +2.5V	$-V_{REF}$		$+V_{REF}$	$-V_{REF}$		$+V_{REF}$	V
Absolute Input Range	+IN	–0.3		$+V_A$ + 0.3				V
	–IN	–0.3		$+V_A$ + 0.3				V
Input Capacitance			15			15		pF
Input Leakage Current	CLK = GND		±1			±1		µA
System Performance								
No Missing Codes		12			12			Bits
Integral Linearity			±0.75	2		±0.5	±1	LSB
Integral Linearity Match			0.5			0.5		LSB
Differential Linearity		–0.9	±0.6		–0.9	±0.4		LSB
Bipolar Offset Error	Referenced to REF_{IN}		±0.75	±4		±0.5	±3	LSB
Bipolar Offset Error Match				3			3	LSB
Positive Gain Error	Referenced to REF_{IN}		±0.15	±0.75		±0.1	±0.5	% of FSR
Positive Gain Error Match				3			3	LSB
Negative Gain Error	Referenced to REF_{IN}		±0.15	±0.75		±0.1	±0.5	% of FSR
Negative Gain Error Match				3			3	LSB
Common-Mode Rejection Ratio	At DC		84			84		dB
	V_{IN} = ±1.25V_{PP} at 50kHz		80			80		dB
Noise			120			120		μV_{RMS}
Power Supply Rejection Ratio			0.3	2		0.3	2	LSB
Sampling Dynamics								
Conversion Time per A/D			1.75			1.75		µs
Acquisition Time			0.25			0.25		µs
Throughput Rate		500			500			kHz
Aperture Delay			3.5			3.5		ns
Aperture Delay Matching			100			100		ps
Aperture Jitter			50			50		ps
Small-Signal Bandwidth			40			40		MHz
Dynamic Characteristics								
Total Harmonic Distortion	V_{IN} = ±2.5V_{PP} at 100kHz		–75			–75		dB
SINAD	V_{IN} = ±2.5V_{PP} at 100kHz		71			71		dB
Spurious Free Dynamic Range	V_{IN} = ±2.5V_{PP} at 100kHz		78			78		dB
Channel-to-Channel Isolation	V_{IN} = ±2.5V_{PP} at 50kHz		–76			–76		dB
Voltage Reference								
Internal Reference Voltage		2.475	2.5	2.525	2.475	2.5	2.525	V
Internal Drift			10			10		ppm/°C
Internal Noise			50			50		μV_{PP}
Internal Source Current			2			2		mA
Internal Load Rejection			0.005			0.005		mV/µA
Internal PSRR			80			80		dB
External Reference Voltage Range		1.2	2.5	2.6	1.2	2.5	2.6	V
Input Current				100			100	µA
Input Capacitance			5			5		pF

ELECTRICAL CHARACTERISTICS (continued)

All specifications T_{MIN} to T_{MAX}, $+V_A = +V_D = +5V$, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz (unless otherwise noted).

PARAMETER	TEST CONDITIONS	ADS7864Y			ADS7864YB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Digital Input/Output								
Logic Family			CMOS			CMOS		
Logic Levels:								
V_{IH}	I_{IH} = +5µA	3.0		$+V_D$ + 0.3	3.0		$+V_D$ + 0.3	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	–0.3		0.8	V
V_{OH}	I_{OH} = –500µA	3.5			3.5			V
V_{OL}	I_{OL} = –500µA			0.4			0.4	V
External Clock		0.2		8	0.2		8	MHz
Data Format			Binary Two's Complement			Binary Two's Complement		
Power-Supply Requirements								
Power Supply Voltage, $+V_A$, $+V_D$		4.75	5	5.25	4.75	5	5.25	V
Quiescent Current, $+V_A$, $+V_D$				10			10	mA
Power Dissipation				50			50	mW

PIN CONFIGURATIONS



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$+V_A$	Analog Power Supply. Normally +5V.
2	AGND	Analog Ground
3	DB15	Data Valid Output: '1' for data valid; '0' for invalid data.
4	DB14	Channel Address Output Pin (see Table 2)
5	DB13	Channel Address Output Pin (see Table 2)
6	DB12	Channel Address Output Pin (see Table 2)
7	DB11	Data Bit 11 - MSB
8	DB10	Data Bit 10
9	DB9	Data Bit 9
10	DB8	Data Bit 8
11	DB7	Data Bit 7
12	DB6	Data Bit 6
13	DB5	Data Bit 5
14	DB4	Data Bit 4
15	DB3	Data Bit 3
16	DB2	Data Bit 2
17	DB1	Data Bit 1
18	DB0	Data Bit 0 - LSB
19	$\overline{BUSY}$	Low when a conversion is in progress.
20	DGND	Digital Ground
21	$+V_D$	Digital Power Supply, +5VDC
22	CLOCK	An external clock must be applied to the CLOCK input.
23	$\overline{RD}$	RD Input. Enables the parallel output when used in conjunction with chip select.
24	$\overline{CS}$	Chip Select
25	$\overline{HOLDC}$	Places Channels C0 and C1 in hold mode.
26	$\overline{HOLDB}$	Places Channels B0 and B1 in hold mode.
27	$\overline{HOLDA}$	Places Channels A0 and A1 in hold mode.
28	BYTE	2 × 8 Output Capability. Active high.
29	A2	A2 Address/Mode Select Pin (see Table 3).
30	A1	A1 Address/Mode Select Pin (see Table 3).
31	A0	A0 Address/Mode Select Pin (see Table 3).
32	$\overline{RESET}$	Reset Pin
33	REFOUT	Reference Out
34	REFIN	Reference In
35	AGND	Analog Ground
36	$+V_A$	Analog Power Supply. Normally +5V.
37	CH A1+	Noninverting Input Channel A1
38	CH A1–	Inverting Input Channel A1
39	CH B1+	Noninverting Input Channel B1
40	CH B1–	Inverting Input Channel B1
41	CH C1+	Noninverting Input Channel C1
42	CH C1–	Inverting Input Channel C1
43	CH C0–	Inverting Input Channel C0
44	CH C0+	Noninverting Input Channel C0
45	CH B0–	Inverting Input Channel B0
46	CH B0+	Noninverting Input Channel B0
47	CH A0–	Inverting Input Channel A0
48	CH A0+	Noninverting Input Channel A0

TYPICAL CHARACTERISTICS

All specifications T_A = +25°C, $+V_A$ = $+V_D$ = +5V, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz (unless otherwise noted)

FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 99.9kHz, –0.2dB)

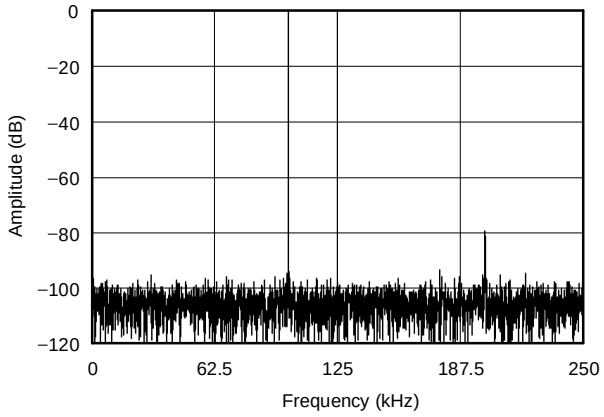


Figure 1.

FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 199.9kHz, -0.2dB)

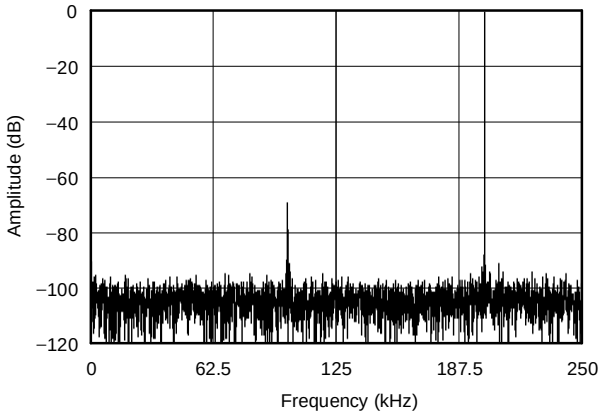


Figure 2.

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-(NOISE+DISTORTION) vs INPUT FREQUENCY

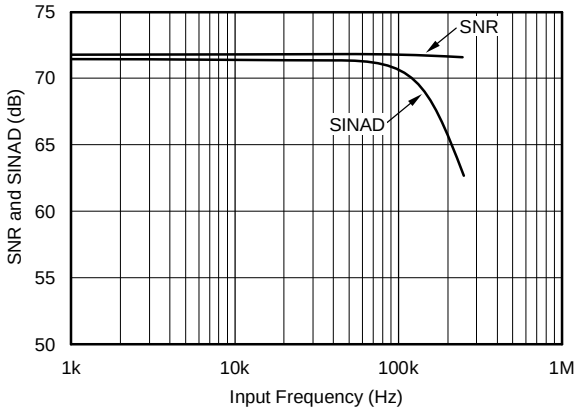


Figure 3.

CHANGE IN SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-(NOISE+DISTORTION) vs TEMPERATURE

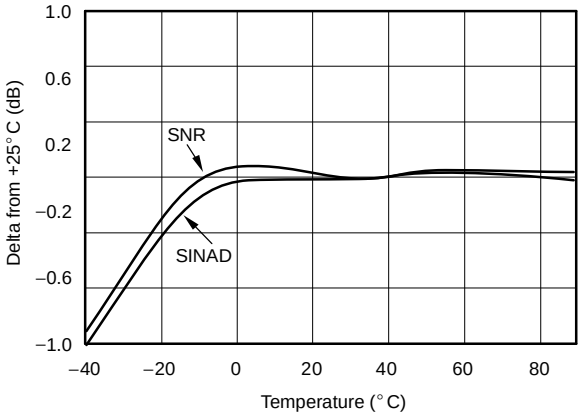


Figure 4.

TYPICAL CHARACTERISTICS (continued)

All specifications T_A = +25°C, $+V_A$ = $+V_D$ = +5V, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz (unless otherwise noted)

CHANGE IN SPURIOUS FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs TEMPERATURE

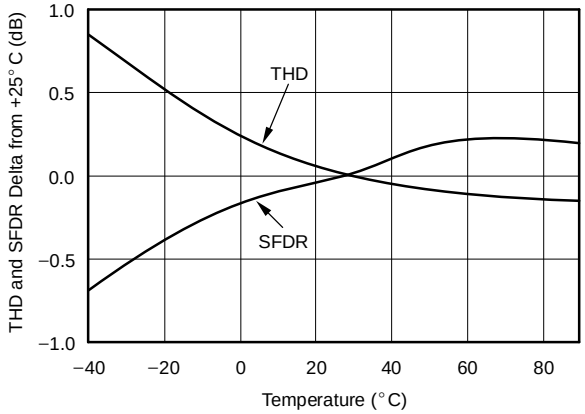


Figure 5.

POSITIVE GAIN MATCH vs TEMPERATURE (Maximum Deviation for All Six Channels)

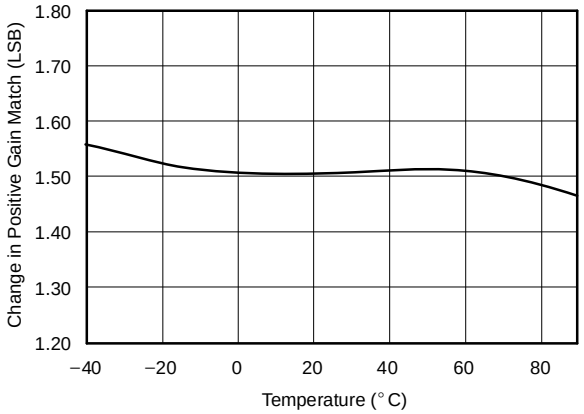


Figure 6.

NEGATIVE GAIN MATCH vs TEMPERATURE (Maximum Deviation for All Six Channels)

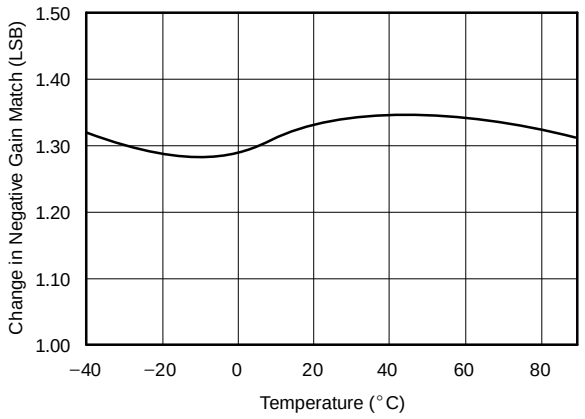


Figure 7.

REFERENCE VOLTAGE vs TEMPERATURE

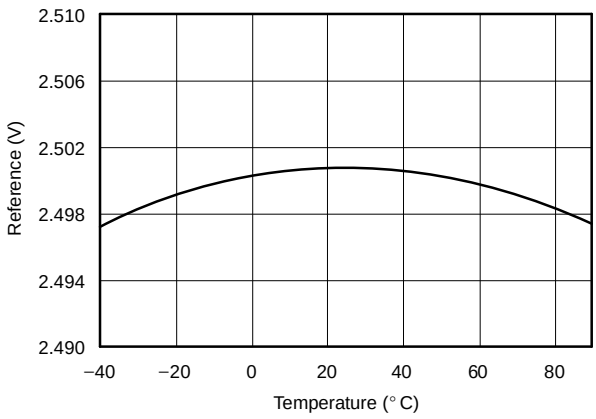


Figure 8.

BIPOLAR ZERO vs TEMPERATURE

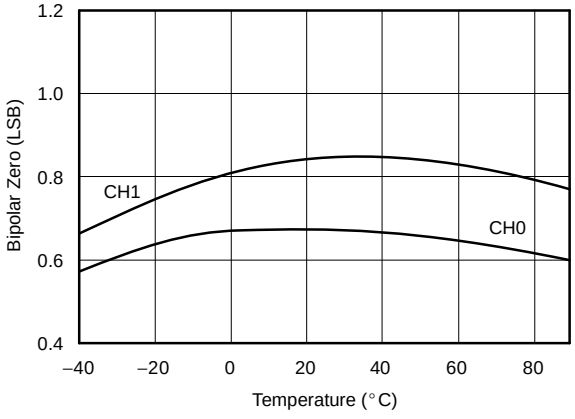


Figure 9.

BIPOLAR ZERO MATCH vs TEMPERATURE

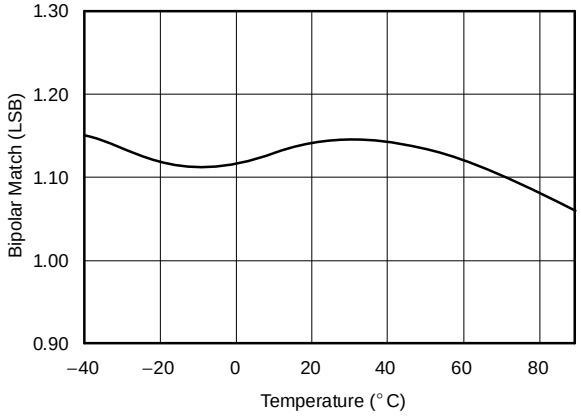


Figure 10.

TYPICAL CHARACTERISTICS (continued)

All specifications T_A = +25°C, $+V_A$ = $+V_D$ = +5V, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz (unless otherwise noted)

DIFFERENTIAL LINEARITY ERROR vs CODE

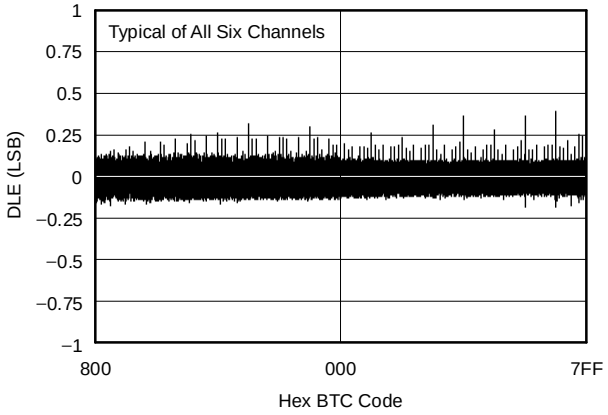


Figure 11.

INTEGRAL LINEARITY ERROR vs CODE

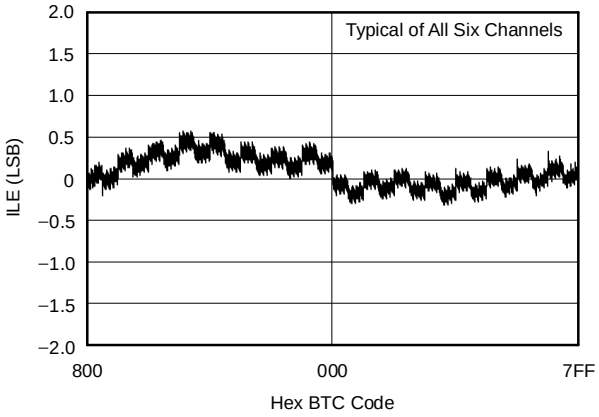


Figure 12.

INTEGRAL LINEARITY ERROR MATCH vs TEMPERATURE Channel A0/Channel C1 (Different Converter, Different Channels)

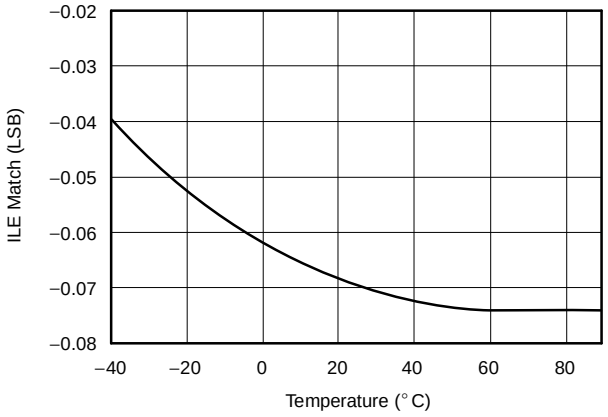


Figure 13.

INTEGRAL LINEARITY ERROR vs TEMPERATURE

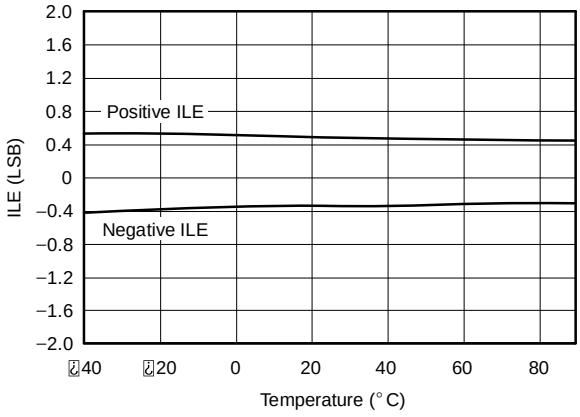


Figure 14.

TYPICAL CHARACTERISTICS (continued)

All specifications T_A = +25°C, $+V_A$ = $+V_D$ = +5V, V_{REF} = internal +2.5V and f_{CLK} = 8MHz, f_{SAMPLE} = 500kHz (unless otherwise noted)

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

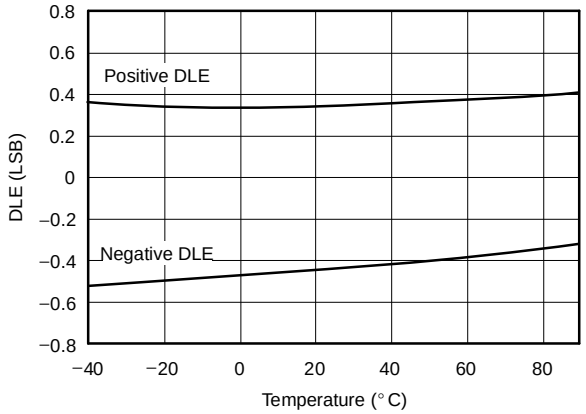


Figure 15.

INTEGRAL LINEARITY ERROR MATCH vs CODE Channel A0/Channel B0 (Same Converter, Different Channels)

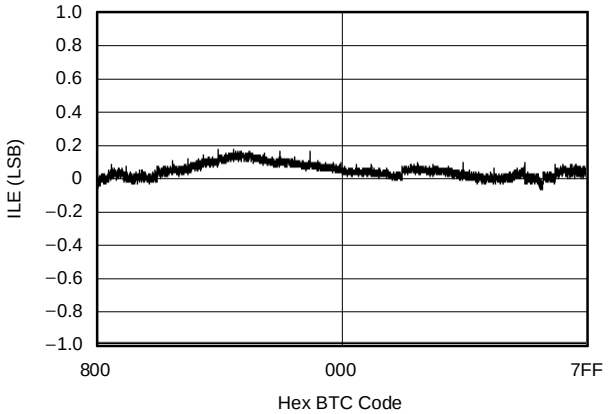


Figure 16.

INTEGRAL LINEARITY ERROR MATCH vs CODE Channel A0/Channel B1 (Different Converter, Different Channels)

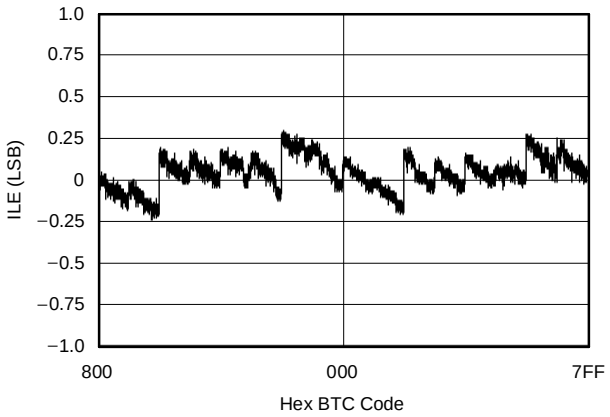


Figure 17.

CHANNEL SEPARATION

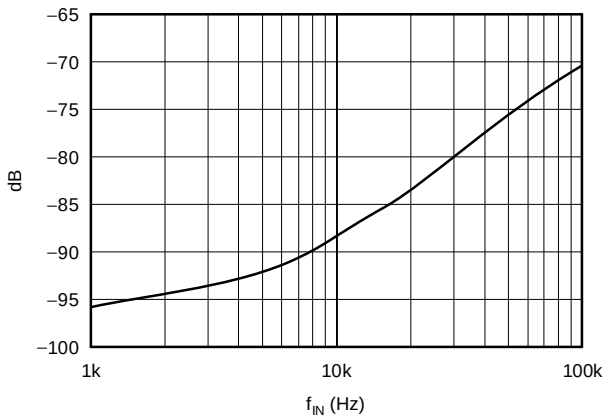


Figure 18.

APPLICATIONS INFORMATION

INTRODUCTION

The ADS7864 is a high speed, low power, dual 12-bit analog-to-digital converter (ADC) that operates from a single +5V supply. The input channels are fully differential with a typical common-mode rejection of 80dB. The part contains dual 2µs successive approximation ADCs, six differential sample-and-hold amplifiers, an internal +2.5V reference with REF_{IN} and REF_{OUT} pins and a high speed parallel interface. There are six analog inputs that are grouped into three channels (A, B and C). Each A/D converter has three inputs (A0/A1, B0/B1 and C0/C1) that can be sampled and converted simultaneously, thus preserving the relative phase information of the signals on both analog inputs. Each pair of channels has a hold signal ($\overline{HOLDA}$, $\overline{HOLDB}$, $\overline{HOLDC}$) to allow simultaneous sampling on all six channels. The part accepts an analog input voltage in the range of $-V_{REF}$ to $+V_{REF}$, centered around the internal +2.5V reference. The part will also accept bipolar input ranges when a level shift circuit is used at the front end (see Figure 25).

A conversion is initiated on the ADS7864 by bringing the $\overline{HOLDX}$ pin low for a minimum of 15ns. $\overline{HOLDX}$ low places both sample-and-hold amplifiers of the X channels in the hold state simultaneously and the conversion process is started on both channels. The $\overline{BUSY}$ output will then go low and remain low for the duration of the conversion cycle. The data can be read from the parallel output bus following the conversion by bringing both $\overline{RD}$ and $\overline{CS}$ low.

Conversion time for the ADS7864 is 1.75µs when an 8MHz external clock is used. The corresponding acquisition time is 0.25µs. To achieve maximum output rate (500kHz), the read function can be performed during at the start of the next conversion.

NOTE: This mode of operation is described in more detail in the *Timing and Control* section of this data sheet.

SAMPLE-AND-HOLD SECTION

The sample-and-hold amplifiers on the ADS7864 allow the ADCs to accurately convert an input sine wave of full-scale amplitude to 12-bit accuracy. The input bandwidth of the sample-and-hold is greater than the Nyquist rate of the ADC (Nyquist equals one-half of the sampling rate) even when the ADC is operated at its maximum throughput rate of 500kHz. The typical small-signal bandwidth of the sample-and-hold amplifiers is 40MHz.

Typical aperture delay time, or the time it takes for the ADS7864 to switch from the sample to the hold mode following the negative edge of the $\overline{HOLDX}$ signal, is 5ns. The average delta of repeated aperture delay values is typically 50ps (also known as aperture jitter). These specifications reflect the ability of the ADS7864 to capture AC input signals accurately at the exact same moment in time.

REFERENCE

Under normal operation, the REF_{OUT} pin (pin 2) should be directly connected to the REF_{IN} pin (pin 1) to provide an internal +2.5V reference to the ADS7864. The ADS7864 can operate, however, with an external reference in the range of 1.2V to 2.6V for a corresponding full-scale range of 2.4V to 5.2V.

The internal reference of the ADS7864 is double-buffered. If the internal reference is used to drive an external load, a buffer is provided between the reference and the load applied to pin 33 (the internal reference can typically source 2mA of current—load capacitance should not exceed 100pF). If an external reference is used, the second buffer provides isolation between the external reference and the CDAC. This buffer is also used to recharge all of the capacitors of both CDACs during conversion.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS7864: single-ended or differential (see Figure 19 and Figure 20). When the input is single-ended, the –IN input is held at the common-mode voltage. The +IN input swings around the same common voltage and the peak-to-peak amplitude is the (common-mode $+V_{REF}$) and the (common-mode $-V_{REF}$). The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 21).

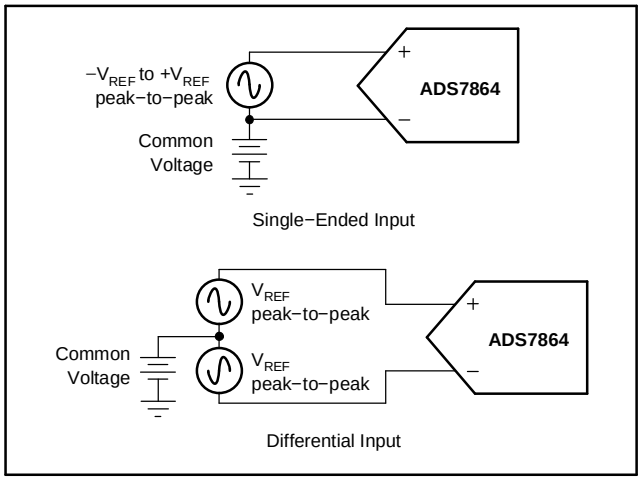
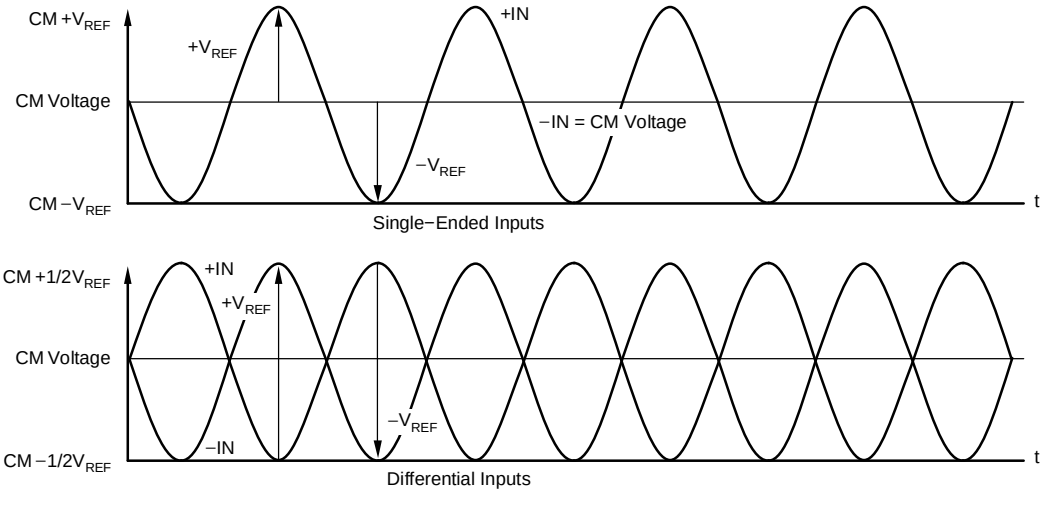


Figure 19. Methods of Driving the ADS7864 Single-Ended or Differential



NOTES: Common−Mode Voltage (Differential Mode) = $\frac{(IN+) - (IN-)}{2}$, Common−Mode Voltage (Single−Ended Mode) = IN−.

The maximum differential voltage between +IN and −IN of the ADS7864 is V_{REF}. See Figures 21 and 22 for a further explanation of the common voltage range for single−ended and differential inputs.

Figure 20. Using the ADS7864 in the Single-Ended and Differential Input Modes

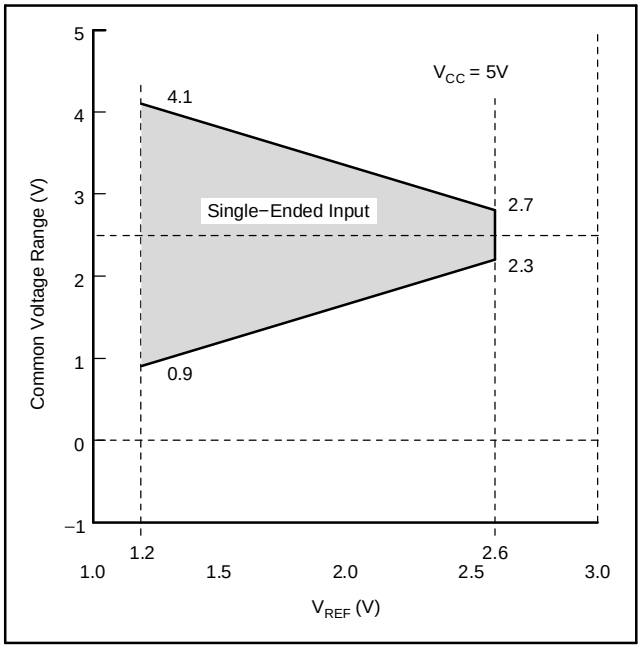


Figure 21. Single-Ended Input: Common-Mode Voltage Range vs V_{REF}

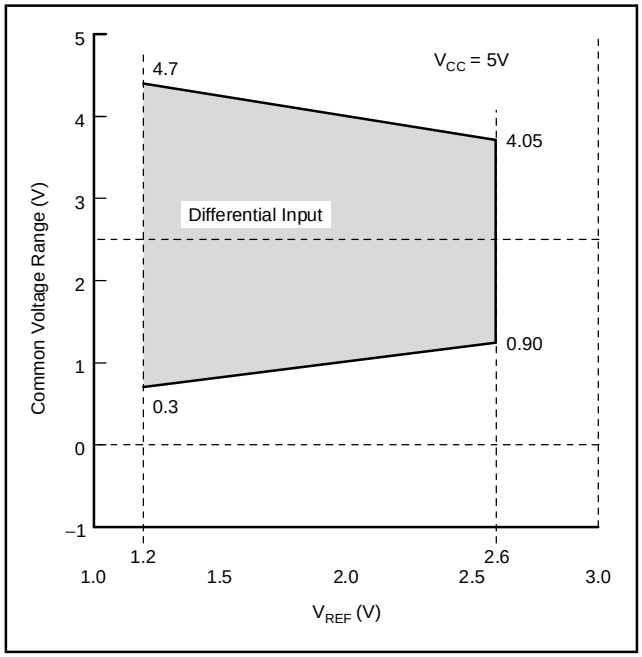


Figure 22. Differential Input: Common-Mode Voltage Range vs V_{REF}

When the input is differential, the amplitude of the input is the difference between the +IN and –IN input, or: (+IN) – (–IN). The peak-to-peak amplitude of each input is $\pm 1/2V_{REF}$ around this common voltage. However, since the inputs are 180° out of phase, the peak-to-peak amplitude of the differential voltage is $+V_{REF}$ to $-V_{REF}$. The value of V_{REF} also determines the range of the voltage that may be common to both inputs (see Figure 22).

In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Otherwise, this may result in offset error, which will change with both temperature and input voltage.

The input current on the analog inputs depend on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS7864 charges the internal capacitor array during the sampling period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (15pF) to a 12-bit settling level within two clock cycles. When the converter goes into the hold mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +IN and –IN inputs should always remain within the range of GND – 300mV to V_{DD} + 300mV.

TRANSITION NOISE

Figure 23 shows a histogram plot for the ADS7864 following 8,000 conversions of a DC input. The DC input was set at output code 2046. All but one of the conversions had an output code result of 2046 (one of the conversions resulted in an output of 2047). The histogram reveals the excellent noise performance of the ADS7864.

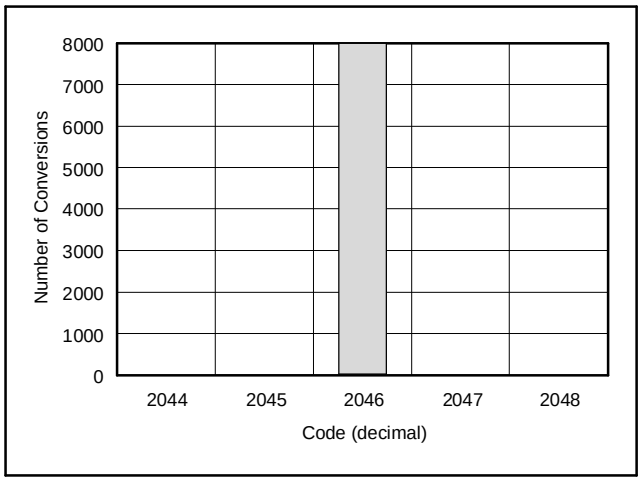


Figure 23. Histogram of 8,000 Conversions of a DC Input

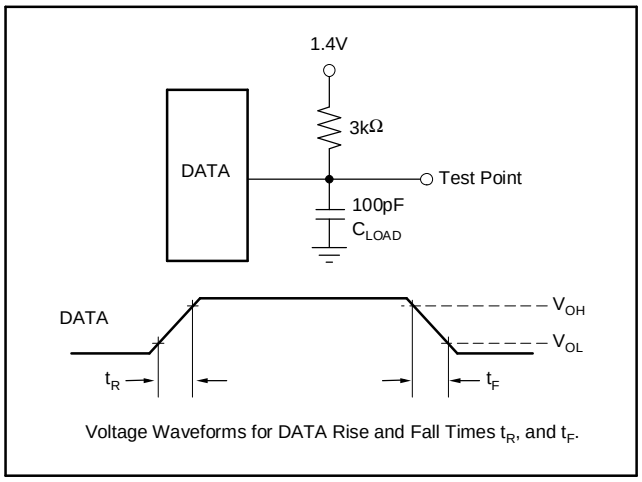
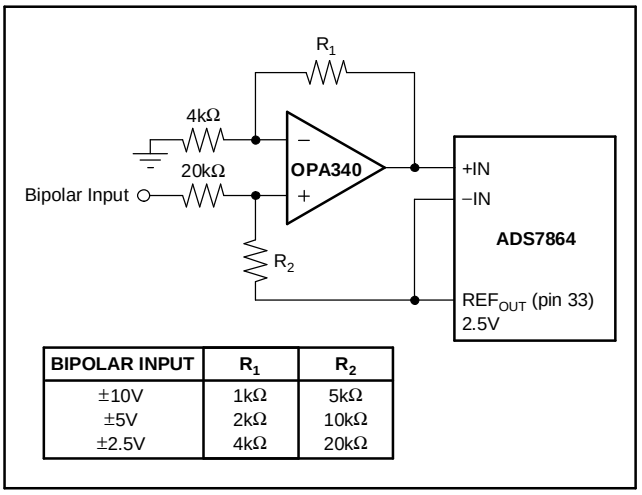


Figure 24. Test Circuits for Timing Specifications

BIPOLAR INPUTS

The differential inputs of the ADS7864 were designed to accept bipolar inputs ($-V_{REF}$ and $+V_{REF}$) around the internal reference voltage (2.5V), which corresponds to a 0V to 5V input range with a 2.5V reference. By using a simple op amp circuit featuring a single amplifier and four external resistors, the ADS7864 can be configured to accept bipolar inputs. The conventional ±2.5V, ±5V, and ±10V input ranges can be interfaced to the ADS7864 using the resistor values shown in Figure 25.



BIPOLAR INPUT	R_1	R_2
±10V	1kΩ	5kΩ
±5V	2kΩ	10kΩ
±2.5V	4kΩ	20kΩ

Figure 25. Level Shift Circuit for Bipolar Input Ranges

TIMING AND CONTROL

The ADS7864 uses an external clock (CLOCK, pin 22) which controls the conversion rate of the CDAC. With an 8MHz external clock, the A/D sampling rate is 500kHz which corresponds to a 2µs maximum throughput time.

THEORY OF OPERATION

The ADS7864 contains two 12-bit A/D converters that operate simultaneously. The three hold signals ($\overline{HOLDA}$, $\overline{HOLDB}$, $\overline{HOLDC}$) select the input MUX and initiate the conversion. A simultaneous hold on all six channels can occur with all three hold signals strobed together. The converted values are saved in six registers. For each read operation the ADS7864 outputs 16 bits of information (12 Data, 3 Channel Address and Data Valid). The Address/Mode signals (A0, A1, A2) select how the data is read from the ADS7864. These Address/Mode signals can define a selection of a single channel, a cycle mode that cycles through all channels or a FIFO mode that sequences the data determined by the order of the Hold signals. The FIFO mode will allow the six registers to be used by a single channel pair, and therefore three locations for CH X0 and three locations for CH X1 can be acquired before they are read from the part.

EXPLANATION OF CLOCK, $\overline{RESET}$ AND $\overline{BUSY}$ PINS

CLOCK—An external clock has to be provided for the ADS7864. The maximum clock frequency is 8MHz. The minimum clock cycle is 125ns (see Figure 26, t_5), and the clock has to remain high (see Figure 26, t_6) or low (see Figure 26, t_7) for at least 40ns.

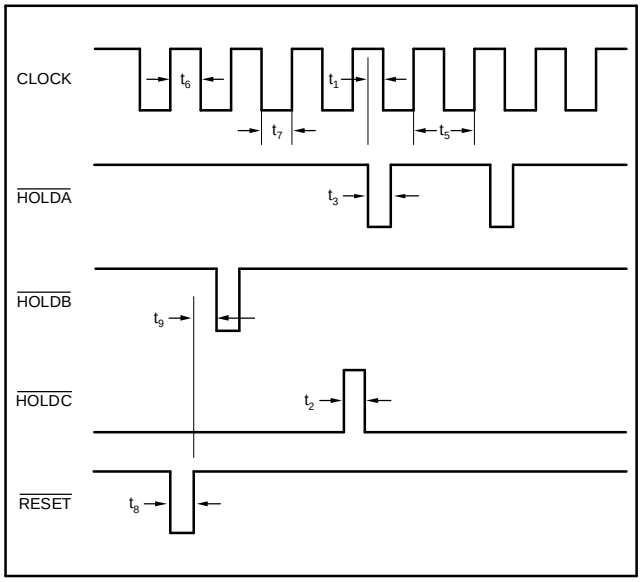


Figure 26. Start of the Conversion

$\overline{RESET}$—Bringing reset low will reset the ADS7864. It will clear all the output registers, stop any actual conversions and will close the sampling switches. Reset has to stay low for at least 20ns (see Figure 26, t_8). The reset should be back high for at least 20ns (see Figure 26, t_9), before starting the next conversion (negative hold edge).

$\overline{BUSY}$—Busy goes low when the internal A/D converters start a new conversion. It stays low as long as the conversion is in progress (see Figure 27, 13 clock-cycles, t_{10}) and rises again after the data is latched to the output register. With Busy going high, the new data can be read. It takes at least 16 clock cycles (see Figure 27, t_{11}) to complete conversion.

START OF A CONVERSION

By bringing one or all of the $\overline{HOLDX}$ signals low, the input data of the corresponding channel X is immediately placed in the hold mode (5ns). The conversion of this channel X follows as soon as the A/D converter is available for the particular channel. If

other channels are already in the hold mode but not converted, then the conversion of channel X is put in the queue until the previous conversion has been completed. If more than one channel goes into hold mode within one clock cycle, then channel A will be converted first if $\overline{HOLDA}$ is one of the triggered hold signals. Next, channel B will be converted, and last, channel C. If it is important to detect a hold command during a certain clock cycle, then the falling edge of the hold signal has to occur at least 10ns before the falling edge of the clock. (see Figure 26, t_1). The hold signal can remain low without initiating a new conversion. The hold signal has to be high for at least 15ns (see Figure 26, t_2) before it is brought low again and hold has to stay low for at least 20ns (see Figure 26, t_3).

In the example of Figure 26, the signal $\overline{HOLDB}$ goes low first and channel B0 and B1 will be converted first. The falling edges of $\overline{HOLDA}$ and $\overline{HOLDC}$ occur within the same clock cycle. Therefore, the channels A0 and A1 will be converted as soon as the channels B0 and B1 are finished (plus acquisition time). When the A-channels are finished, the C-channels will be converted. The second $\overline{HOLDA}$ signal is ignored, as the A-channels are not converted at this point in time.

Once a particular hold signal goes low, further impulses of this hold signal are ignored until the conversion is finished or the part is reset. When the conversion is finished ($\overline{BUSY}$ signal goes high), the sampling switches will close and sample the selected channel. The start of the next conversion must be delayed to allow the input capacitor of the ADS7864 to be fully charged. This delay time depends on the driving amplifier, but should be at least 175ns (see Figure 27, t_4).

The ADS7864 can also convert one channel continuously, as it is shown in Figure 27 with channel B. Therefore, $\overline{HOLDA}$ and $\overline{HOLDC}$ are kept high all the time. To gain acquisition time, the falling edge of $\overline{HOLDB}$ takes place just before the falling edge of clock. One conversion requires 16 clock cycles. Here, data is read after the next conversion is initiated by $\overline{HOLDB}$. To read data from channel B, A1 is set high and A2 is low. As A0 is low during the first reading (A2 A1 A0 = 010) data B0 is put to the output. Before the second $\overline{RD}$, A0 switches high (A2 A1 A0 = 011) so data from channel B1 is read.

Table 1. Timing Specifications

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	$\overline{HOLD}$ (A, B, C) before falling edge of clock	10			ns
t_2	$\overline{HOLD}$ high time to be recognized again	15			ns
t_3	$\overline{HOLD}$ low time	20			ns
t_4	Input capacitor charge time	175			ns
t_5	Clock period	125			ns
t_6	Clock high time	40			ns
t_7	Clock low time	40			ns
t_8	Reset pulse width	20			ns
t_9	First hold after reset	20			ns
t_{10}	Conversion time		$12.5 \times t_5$		ns
t_{11}	Successive conversion time ($16 \times t_5$)	2			µs
t_{12}	Address setup before $\overline{RD}$	10			ns
t_{13}	$\overline{CS}$ before end of $\overline{RD}$	30			ns
t_{14}	$\overline{RD}$ high time	30			ns

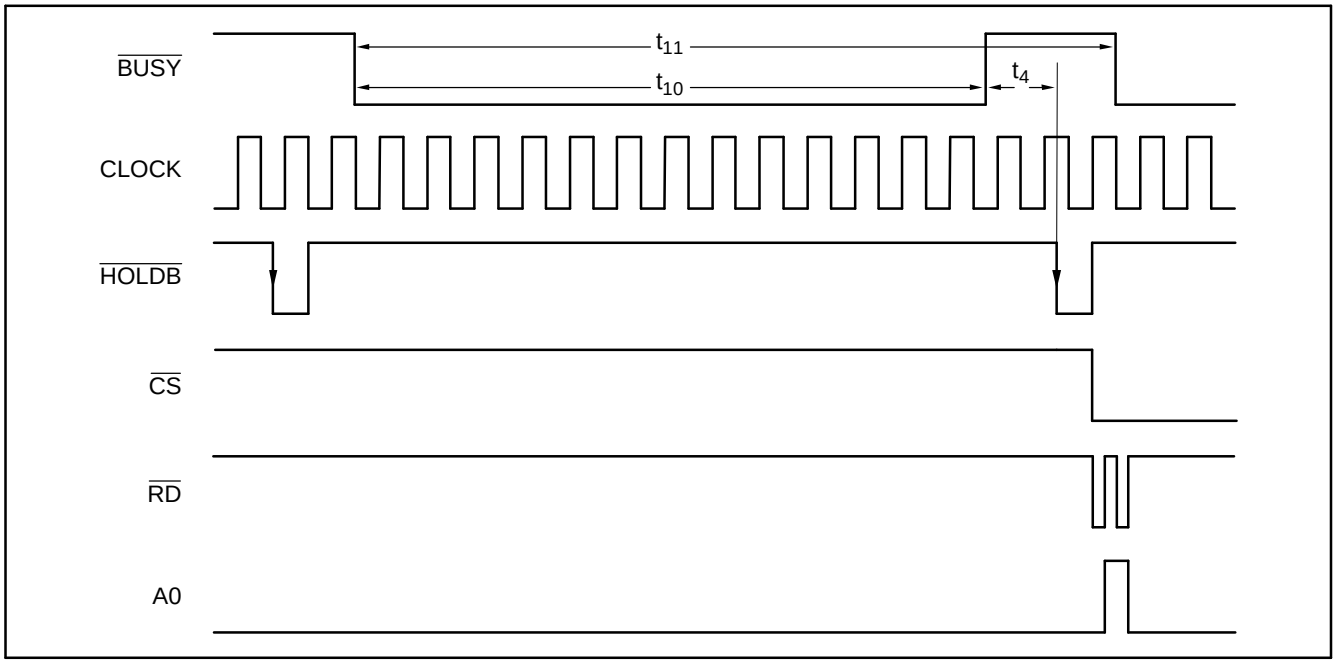


Figure 27. Timing of One Conversion Cycle

READING DATA ($\overline{RD}$, $\overline{CS}$)—In general, the channel/data outputs are in tristate. Both $\overline{CS}$ and $\overline{RD}$ have to be low to enable these outputs. $\overline{RD}$ and $\overline{CS}$ have to stay low together for at least 30ns (see Figure 28, t_{13}) before the output data is valid. $\overline{RD}$ has to remain high for at least 30ns (see Figure 28, t_{14}) before bringing it back low for a subsequent read command.

12.5 clock-cycles after the start of a conversion ($\overline{BUSY}$ going low), the new data is latched into its output register. If a read process is initiated around 12.5 clock cycles after $\overline{BUSY}$ went low, $\overline{RD}$ and $\overline{CS}$ should stay low for at least 50ns to get the new data stored to its register and switched to the output.

$\overline{CS}$ being low tells the ADS7864 that the bus on the board is assigned to the ADS7864. If an A/D converter shares a bus with digital gates, there is a possibility that digital (high frequency) noise may be coupled into the A/D converter. If the bus is just used by the ADS7864, $\overline{CS}$ can be hardwired to ground. Reading data at the falling edge of one of the hold signals might cause distortion of the hold value.

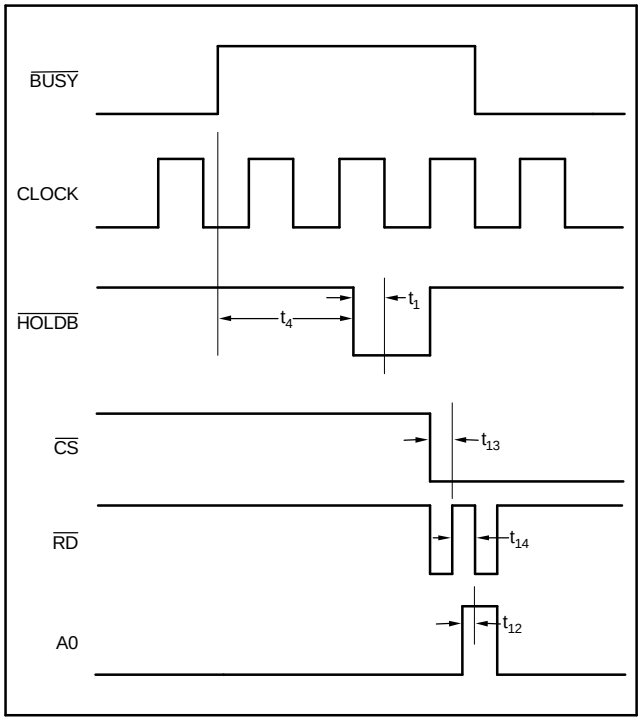


Figure 28. Timing for Reading Data

OUTPUT CODE (DB15…DB0)

The ADS7864 has a 16-bit output word. DB15 is '1' if the output contains valid data. This is important for the FIFO mode. Valid Data can be read until DB15 switches to 0. DB14, DB13 and DB12 store channel information as indicated in Table 2 (Channel Truth Table). The 12-bit output data is stored from DB11 (MSB) to DB0 (LSB).

BYTE—If there is only an 8-bit bus available on a board, then Byte can be set high (see Figure 29 and Figure 30). In this case, the lower eight bits can be read at the output pins DB7 to DB0 at the first $\overline{RD}$ signal, and the higher bits after the second $\overline{RD}$ signal.

Table 2. Channel Truth Table

DATA CHANNEL	DB14	DB13	DB12
A0	0	0	0
A1	0	0	1
B0	0	1	0
B1	0	1	1
C0	1	0	0
C1	1	0	1

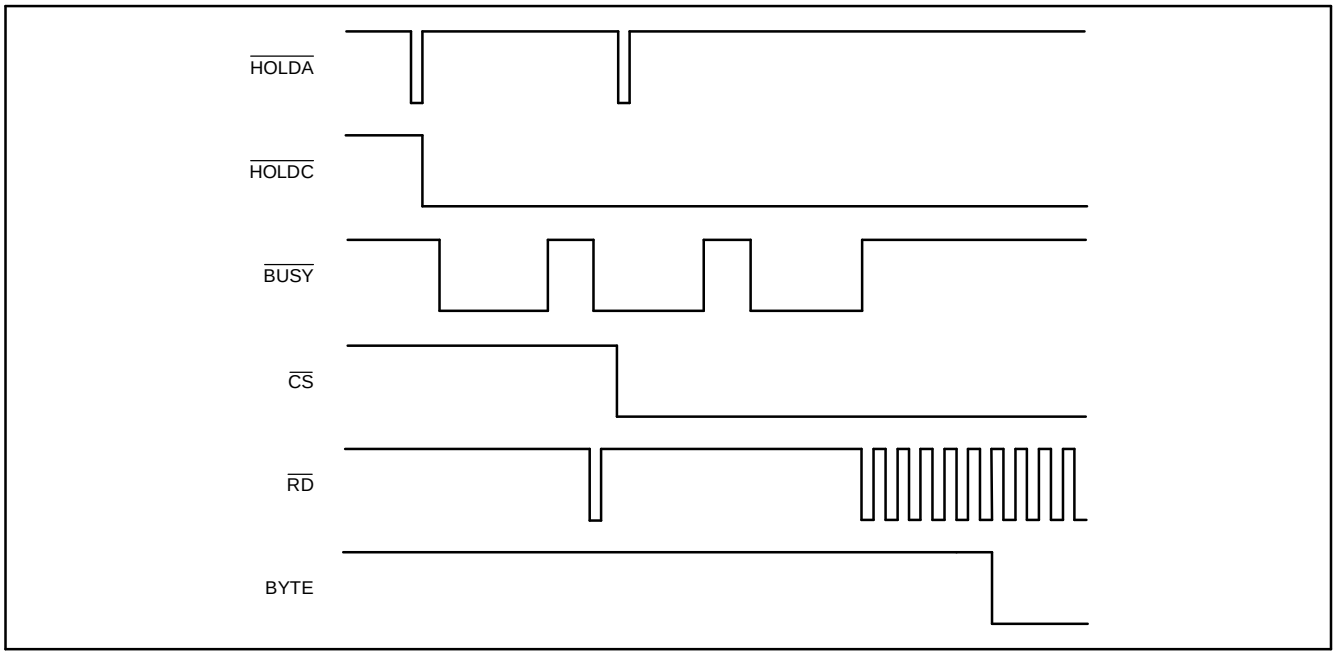


Figure 29. Reading Data in Cycling Mode

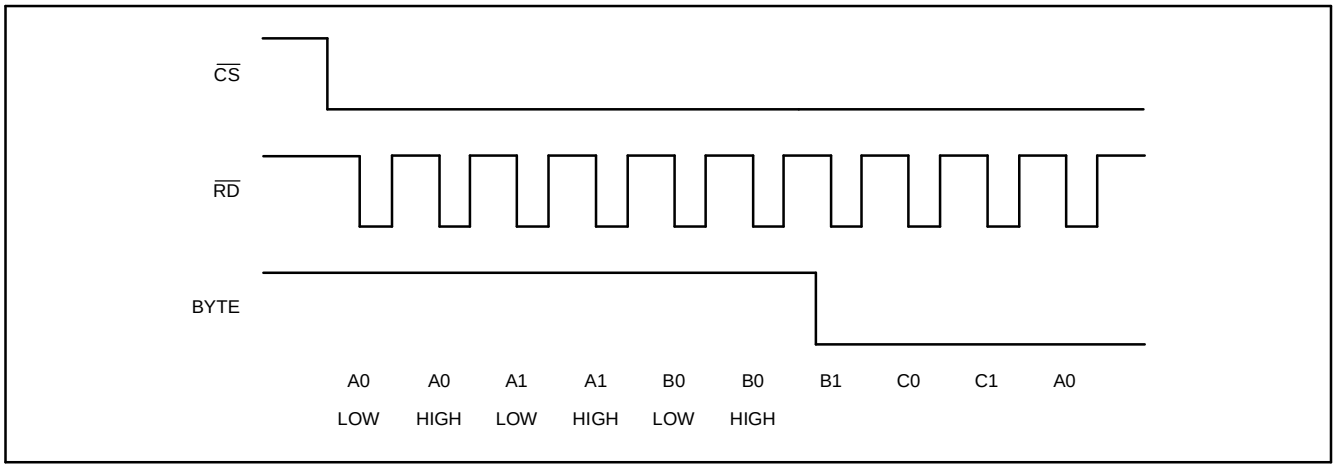


Figure 30. Reading Data in Cycling Mode

GETTING DATA

The ADS7864 has three different output modes that are selected with A2, A1 and A0. A2A1A0 are only active when $\overline{RD}$ and $\overline{CS}$ are both low. After a reset occurs, A2A1A0 are set to 000.

With (A2 A1 A0) = 000 to 101 a particular channel can directly be addressed (see Table 3 and Figure 27). The channel address should be set at least 10ns (see Figure 28, t_{12}) before the falling edge of $\overline{RD}$ and should not change as long as $\overline{RD}$ is low.

Table 3. Address/Mode Truth Table

CHANNEL SELECTED/ MODE	A2	A1	A0
A0	0	0	0
A1	0	0	1
B0	0	1	0
B1	0	1	1
C0	1	0	0
C1	1	0	1
Cycle Mode	1	1	0
FIFO Mode	1	1	1

With (A2 A1 A0) = 110 the interface is running in a cycle mode (see Figure 29 and Figure 30). Here, data from channel A0 is read on the first $\overline{RD}$ signal, then A1 on the second, followed by B0, B1, C0 and finally C1 before reading A0 again. Data from channel A0 is brought to the output first after a reset-signal or after powering the part up.

The third mode is a FIFO mode that is addressed with (A2 A1 A0 = 111). Data of the channel that is converted first will be read first. So, if a particular channel is most interesting and is converted more frequently (e.g., to get a history of a particular channel) then there are three output registers per channel available to store data. When the ADS7864 is operated in the FIFO mode, an initial $\overline{RD}/\overline{CS}$ is necessary (after power up and after reset), so that the internal address is set to '111', before the first conversion starts.

If a read process is just going on ($\overline{RD}$ signal low) and new data has to be stored, then the ADS7864 will wait until the read process is finished ($\overline{RD}$ signal going high) before the new data gets latched into its output register.

At time t_A (see Figure 31) the ADS7864 resets. With the reset signal, all conversions and scheduled conversions are cancelled. The data in the output registers are also cleared. With a reset, a running conversion gets interrupted and all channels go into the sample mode again.

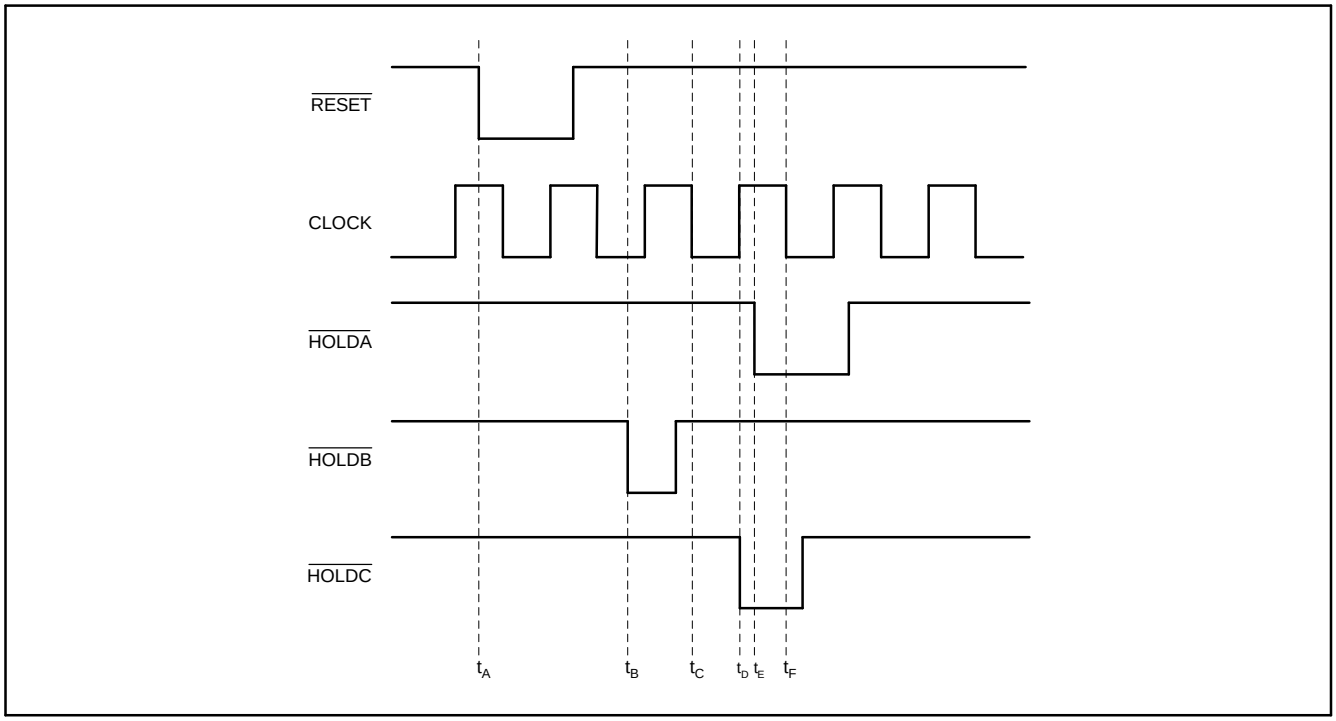


Figure 31. Example of Hold Signals

At time t_B a $\overline{HOLDB}$ signal occurs. With the next falling clock edge (t_C) the ADS7864 puts channel B into the loop to be converted next. As the reset signal occurred at t_A, the conversion of channel B will be started with the next rising edge of the clock after t_C.

Within the next clock cycle (t_C to t_F), $\overline{HOLDC}$ (t_D) and $\overline{HOLDA}$ (t_E) occur. If more than one hold signals get active within one clock cycle, channel A will be converted first. Therefore, as soon as the conversion of channel B is done, the conversion of channel A will be initiated. After this second conversion, channel C will be converted.

The 16 bit output word has following structure:

Valid Data	3-Bit Channel Information	12-Bit Data Word

Bit 15 shows if the FIFO is empty (low) or if it contains channel information (high). Bits 12 to 14 contain the Channel for the 12-bit data word (Bit 0 to 11). If the data is from channel A0, then bits 14 to 12 are '000'. The Channel bit pattern is outlined in Table 2 (Channel Truth Table).

New data is always written into the next available register. At t_0 (see Figure 32), the reset deletes all the existing data. At t_1 the new data of the channels A0 and A1 are put into registers 0 and 1. On t_2 the read process of channel A0 data is finished. Therefore, this data is dumped and A1 data is shifted to register 0. At t_3 new data is available, this time from channel B0 and B1. This data is written into the next available registers (register 1 and 2). The new data of channel C0 and C1 at t_4 is put on top (registers 3 and 4).

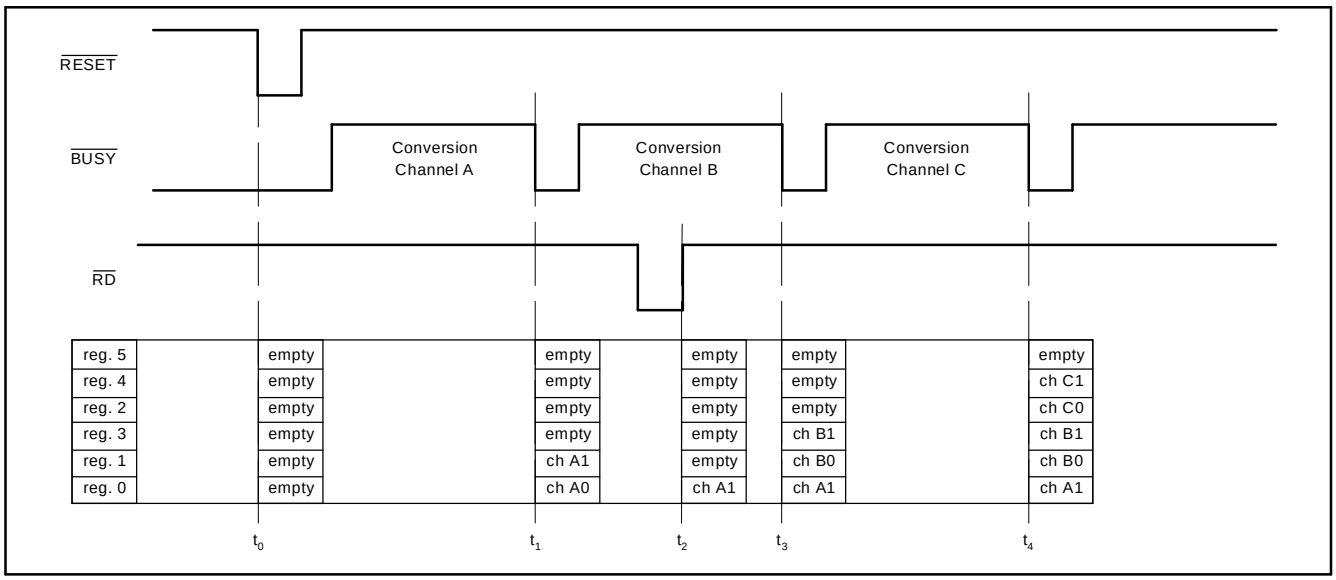


Figure 32. Functionality Diagram of FIFO Registers

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7864 circuitry. This is particularly true if the CLOCK input is approaching the maximum throughput rate. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are ***n*** 'windows' in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic or high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. These errors can change if the external event changes in time with respect to the CLOCK input. With this in mind, power to the ADS7864 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply. On average, the ADS7864 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A bypass capacitor must not be used when using the internal reference (tie pin 33 directly to pin 34). The AGND and DGND pins should be connected to a clean ground point. In all cases, this should be the ‘analog’ ground. Avoid connections which are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7864Y/250	ACTIVE	TQFP	PFB	48	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS7864Y	Samples
ADS7864Y/250G4	ACTIVE	TQFP	PFB	48	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS7864Y	Samples
ADS7864Y/2K	ACTIVE	TQFP	PFB	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		ADS7864Y	Samples
ADS7864YB/250	ACTIVE	TQFP	PFB	48	250	RoHS & Green	Call TI	Level-2-260C-1 YEAR		ADS7864Y B	Samples
ADS7864YB/2K	ACTIVE	TQFP	PFB	48	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		ADS7864Y B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

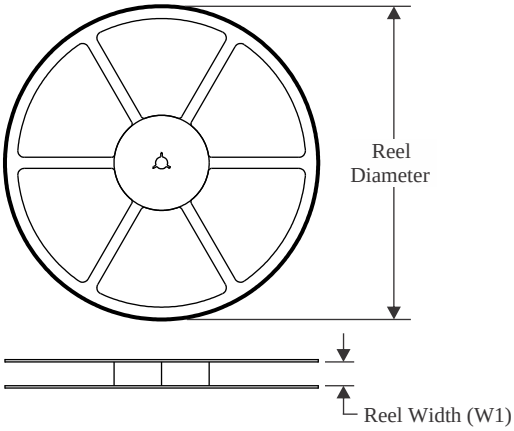
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

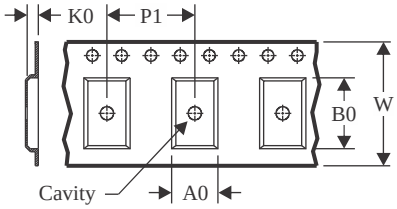
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

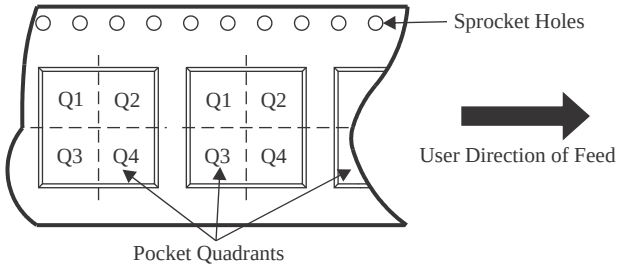


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

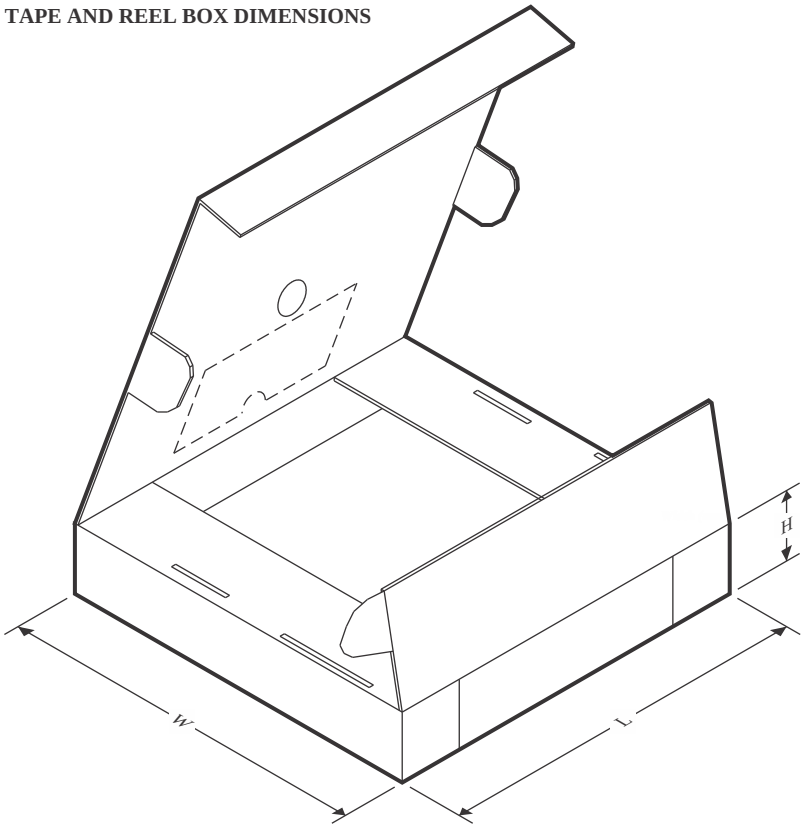
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7864Y/2K	TQFP	PFB	48	2000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2
ADS7864YB/2K	TQFP	PFB	48	2000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

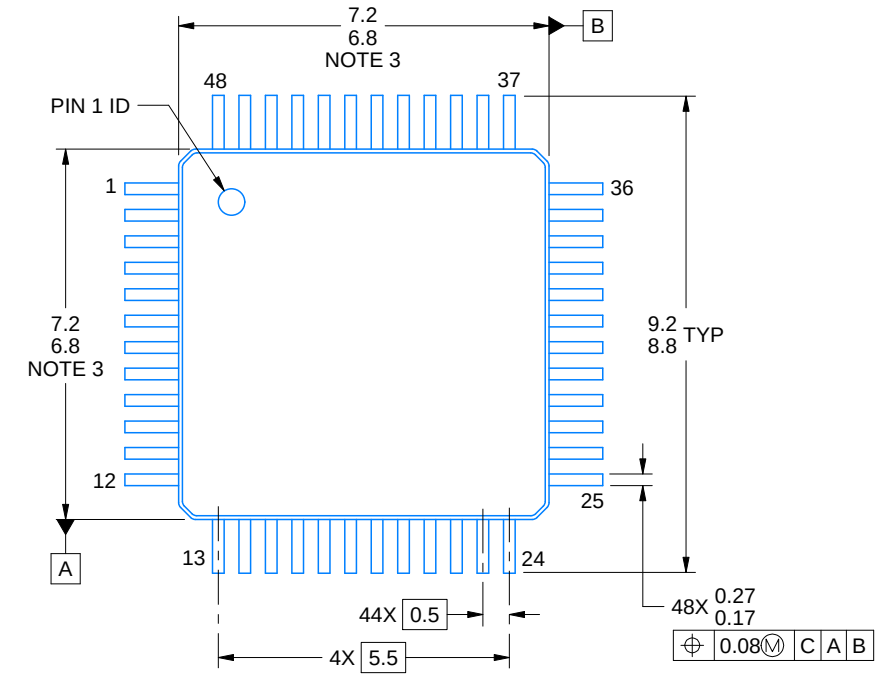
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7864Y/2K	TQFP	PFB	48	2000	350.0	350.0	43.0
ADS7864YB/2K	TQFP	PFB	48	2000	350.0	350.0	43.0

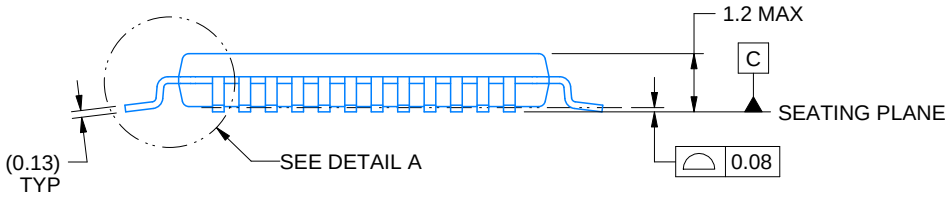
PACKAGE OUTLINE

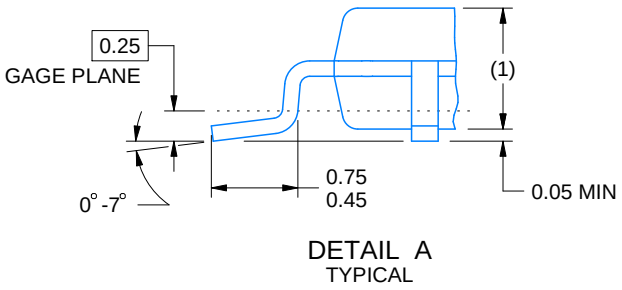
PFB0048A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK





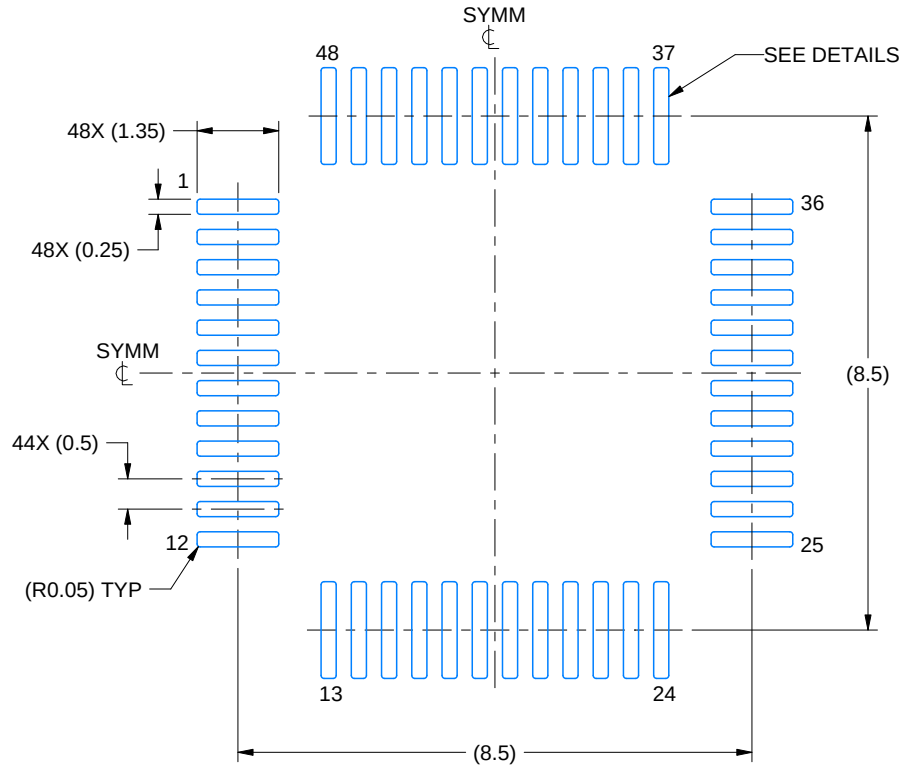


DETAIL A
TYPICAL

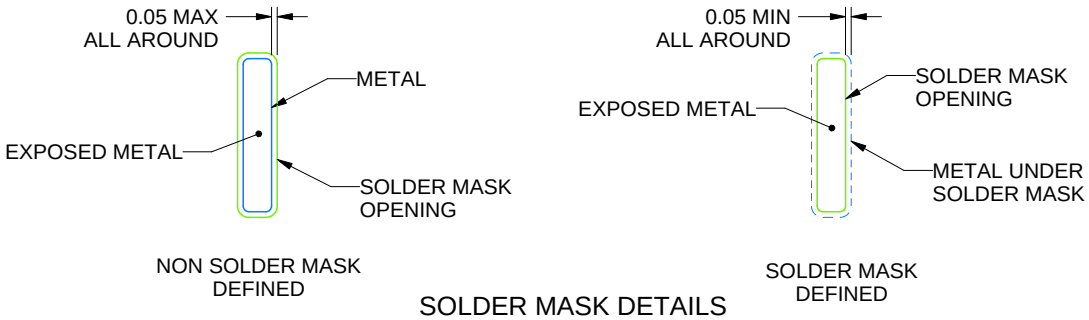
4215157/A 03/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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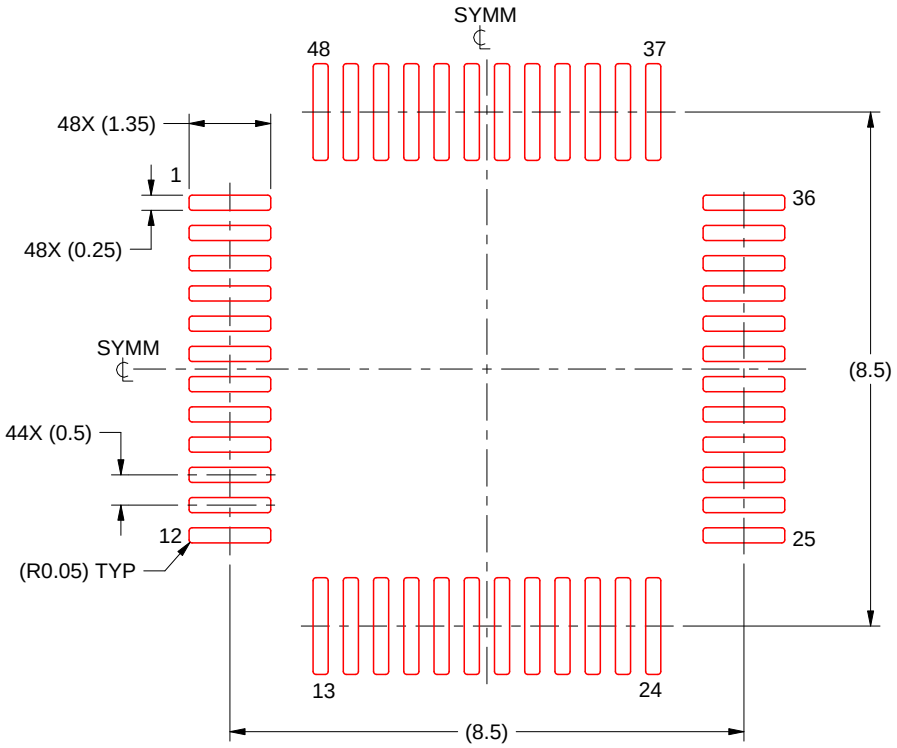
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
SCALE:8X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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