

# AFE7953 2T2R RF Sampling AFE with 12 GSPS DACs and 3 GSPS ADCs

## 1 Features

- [Request full data sheet](#)
- Dual RF sampling 12-GSPS transmit DACs
- Dual RF sampling 3-GSPS receive ADCs
- Maximum RF signal bandwidth: 400 MHz
- RF frequency range: 600 MHz - 12 GHz
- Digital step attenuators (DSA):
  - TX: 40 dB range, 0.125-dB steps
  - RX: 25 dB range, 0.5-dB steps
- Single or dual-band DUC or DDCs
- 16x NCOs per TX or RX
- Optional Internal PLL or VCO for DAC or ADC clocks or external clock at DAC or ADC sample rate
- SerDes data interface:
  - JESD204B and JESD204C compatible
  - 8 SerDes transceivers up to 29.5 Gbps
  - Subclass 1 multi-device synchronization
- Package: 17-mm × 17-mm FCBGA, 0.8-mm pitch

## 2 Applications

- [Radar](#)
- [Seeker front end](#)
- [Defense radio](#)
- [Tactical communications infrastructure](#)
- [Wireless communications test](#)

## 3 Description

The AFE7953 is a high performance, wide bandwidth multi-channel transceiver, integrating two RF sampling transmitter chains and two RF sampling receiver chains. With operation up to 12 GHz, this device enables direct RF sampling in the L, S, C and X-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

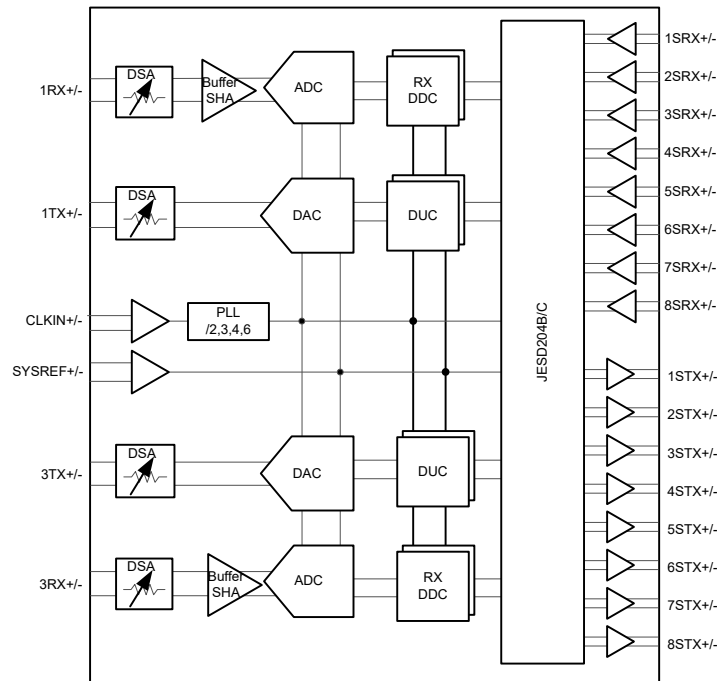
The TX signal paths support interpolation and digital up conversion options that deliver up to 400 MHz of signal bandwidth per TX channel. The output of the DUCs drives a 12-GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2<sup>nd</sup> Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40-dB range and 1-dB analog and 0.125-dB digital steps.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
AFE7953	FC-BGA	17 mm × 17 mm

(1) For more information, see *Mechanical, Packaging, and Orderable Information*.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Functional Block Diagram**



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	6.8 Digital Electrical Characteristics.....	<b>18</b>
<b>2 Applications</b> .....	<b>1</b>	6.9 Power Supply Electrical Characteristics.....	<b>20</b>
<b>3 Description</b> .....	<b>1</b>	6.10 Timing Requirements.....	<b>24</b>
<b>4 Description (continued)</b> .....	<b>3</b>	6.11 Switching Characteristics.....	<b>25</b>
<b>5 Revision History</b> .....	<b>3</b>	6.12 Typical Characteristics.....	<b>26</b>
<b>6 Specifications</b> .....	<b>4</b>	<b>7 Device and Documentation Support</b> .....	<b>117</b>
6.1 Absolute Maximum Ratings.....	<b>4</b>	7.1 Receiving Notification of Documentation Updates..	<b>117</b>
6.2 ESD Ratings.....	<b>4</b>	7.2 Support Resources.....	<b>117</b>
6.3 Recommended Operating Conditions.....	<b>5</b>	7.3 Trademarks.....	<b>117</b>
6.4 Thermal Information AFE79xx.....	<b>5</b>	7.4 Electrostatic Discharge Caution.....	<b>117</b>
6.5 Transmitter Electrical Characteristics.....	<b>6</b>	7.5 Glossary.....	<b>117</b>
6.6 RF ADC Electrical Characteristics.....	<b>12</b>	<b>8 Mechanical, Packaging, and Orderable Information</b>	<b>117</b>
6.7 PLL/VCO/Clock Electrical Characteristics.....	<b>16</b>		

## 4 Description (continued)

Each receiver chain includes a 25-dB range DSA (Digital Step Attenuator), followed by a 3-GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of signal bandwidth of up to 400 MHz per RX channel.

## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2023	*	Initial Release

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	-0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	-0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVC0, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8	-0.5	2.1	V
Pin Voltage Range	{1/2}RXIN+/-	-0.5	VDDR1P8+0.3	V
	{1/2}TXOUT+/-	-0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	-0.3	1.4	V
	{1:8}SRX+/-	-0.3	1.4	V
	{1:8}STX+/-	-0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESET, BISTB0, BISTB1	-0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	-0.3	VDDCLK1P8 + 0.3	V
SRDAMUX1, SRDAMUX2	-0.3	VDDA1P8+0.3	V	
Peak Input Current	any input		20	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	1000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins	150	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/ PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/ TXENC/PLL/PLLVCO/FB/FBCLK/ GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T <sub>A</sub>	Ambient temperature	-40		85	°C
T <sub>J</sub>	Operating Junction Temperature			110 <sup>(1)</sup>	°C
	Maximum Operating Junction Temperature	125			°C

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

### 6.4 Thermal Information AFE79xx

THERMAL METRIC <sup>(1)</sup>		17mmx17mm FC-BGA	UNIT
		400 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	16.2	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.42	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	4.85	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.12	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	4.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Transmitter Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{DAC} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC <sub>RES</sub>	DAC resolution			14		bits
f <sub>RFout</sub>	RF output frequency range	f <sub>DAC</sub> = 12 GSPS, 1 <sup>st</sup> Nyquist	600		6000	MHz
		f <sub>DAC</sub> = 12 GSPS, 2 <sup>nd</sup> Nyquist	6000		12000	
		f <sub>DAC</sub> = 9 GSPS, 1 <sup>st</sup> Nyquist	600		4500	
		f <sub>DAC</sub> = 9 GSPS, 2 <sup>nd</sup> Nyquist	4500		9000	
		f <sub>DAC</sub> = 6 GSPS, 1 <sup>st</sup> Nyquist	600		3000	
		f <sub>DAC</sub> = 6 GSPS, 2 <sup>nd</sup> Nyquist	3000		6000	
P <sub>max_FS</sub>	Max Full Scale Output Power, max gain 1 tone, at device pins	f <sub>out</sub> = 850 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS		4.2		dBm
		f <sub>out</sub> = 1800 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS		4.6		dBm
		f <sub>out</sub> = 2600 MHz, f <sub>DAC</sub> = 8847.36 MSPS, -0.5dBFS		4.0		dBm
		f <sub>out</sub> = 3500 MHz, -0.5dBFS		3.9		dBm
		f <sub>out</sub> = 4900 MHz, -0.5dBFS		3.1		dBm
		f <sub>out</sub> = 3500 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS, straight mode		1.0		dBm
		f <sub>out</sub> = 4900 MHz, f <sub>DAC</sub> = 5898.24 MSPS, -0.5dBFS, straight mode		0.1		dBm
		f <sub>out</sub> = 4900 MHz, f <sub>DAC</sub> = 8847.36 MSPS, -0.5dBFS, straight mode		-0.7		dBm
		f <sub>out</sub> = 8100 MHz, -0.1dBFS, mixed mode		-2.8		dBm
f <sub>out</sub> = 9600 MHz, -0.1dBFS, mixed mode		-4.3		dBm		
R <sub>TERM</sub>	Output termination resistor	Default setting		50		Ω
ATT <sub>range</sub>	DSA Attenuation range			40		dB
ATT <sub>step</sub>	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		±0.2		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, after calibration		±0.1		dB
ATT <sub>phase-err</sub>	DSA Gain Steps Phase accuracy, any 8dB range	f <sub>out</sub> = 850MHz <sup>(1)</sup>		±1		deg
		f <sub>out</sub> = 1800MHz <sup>(1)</sup>		±1		deg
		f <sub>out</sub> = 2600MHz <sup>(1)</sup>		±1		deg
		f <sub>out</sub> = 3500MHz <sup>(1)</sup>		±1		deg
		f <sub>out</sub> = 4900MHz <sup>(1)</sup>		±1		deg
		f <sub>out</sub> = 8100MHz <sup>(1)</sup>		±2		deg
		f <sub>out</sub> = 9600MHz <sup>(1)</sup>		±2		deg
G <sub>flat</sub>	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F <sub>out</sub> < 4.9G		1.2		

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion, 2 tones at $f_{\text{IF}} \pm 10\text{ MHz}$	$f_{\text{out}} = 850\text{MHz}$ , -7dBFS each tone		-66		dBc
		$f_{\text{out}} = 1800\text{MHz}$ , -7dBFS each tone		-63		dBc
		$f_{\text{out}} = 2600\text{MHz}$ , -7dBFS each tone		-62		dBc
		$f_{\text{out}} = 3500\text{MHz}$ , -7dBFS each tone		-61		dBc
		$f_{\text{out}} = 4900\text{MHz}$ , -7dBFS each tone		-57		dBc
		$f_{\text{out}} = 8100\text{MHz}$ , -7dBFS each tone		-55		dBc
		$f_{\text{out}} = 9600\text{MHz}$ , -7dBFS each tone		-52		dBc
		$f_{\text{out}} = 850\text{MHz}$ , -13dBFS each tone		-74.4		dBc
		$f_{\text{out}} = 1800\text{MHz}$ , -13dBFS each tone		-71.1		dBc
		$f_{\text{out}} = 2600\text{MHz}$ , -13dBFS each tone		-73		dBc
		$f_{\text{out}} = 3500\text{MHz}$ , -13dBFS each tone		-72		dBc
		$f_{\text{out}} = 4900\text{MHz}$ , -13dBFS each tone		-67.8		dBc
		$f_{\text{out}} = 8100\text{MHz}$ , -13dBFS each tone		-64		dBc
		$f_{\text{out}} = 9600\text{MHz}$ , -13dBFS each tone		-68		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		50.8		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		51.9		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		42		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		44		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		46.1		dBc
$f_s/2 - f_{\text{OUT}}$	Interleaving Image	$f_{\text{DAC}} = 5898.24\text{MSPS}$ , interleave mode		-51.9		dBc
		$f_{\text{DAC}} = 8847.36\text{ MSPS}$ , interleave mode		-46.0		dBc
		$f_{\text{DAC}} = 11796.48\text{MSPS}$ , interleave mode		-41		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-49		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-48		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-47		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 850\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 1800\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-64		dBc
		$f_{\text{out}} = 2600\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-45		dBc
		$f_{\text{out}} = 3500\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-57		dBc
		$f_{\text{out}} = 4900\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-58		dBc
		$f_{\text{out}} = 8100\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 9600\text{ MHz}$ , $A_{\text{OUT}} = -12\text{dBFS}$		-62		dBc

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850 \text{ MHz}$		-62		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-55		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-57		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-60		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-54		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		-54		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		-56		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-78		dBc
		$f_{\text{out}} = 8100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{out}} = 9600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	$f_{\text{out}} = 850 \text{ MHz}$		-81		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		-88		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		-86		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		-79		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		-86		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		-87		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		-85		dBc
		$f_{\text{out}} = 850 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{out}} = 1800 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-98		dBc
		$f_{\text{out}} = 2600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 3500 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 4900 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 8100 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 9600 \text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{out}} = 850 \text{ MHz}$		68.5		dBc
		$f_{\text{out}} = 1800 \text{ MHz}$		79.4		dBc
		$f_{\text{out}} = 2600 \text{ MHz}$		77		dBc
		$f_{\text{out}} = 3500 \text{ MHz}$		75		dBc
		$f_{\text{out}} = 4900 \text{ MHz}$		76		dBc
		$f_{\text{out}} = 8100 \text{ MHz}$		61		dBc
		$f_{\text{out}} = 9600 \text{ MHz}$		64		dBc
$f_s/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-64		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-75		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-67		dBFS
$f_s/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-49		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-48		dBFS
		$f_{\text{DAC}} = 11796.48 \text{ MSPS}$		-48		dBFS



## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3*f <sub>S</sub> /4	Fixed Spur	2nd Nyquist, f <sub>DAC</sub> = 5898.24MSPS		-76		dBFS
		2nd Nyquist, f <sub>DAC</sub> = 8847.36MSPS		-89		dBFS
		2nd Nyquist, f <sub>DAC</sub> = 11796.48MSPS		-63		dBFS
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 0.85 GHz	Atten=0dB, Pout=-13dBFS		-68.5		dBc
		Atten=20dB, Pout=-13dBFS		-67.2		dBc
		Atten=28dB, Pout=-13dBFS		-64.5		dBc
		Atten=39dB, Pout=-13dBFS		-53.9		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 1.8425 GHz	Atten=0dB, Pout=-13dBFS		-70.7		dBc
		Atten=20dB, Pout=-13dBFS		-68.3		dBc
		Atten=28dB, Pout=-13dBFS		-62.9		dBc
		Atten=39dB, Pout=-13dBFS		-52.0		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 2.6 GHz	Atten=0dB, Pout=-13dBFS		-71		dBc
		Atten=20dB, Pout=-13dBFS		-68		dBc
		Atten=28dB, Pout=-13dBFS		-62		dBc
		Atten=39dB, Pout=-13dBFS		-51.3		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 3.5 GHz	Atten=0dB, Pout=-13dBFS		-70		dBc
		Atten=20dB, Pout=-13dBFS		-67		dBc
		Atten=28dB, Pout=-13dBFS		-60		dBc
		Atten=39dB, Pout=-13dBFS		-49.8		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier f <sub>out</sub> = 4.9 GHz	Atten=0dB, Pout=-13dBFS		-68.8		dBc
		Atten=20dB, Pout=-13dBFS		-65.9		dBc
		Atten=28dB, Pout=-13dBFS		-60.6		dBc
		Atten=39dB, Pout=-13dBFS		-49.5		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 2.6 GHz	Atten=0dB, Pout=-13dBFS		-65		dBc
		Atten=20dB, Pout=-13dBFS		-62		dBc
		Atten=20dB, Pout=-13dBFS		-55		dBc
		Atten=39dB, Pout=-13dBFS		-44.3		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 3.5 GHz	Atten=0dB, Pout=-13dBFS		-64		dBc
		Atten=20dB, Pout=-13dBFS		-59		dBc
		Atten=28dB, Pout=-13dBFS		-52		dBc
		Atten=39dB, Pout=-13dBFS		-41.1		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 4.9 GHz	Atten=0dB, Pout=-13dBFS		-64.1		dBc
		Atten=20dB, Pout=-13dBFS		-60.4		dBc
		Atten=28dB, Pout=-13dBFS		-53.5		dBc
		Atten=39dB, Pout=-13dBFS		-42.5		dBc
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier f <sub>out</sub> = 8.1 GHz	Atten=0dB, Pout=-13dBFS		-58		dBc
		Atten=20dB, Pout=-13dBFS		-53		dBc
		Atten=28dB, Pout=-13dBFS		-46		dBc
		Atten=39dB, Pout=-13dBFS		-36		dBc

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPR <sub>1xcarr</sub>	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-57		dBc
		Atten=20dB, Pout=-13dBFS		-50		dBc
		Atten=28dB, Pout=-13dBFS		-42		dBc
		Atten=39dB, Pout=-13dBFS		-31		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.2		%
		$F_{\text{out}} = 1.8425\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.3		%
		$F_{\text{out}} = 2.6\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.28		%
		$F_{\text{out}} = 3.5\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.38		%
		$F_{\text{out}} = 4.9\text{ GHz}$ , $P_{\text{OUT}} = -13\text{dBFS}$		0.4		%
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-157.6		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-153.3		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-147.9		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-136.9		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-158.4		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-152.2		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-145.6		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$ , Pout=-13dBFS		-134.6		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-157		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-151		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-144		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$ , Pout=-13dBFS		-133.0		dBFS/Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-158		dBFS/Hz
		Atten=20dB, Pout=-13dBFS		-150		dBFS/Hz
		Atten=28dB, Pout=-13dBFS		-143		dBFS/Hz
		Atten=39dB, Pout=-13dBFS		-131.8		dBFS/Hz

## 6.5 Transmitter Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{\text{DAC}} = 11796.48\text{MSPS}$ ; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1<sup>st</sup> Nyquist, non-interleave mix mode for 2<sup>nd</sup> Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD <sub>dBFS</sub>	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-155.5		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147.8		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140.8		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129.6		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 50MHz offset $F_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-153		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
NSD <sub>dBFS</sub>	Noise Spectral Density 50MHz offset $F_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-152		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
S22	Output Return Loss, <6GHz, +/- fc * 10%	with matching		-17		dB
	Output Return Loss, >8GHz, +/- fc * 10%	with matching		-10		dB
PN <sub>TXADD</sub>	Additive Phase Noise External Clock Mode <sup>(2)</sup>	$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{Hz}$		-88		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{kHz}$		-102		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{kHz}$		-110		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{kHz}$		-123		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 1\text{MHz}$		-136		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 10\text{MHz}$		-143		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$ , $f_{\text{OFFSET}} = 100\text{MHz}$		-146		dBc/Hz

- (1) After DSA calibration procedure  
(2) Single side band, input clock phase noise subtracted.

## 6.6 RF ADC Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{J,MAX} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{ADC} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{REF} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{CLK} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC <sub>RES</sub>	ADC resolution			14		bits
F <sub>RFIn</sub>	RF input frequency range		600		12000	MHz
P <sub>FS_CW,min</sub>	Min Full scale input power, at device pins (1)	f <sub>IN</sub> = 830 MHz, DSA=0dB		-2.9		dBm
		f <sub>IN</sub> = 1760 MHz, DSA=0dB		-2.8		dBm
		f <sub>IN</sub> = 2610 MHz, DSA=0dB		-1.8		dBm
		f <sub>IN</sub> = 3610 MHz, DSA=0dB		-0.4		dBm
		f <sub>IN</sub> = 4910 MHz, DSA=0dB		0.1		dBm
		f <sub>IN</sub> = 8150 MHz, DSA=0dB		2.1		dBm
		f <sub>IN</sub> = 9610 MHz, DSA=0dB		4.3		dBm
P <sub>FS_CW,MAX</sub>	MAX Full scale input power - reliability limited, at device pins	f <sub>IN</sub> = 830 MHz, DSA = 20dB		16.7		dBm
		f <sub>IN</sub> = 1760 MHz, DSA = 20dB		17.0		dBm
		f <sub>IN</sub> = 2610 MHz, DSA = 20dB		18		dBm
		f <sub>IN</sub> = 3610 MHz, DSA = 20dB		18.5		dBm
		f <sub>IN</sub> = 4910 MHz, DSA = 20dB		19.3		dBm
		f <sub>IN</sub> = 8150 MHz, DSA = 20dB		21.3		dBm
		f <sub>IN</sub> = 9610 MHz, DSA = 20dB		23.5		dBm
S11	Input Return Loss	with matching network		-12.0		dB
ATT <sub>range</sub>	DSA Attenuation range			25.0		dB
ATT <sub>step</sub>	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), F <sub>in</sub> =3610MHz, after calibration		±0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	F <sub>in</sub> =3610MHz, after calibration		±0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	F <sub>in</sub> =4910MHz, after calibration		±1.8		deg
NSD	Noise Density (small signal)	f <sub>IN</sub> = 830 MHz, DSA = 3dB <sup>(3)</sup>		-155.2		dBFS/Hz
		f <sub>IN</sub> = 1760 MHz, DSA = 3dB <sup>(3)</sup>		-155.0		dBFS/Hz
		f <sub>IN</sub> = 2610 MHz, DSA = 3dB <sup>(3)</sup>		-154.4		dBFS/Hz
		f <sub>IN</sub> = 3610 MHz, DSA = 3dB <sup>(3)</sup>		-154.1		dBFS/Hz
		f <sub>IN</sub> = 4910 MHz, DSA = 3dB <sup>(3)</sup>		-155.1		dBFS/Hz
		f <sub>IN</sub> = 8150 MHz, DSA = 3dB <sup>(3)</sup>		-150		dBFS/Hz
		f <sub>IN</sub> = 9610 MHz, DSA = 3dB <sup>(3)</sup>		-151		dBFS/Hz
		f <sub>IN</sub> = 830 MHz, 3<=Atten<=22		-156.0		dBFS/Hz
		f <sub>IN</sub> = 1760 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f <sub>IN</sub> = 2610 MHz, 3<=Atten<=25		-155.7		dBFS/Hz
		f <sub>IN</sub> = 3610 MHz, 3<=Atten<=25		-155.4		dBFS/Hz
		f <sub>IN</sub> = 4910 MHz, 3<=Atten<=25		-155.8		dBFS/Hz
		f <sub>IN</sub> = 8150 MHz, 3<=Atten<=25		-152.5		dBFS/Hz
		f <sub>IN</sub> = 9610 MHz, 3<=Atten<=25		-152.5		dBFS/Hz

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{A,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF <sub>min</sub>	Noise Figure min DSA Atten=0 - 3dB	$f_{\text{IN}} = 830\text{ MHz}$		19.1		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		19.0		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		20.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		22.8		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		22.4		dB
		$f_{\text{IN}} = 8150\text{ MHz}$		27.3		dB
		$f_{\text{IN}} = 9610\text{ MHz}$		30		dB
NF	Noise Figure DSA Atten=4dB	$f_{\text{IN}} = 830\text{ MHz}^{(4)}$		20.0		dB
		$f_{\text{IN}} = 1760\text{ MHz}^{(4)}$		20.6		dB
		$f_{\text{IN}} = 2610\text{ MHz}^{(4)}$		21.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}^{(4)}$		23.5		dB
		$f_{\text{IN}} = 4910\text{ MHz}^{(4)}$		22.3		dB
		$f_{\text{IN}} = 8150\text{ MHz}^{(4)}$		27.9		dB
		$f_{\text{IN}} = 9610\text{ MHz}^{(4)}$		30.7		dB
NF <sub>max</sub>	Noise Figure DSA Atten=20dB	$f_{\text{IN}} = 830\text{ MHz}$		34.7		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		35.2		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		36.0		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		37.3		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		37.6		dB
		$f_{\text{IN}} = 8150\text{ MHz}$		42.8		dB
		$f_{\text{IN}} = 9610\text{ MHz}$		45		dB
IMD3	3 <sup>rd</sup> order intermodulation 2 tones at $f_{\text{IN}} \pm 10\text{MHz}$ -7dBFS each tone	$f_{\text{IN}} = 840\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-82.4		dBc
		$f_{\text{IN}} = 1770\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-84.1		dBc
		$f_{\text{IN}} = 2610\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-74		dBc
		$f_{\text{IN}} = 3610\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-77		dBc
		$f_{\text{IN}} = 4920\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-75.9		dBc
		$f_{\text{IN}} = 8150\text{ MHz}, 3 \leq \text{Atten} \leq 12,$ 25MHz tone spacing		-55		dBc
		$f_{\text{IN}} = 9610\text{ MHz}, 3 \leq \text{Atten} \leq 12,$ 25MHz tone spacing		-60		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3$ dBFS	$f_{\text{IN}} = 830\text{ MHz}$		88.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		80.6		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		78.9		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		78		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		71		dBFS

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -3 \text{ dBFS}^{(2) (5)}$	$f_{\text{IN}} = 830 \text{ MHz}$		-85.5		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-90.5		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-87		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-84.2		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-70		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -3 \text{ dBFS}^{(5)}$	$f_{\text{IN}} = 830 \text{ MHz}$		-80.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-85.3		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-75.4		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-70		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -3 \text{ dBFS}^{(5)}$	$f_{\text{IN}} = 830 \text{ MHz}$		-88.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-80.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-81.7		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-71		dBFS
SFDR	Spurious Free Dynamic Range $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830 \text{ MHz}$		89.2		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		88.8		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		95		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		90		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		89.8		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		83		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		80		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16^{(5)}$	$f_{\text{IN}} = 830 \text{ MHz, with board trim}$		-79.0		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz, with board trim}$		-101.6		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz, with board trim}$		-100		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz, with board trim}$		-101		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz, with board trim}$		-99.1		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz, with board trim}$		-107		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz, with board trim}$		-107		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -13 \text{ dBFS}$ $0 \leq \text{Atten} \leq 16^{(5)}$	$f_{\text{IN}} = 830 \text{ MHz}$		-95.4		dBFS
		$f_{\text{IN}} = 1760 \text{ MHz}$		-95.2		dBFS
		$f_{\text{IN}} = 2610 \text{ MHz}$		-98		dBFS
		$f_{\text{IN}} = 3610 \text{ MHz}$		-97		dBFS
		$f_{\text{IN}} = 4910 \text{ MHz}$		-94		dBFS
		$f_{\text{IN}} = 8150 \text{ MHz}$		-100		dBFS
		$f_{\text{IN}} = 9610 \text{ MHz}$		-102		dBFS

## 6.6 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 11796.48\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD <sub>n</sub> , n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16^{(5)}$	$f_{\text{IN}} = 830\text{ MHz}$		-89.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-88.8		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-83		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-80		dBFS

- (1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) NLE correction of HD2
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB
- (5) DDC Bypass (TI only test mode)

## 6.7 PLL/VCO/Clock Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f<sub>DAC</sub> = f<sub>VCO</sub>, f<sub>OUT</sub> = f<sub>DAC</sub>/4, normalized to f<sub>VCO</sub>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>VCO1</sub>	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f <sub>VCO2</sub>	VCO2 min frequency				8.8	GHz
	VCO2 max frequency		9.1			GHz
f <sub>VCO3</sub>	VCO3 min frequency				9.7	GHz
	VCO3 max frequency		10.24			GHz
f <sub>VCO4</sub>	VCO4 min frequency				11.6	GHz
	VCO4 max frequency		12.08			GHz
DIV <sub>DAC</sub>	DAC sample rate divider			1, 2 or 3		
DIV <sub>FBAD</sub> C	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
DIV <sub>RXAD</sub> C	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN <sub>VCO</sub>	Closed Loop Phase Noise F <sub>PLL</sub> = 11.79848 GHz F <sub>REF</sub> =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		-141		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> =8.84736 GHz F <sub>REF</sub> =491.52MHz	600kHz		-114		dBc/Hz
		800kHz		-118		dBc/Hz
		1MHz		-120		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-135		dBc/Hz
		50MHz		-142		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> = 9.8403 GHz F <sub>REF</sub> =491.52MHz	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-134		dBc/Hz
		50MHz		-140		dBc/Hz
	Closed Loop Phase Noise F <sub>PLL</sub> = 7.86432GHz F <sub>REF</sub> =491.52MHz	600kHz		-116		dBc/Hz
		800kHz		-119		dBc/Hz
		1MHz		-122		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-136		dBc/Hz
		50MHz		-143		dBc/Hz
F <sub>rms</sub>	Clock PLL integrated phase error <sup>(1)</sup>	f <sub>PLL</sub> =11.79848 GHz, [1KHz, 100MHz]		-43.4		dBc/Hz
		f <sub>PLL</sub> =8.8536 GHz, [1KHz, 100MHz]		-47.6		dBc/Hz
		f <sub>PLL</sub> =9.8304 GHz, [1KHz, 100MHz]		-46.2		dBc/Hz
f <sub>PFD</sub>	PFD frequency		100		500	MHz
PN <sub>pll_flat</sub>	Normalized PLL flat Noise	f <sub>VCO</sub> = 11796.48MHz		-226.5		dBc/Hz
F <sub>REF</sub>	Input Clock frequency		0.1		12	GHz
V <sub>SS</sub>	Input Clock level		0.6		1.8	Vppdiff



## 6.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is TA,MIN = -40°C to TJ,MAX = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f<sub>DAC</sub> = f<sub>VCO</sub>, f<sub>OUT</sub> = f<sub>DAC</sub>/4, normalized to f<sub>VCO</sub>.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance <sup>(2)</sup>	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

- (1) Single Sideband, not including the reference clock contribution  
(2) Refer to S11 data available from TI for impedance vs frequency

## 6.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CML SerDes Inputs [8:1]SRX+/-</b>						
V <sub>SRDIFF</sub>	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V <sub>SRCOM</sub>	SerDes Input Common Mode		0.4	0.5	0.6	V
Z <sub>SRdiff</sub>	SerDes Internal Differential Termination <sup>(1)</sup>			100		Ω
F <sub>SerDes</sub>	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance <sup>(2)</sup>	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
<b>CML SerDes Outputs [8:1]STX+/-</b>						
V <sub>STDIFF</sub>	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V <sub>STCOM</sub>	SerDes Output Common Mode		0.4	0.45	0.55	V
Z <sub>STdiff</sub>	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
<b>CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1</b>						
V <sub>IH</sub>	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V <sub>IL</sub>	Low-Level Input Voltage				0.4×VDD1 P8GPIO	V
I <sub>IH</sub>	High-Level Input Current		-250		250	μA
I <sub>IL</sub>	Low-Level Input Current		-250		250	μA
C <sub>L</sub>	CMOS input capacitance			2		pF
V <sub>OH</sub>	High-Level Output Voltage		VDD1P8G PIO-0.2			V
V <sub>OL</sub>	Low-Level Output Voltage				0.2	V
<b>Differential Inputs: SYSREF+/- Mode A</b>						
Clock <sub>MODE</sub>				PLL Clock Mode Only		
F <sub>SYSREFMAX</sub>	SYSREF Input Frequency Maximum			40		MHz
V <sub>SWINGSRMAX</sub>	SYSREF Input Swing Maximum			1.8		Vppdiff <sup>(3)</sup>
V <sub>SWINGSRMIN</sub>	SYSREF Input Swing Minimum	f <sub>REF</sub> < 500MHz		0.3		Vppdiff <sup>(3)</sup>
V <sub>SWINGSRMIN</sub>	SYSREF Input Swing Minimum	f <sub>REF</sub> > 500MHz		0.6		Vppdiff <sup>(3)</sup>
V <sub>COMSRMAX</sub>	SYSREF Input Common Mode Voltage Maximum			0.8		V
V <sub>COMSRMIN</sub>	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z <sub>T</sub>	Input termination	differential		100 <sup>(1)</sup>		Ω
C <sub>L</sub>	Input capacitance	Each pin to GND		0.5		pF
<b>LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-</b>						
V <sub>ICOM</sub>	Input Common Voltage			1.2		V
V <sub>ID</sub>	Differential Input Voltage swing			450		Vppdiff <sup>(3)</sup>
Z <sub>T</sub>	Input termination	differential		100		Ω

## 6.8 Digital Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T<sub>A,MIN</sub> = -40°C to T<sub>J,MAX</sub> = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-</b>						
V <sub>OCOM</sub>	Output Common Voltage			1.2		V
V <sub>OD</sub>	Differential Output Voltage swing			500		V <sub>ppdiff</sub> <sup>(3)</sup>
Z <sub>T</sub>	Internal Termination			100		Ω

- (1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
- (2) Loss tolerance is bump to bump from STX to SRX
- (3) V<sub>ppdiff</sub> is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

## 6.9 Power Supply Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ , nominal power supplies, 1 tone at -1 dBFS, DSA Attenuation = 0dB, TX straight mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1a: 2T2R - TDD, 50%/50% duty cycle TX: 125 MSPS input, 24x Int, $f_{\text{DAC}} = 3$ GSPS RX: $f_{\text{ADC}} = 1.5$ GSPS, 12x Dec, 125 MSPS output $f_{\text{OUT}} = f_{\text{IN}} = 1$ GHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		345		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			286		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			69		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			488		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			599		mA
$P_{\text{diss}}$	Power Dissipation			2399		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1b: 2T2R - TX active, RX in standby, TX: 125 MSPS input, 24x Int, $f_{\text{DAC}} = 3$ GSPS RX: $f_{\text{ADC}} = 1.5$ GSPS, 12x Dec, 125 MSPS output $f_{\text{OUT}} = f_{\text{IN}} = 1$ GHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		349		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			270		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			69		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			531		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			583		mA
$P_{\text{diss}}$	Power Dissipation			2414		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1c: 2T2R - RX active, TX in standby TX: 125 MSPS input, 24x Int, $f_{\text{DAC}} = 3$ GSPS RX: $f_{\text{ADC}} = 1.5$ GSPS, 12x Dec, 125 MSPS output $f_{\text{OUT}} = f_{\text{IN}} = 1$ GHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-4-8-1		341		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			302		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			69		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			446		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			616		mA
$P_{\text{diss}}$	Power Dissipation			2384		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 2T2R - FDD TX: 125MSPS input, 24x Int, $f_{\text{DAC}} = 3$ GSPS RX: $f_{\text{ADC}} = 1.5$ GSPS, 12x Dec, 125MSPS output $f_{\text{OUT}} = 1$ GHz, $f_{\text{IN}} = 1$ GHz Serdes: 8b/10b, 10Gbps TX/RX LMFS: 1-4-8-1		600		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			323		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			69		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			703		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			805		mA
$P_{\text{diss}}$	Power Dissipation			3374		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ , nominal power supplies, 1 tone at -1 dBFS, DSA Attenuation = 0dB, TX straight mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3a: 2T2R - TDD, 50%/50% duty cycle TX: 500 MSPS input, 24x Int, $f_{\text{DAC}} = 12$ GSPS RX: $f_{\text{ADC}} = 3$ GSPS, 6x Dec, 500 MSPS output $f_{\text{OUT}}=f_{\text{IN}} = 3.5$ GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		361		mA	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			306		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0				71		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF				875		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				1336		mA
$P_{\text{diss}}$	Power Dissipation				3614		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3b: 2T2R - TX active, RX in standby TX: 500 MSPS input, 24x Int, $f_{\text{DAC}} = 12$ GSPS RX: $f_{\text{ADC}} = 3$ GSPS, 6x Dec, 500 MSPS output $f_{\text{OUT}}=f_{\text{IN}} = 3.5$ GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		345		mA	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			277		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0				72		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF				1123		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				1473		mA
$P_{\text{diss}}$	Power Dissipation				3958		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3c: 2T2R - RX active, TX in standby TX: 500 MSPS input, 24x Int, $f_{\text{DAC}} = 12$ GSPS RX: $f_{\text{ADC}} = 3$ GSPS, 6x Dec, 500 MSPS output $f_{\text{OUT}}=f_{\text{IN}} = 3.5$ GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		377		mA	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			336		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0				71		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF				627		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				1198		mA
$P_{\text{diss}}$	Power Dissipation				3270		mW
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 2T2R - FDD TX: 500MSPS input, 24x Int, $f_{\text{DAC}} = 12$ GSPS RX: $f_{\text{ADC}} = 3$ GSPS, 6x Dec, 500MSPS output $f_{\text{OUT}} = 3.5\text{GHz}$ , $f_{\text{IN}} = 3.7$ GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 2-4-4-1		635		mA	
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			357		mA	
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0				72		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF				1417		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9				1952		mA
$P_{\text{diss}}$	Power Dissipation				5421		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,MIN} = -40^\circ\text{C}$  to  $T_{A,MAX} = +110^\circ\text{C}$ , nominal power supplies, 1 tone at -1 dBFS, DSA Attenuation = 0dB, TX straight mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5a: 2T2R - TDD, 50%/50% duty cycle TX: dual 125 MSPS input, 48x Int, $f_{DAC} = 6$ GSPS, MixMode RX: dual $f_{ADC} = 3$ GSPS, 24x Dec, 125 MSPS output $f_{OUT}=f_{IN} = 3.5$ GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		363		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			302		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			71		mA
$I_{VDD1P2}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			683		mA
	Group 1A: DVDD0P9 + VDDT0P9			1177		mA
	Power Dissipation			3234		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5b: 2T2R - TX active, RX in Standby TX: dual 125 MSPS input, 48x Int, $f_{DAC} = 6$ GSPS, MixMode RX: dual $f_{ADC} = 3$ GSPS, 24x Dec, 125 MSPS output $f_{OUT}=f_{IN} = 3.5$ and 3.6 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		349		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			273		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			72		mA
$I_{VDD1P2}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			757		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			1182		mA
$P_{diss}$	Power Dissipation			3252		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5c: 2T2R - RX active, TX in standby TX: dual 125 MSPS input, 48x Int, $f_{DAC} = 6$ GSPS, MixMode RX: dual $f_{ADC} = 3$ GSPS, 24x Dec, 125 MSPS output $f_{OUT}=f_{IN} = 3.5$ and 3.6 GHz Serdes: 8b/10b, 20 Gbps TX/RX LMFS: 1-8-16-1		377		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			331		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			71		mA
$I_{VDD1P2}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			610		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			1172		mA
$P_{diss}$	Power Dissipation			3217		mW
$I_{VDD1P8}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 6: 2T2R FDD TX: dual 125 MSPS input, 48x Int, $f_{DAC} = 6$ GSPS, MixMode RX: dual $f_{ADC} = 3$ GSPS, 24x Dec, 125 MSPS output $f_{OUT} = 3.5$ and 3.55GHz, $f_{IN} = 3.6$ and 3.65 GHz Serdes: 8b/10b, 10 Gbps TX/RX LMFS: 1-8-16-1		639		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8			351		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			72		mA
$I_{VDD1P2}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			1046		mA
$I_{VDD0P9}$	Group 1A: DVDD0P9 + VDDT0P9			1734		mA
$P_{diss}$	Power Dissipation			4770		mW

## 6.9 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ , nominal power supplies, 1 tone at -1 dBFS, DSA Attenuation = 0dB, TX straight mode, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VDD1P8}}$	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 7: same configuration as mode 2, Sleep Mode. SLEEP pin is pull high.		22		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			181		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			16		mA
$I_{\text{VDD1P2}}$	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			49		mA
$I_{\text{VDD0P9}}$	Group 1A: DVDD0P9 + VDDT0P9			213		mA
$P_{\text{diss}}$	Power Dissipation			649		mW

## 6.10 Timing Requirements

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
<b>Timing: SYSREF+/-</b>					
$t_{\text{s}}(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{\text{h}}(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
<b>Timing: Serial ports</b>					
$t_{\text{s}}(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK			15	ns
$t_{\text{h}}(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK <sup>(1)</sup>		$5 + t_{\text{SCLK}}$		ns
$t_{\text{s}}(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK			15	ns
$t_{\text{h}}(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK			5	ns
$t_{\text{(SCLK)_W}}$	Minimum SCLK period: registers write			25	ns
$t_{\text{(SCLK)_R}}$	Minimum SCLK period: registers read			50	ns
$t_{\text{d}}(\text{data\_out})$	Minimum Data Output delay after Falling Edge of SCLK			0	ns
	Maximum Data Output delay after Falling Edge of SCLK			15	ns
$t_{\text{RESET}}$	Minimum $\overline{\text{RESET}}$ Pulse Width		1		ms

(1)  $\overline{\text{SDEN}}$  need to be held one more extra clock cycle with the last SCLK edge



## 6.11 Switching Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; TX Input Rate = 491.52MSPS,  $f_{\text{DAC}} = 8847.36\text{MSPS}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

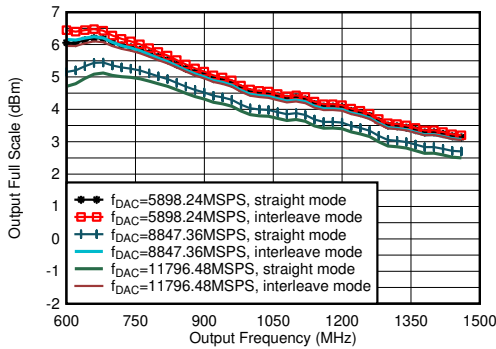
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TX Channel Latency</b>						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
$t_{\text{JESD TX}}$	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles <sup>(1)</sup>
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
<b>RX Channel Latency</b>						
	SerDes Transmitter Analog Delay			3.6		ns
$t_{\text{JESD RX}}$	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles <sup>(1)</sup>
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
<b>FB Channel Latency</b>						
	SerDes Transmitter Analog Delay			3.6		ns
$t_{\text{JESD FB}}$	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles <sup>(1)</sup>
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

## 6.12 Typical Characteristics

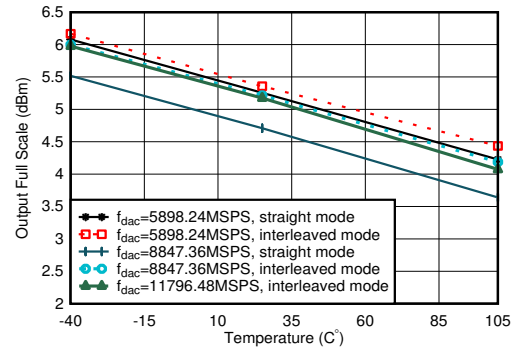
### 6.12.1 TX Typical Characteristics 800 MHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



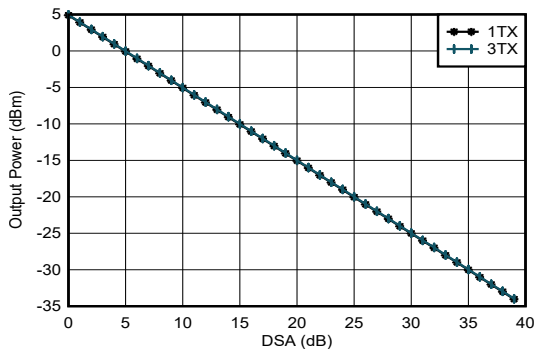
including PCB and cable losses,  $A_{out} = -0.5$  dBFS, DSA = 0, 0.8 GHz matching

**Figure 6-1. TX Output Fullscale vs Output Frequency**



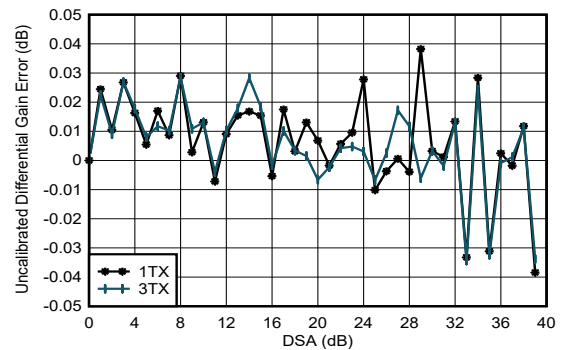
including PCB and cable losses,  $A_{out} = -0.5$  dBFS, DSA = 0, 0.8 GHz matching

**Figure 6-2. TX Output Fullscale vs Temperature**



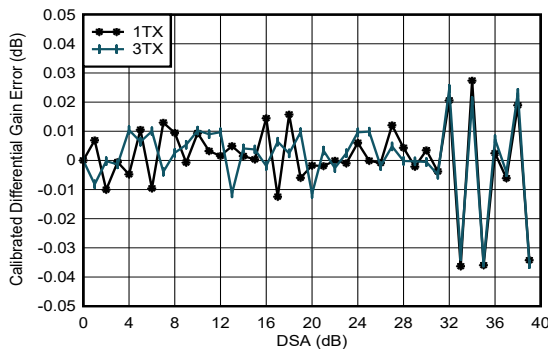
$f_{DAC} = 11796.48$  MSPS, interleave mode,  $A_{out} = -0.5$  dBFS, matching 0.8 GHz

**Figure 6-3. TX Output Power vs DSA Setting and Channel at 0.85 GHz**



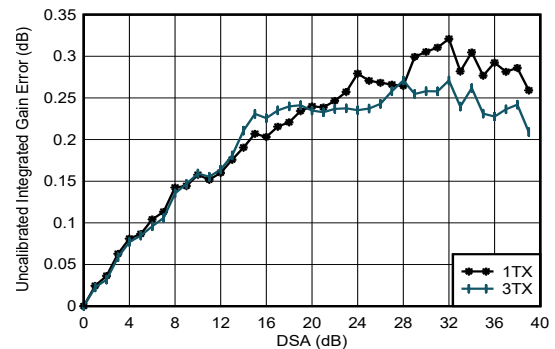
$f_{DAC} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{OUT}(DSA \text{ Setting} - 1) - P_{OUT}(DSA \text{ Setting}) + 1$

**Figure 6-4. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz**



$f_{DAC} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{OUT}(DSA \text{ Setting} - 1) - P_{OUT}(DSA \text{ Setting}) + 1$

**Figure 6-5. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz**

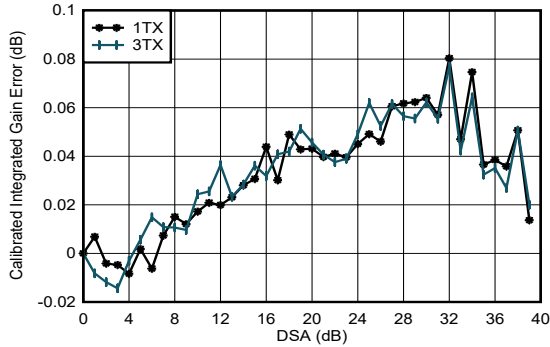


$f_{DAC} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{OUT}(DSA \text{ Setting}) - P_{OUT}(DSA \text{ Setting} = 0) + DSA \text{ Settings}$

**Figure 6-6. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz**

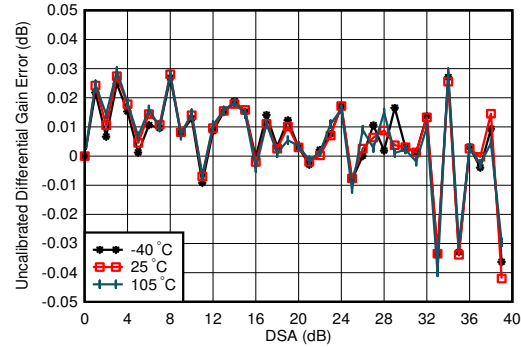
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



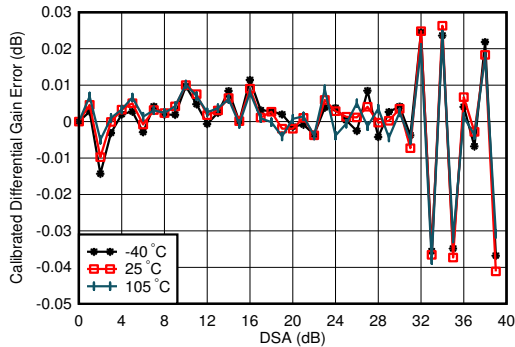
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 6-7. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz**



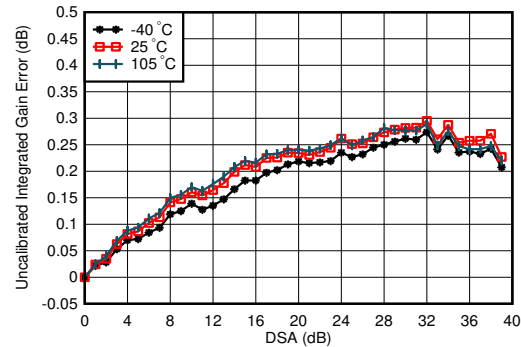
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-8. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz**



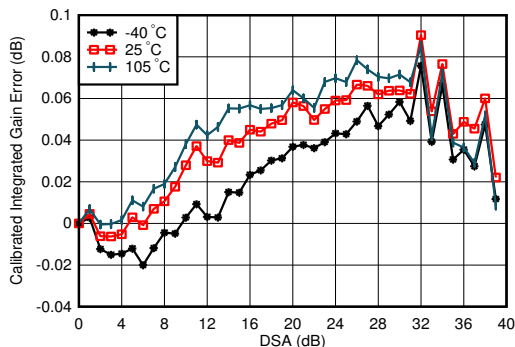
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-9. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz**



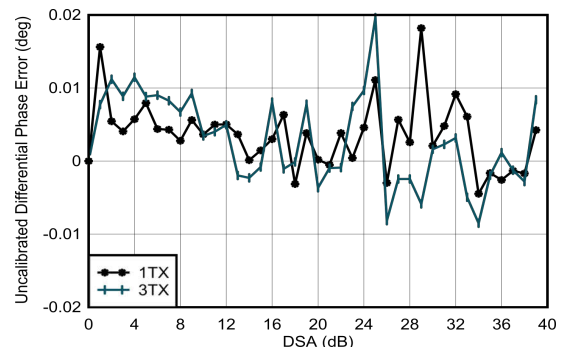
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 6-10. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz**



$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

**Figure 6-11. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz**

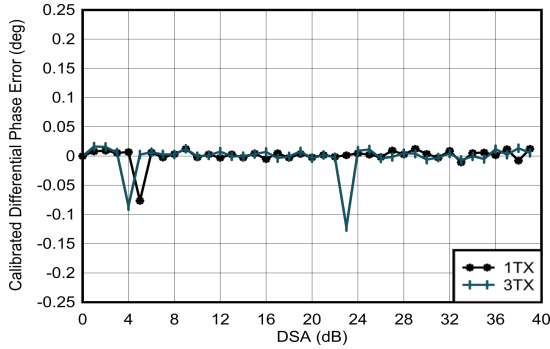


$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-12. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz**

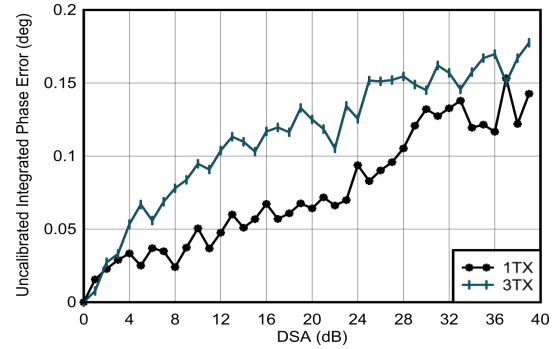
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



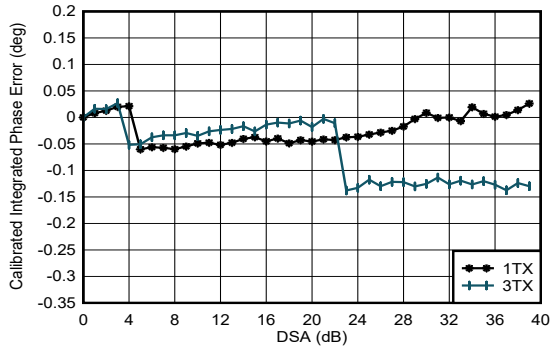
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
Phase DNL spike may occur at any DSA setting.

**Figure 6-13. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz**



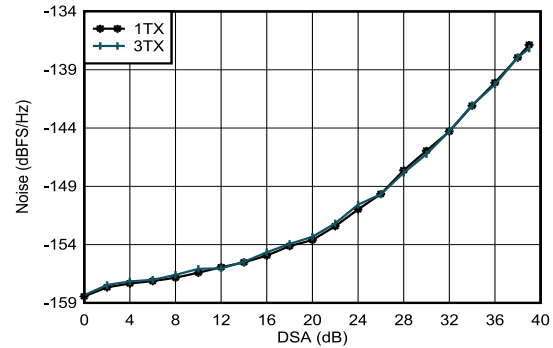
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 6-14. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz**



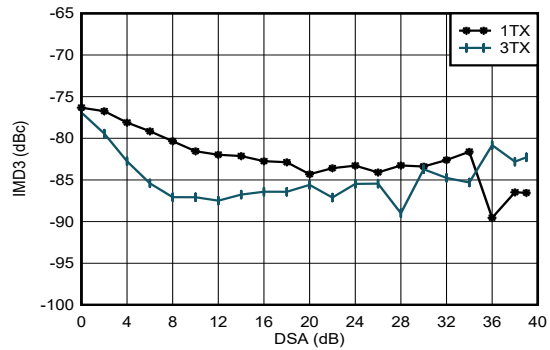
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 6-15. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz**



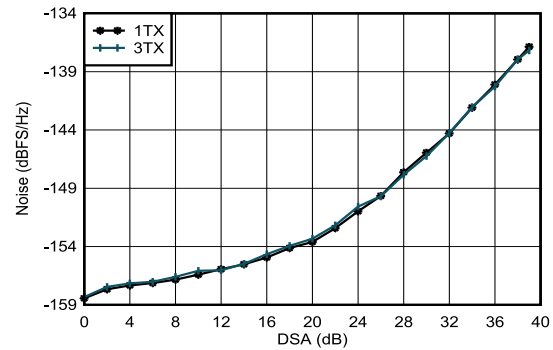
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 6-16. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz**



$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz  
Integrated Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

**Figure 6-17. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz**

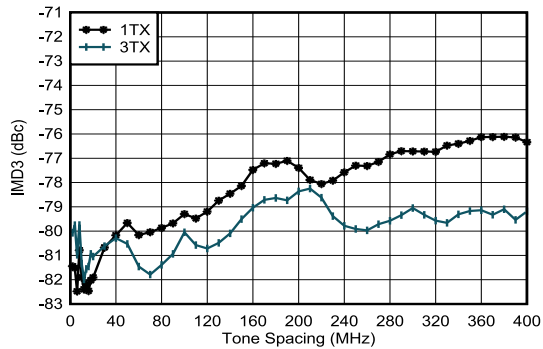


$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 0.8 GHz,  
 $P_{\text{OUT}} = -13$  dBFS

**Figure 6-18. TX Output Noise vs Channel and Attenuation at 0.85 GHz**

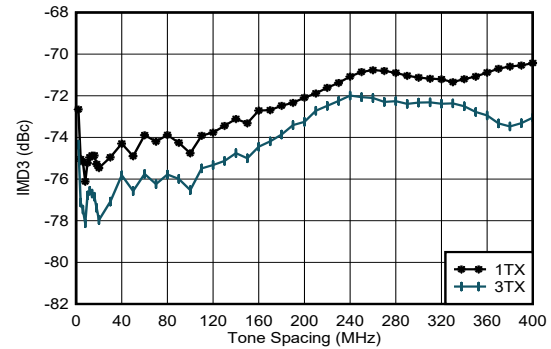
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



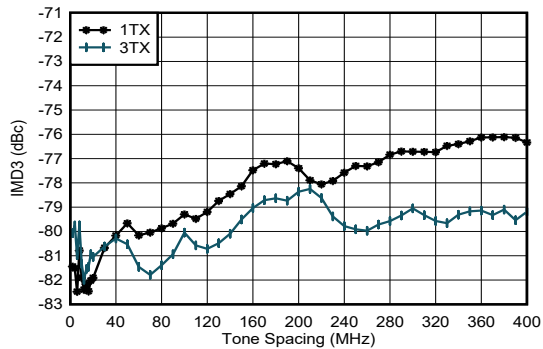
$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode,  $f_{\text{CENTER}} = 0.85$  GHz, matching at 0.8 GHz, -13 dBFS each tone

**Figure 6-19. TX IMD3 vs DSA Setting at 0.85 GHz**



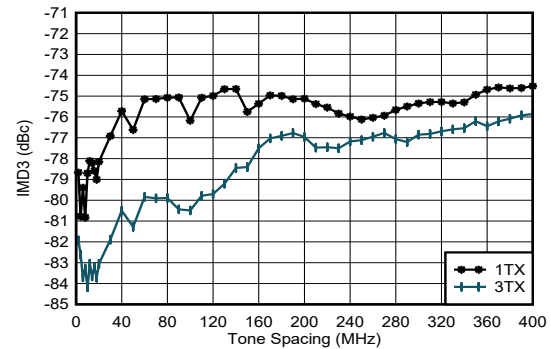
$f_{\text{DAC}} = 5898.24$  MSPS, straight mode,  $f_{\text{CENTER}} = 0.85$  GHz, matching at 0.8 GHz, -13 dBFS each tone

**Figure 6-20. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz**



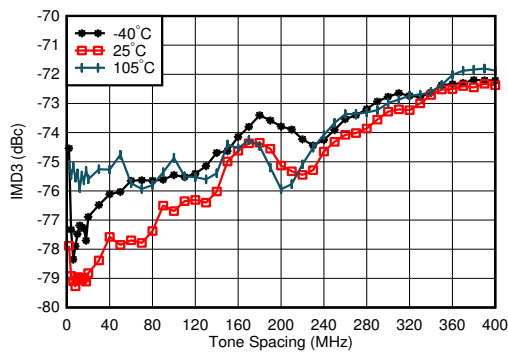
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode,  $f_{\text{CENTER}} = 0.85$  GHz, matching at 0.8 GHz, -13 dBFS each tone

**Figure 6-21. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz**



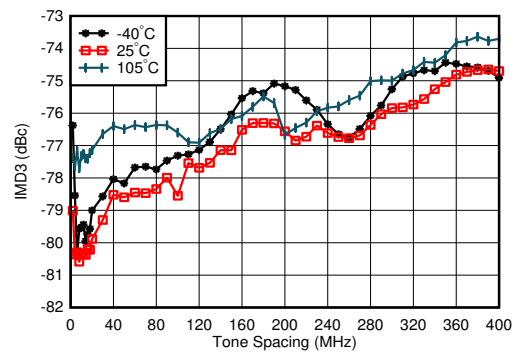
$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode,  $f_{\text{CENTER}} = 0.85$  GHz, matching at 0.8 GHz, -13 dBFS each tone

**Figure 6-22. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz**



$f_{\text{DAC}} = 5898.24$  MSPS, straight mode,  $f_{\text{CENTER}} = 0.85$  GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

**Figure 6-23. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz**

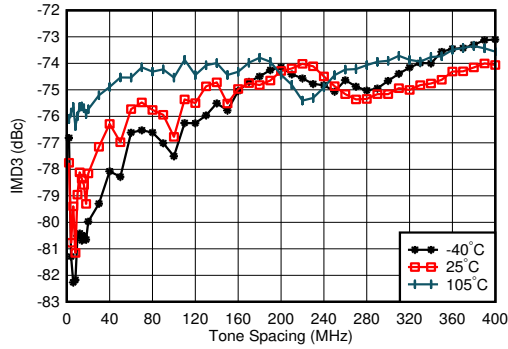


$f_{\text{DAC}} = 8847.36$  MSPS, straight mode,  $f_{\text{CENTER}} = 0.85$  GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

**Figure 6-24. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz**

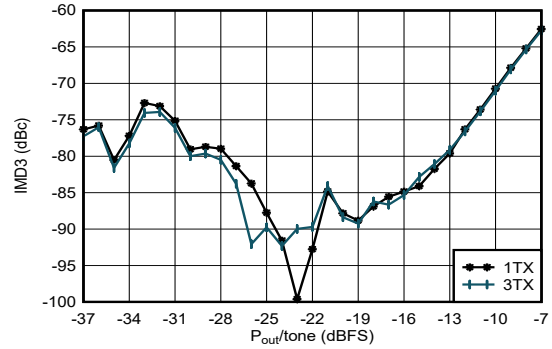
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



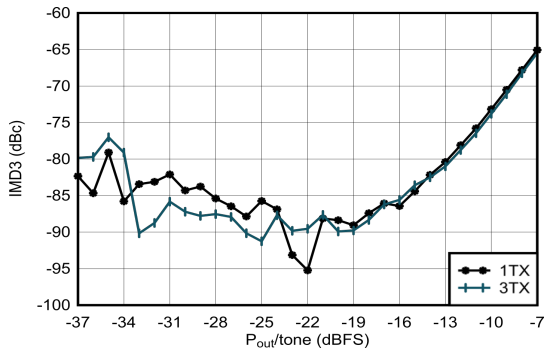
$f_{DAC} = 11796.48$  MSPS, straight mode,  $f_{CENTER} = 0.85$  GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

**Figure 6-25. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz**



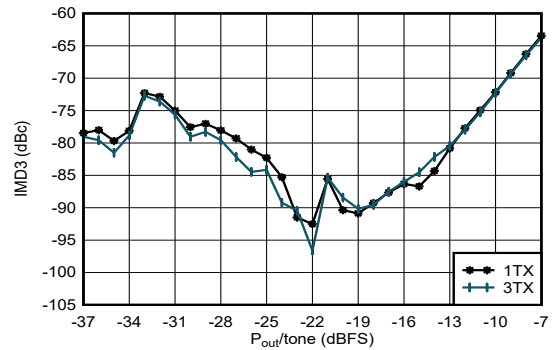
$f_{DAC} = 5898.24$  MSPS, straight mode,  $f_{CENTER} = 0.85$  GHz,  $f_{SPACING} = 20$  MHz, matching at 0.8 GHz

**Figure 6-26. TX IMD3 vs Digital Level at 0.85 GHz**



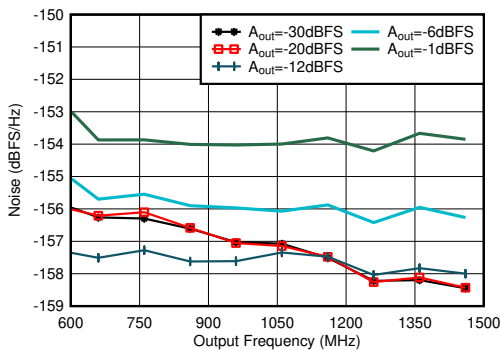
$f_{DAC} = 8847.36$  MSPS, straight mode,  $f_{CENTER} = 0.85$  GHz,  $f_{SPACING} = 20$  MHz, matching at 0.8 GHz

**Figure 6-27. TX IMD3 vs Digital Level at 0.85 GHz**



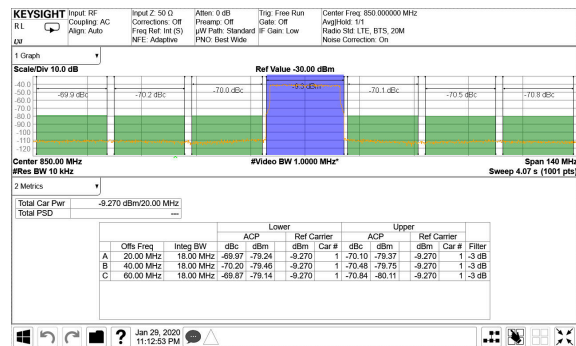
$f_{DAC} = 11796.48$  MSPS, interleave mode,  $f_{CENTER} = 0.85$  GHz,  $f_{SPACING} = 20$  MHz, matching at 0.8 GHz

**Figure 6-28. TX IMD3 vs Digital Level at 0.85 GHz**



Matching at 2.6 GHz, Single tone,  $f_{DAC} = 11.79648$  GSPPS, interleave mode, 40-MHz offset, DSA = 0dB

**Figure 6-29. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz**

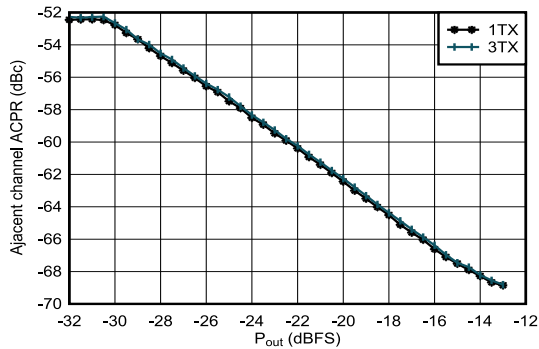


TM1.1,  $P_{OUT\_RMS} = -13$  dBFS

**Figure 6-30. TX 20-MHz LTE Output Spectrum at 0.85 GHz**

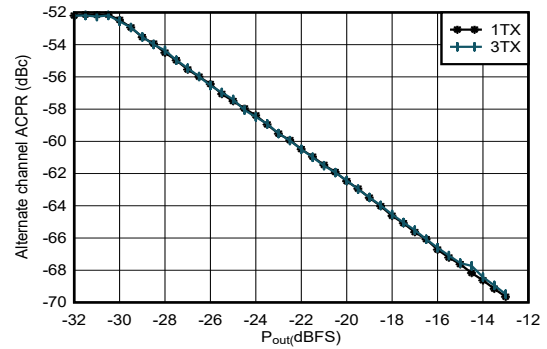
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



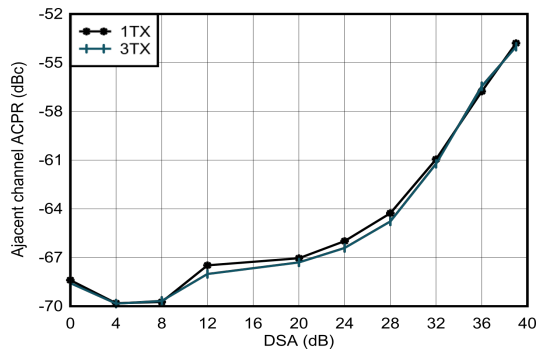
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-31. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz**



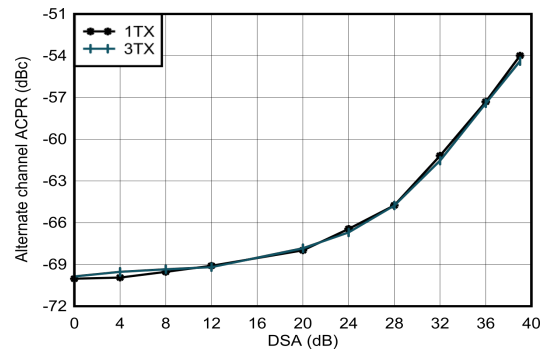
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-32. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz**



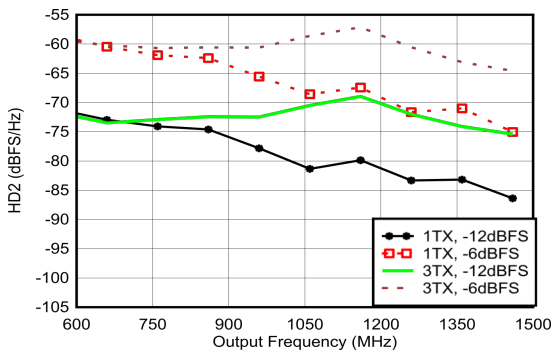
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-33. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz**



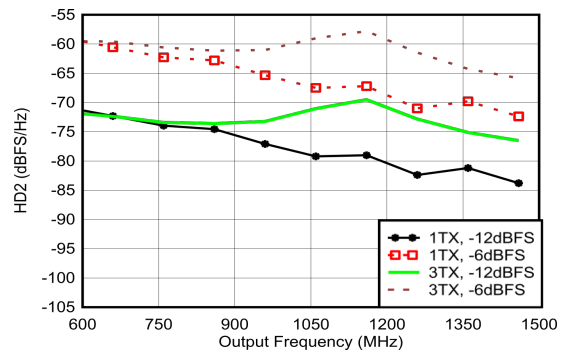
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-34. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz**



Matching at 0.8 GHz,  $f_{DAC} = 5898.24\text{G}$  SPS, straight mode

**Figure 6-35. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz**

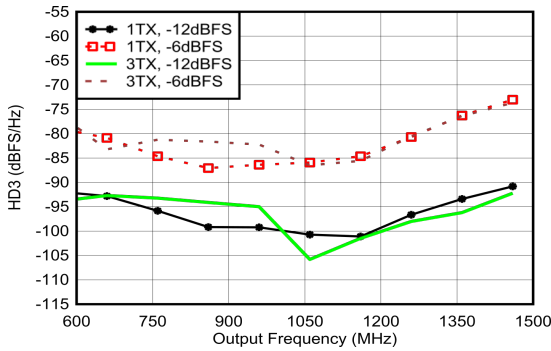


Matching at 0.8 GHz,  $f_{DAC} = 8847.36$  GSPS, straight mode

**Figure 6-36. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz**

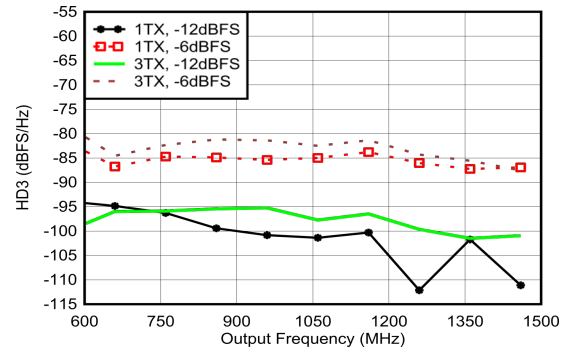
### 6.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



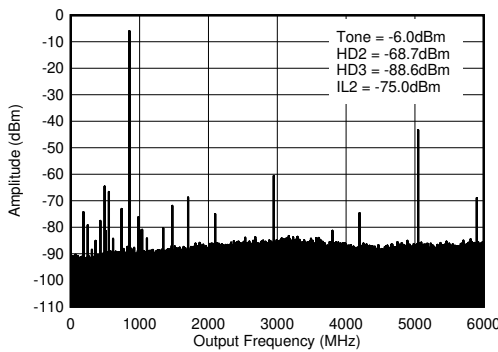
Matching at 0.8 GHz,  $f_{\text{DAC}} = 5898.24$  MSPS, straight mode, normalized to output power at harmonic frequency

**Figure 6-37. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz**



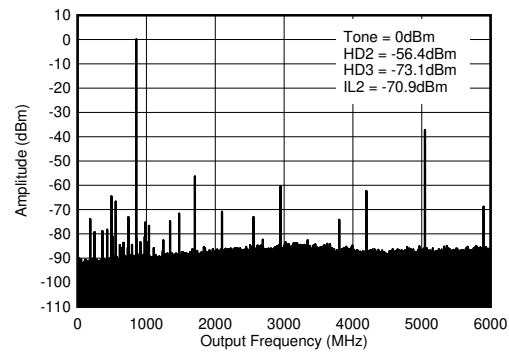
Matching at 0.8 GHz,  $f_{\text{DAC}} = 8847.36$  MSPS, straight mode, normalized to output power at harmonic frequency

**Figure 6-38. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz**



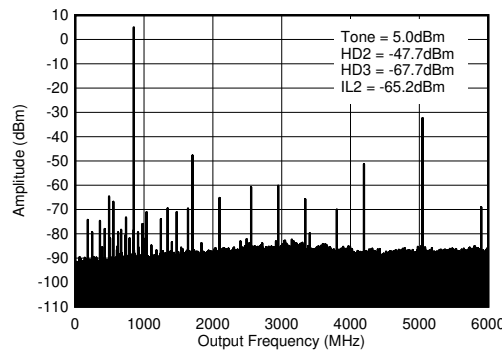
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-39. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**



$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-40. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**



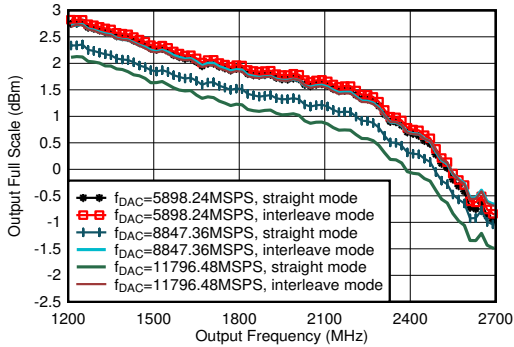
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$ .

**Figure 6-41. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ( $0-f_{\text{DAC}}$ )**



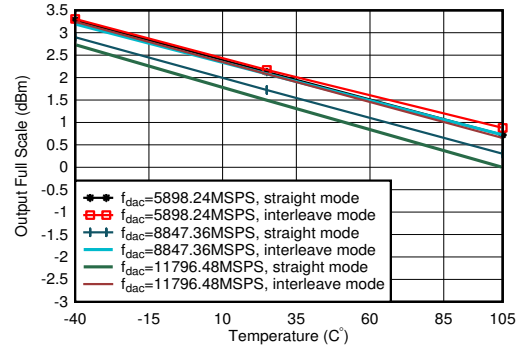
### 6.12.2 TX Typical Characteristics at 1.8 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



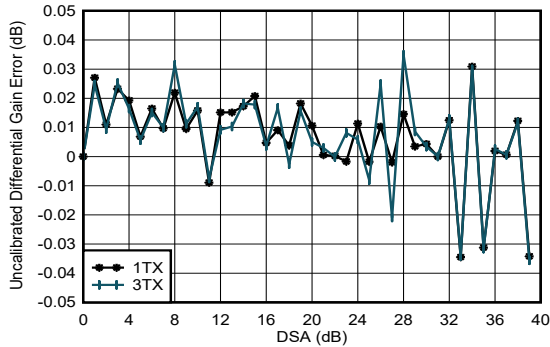
including PCB and cable losses,  $A_{out} = -0.5$  dBFS, DSA = 0, 1.8 GHz matching

Figure 6-42. TX Output Fullscale vs Output Frequency



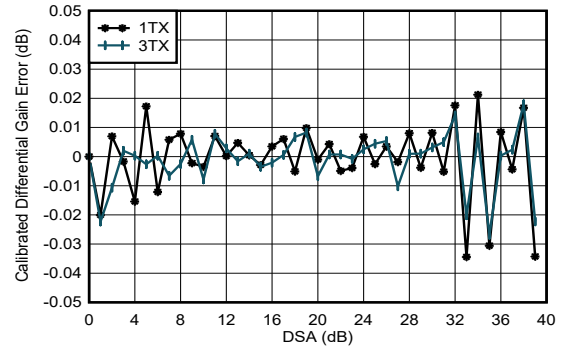
$A_{out} = -0.5$  dBFS, matching 1.8 GHz

Figure 6-43. TX Output Power vs Temperature at 1.8 GHz



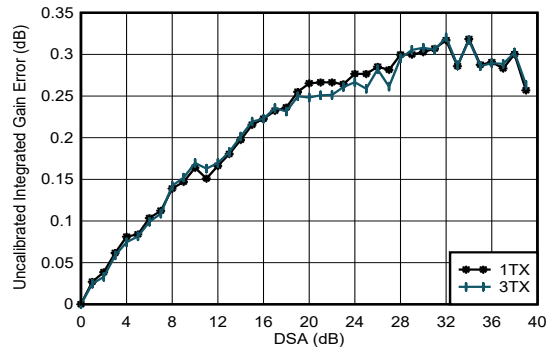
$f_{DAC} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{OUT}(DSA \text{ Setting} - 1) - P_{OUT}(DSA \text{ Setting}) + 1$

Figure 6-44. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz



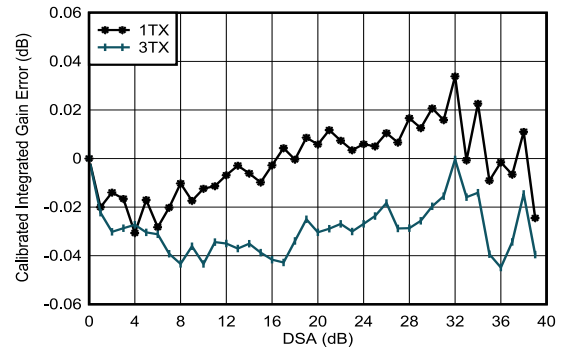
$f_{DAC} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{OUT}(DSA \text{ Setting} - 1) - P_{OUT}(DSA \text{ Setting}) + 1$

Figure 6-45. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz



$f_{DAC} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{OUT}(DSA \text{ Setting}) - P_{OUT}(DSA \text{ Setting} = 0) + (DSA \text{ Setting})$

Figure 6-46. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz

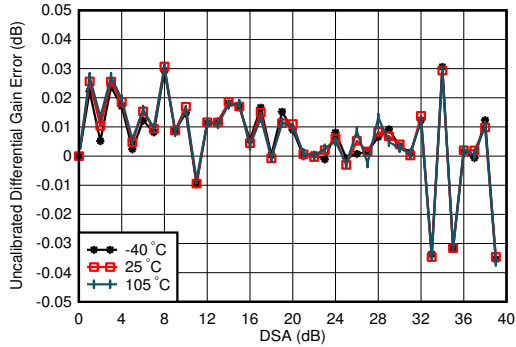


$f_{DAC} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{OUT}(DSA \text{ Setting}) - P_{OUT}(DSA \text{ Setting} = 0) + (DSA \text{ Setting})$

Figure 6-47. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz

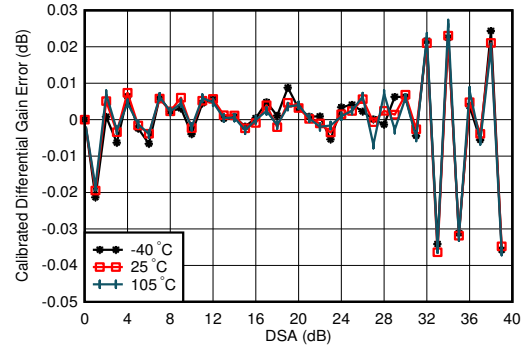
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



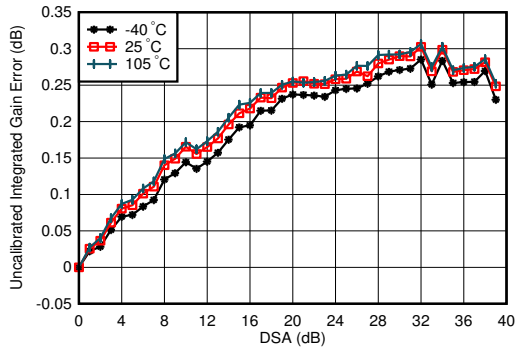
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-48. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz**



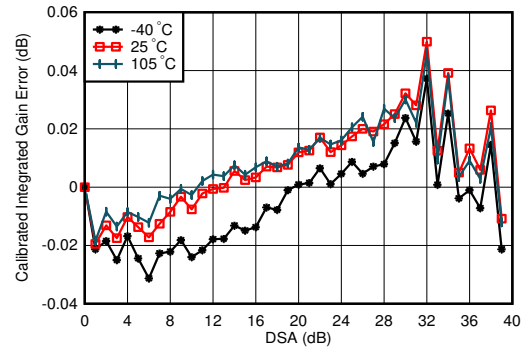
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-49. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz**



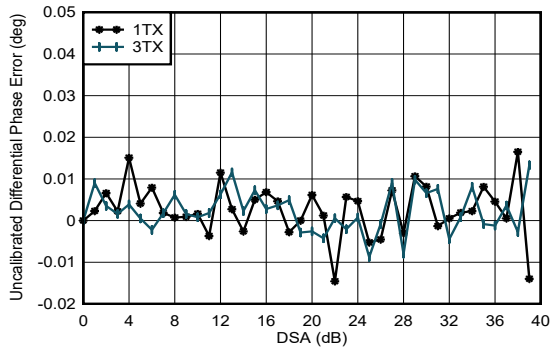
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-50. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz**



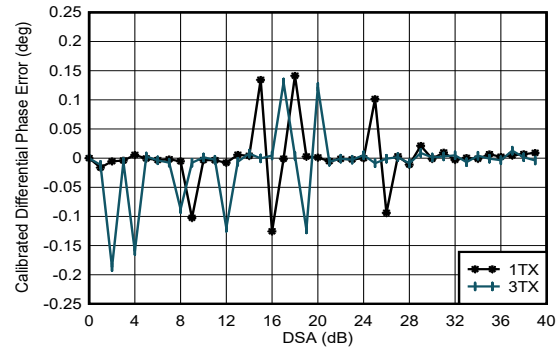
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-51. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz**



$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-52. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz**

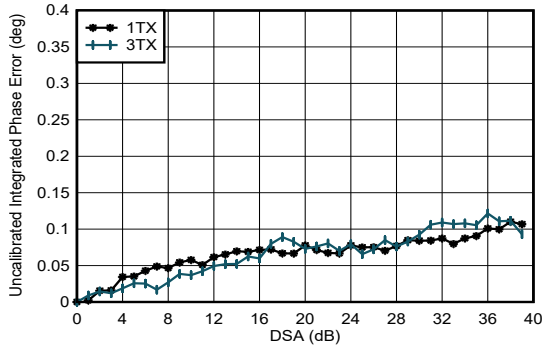


$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$   
Phase DNL spike may occur at any DSA setting.

**Figure 6-53. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz**

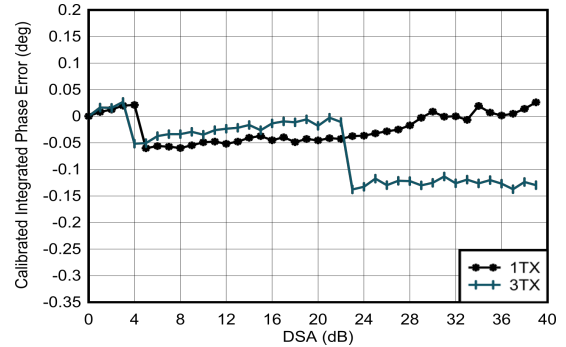
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



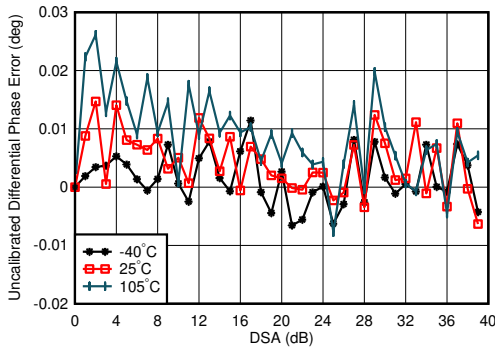
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-54. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz**



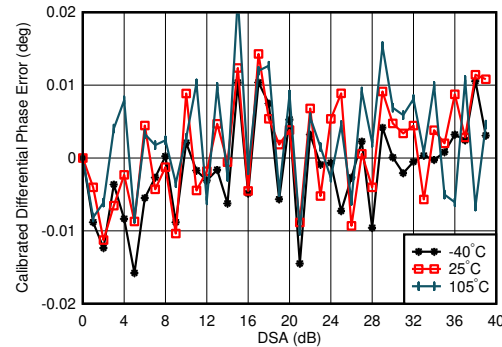
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-55. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz**



$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-56. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz**

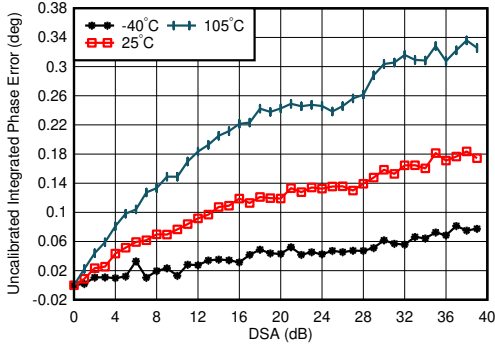


$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-57. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz**

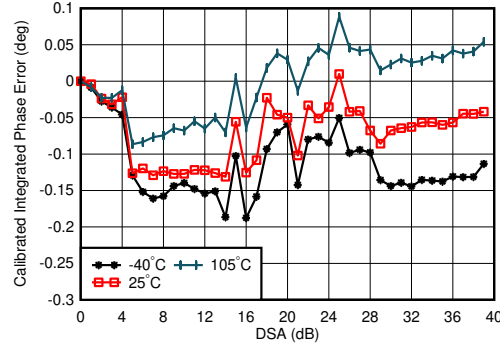
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



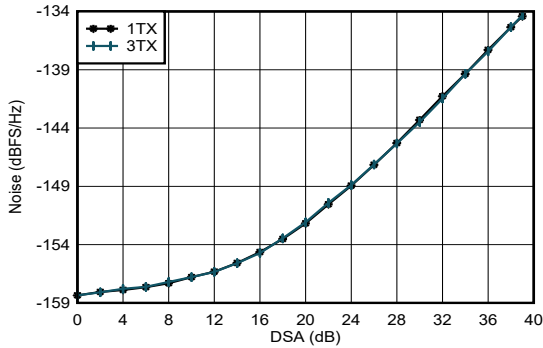
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-58. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz**



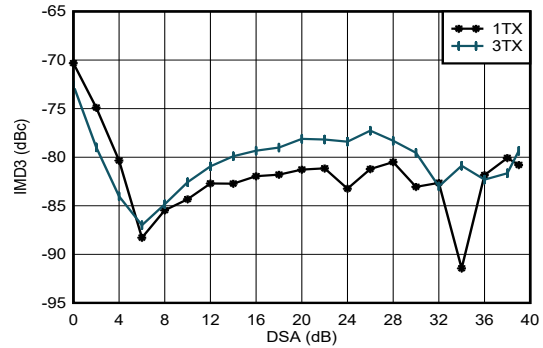
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-59. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz**



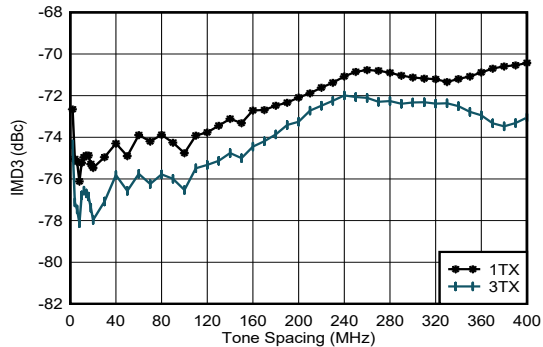
$f_{\text{DAC}} = 5898.24$  MSPS, interleave mode, matching at 1.8 GHz,  $P_{\text{OUT}} = -13$  dBFS

**Figure 6-60. TX Output Noise vs Channel and Attenuation at 1.8 GHz**



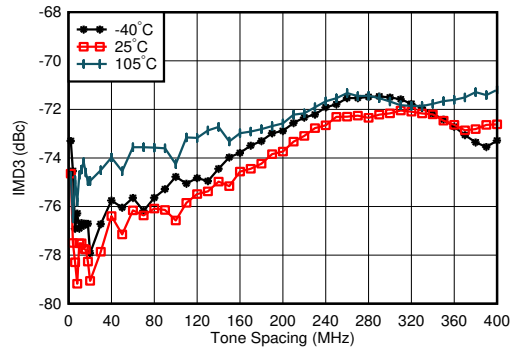
$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode,  $f_{\text{CENTER}} = 1.8$  GHz, matching at 1.8 GHz,  $-13$  dBFS each tone

**Figure 6-61. TX IMD3 vs DSA Setting at 1.8 GHz**



$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode,  $f_{\text{CENTER}} = 1.8$  GHz, matching at 1.8 GHz,  $-13$  dBFS each tone

**Figure 6-62. TX IMD3 vs Tone Spacing and Channel at 1.8 GHz**

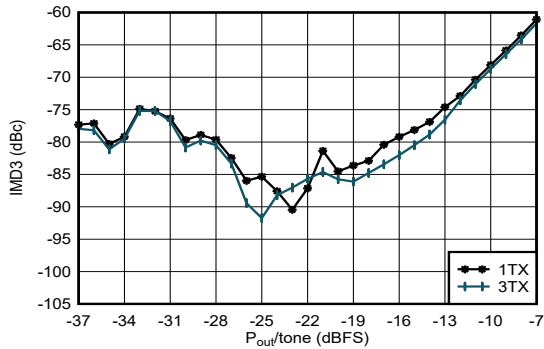


$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode,  $f_{\text{CENTER}} = 1.8$  GHz, matching at 1.8 GHz,  $-13$  dBFS each tone, worst channel

**Figure 6-63. TX IMD3 vs Tone Spacing and Temperature at 1.8 GHz**

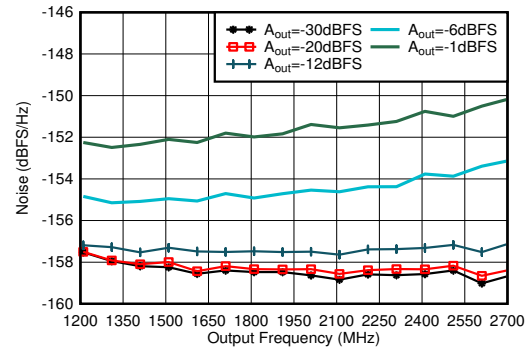
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



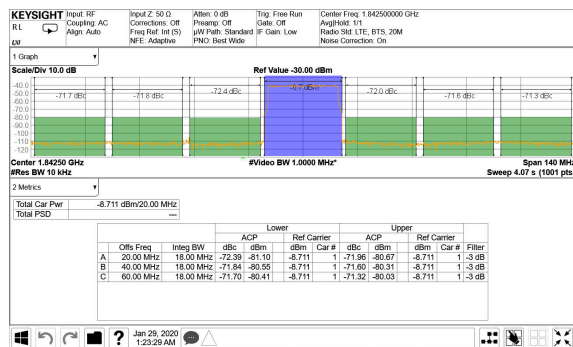
$f_{DAC} = 11796.48$  MSPS, interleave mode,  $f_{CENTER} = 1.8$  GHz,  
 $f_{SPACING} = 20$  MHz, matching at 1.8 GHz

**Figure 6-64. TX IMD3 vs Digital Level at 1.8 GHz**



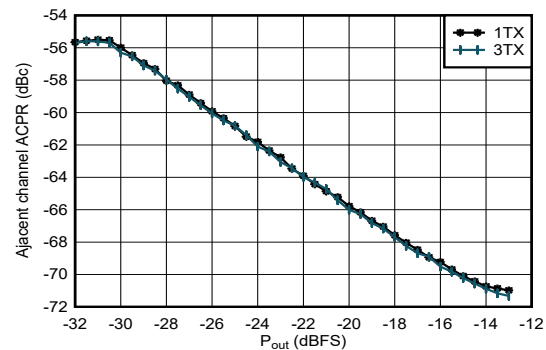
Matching at 2.6 GHz, Single tone,  $f_{DAC} = 11.79648$  GSPS,  
interleave mode, 40-MHz offset

**Figure 6-65. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz**



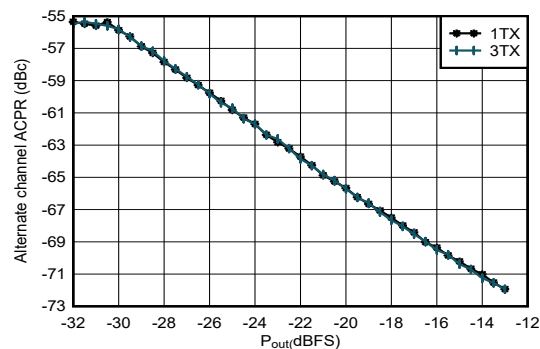
TM1.1,  $P_{OUT\_RMS} = -13$  dBFS

**Figure 6-66. TX 20-MHz LTE Output Spectrum at 1.8425 GHz**



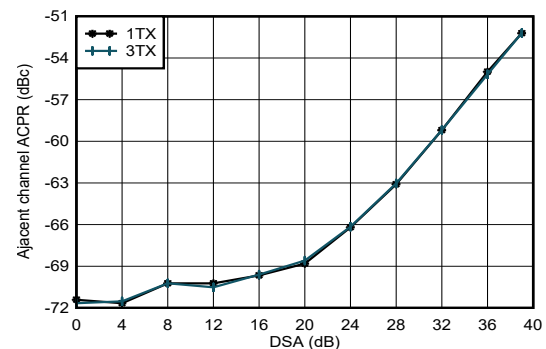
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-67. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz**



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-68. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz**

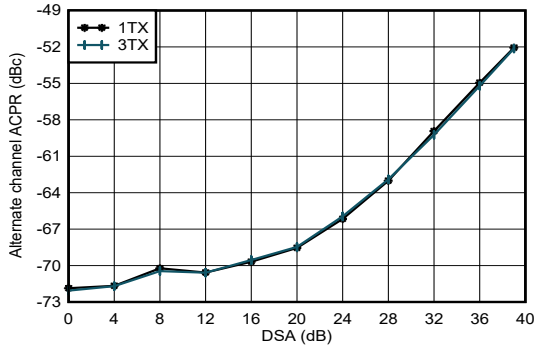


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-69. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz**

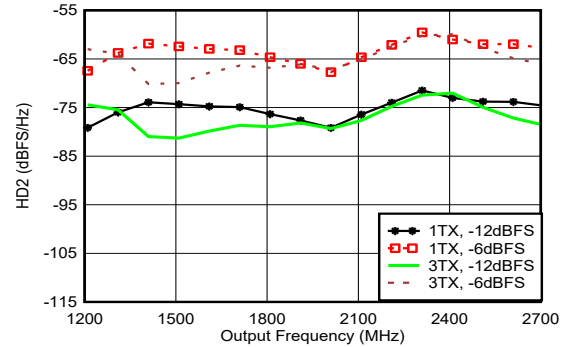
### 6.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



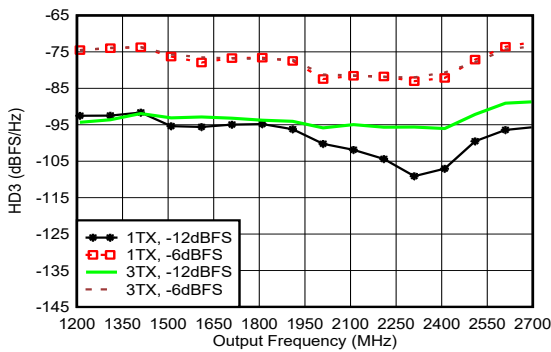
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-70. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz**



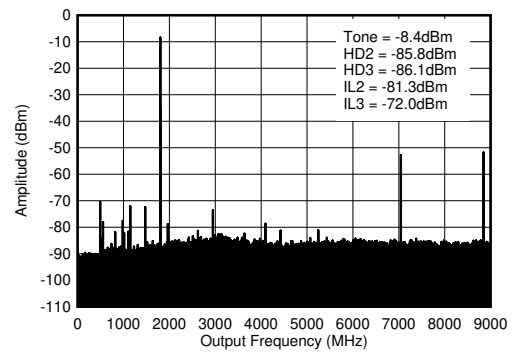
Matching at 1.8 GHz,  $f_{DAC} = 11.79648$  GSPPS, interleave mode, normalized to output power at harmonic frequency

**Figure 6-71. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz**



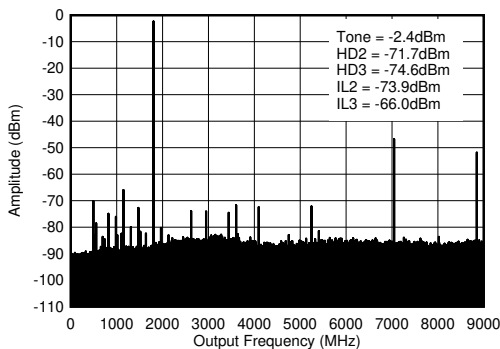
Matching at 1.8 GHz,  $f_{DAC} = 11.79648$  GSPPS, interleave mode, normalized to output power at harmonic frequency

**Figure 6-72. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz**



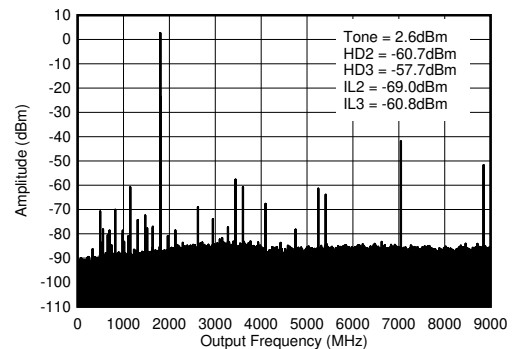
$f_{DAC} = 8847.36$  MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses.  $IL_n = f_S/n \pm f_{OUT}$  and is due to mixing with digital clocks.

**Figure 6-73. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{DAC}$ )**



$f_{DAC} = 8847.36$  MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses.  $IL_n = f_S/n \pm f_{OUT}$  and is due to mixing with digital clocks.

**Figure 6-74. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{DAC}$ )**

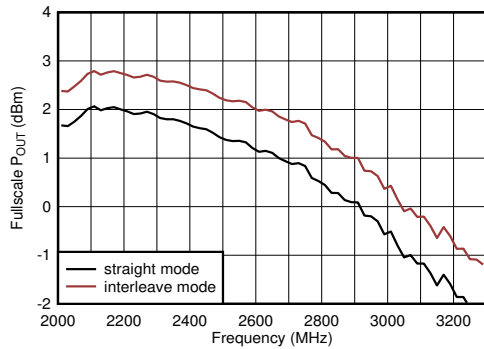


$f_{DAC} = 8847.36$  MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses.  $IL_n = f_S/n \pm f_{OUT}$  and is due to mixing with digital clocks.

**Figure 6-75. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ( $0-f_{DAC}$ )**

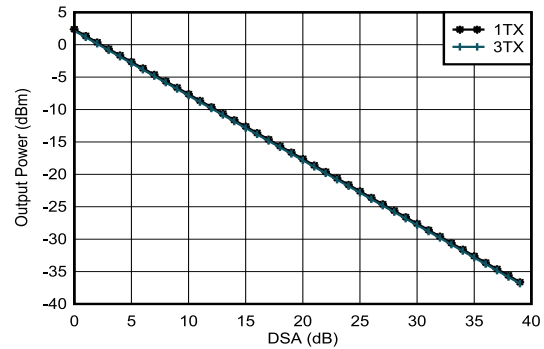
### 6.12.3 TX Typical Characteristics at 2.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



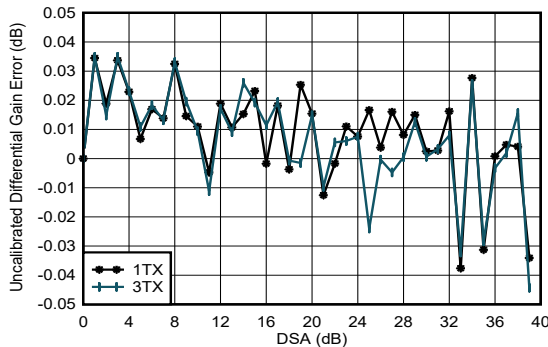
Including PCB and cable losses,  $A_{\text{out}} = -0.5$  dBFS, DSA = 0, 2.6 GHz matching

**Figure 6-76. TX Full Scale vs RF Frequency at 11796.48 MSPS**



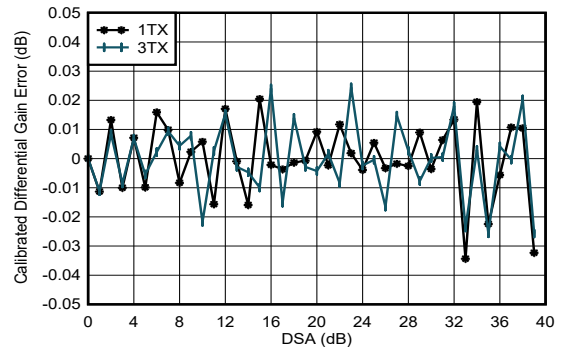
$f_{\text{DAC}} = 8847.36$  MSPS,  $A_{\text{out}} = -0.5$  dBFS, matching 2.6 GHz

**Figure 6-77. TX Output Power vs DSA Setting and Channel at 2.6 GHz**



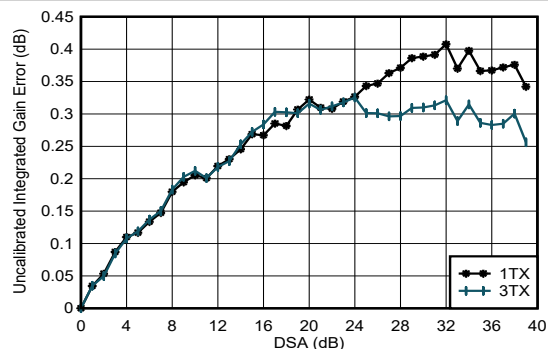
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-78. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz**



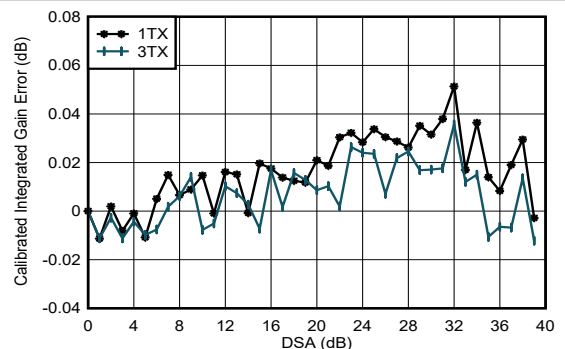
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-79. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz**



$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-80. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz**

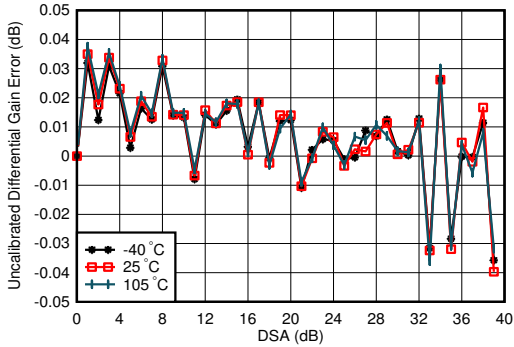


$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-81. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz**

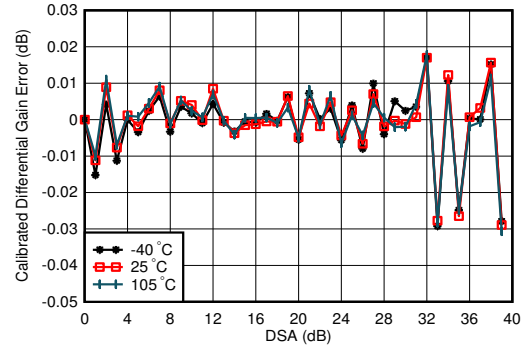
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



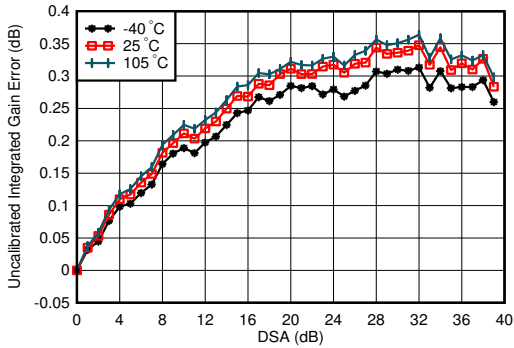
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-82. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz**



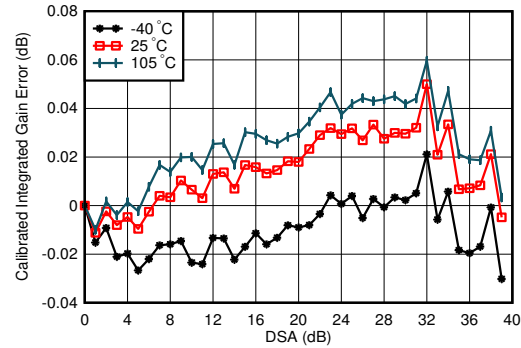
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-83. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz**



$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-84. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz**



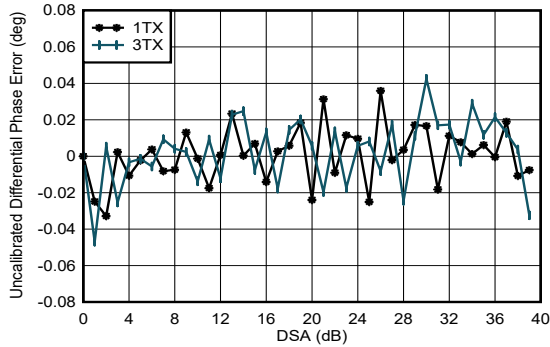
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-85. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz**



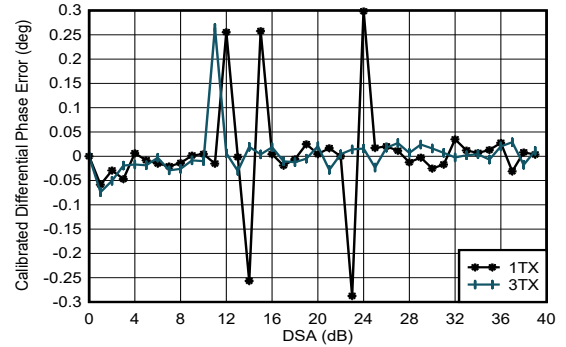
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

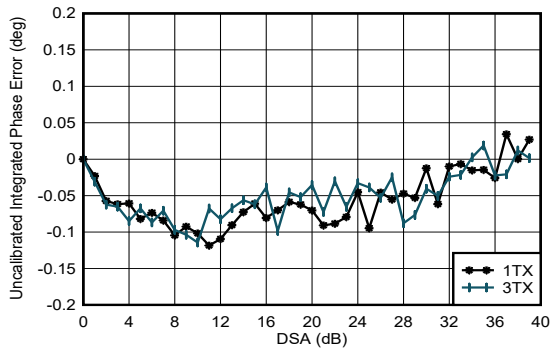
**Figure 6-86. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz**



$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

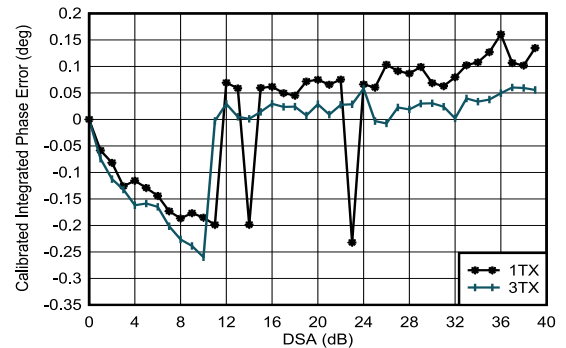
Phase DNL spike may occur at any DSA setting.

**Figure 6-87. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz**



$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-88. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz**

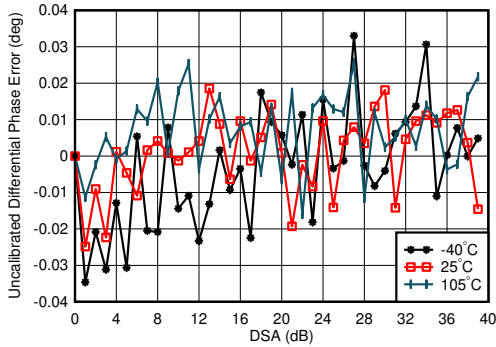


$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-89. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz**

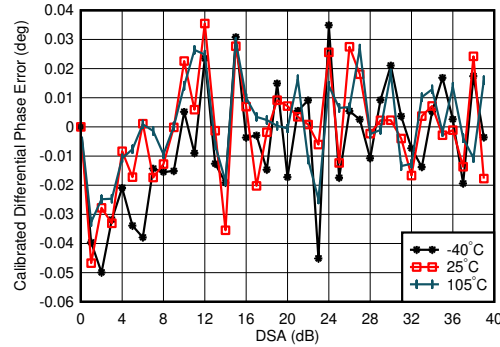
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



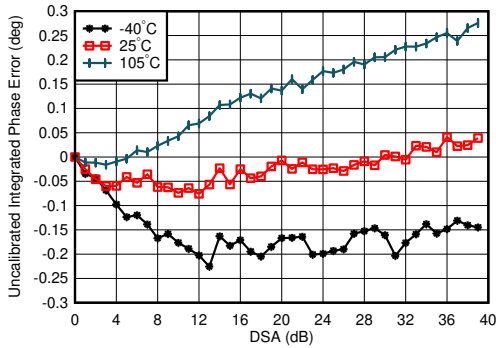
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-90. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz**



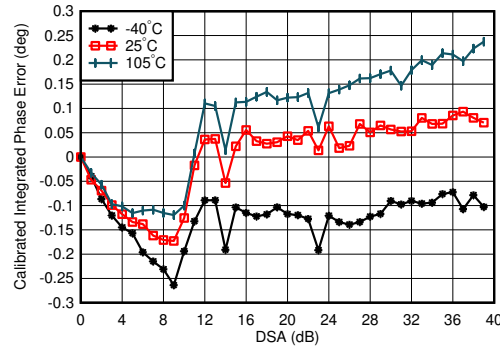
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-91. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz**



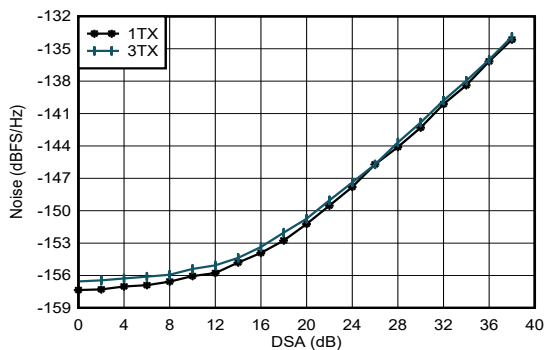
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz, channel with the medium variation over DSA setting at 25°C  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-92. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz**



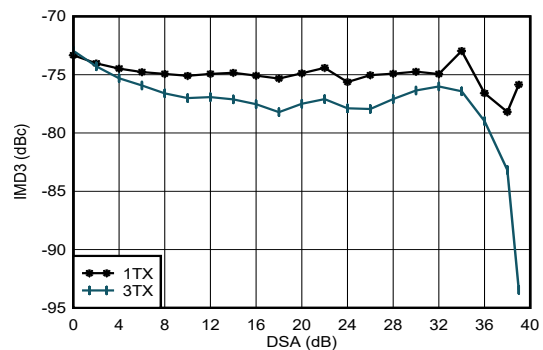
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-93. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz**



$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, matching at 2.6 GHz,  $P_{\text{OUT}} = -13$  dBFS

**Figure 6-94. TX Output Noise vs Channel and Attenuation at 2.6 GHz**

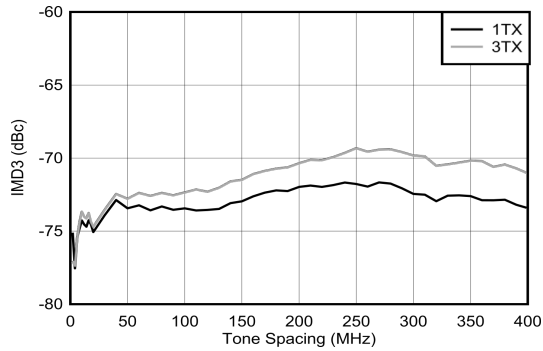


$f_{\text{DAC}} = 8847.36$  MSPS, straight mode,  $f_{\text{CENTER}} = 2.6$  GHz, matching at 2.6 GHz,  $-13$  dBFS each tone

**Figure 6-95. TX IMD3 vs DSA Setting at 2.6 GHz**

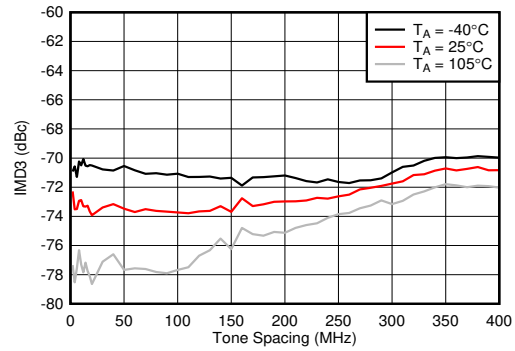
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



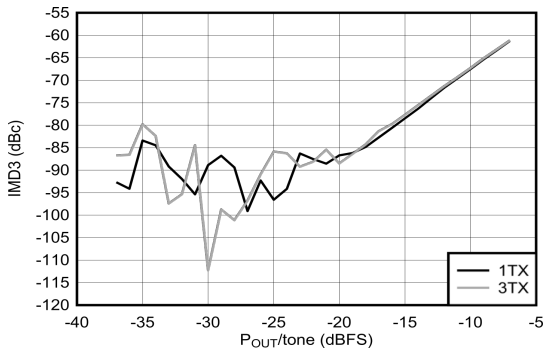
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode,  $f_{\text{CENTER}} = 2.6$  GHz, matching at 2.6 GHz, -13 dBFS each tone

Figure 6-96. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz



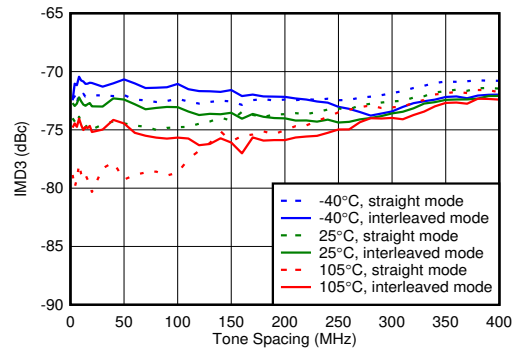
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode,  $f_{\text{CENTER}} = 2.6$  GHz, matching at 2.6 GHz, -13 dBFS each tone, worst channel.

Figure 6-97. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



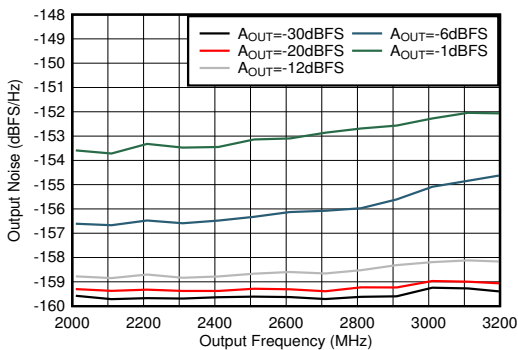
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode,  $f_{\text{CENTER}} = 2.6$  GHz,  $f_{\text{SPACING}} = 20$  MHz, matching at 2.6 GHz

Figure 6-98. TX IMD3 vs Digital Level at 2.6 GHz



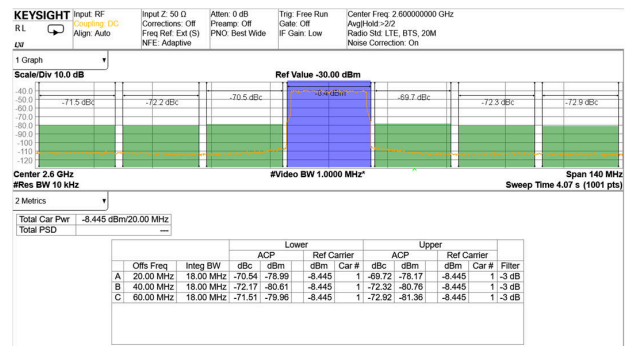
$f_{\text{DAC}} = 8847.36$  MSPS, straight mode,  $f_{\text{CENTER}} = 2.6$  GHz, matching at 2.6 GHz, -13 dBFS each tone

Figure 6-99. TX IMD3 vs Tone Spacing and Temperature



Matching at 2.6 GHz, Single tone,  $f_{\text{DAC}} = 11.79648$  GSPS, interleave mode, 40-MHz offset

Figure 6-100. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz

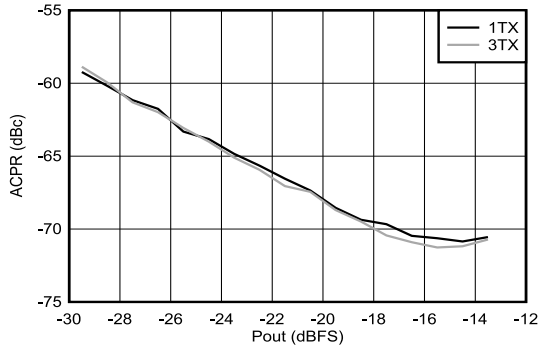


TM1.1,  $P_{\text{OUT\_RMS}} = -13$  dBFS

Figure 6-101. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)

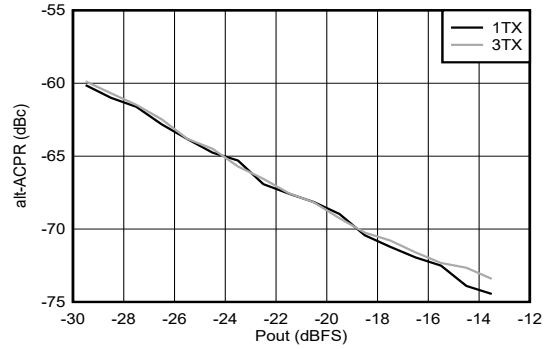
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



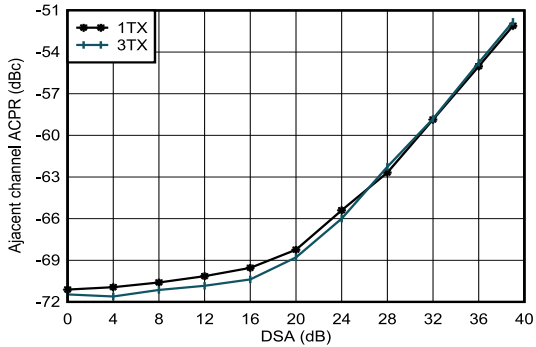
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-102. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz**



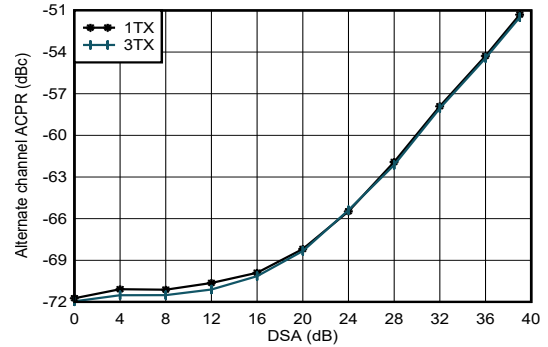
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-103. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz**



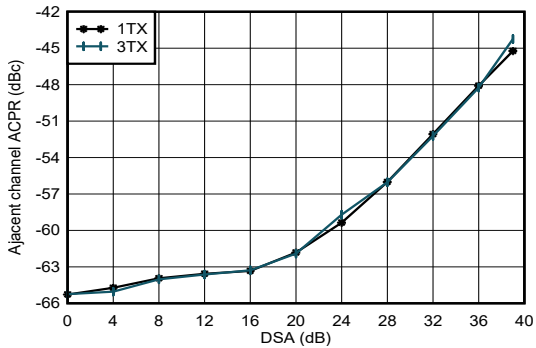
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-104. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz**



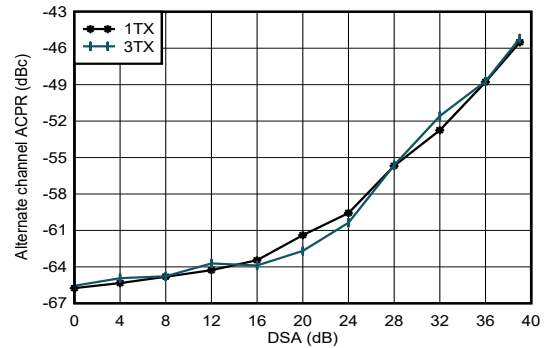
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-105. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz**



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-106. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz**

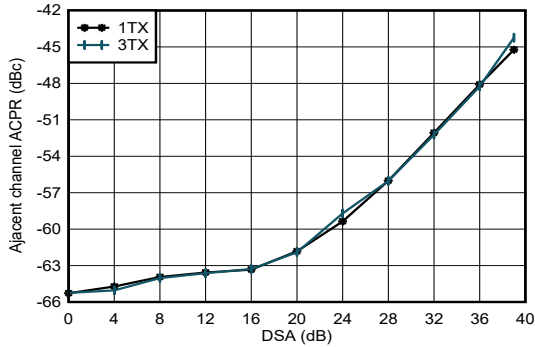


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-107. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz**

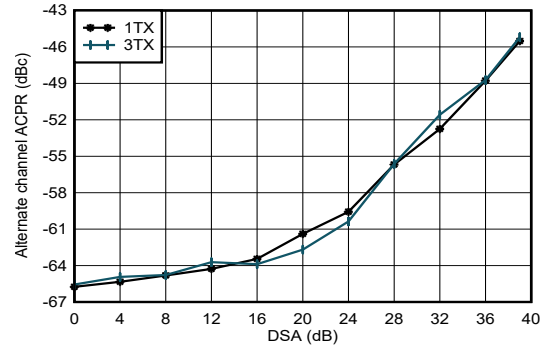
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



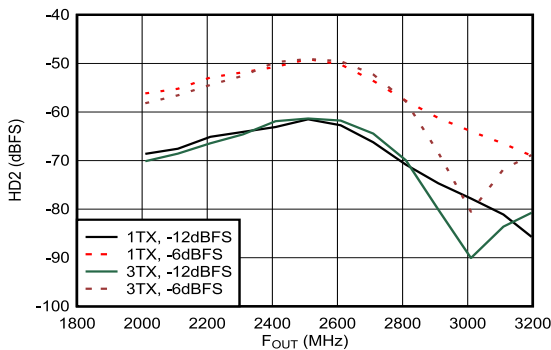
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 6-108. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



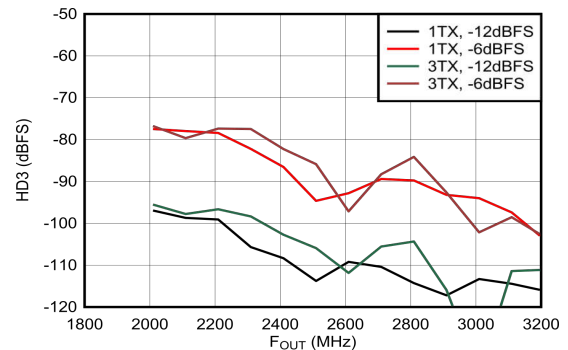
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 6-109. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



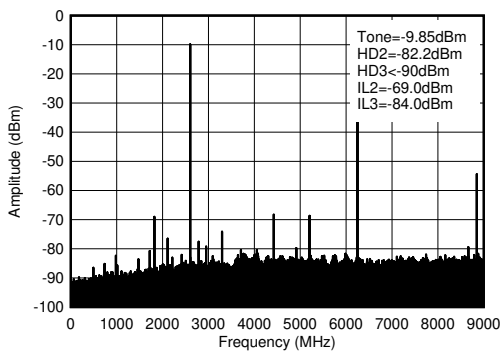
Matching at 2.6 GHz,  $f_{\text{DAC}} = 11.79648$  GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 6-110. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz



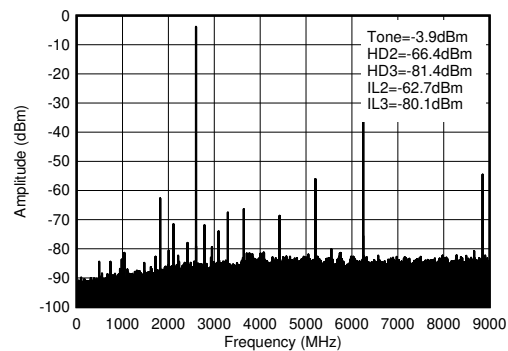
Matching at 2.6 GHz,  $f_{\text{DAC}} = 11.79648$  GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 6-111. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz



$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

Figure 6-112. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )

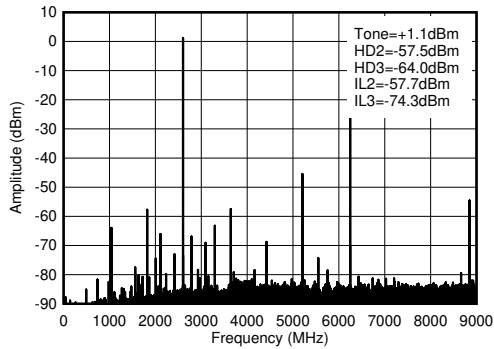


$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

Figure 6-113. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )

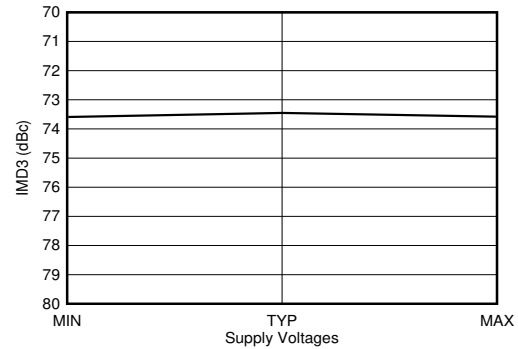
### 6.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 8847.36$  MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses.  $\text{IL}_n = f_s/n \pm f_{\text{OUT}}$  and is due to mixing with digital clocks.

**Figure 6-114. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ( $0-f_{\text{DAC}}$ )**

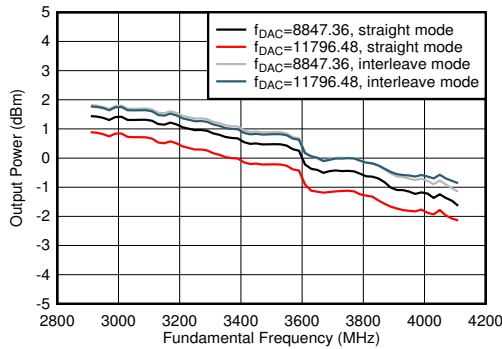


$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = -13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

**Figure 6-115. TX IMD3 vs Supply Voltage at 2.6 GHz**

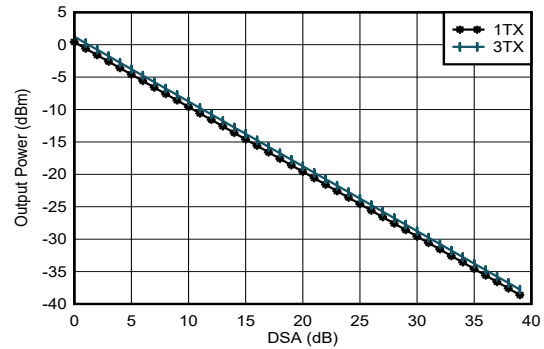
### 6.12.4 TX Typical Characteristics at 3.5 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



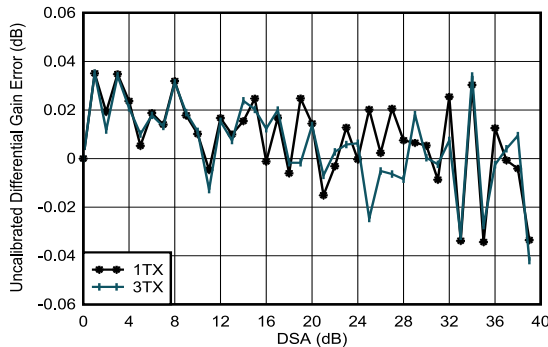
$A_{\text{out}} = -0.5\text{dBFS}$ , 3.5 GHz Matching, included PCB and cable losses

**Figure 6-116. TX Output Power vs Frequency**



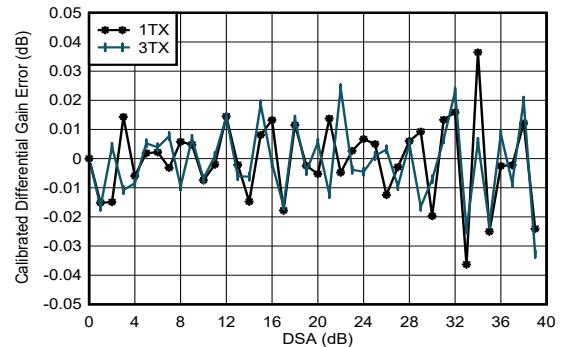
$A_{\text{out}} = -0.5\text{dBFS}$ , 3.5 GHz Matching, included PCB and cable losses

**Figure 6-117. TX Output Power vs DSA Setting at 3.5 GHz**



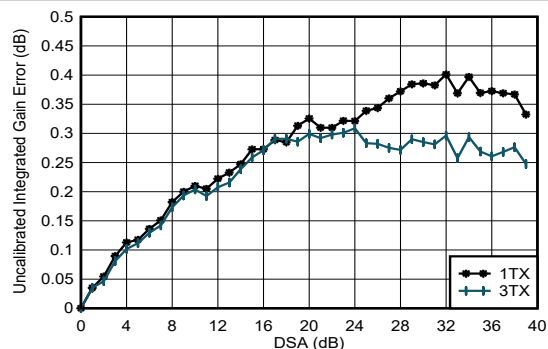
3.5 GHz Matching, included PCB and cable losses  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-118. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz**



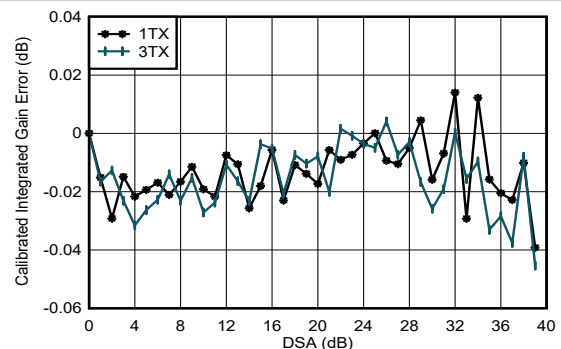
3.5 GHz Matching, included PCB and cable losses  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-119. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz**



3.5 GHz Matching, included PCB and cable losses  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-120. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz**

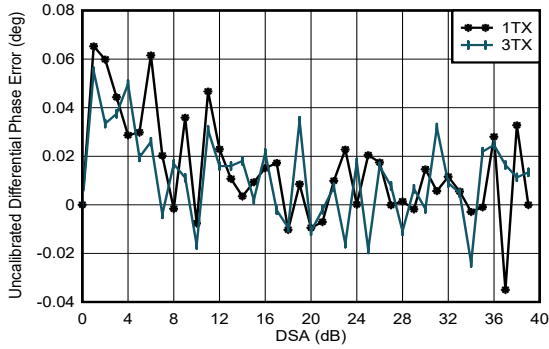


3.5 GHz Matching, included PCB and cable losses  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-121. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz**

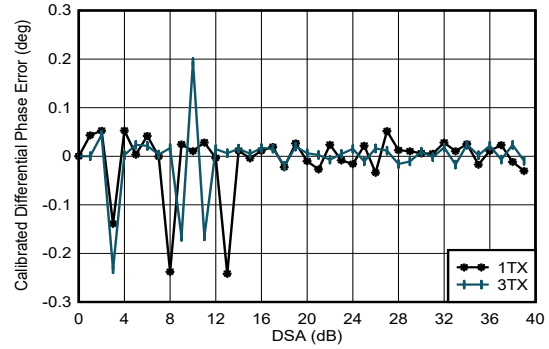
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



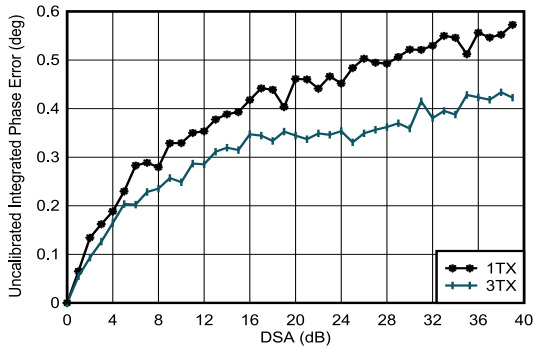
3.5 GHz Matching, included PCB and cable losses

**Figure 6-122. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz**



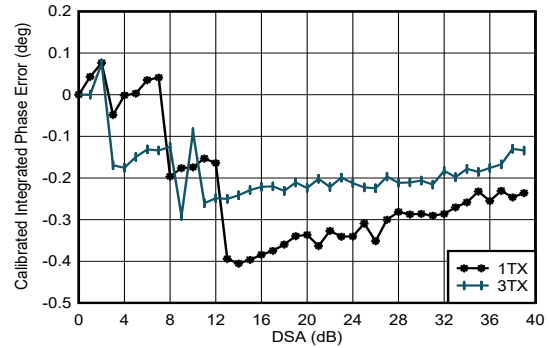
3.5 GHz Matching, included PCB and cable losses  
Phase DNL spike may occur at any DSA setting.

**Figure 6-123. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz**



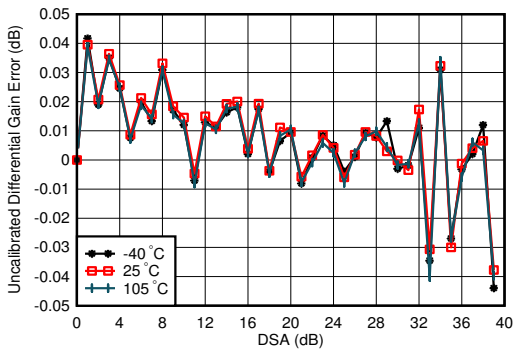
3.5 GHz Matching, included PCB and cable losses

**Figure 6-124. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz**



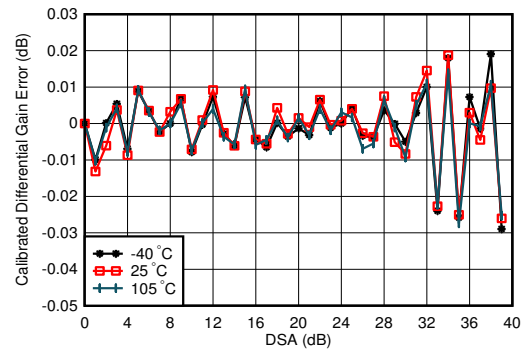
3.5 GHz Matching, included PCB and cable losses

**Figure 6-125. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz**



3.5 GHz Matching, 1TX

**Figure 6-126. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz**



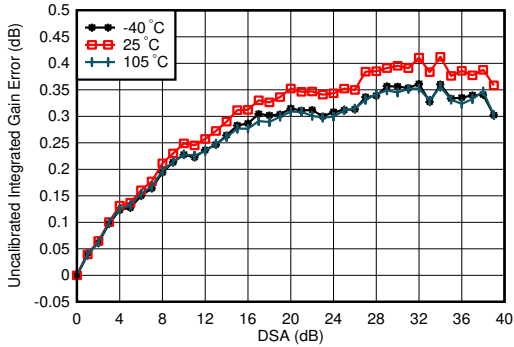
3.5 GHz Matching, 1TX, Calibrated at 25°C

**Figure 6-127. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz**



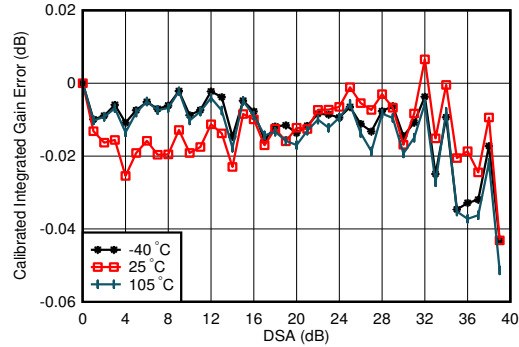
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



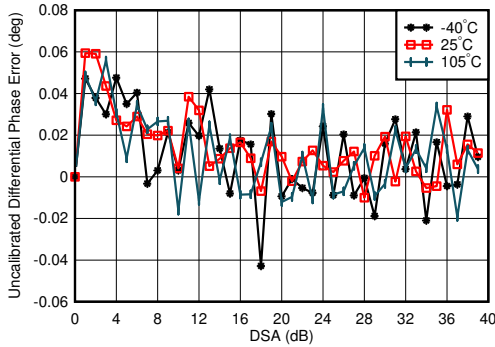
3.5 GHz Matching, 1TX

**Figure 6-128. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz**



3.5 GHz Matching, 1TX, Calibrated at 25°C

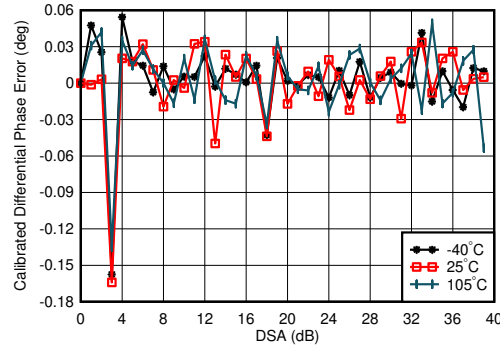
**Figure 6-129. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz**



3.5 GHz Matching, 1TX

$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

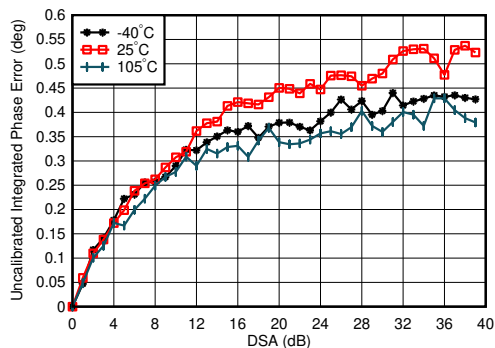
**Figure 6-130. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz**



3.5 GHz Matching, 1TX, Calibrated at 25°C

$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

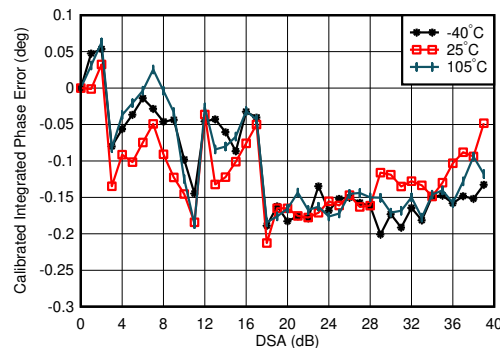
**Figure 6-131. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz**



3.5 GHz Matching, 1TX

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 6-132. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz**



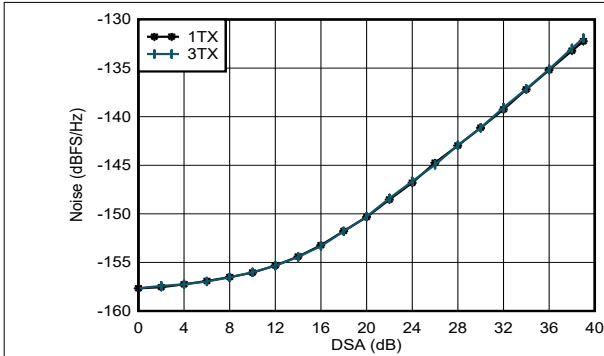
3.5 GHz Matching, 1TX, Calibrated at 25°C

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**Figure 6-133. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz**

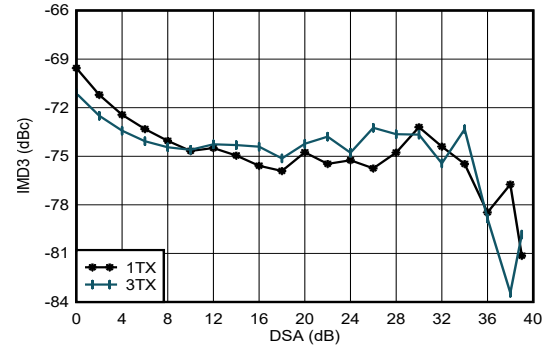
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



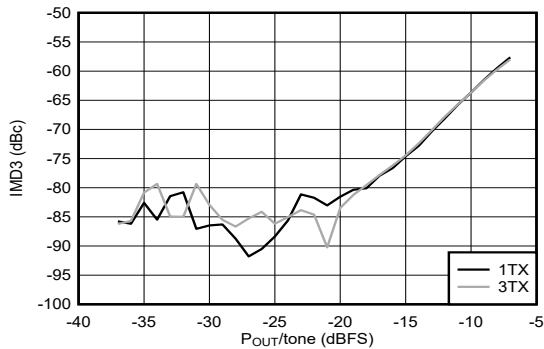
A.  $f_{\text{DAC}} = 11796.48$  MSPS, interleave mode, matching at 3.5 GHz,  $A_{\text{out}} = -13$  dBFS.

**Figure 6-134. TX NSD vs DSA Setting at 3.5 GHz**



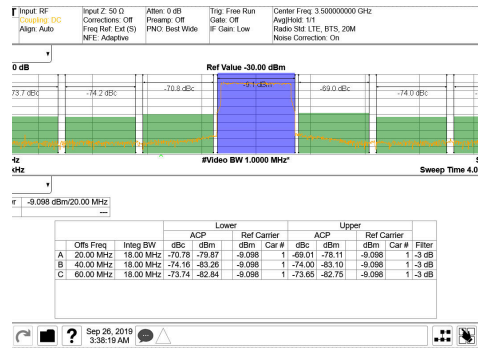
20-MHz tone spacing, 3.5 GHz Matching,  $-13$  dBFS each tone, included PCB and cable losses

**Figure 6-135. TX IMD3 vs DSA Setting at 3.5 GHz**



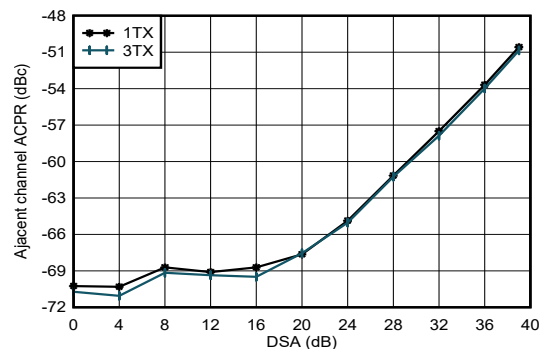
20-MHz tone spacing, 3.5 GHz Matching

**Figure 6-136. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz**



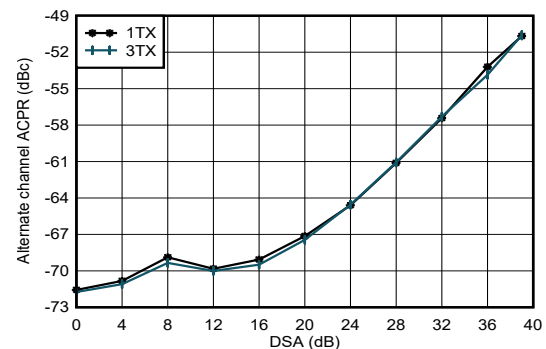
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-137. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)**



3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-138. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz**

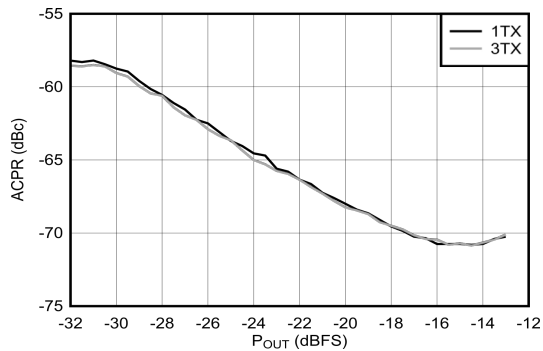


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-139. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz**

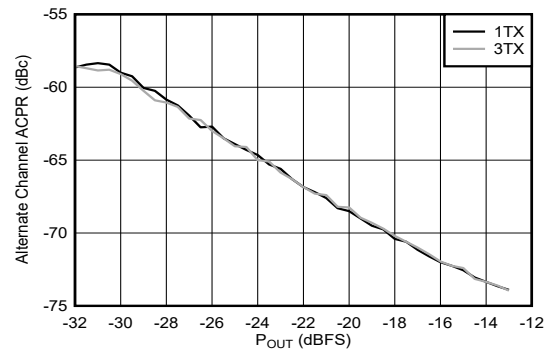
### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



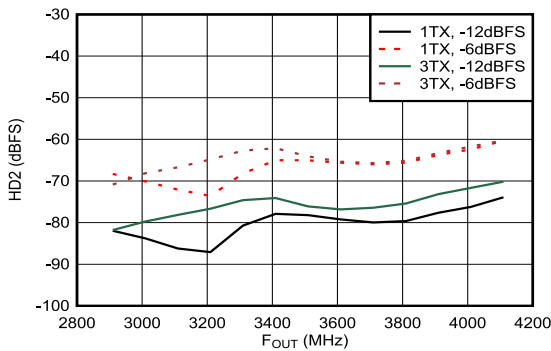
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 6-140. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz



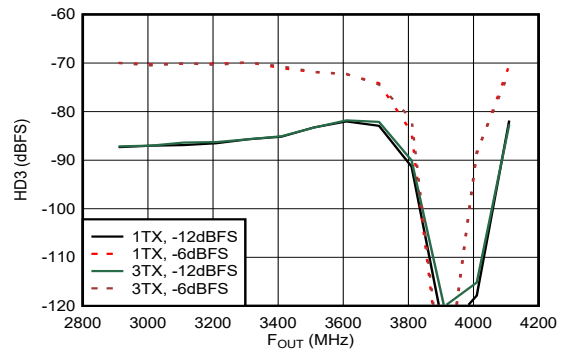
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 6-141. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz



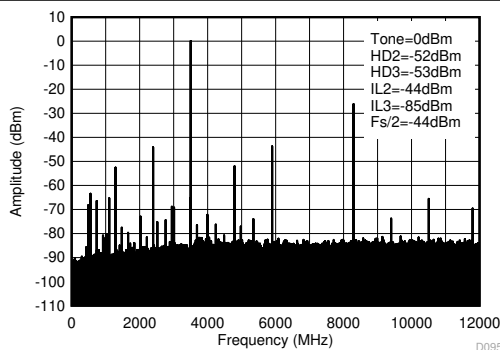
Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648$  GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 6-142. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



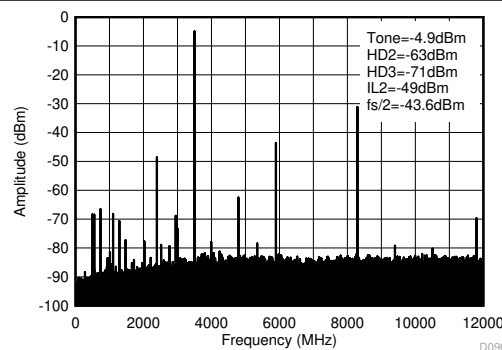
Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648$  GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

Figure 6-143. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz



Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648$  GSPS, interleave mode.

Figure 6-144. TX Single Tone (-1 dBFS) Output Spectrum at 3.5 GHz (0 -  $f_{\text{DAC}}$ )

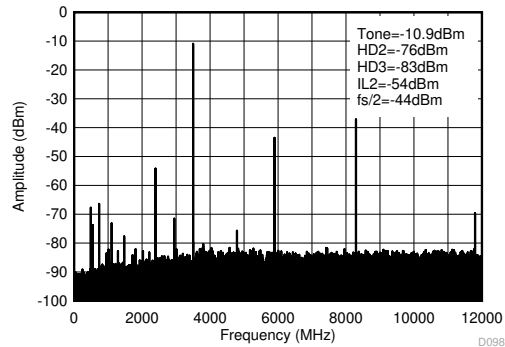


Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648$  GSPS, interleave mode.

Figure 6-145. TX Single Tone (-6 dBFS) Output Spectrum at 3.5 GHz (0 -  $f_{\text{DAC}}$ )

### 6.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled

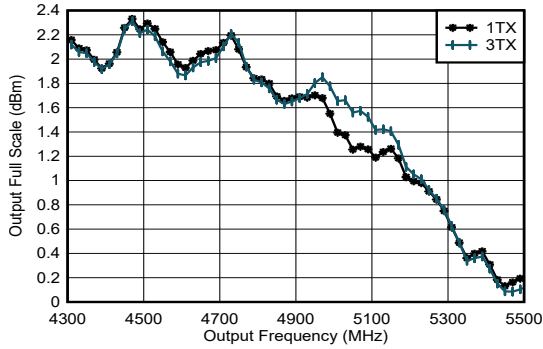


Matching at 3.5 GHz,  $f_{\text{DAC}} = 11.79648$  GSPS, interleave mode.

**Figure 6-146. TX Single Tone (-12 dBFS) Output Spectrum at 3.5 GHz (0- $f_{\text{DAC}}$ )**

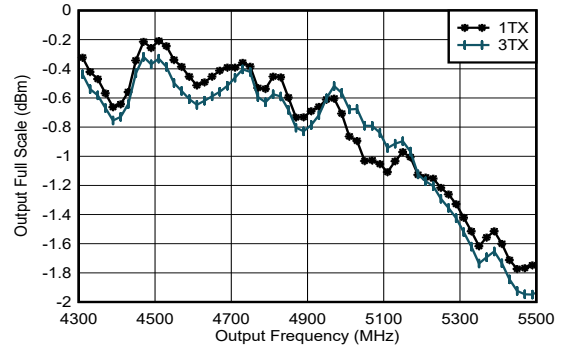
### 6.12.5 TX Typical Characteristics at 4.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



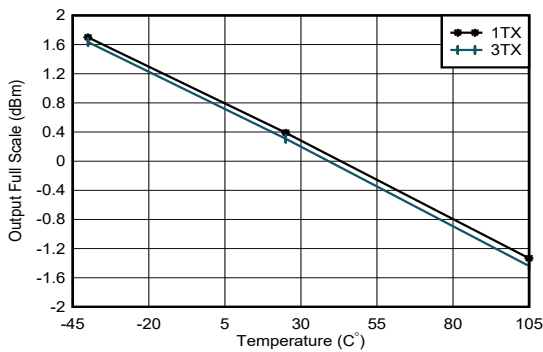
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5$  dBFS, DSA = 0, 4.9 GHz matching

**Figure 6-147. TX Full Scale vs RF Frequency and Channel at 11796.48 MSPS**



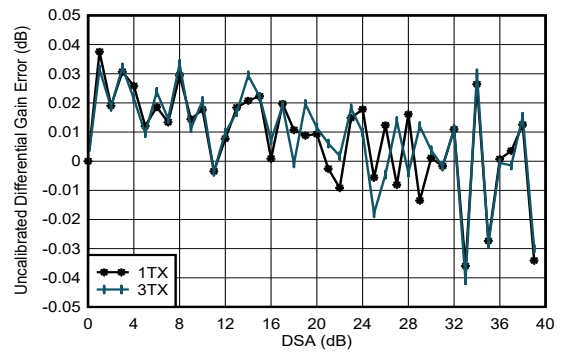
Excluding PCB and cable losses,  $A_{\text{out}} = -0.5$  dBFS, DSA = 0, 4.9 GHz matching

**Figure 6-148. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Straight Mode, 2nd Nyquist Zone**



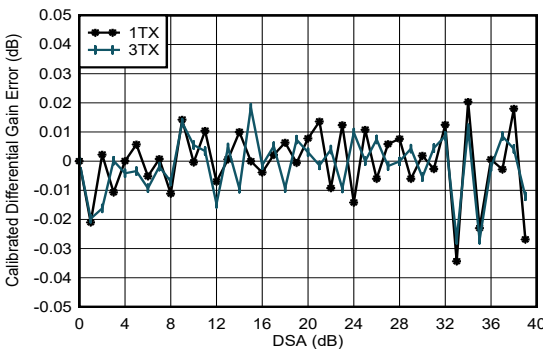
$f_{\text{DAC}} = 11796.48$  MSPS,  $A_{\text{out}} = -0.5$  dBFS, matching 4.9 GHz

**Figure 6-149. TX Output Power vs DSA Setting and Channel at 4.9 GHz**



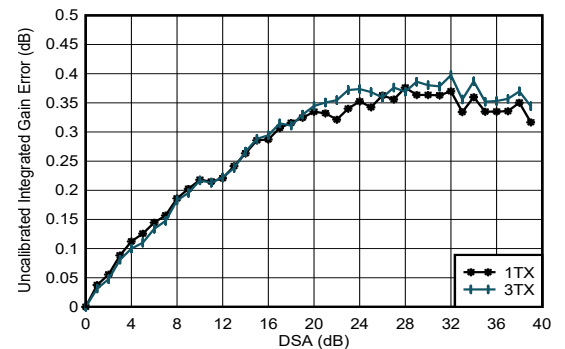
$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode, matching at 4.9 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-150. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz**



$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode, matching at 4.9 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-151. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz**

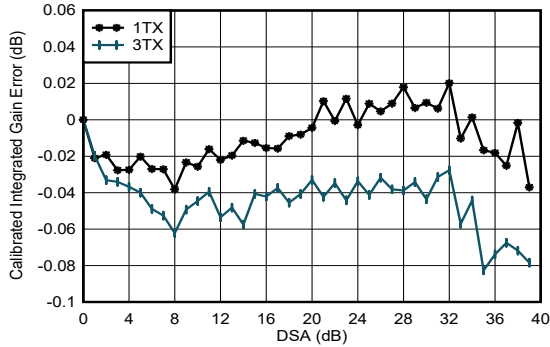


$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode, matching at 4.9 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-152. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz**

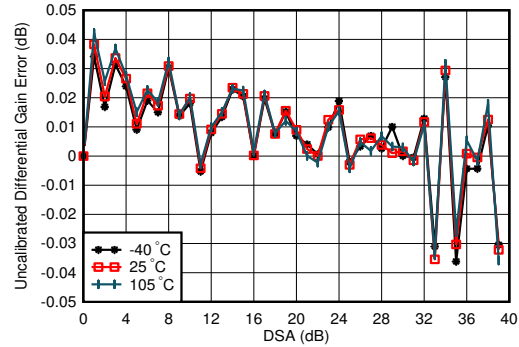
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



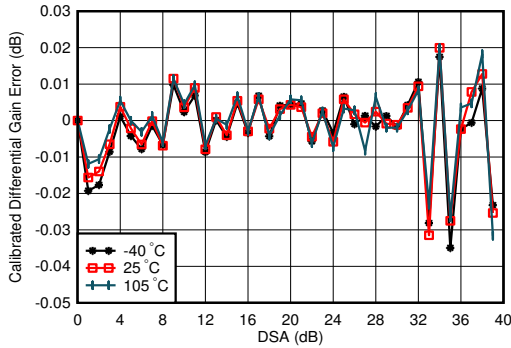
$f_{\text{DAC}} = 11796.48$  MSPS, interleave mode, matching at 4.9 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-153. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz**



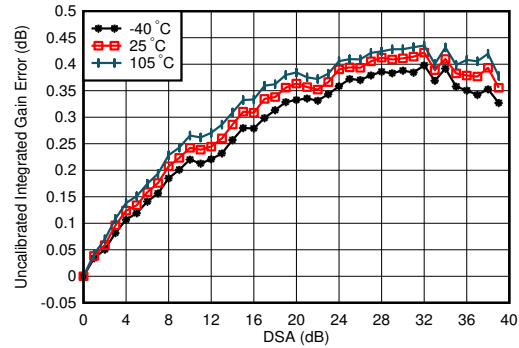
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-154. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz**



$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz  
Differential Gain Error =  $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

**Figure 6-155. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz**

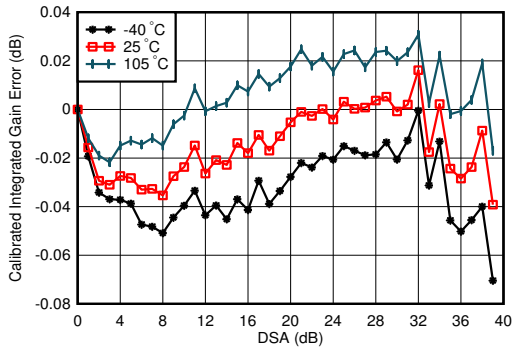


$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz  
Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-156. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz**

### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

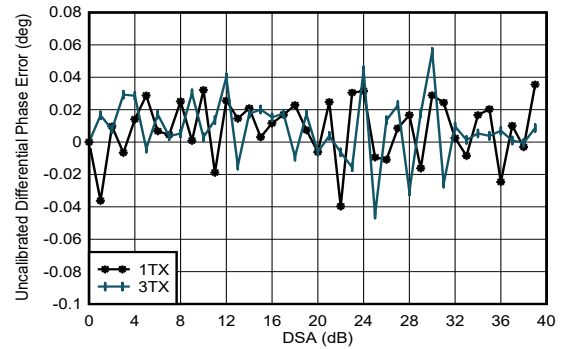
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz

Integrated Gain Error =  $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

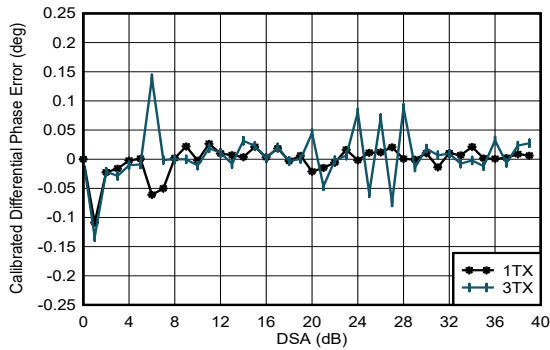
**Figure 6-157. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz**



$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-158. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz**

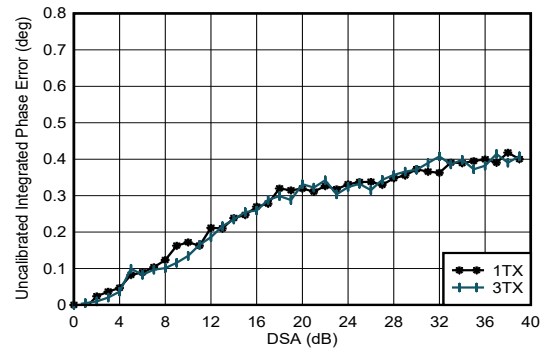


$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Phase DNL spike may occur at any DSA setting.

**Figure 6-159. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz**



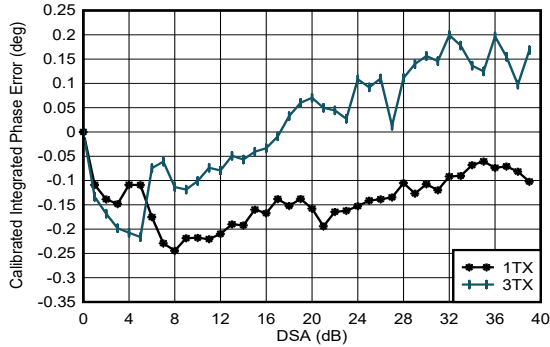
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-160. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz**

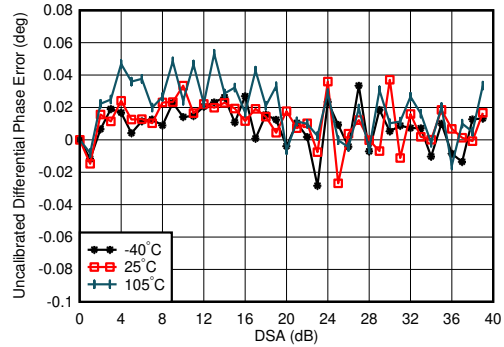
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



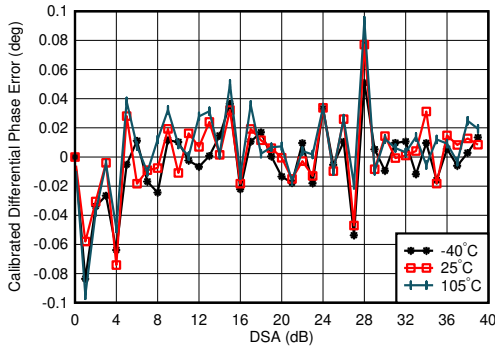
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-161. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz**



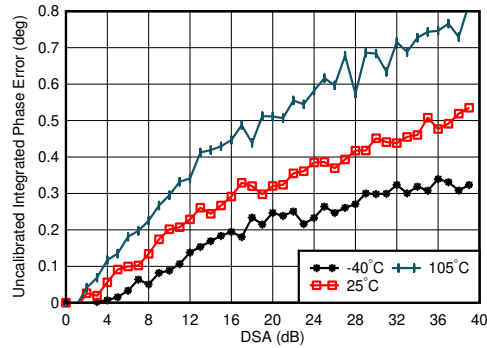
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-162. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz**



$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz  
 Differential Phase Error =  $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

**Figure 6-163. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz**



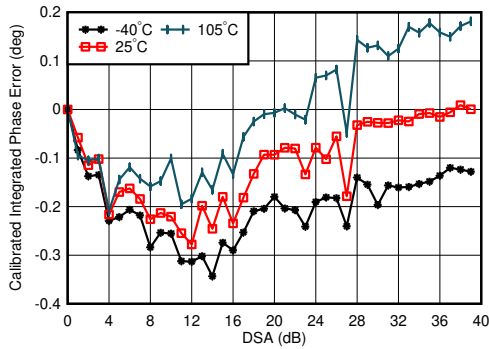
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz  
 Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-164. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz**



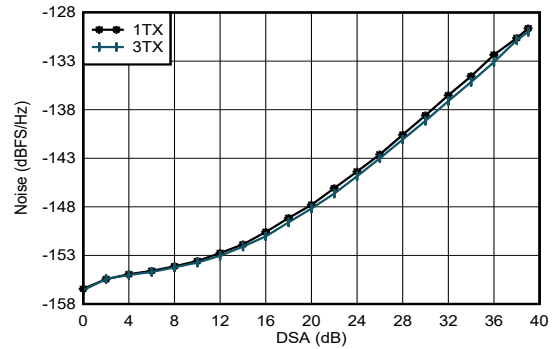
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



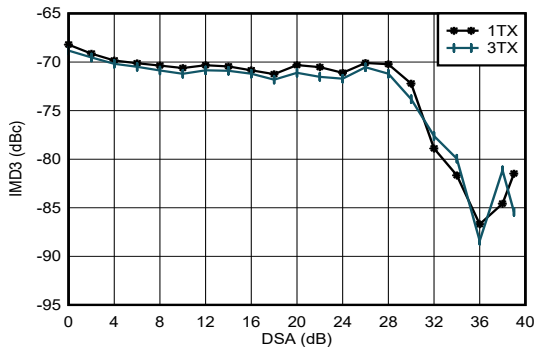
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz, channel with the median variation over DSA setting at  $25^\circ\text{C}$   
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-165. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz**



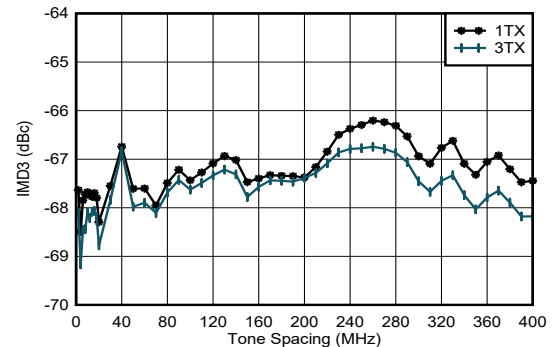
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz,  $P_{\text{OUT}} = -13$  dBFS

**Figure 6-166. TX Output Noise vs Channel and Attenuation at 2.6 GHz**



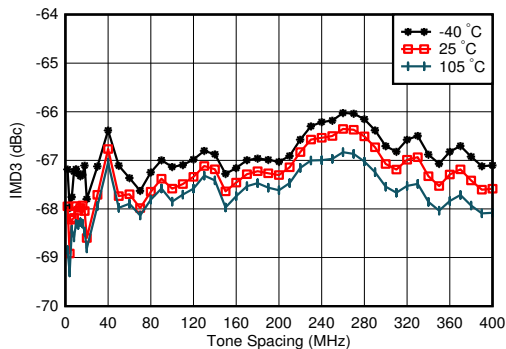
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ ,  $-13$  dBFS each tone

**Figure 6-167. TX IMD3 vs DSA Setting at 4.9 GHz**



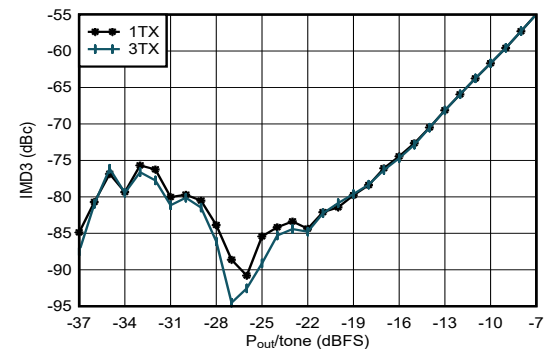
$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9\text{GHz}$ ,  $-13$  dBFS each tone

**Figure 6-168. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz**



$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9$  GHz,  $-13$  dBFS each tone, worst channel

**Figure 6-169. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz**

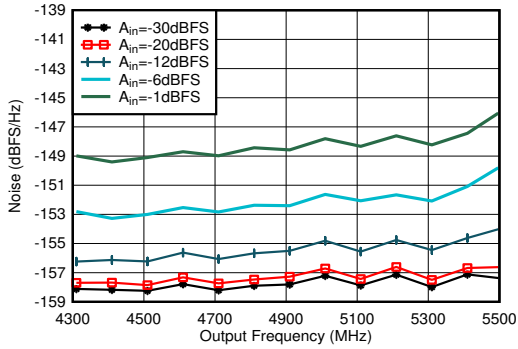


$f_{\text{DAC}} = 11796.48$  MSPS, interleaved mode, matching at 4.9 GHz,  $f_{\text{CENTER}} = 4.9$  GHz,  $f_{\text{SPACING}} = 20$  MHz

**Figure 6-170. TX IMD3 vs Digital Level at 4.9 GHz**

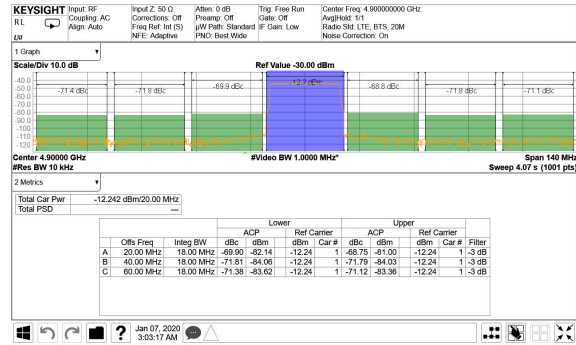
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



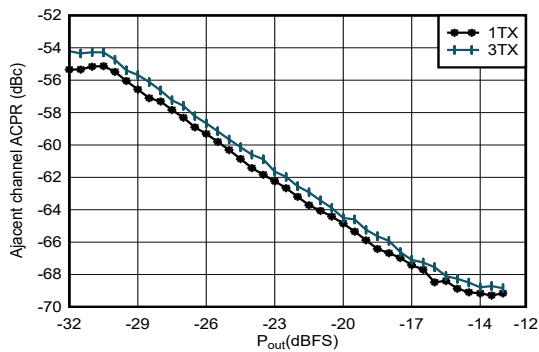
Matching at 4.9 GHz, Single tone,  $f_{DAC} = 11.79648$  GSPS, interleave mode, 40-MHz offset, DSA=0dB

**Figure 6-171. TX Single Tone Output Noise vs Frequency and Amplitude at 4.9 GHz**



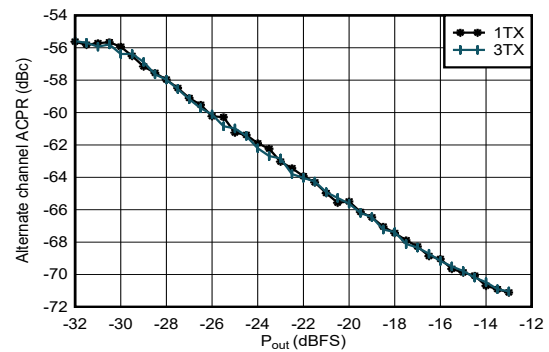
TM1.1,  $P_{OUT\_RMS} = -13$  dBFS

**Figure 6-172. TX 20-MHz LTE Output Spectrum at 4.9 GHz**



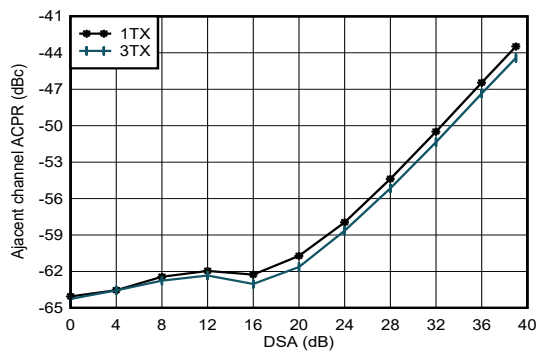
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-173. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz**



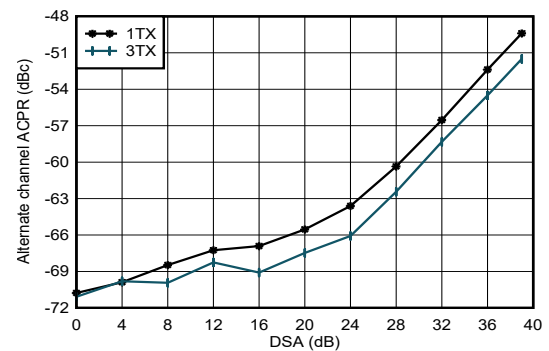
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-174. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz**



Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-175. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz**

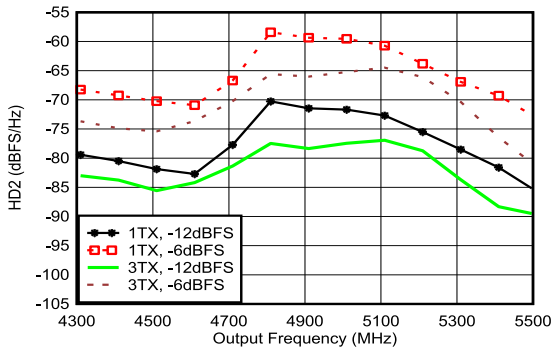


Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

**Figure 6-176. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz**

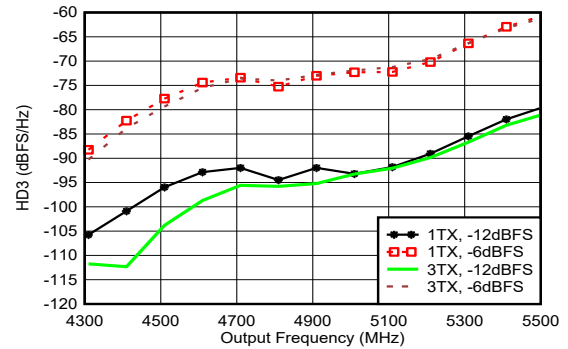
### 6.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), interleave mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB,  $\text{Sin}(x)/x$  enabled, DSA calibrated, TX Clock Dither Enabled



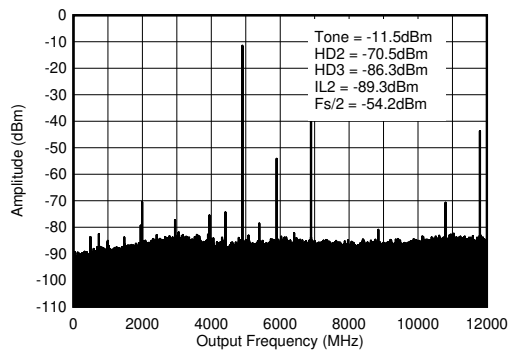
Matching at 4.9 GHz,  $f_{DAC} = 11.79648$  GSPPS, interleave mode, normalized to output power at harmonic frequency

**Figure 6-177. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz**



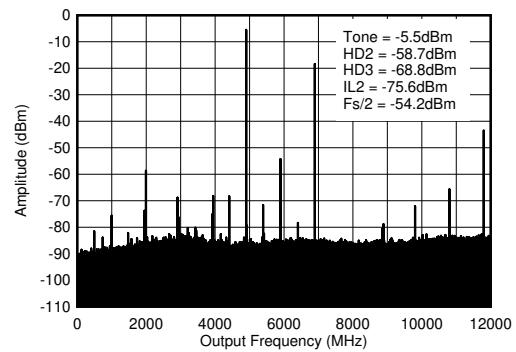
Matching at 4.9 GHz,  $f_{DAC} = 11.79648$  GSPPS, interleave mode, normalized to output power at harmonic frequency

**Figure 6-178. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz**



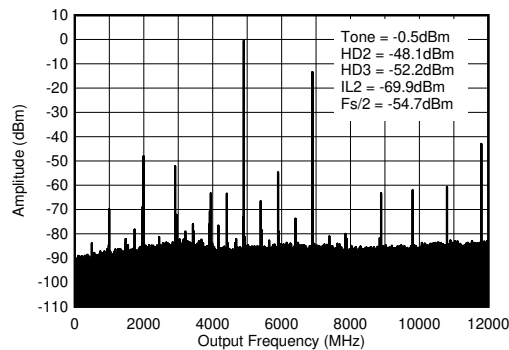
$f_{DAC} = 11796.48$  MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$ .

**Figure 6-179. TX Single Tone (-12 dBFS) Output Spectrum at 4.9 GHz ( $0-f_{DAC}$ )**



$f_{DAC} = 11796.48$  MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$ .

**Figure 6-180. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz ( $0-f_{DAC}$ )**

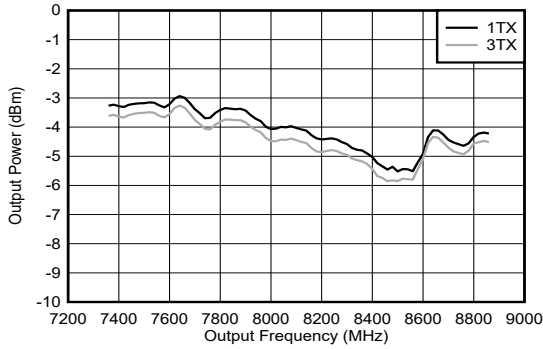


$f_{DAC} = 11796.48$  MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses.  $IL_n = f_s/n \pm f_{OUT}$ .

**Figure 6-181. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz ( $0-f_{DAC}$ )**

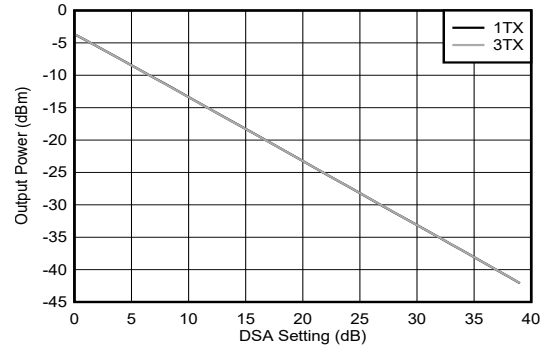
### 6.12.6 TX Typical Characteristics at 8.1 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



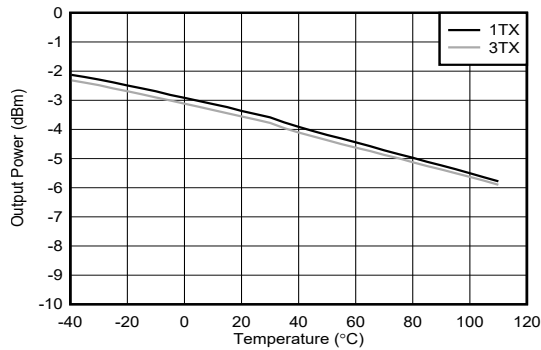
includes PCB and cable losses.

**Figure 6-182. TX Output Power vs Frequency at 8.11 GHz**



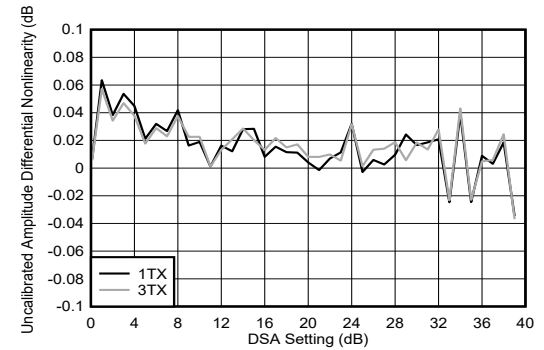
includes PCB and cable losses.

**Figure 6-183. TX Output Power vs DSA Setting at 8.11 GHz**

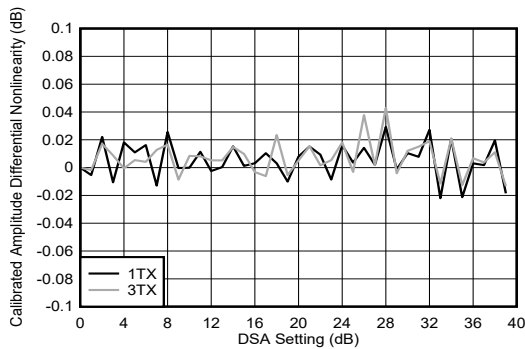


includes PCB and cable losses.

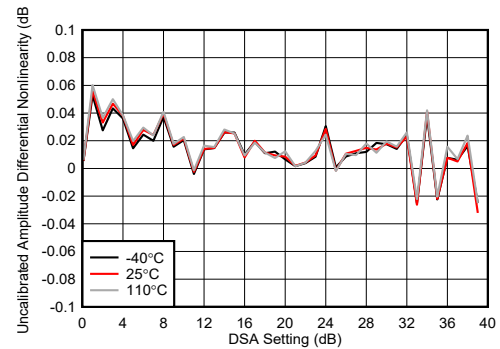
**Figure 6-184. TX Output Power vs Temperature at 8.11 GHz**



**Figure 6-185. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz**



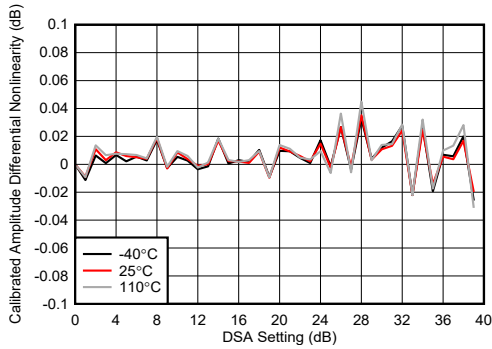
**Figure 6-186. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz**



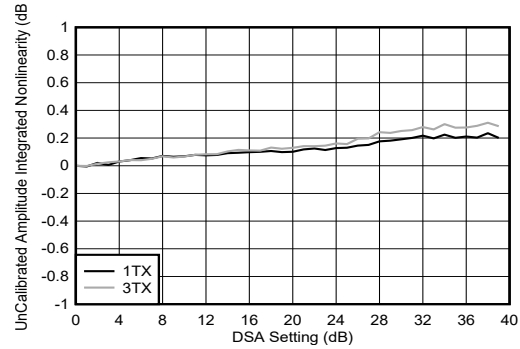
**Figure 6-187. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz**

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

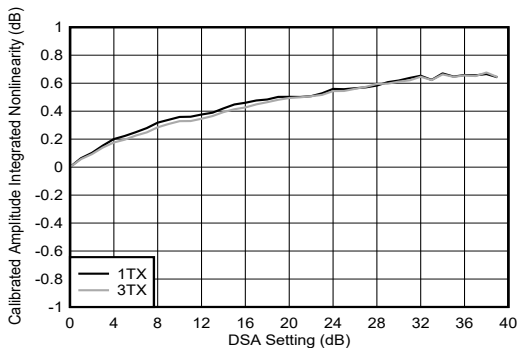
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



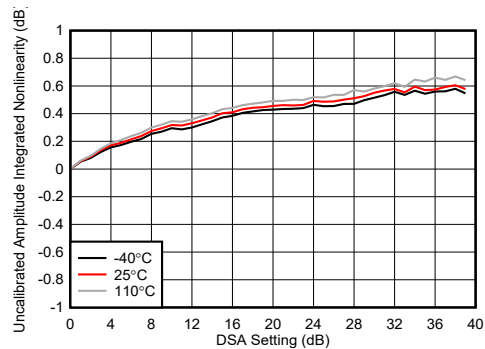
**Figure 6-188. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz**



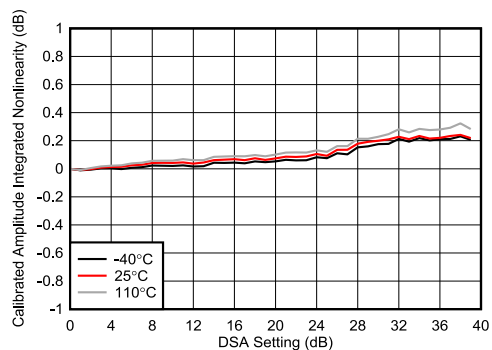
**Figure 6-189. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz**



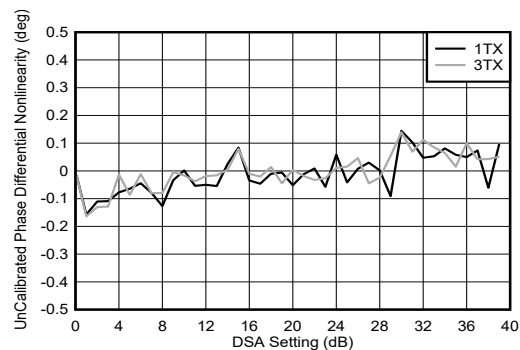
**Figure 6-190. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz**



**Figure 6-191. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz**



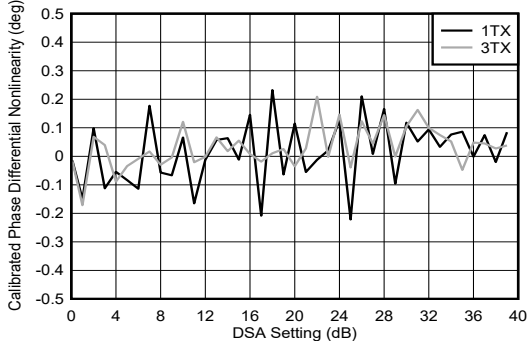
**Figure 6-192. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz**



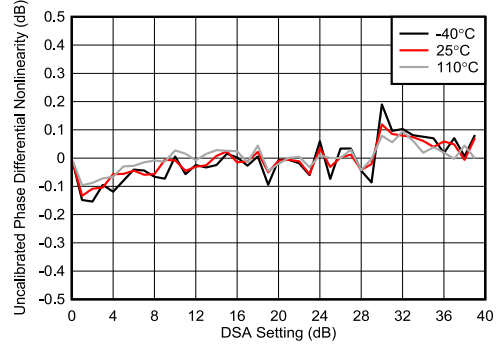
**Figure 6-193. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz**

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

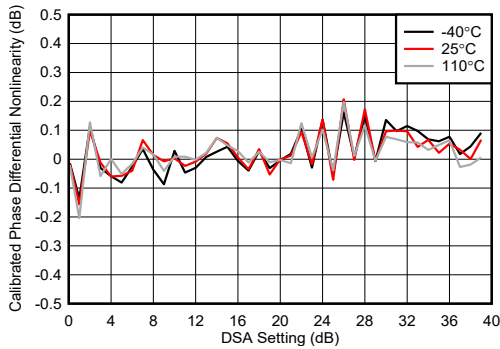
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



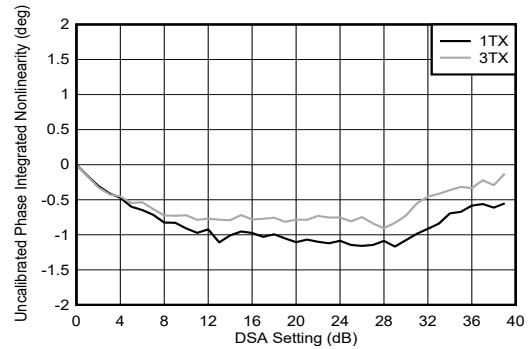
**Figure 6-194. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz**



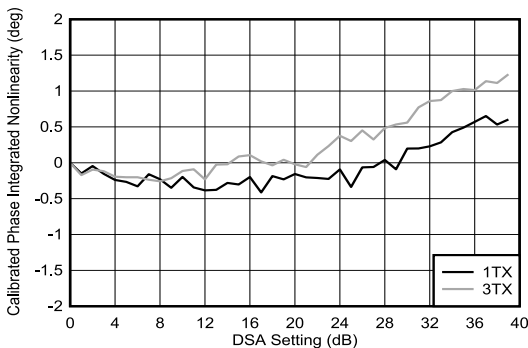
**Figure 6-195. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz**



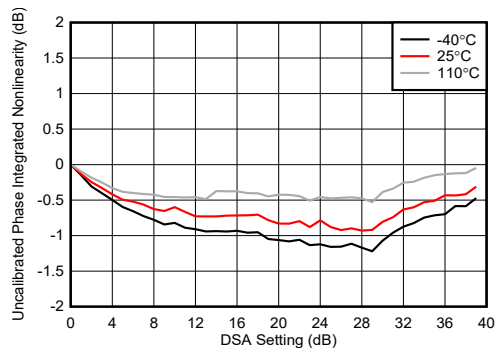
**Figure 6-196. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz**



**Figure 6-197. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz**



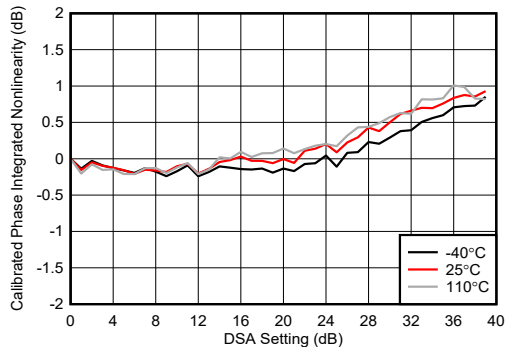
**Figure 6-198. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz**



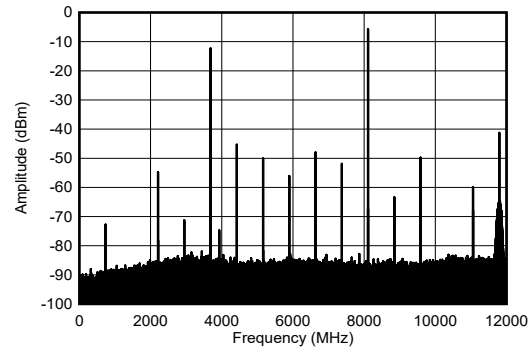
**Figure 6-199. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz**

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

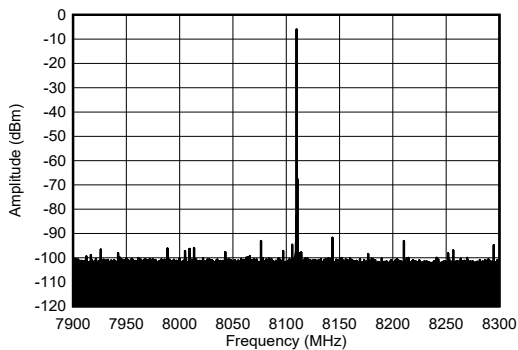
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



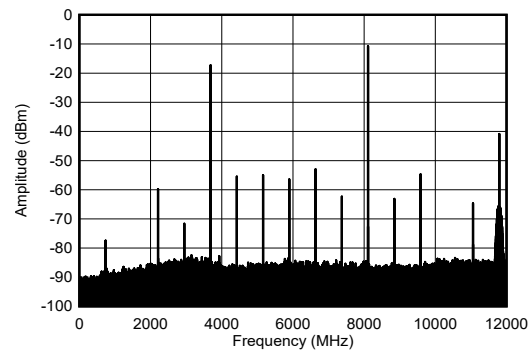
**Figure 6-200. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz**



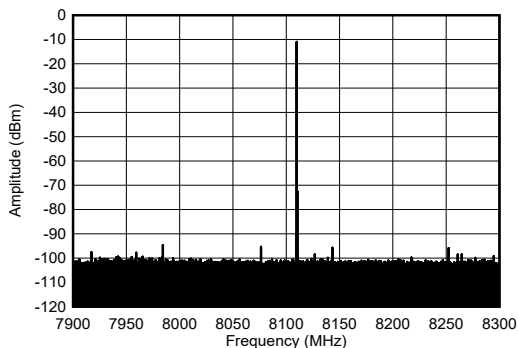
**Figure 6-201. TX Single Tone Output Spectrum at 8.11 GHz**  
-1 dBFS



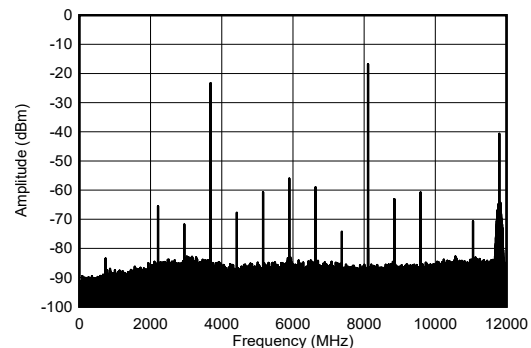
**Figure 6-202. TX Single Tone Output Spectrum at 8.11 GHz**  
-1 dBFS



**Figure 6-203. TX Single Tone Output Spectrum at 8.11 GHz**  
-6 dBFS



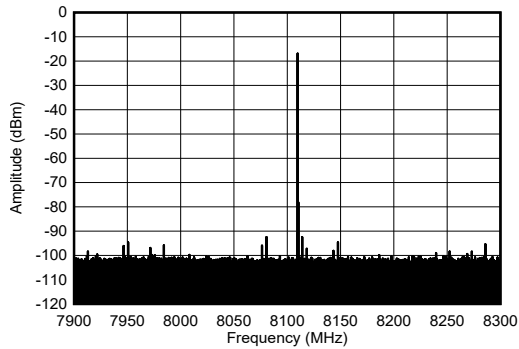
**Figure 6-204. TX Single Tone Output Spectrum at 8.11 GHz**  
-6 dBFS



**Figure 6-205. TX Single Tone Output Spectrum at 8.11 GHz**  
-12 dBFS

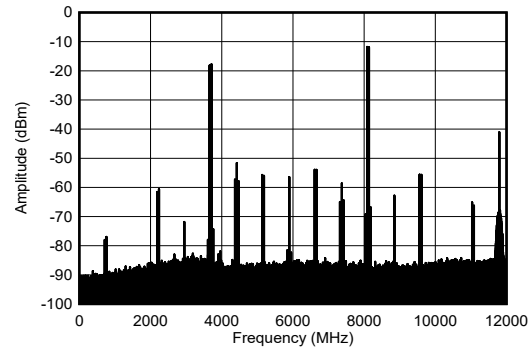
### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



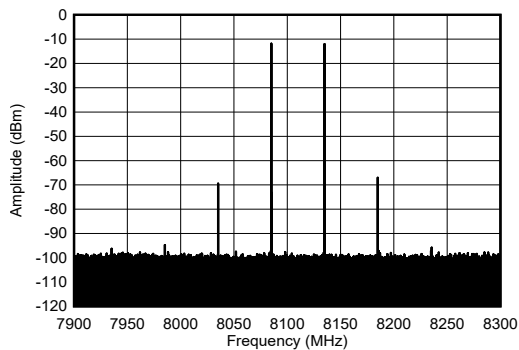
-12 dBFS

Figure 6-206. TX Single Tone Output Spectrum at 8.11 GHz



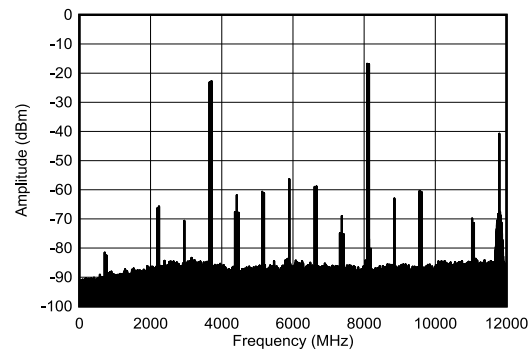
50 MHz tone spacing, -7 dBFS each tone

Figure 6-207. TX Dual Tone Output Spectrum at 8.11 GHz



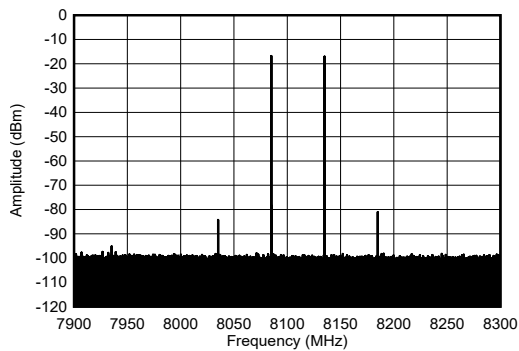
50 MHz tone spacing, -7 dBFS each tone

Figure 6-208. TX Dual Tone Output Spectrum at 8.11 GHz



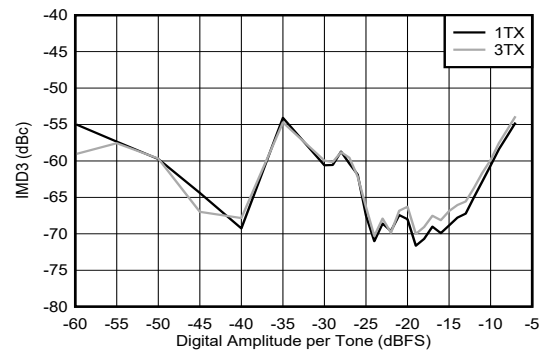
50 MHz tone spacing, -12 dBFS each tone

Figure 6-209. TX Dual Tone Output Spectrum at 8.11 GHz



50 MHz tone spacing, -12 dBFS each tone

Figure 6-210. TX Dual Tone Output Spectrum at 8.11 GHz



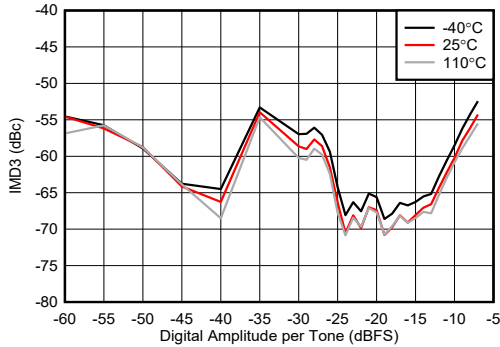
-7 dBFS each tone, 50 MHz tone spacing

Figure 6-211. TX IMD3 vs Digital Amplitude at 8.11 GHz



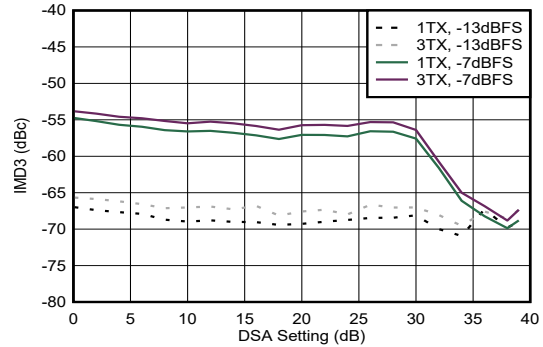
### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



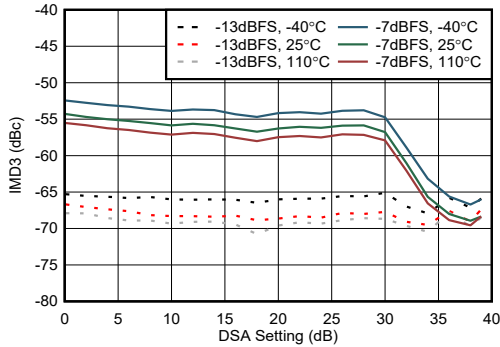
-7 dBFS each tone, 50 MHz tone spacing

Figure 6-212. TX IMD3 vs Digital Amplitude at 8.11 GHz



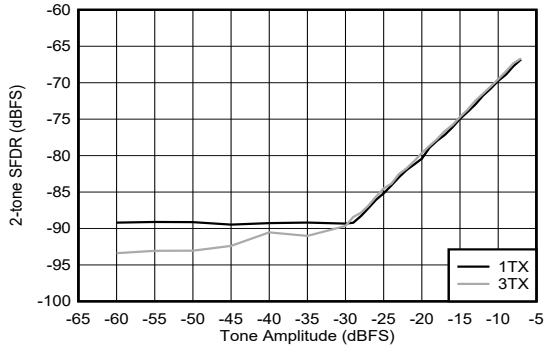
50 MHz tone spacing

Figure 6-213. TX IMD3 vs DSA Setting at 8.11 GHz



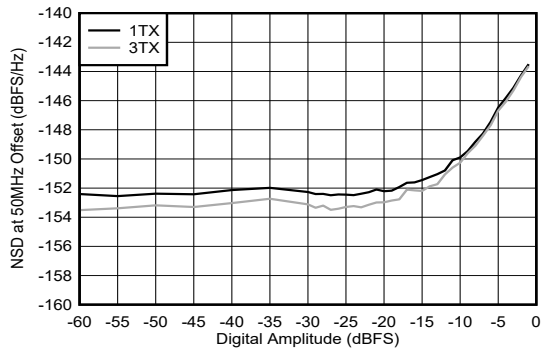
50 MHz tone spacing

Figure 6-214. TX IMD3 vs DSA Setting at 8.11 GHz



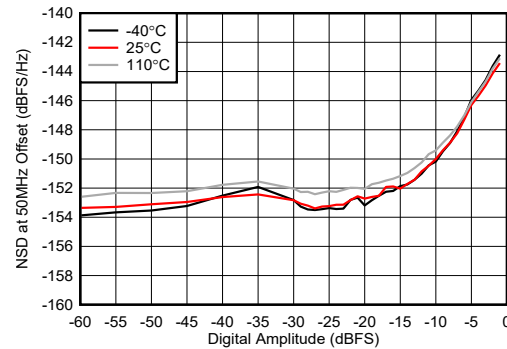
50 MHz tone spacing

Figure 6-215. TX 2-Tone SFDR vs Digital Amplitude at 8.11 GHz



50 MHz offset

Figure 6-216. TX NSD vs Digital Amplitude at 8.11 GHz

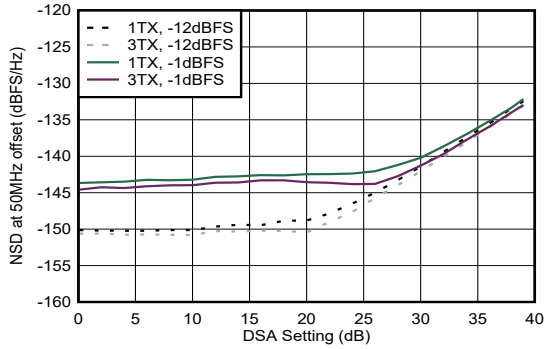


50 MHz offset

Figure 6-217. TX NSD vs Digital Amplitude at 8.11 GHz

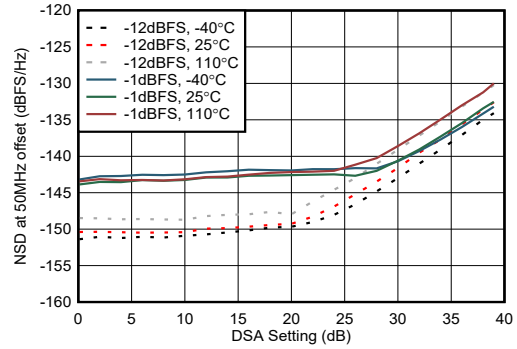
### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching



50 MHz offset

Figure 6-218. TX NSD vs DSA Setting at 8.11 GHz



50 MHz offset

Figure 6-219. TX NSD vs DSA Setting at 8.11 GHz

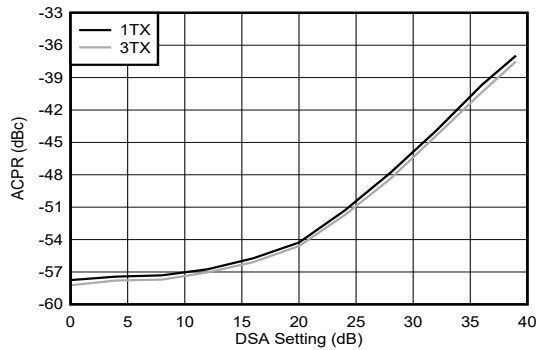


Figure 6-220. TX NR100MHz ACPR vs DSA Setting 8.11 GHz

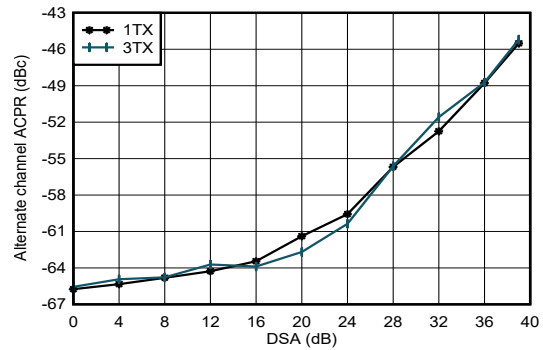


Figure 6-221. TX NR100 MHz alt-ACPR vs DSA Setting 8.11 GHz

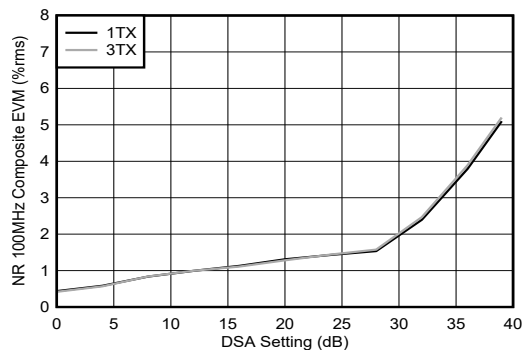


Figure 6-222. TX NR100 MHz EVM vs DSA Setting 8.11 GHz

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching

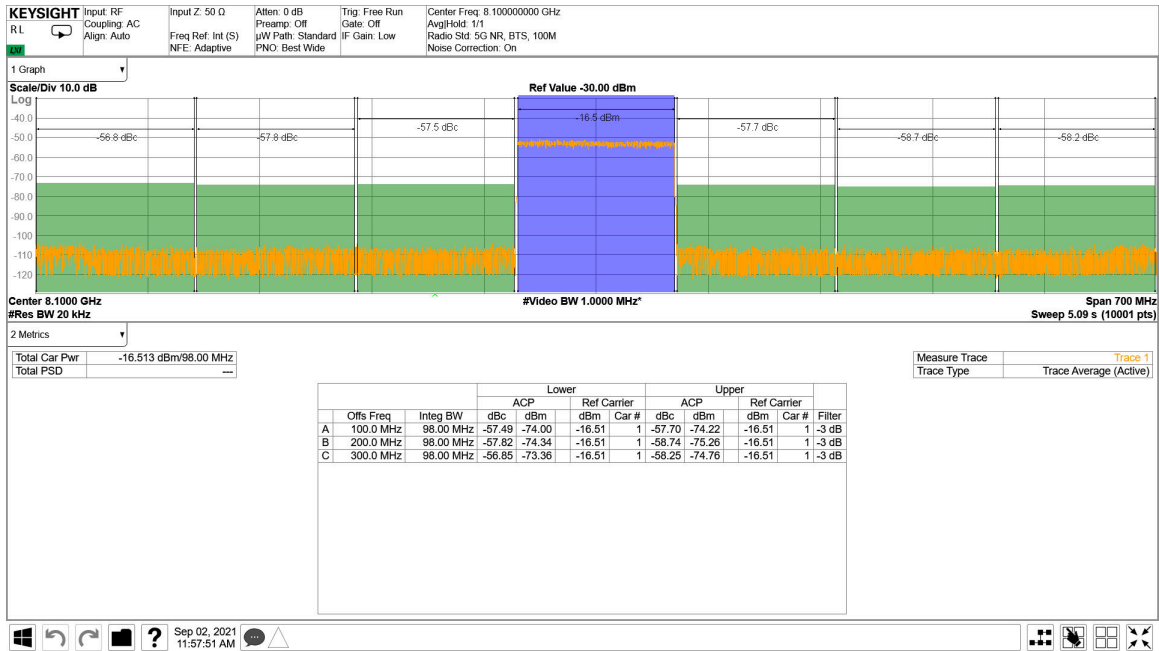


Figure 6-223. TX 100 MHz NR Output Spectrum at 8.1 GHz

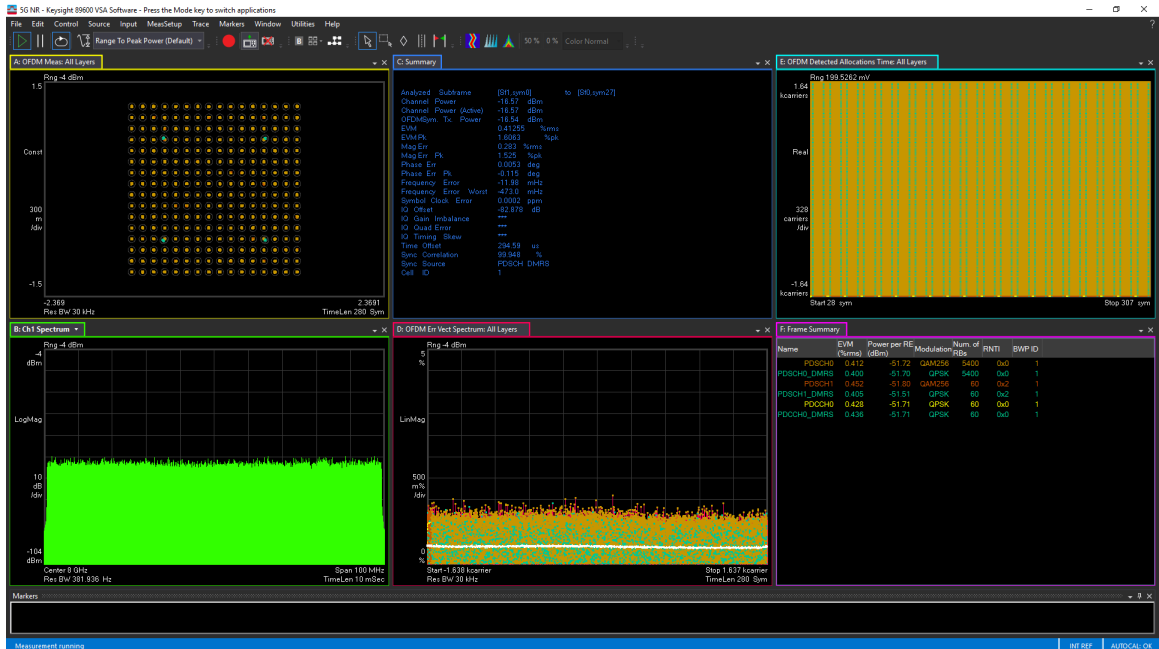


Figure 6-224. TX 100 MHz NR EVM at 8.1 GHz

### 6.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (24x interpolation), mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1 GHz matching

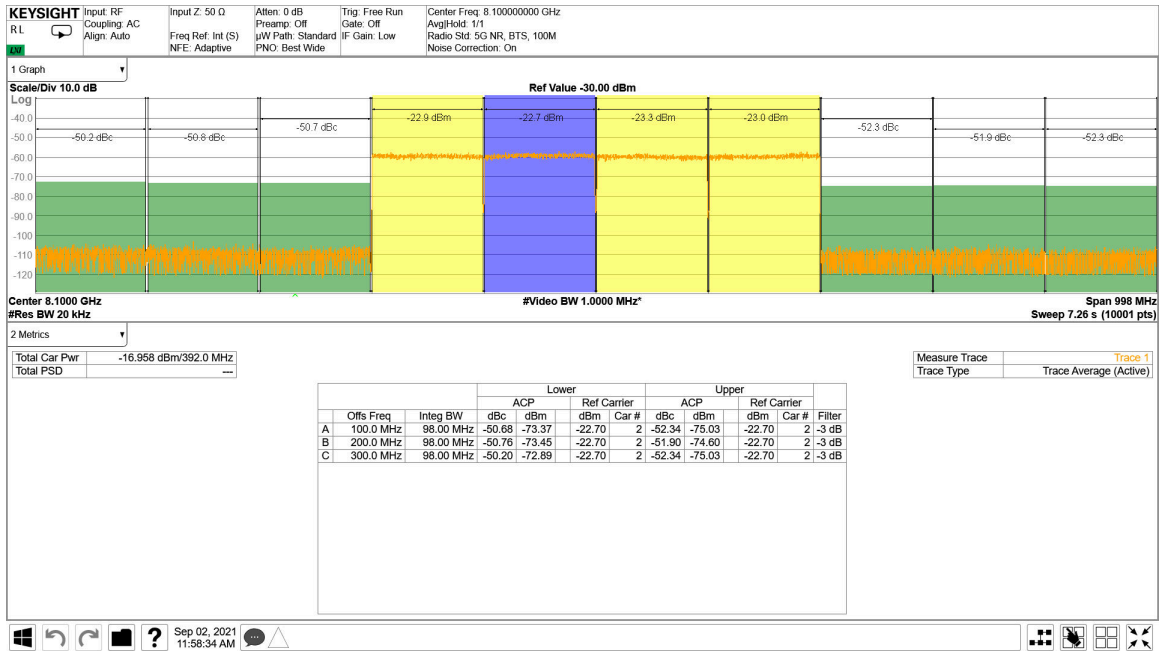


Figure 6-225. TX 4x100 MHz NR Output Spectrum 8.1 GHz

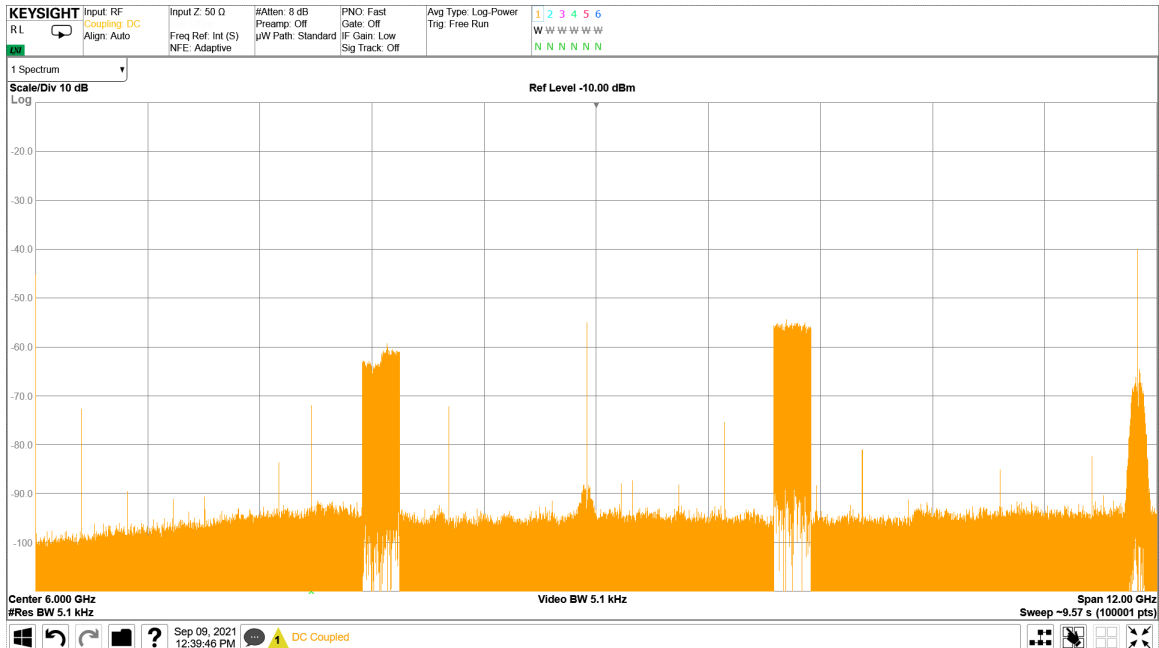
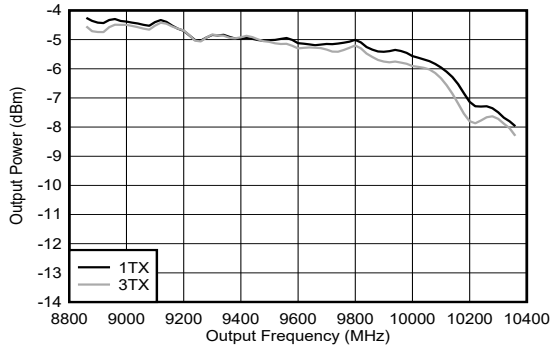


Figure 6-226. TX 4x100 MHz NR Output Spectrum 8.1 GHz

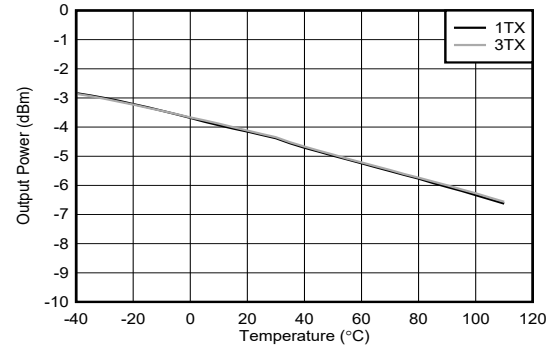
### 6.12.7 TX Typical Characteristics at 9.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching



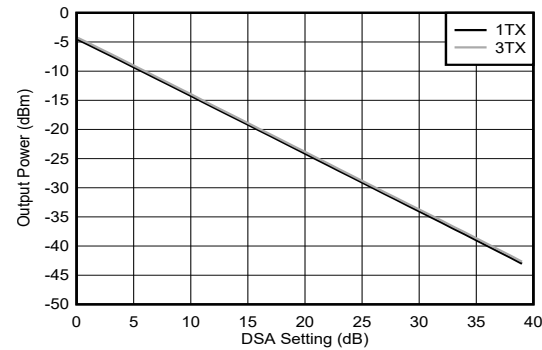
Includes PCB and cable losses.

**Figure 6-227. TX Output Power vs Frequency at 9.61 GHz**



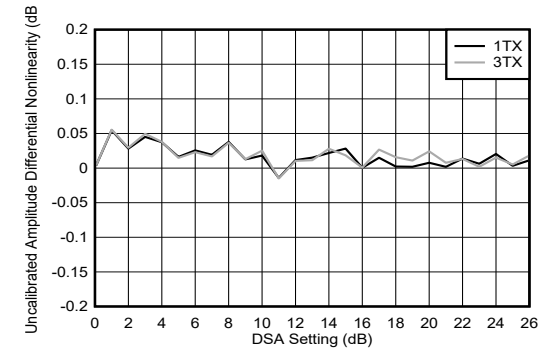
Includes PCB and cable losses.

**Figure 6-228. TX Output Power vs Frequency at 9.61 GHz**

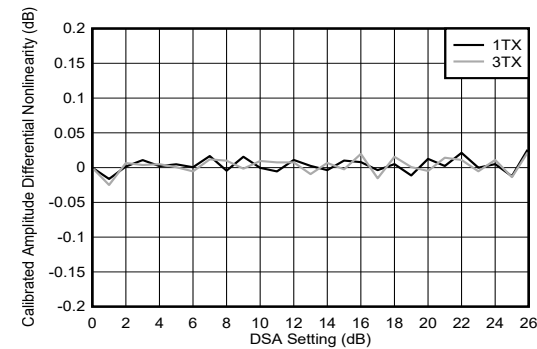


Includes PCB and cable losses.

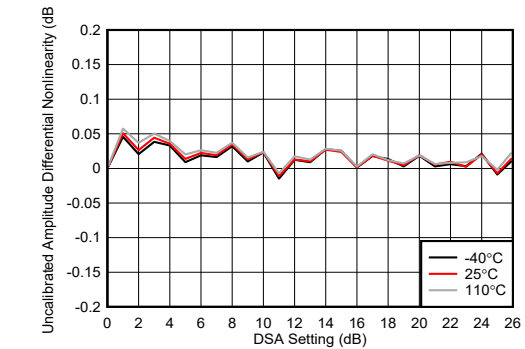
**Figure 6-229. TX Output Power vs DSA Setting at 9.61 GHz**



**Figure 6-230. TX DSA Uncalibrated Amplitude Differential Nonlinearity**



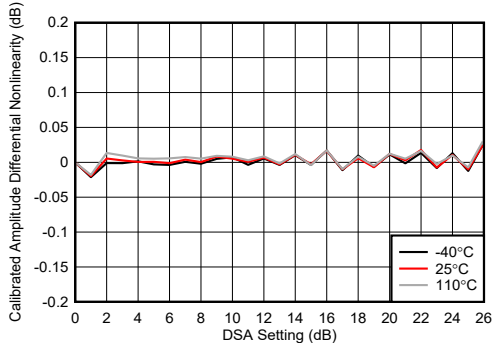
**Figure 6-231. TX DSA Calibrated Amplitude Differential Nonlinearity**



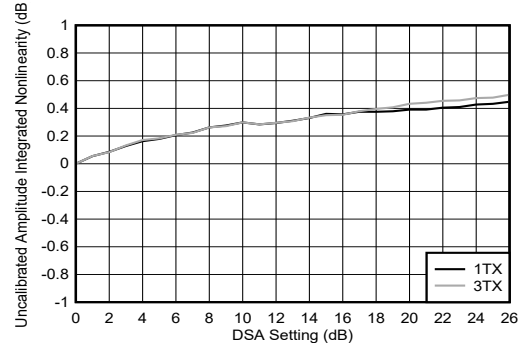
**Figure 6-232. TX DSA Uncalibrated Amplitude Differential Nonlinearity**

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

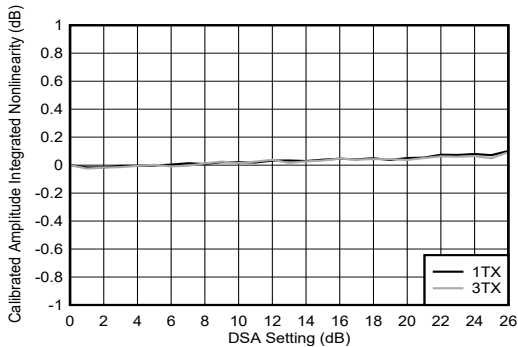
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching



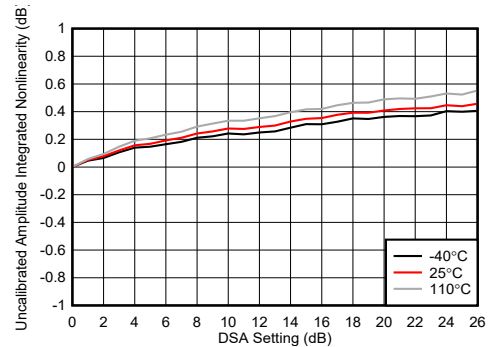
**Figure 6-233. TX DSA Calibrated Amplitude Differential Nonlinearity**



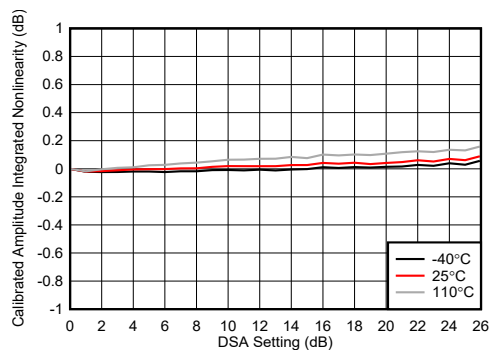
**Figure 6-234. TX DSA Uncalibrated Amplitude Integrated Nonlinearity**



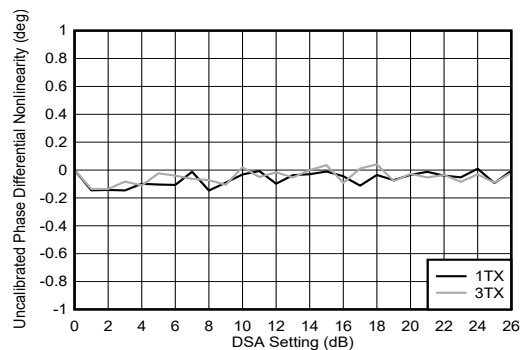
**Figure 6-235. TX DSA Calibrated Amplitude Integrated Nonlinearity**



**Figure 6-236. TX DSA Uncalibrated Amplitude Integrated Nonlinearity**



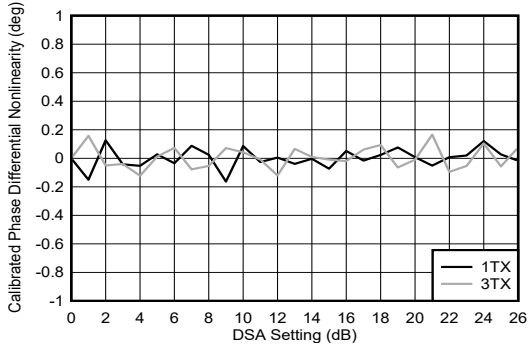
**Figure 6-237. TX DSA Calibrated Amplitude Integrated Nonlinearity**



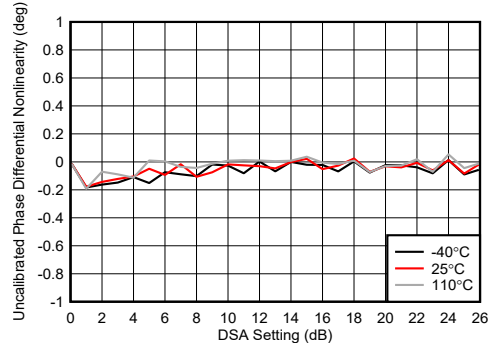
**Figure 6-238. TX DSA Uncalibrated Phase Differential Nonlinearity**

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

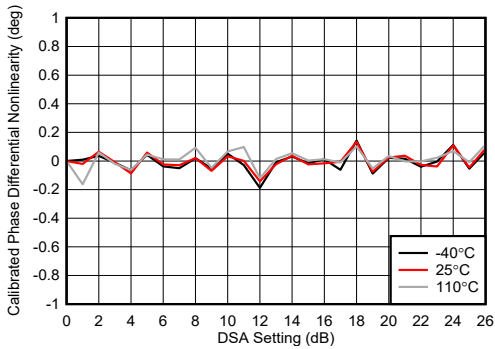
Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching



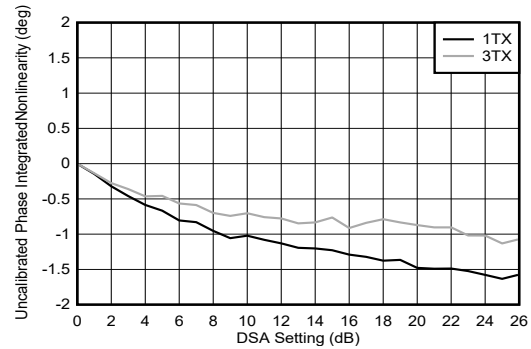
**Figure 6-239. TX DSA Calibrated Phase Differential Nonlinearity**



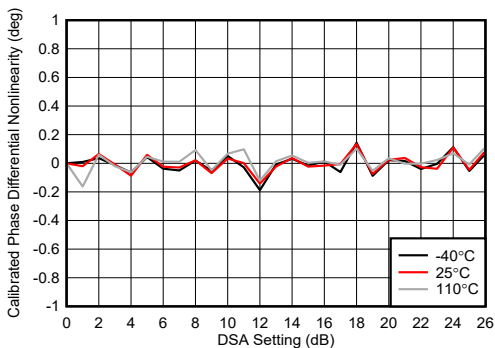
**Figure 6-240. TX DSA Uncalibrated Phase Differential Nonlinearity**



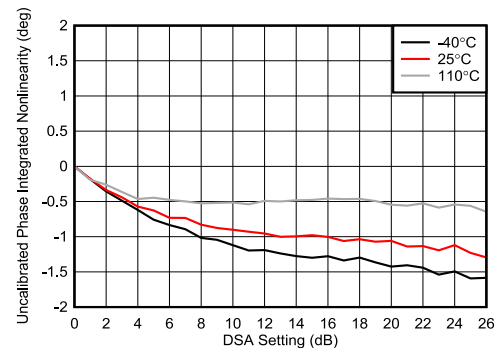
**Figure 6-241. TX DSA Calibrated Phase Differential Nonlinearity**



**Figure 6-242. TX DSA Uncalibrated Phase Integrated Nonlinearity**



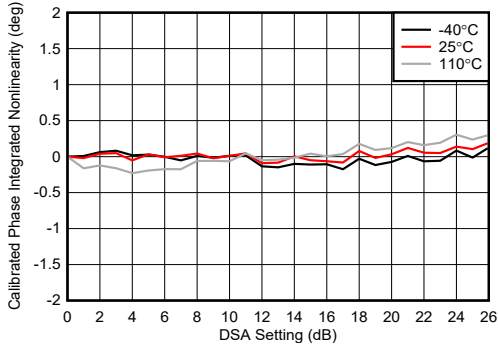
**Figure 6-243. TX DSA Calibrated Phase Integrated Nonlinearity**



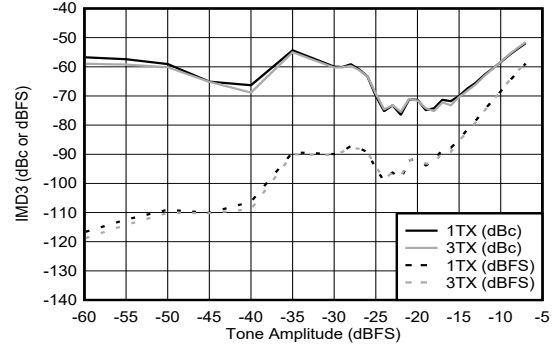
**Figure 6-244. TX DSA Uncalibrated Phase Integrated Nonlinearity**

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching

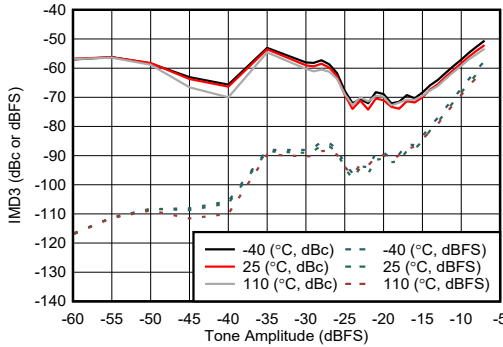


**Figure 6-245. TX DSA Calibrated Amplitude Integrated Nonlinearity**



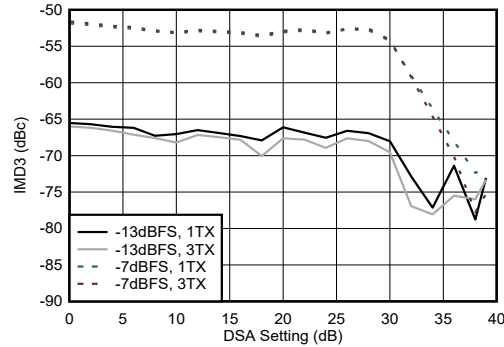
50 MHz tone spacing

**Figure 6-246. TX IMD3 vs Digital Amplitude at 9.61 GHz**



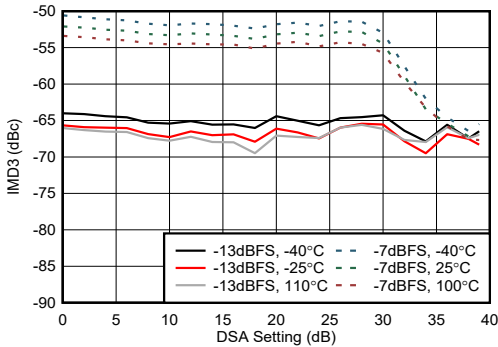
50 MHz tone spacing

**Figure 6-247. TX IMD3 vs Digital Amplitude at 9.61 GHz**



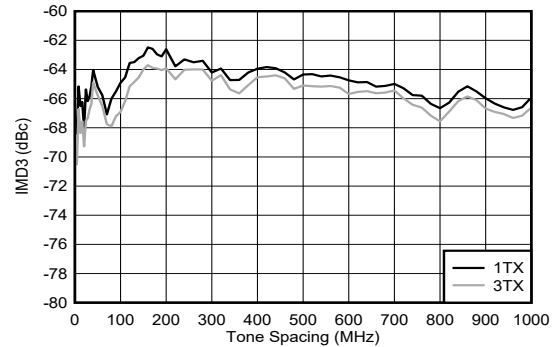
50 MHz tone spacing

**Figure 6-248. TX IMD3 vs DSA Setting at 9.61 GHz**



50 MHz tone spacing

**Figure 6-249. TX IMD3 vs DSA Setting at 9.61 GHz**



**Figure 6-250. TX IMD3 vs Tone Spacing at 9.61 GHz**



### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching

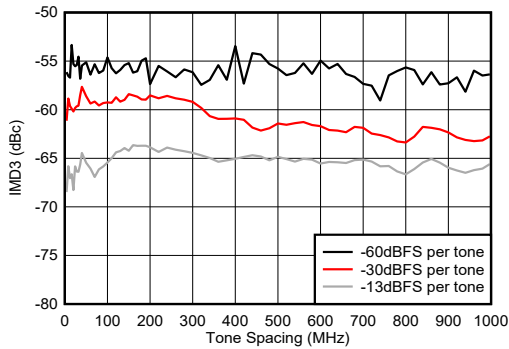


Figure 6-251. TX IMD3 vs Tone Spacing at 9.61 GHz

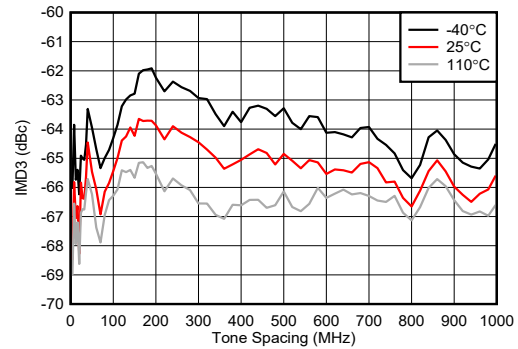


Figure 6-252. TX IMD3 vs Tone Spacing at 9.6 1GHz

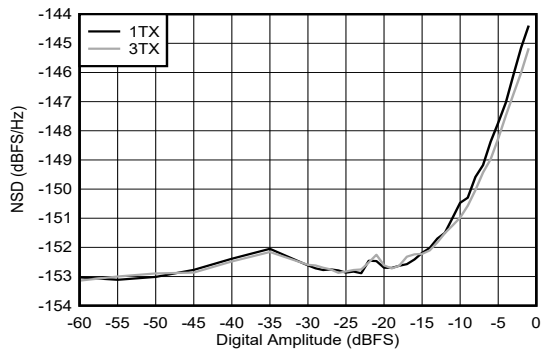


Figure 6-253. TX NSD vs Digital Amplitude at 9.61 GHz

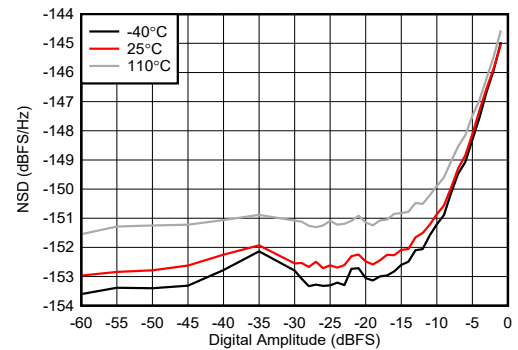


Figure 6-254. TX NSD vs Digital Amplitude at 9.61 GHz

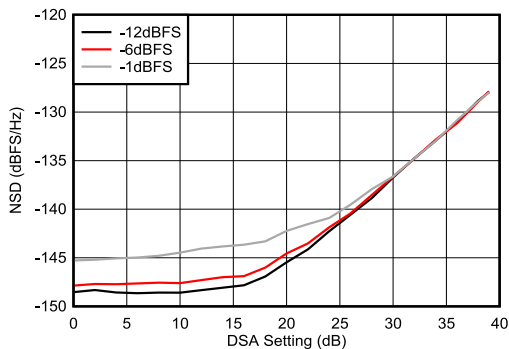


Figure 6-255. TX NSD vs DSA Setting at 9.61 GHz

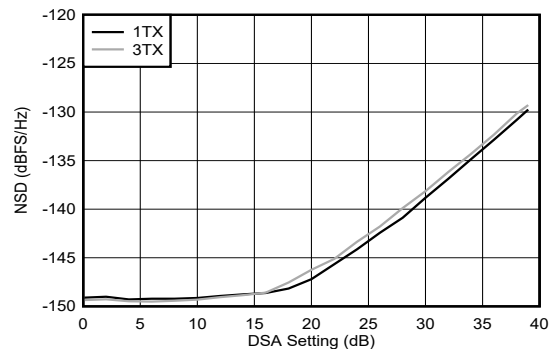


Figure 6-256. TX NSD vs DSA Setting at 9.61 GHz

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching

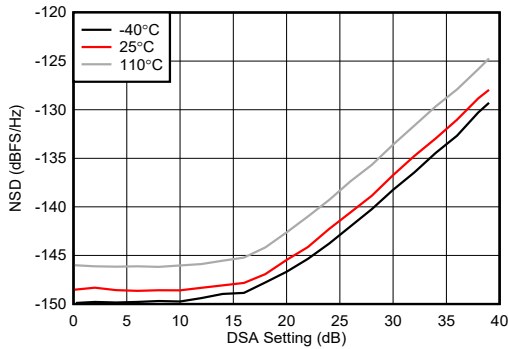
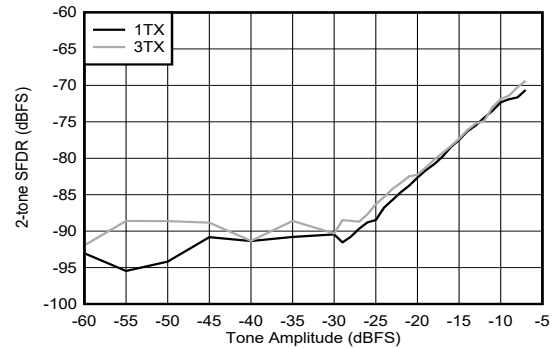
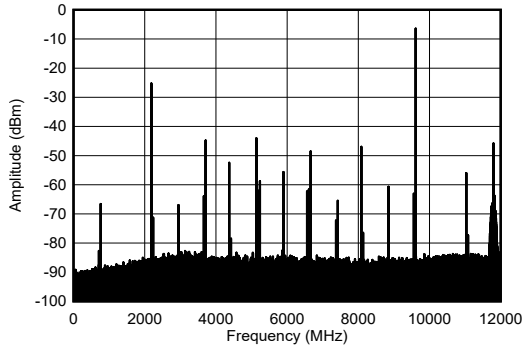


Figure 6-257. TX NSD vs DSA Setting at 9.61 GHz



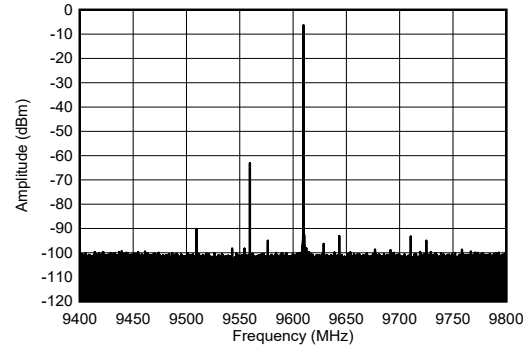
50 MHz tone spacing

Figure 6-258. TX 2-tone SFDR vs Digital Amplitude at 9.61 GHz



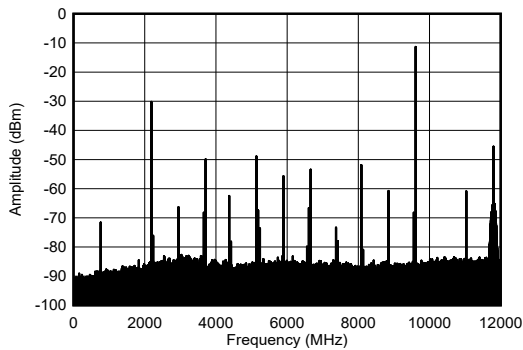
Includes PCB and cable losses.

Figure 6-259. TX Single Tone Spectrum at 9.61 GHz and -1 dBFS (wideband)



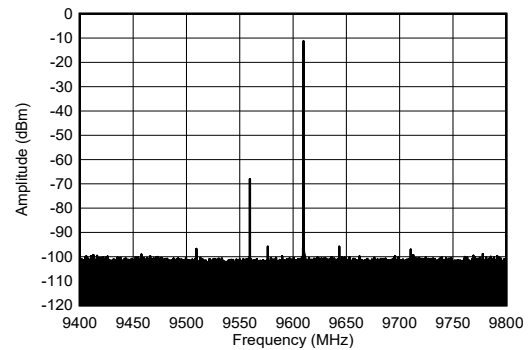
Includes PCB and cable losses.

Figure 6-260. TX Single Tone Spectrum at 9.61 GHz and -1 dBFS (1.2 GHz BW)



Includes PCB and cable losses.

Figure 6-261. TX Single Tone Spectrum at 9.61 GHz and -6 dBFS (wideband)

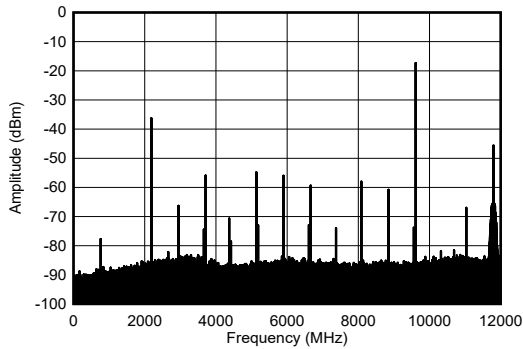


Includes PCB and cable losses.

Figure 6-262. TX Single Tone Spectrum at 9.61 GHz and -6 dBFS (1.2 GHz BW)

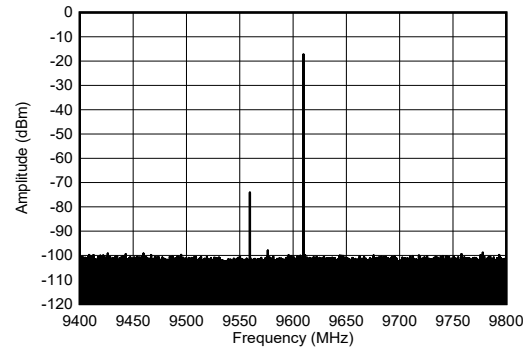
### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching



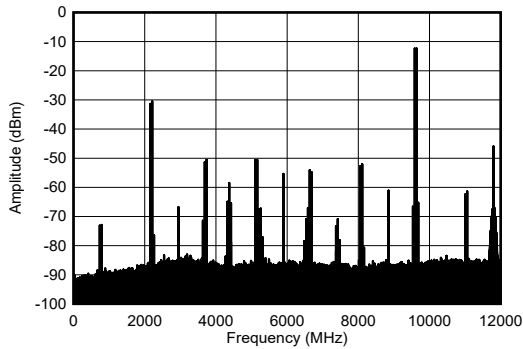
Includes PCB and cable losses.

**Figure 6-263. TX Single Tone Spectrum at 9.61 GHz and -12 dBFS (wideband)**



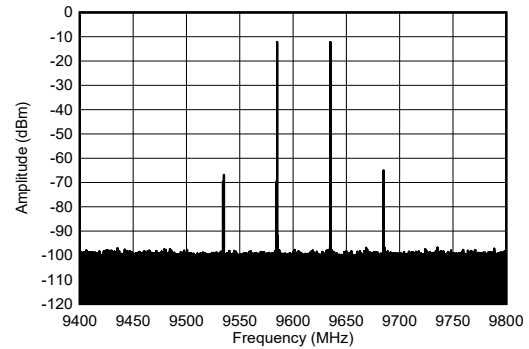
Includes PCB and cable losses.

**Figure 6-264. TX Single Tone Spectrum at 9.61 GHz and -12 dBFS (1.2GHz BW)**



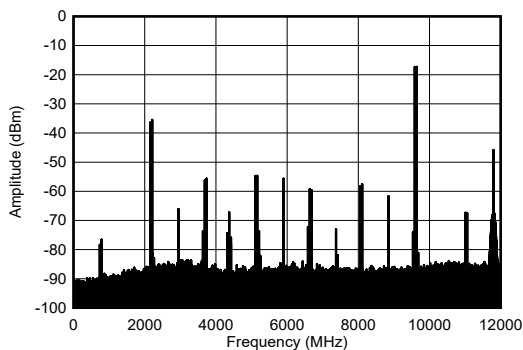
Includes PCB and cable losses, 50 MHz tone spacing.

**Figure 6-265. TX 2-Tone Spectrum at 9.61 GHz and -7 dBFS (wideband)**



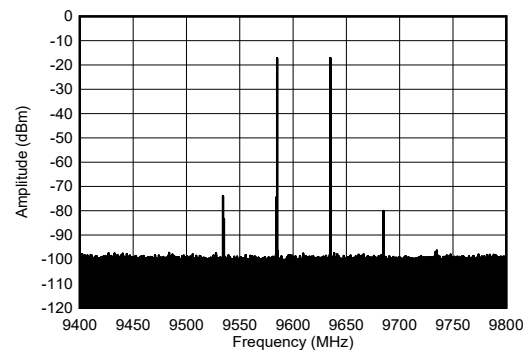
Includes PCB and cable losses, 50 MHz tone spacing.

**Figure 6-266. TX 2-Tone Spectrum at 9.61 GHz and -7 dBFS (1.2 GHz BW)**



Includes PCB and cable losses, 50 MHz tone spacing.

**Figure 6-267. TX 2-Tone Spectrum at 9.61 GHz and -12 dBFS (wideband)**

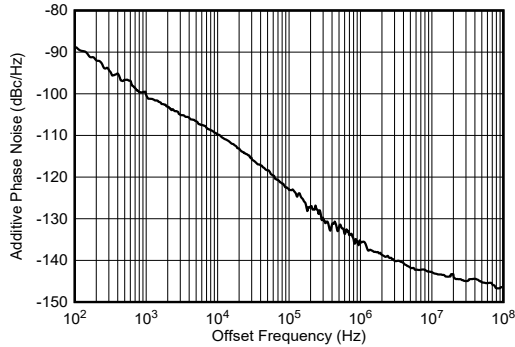


Includes PCB and cable losses, 50 MHz tone spacing.

**Figure 6-268. TX 2-Tone Spectrum at 9.61 GHz and -12 dBFS (1.2 GHz BW)**

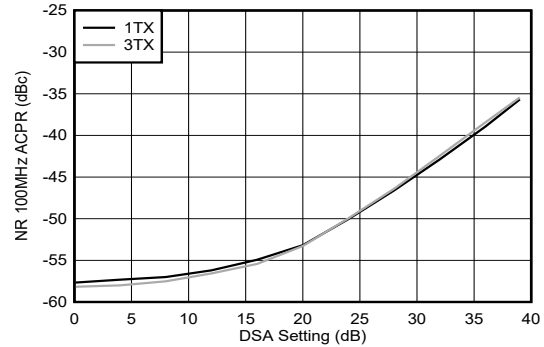
### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{DAC} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{REF} = 491.52$  MHz,  $A_{OUT} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching

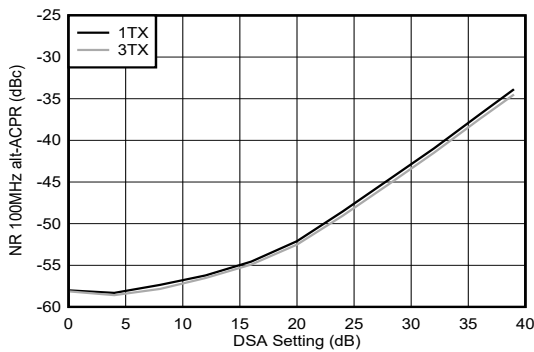


Single sideband, external clock mode, input clock phase noise removed

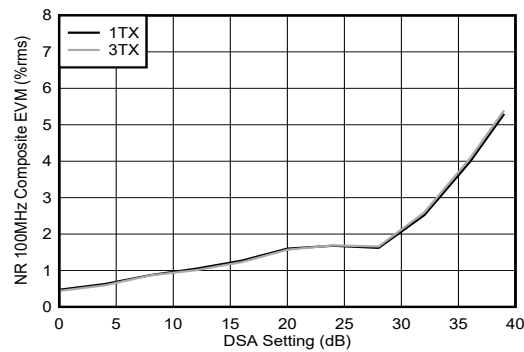
**Figure 6-269. TX Additive Phase Noise vs Offset Frequency at 9.61 GHz**



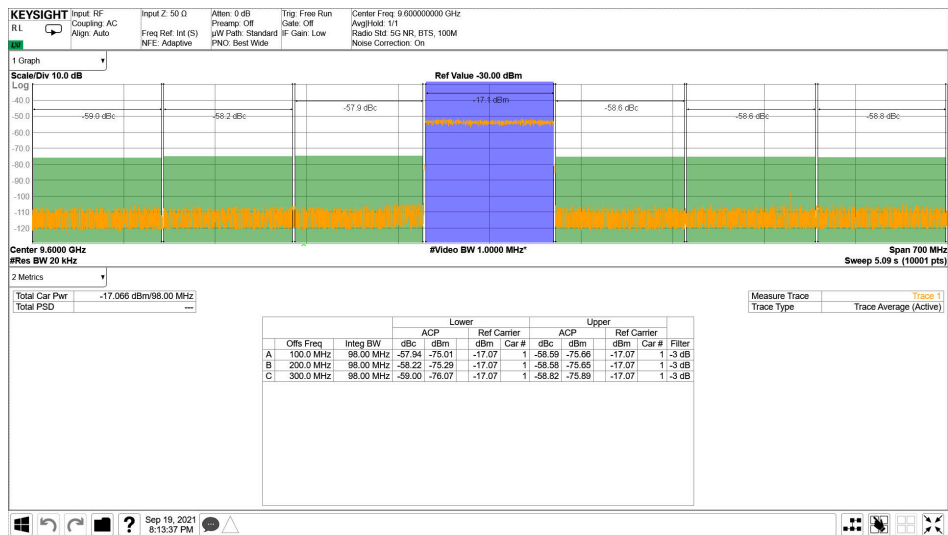
**Figure 6-270. TX NR100 MHz ACPR vs DSA Setting at 9.61 GHz**



**Figure 6-271. TX NR100 MHz alt-ACPR vs DSA Setting at 9.61 GHz**



**Figure 6-272. TX NR100 MHz EVM vs DSA Setting at 9.61 GHz**

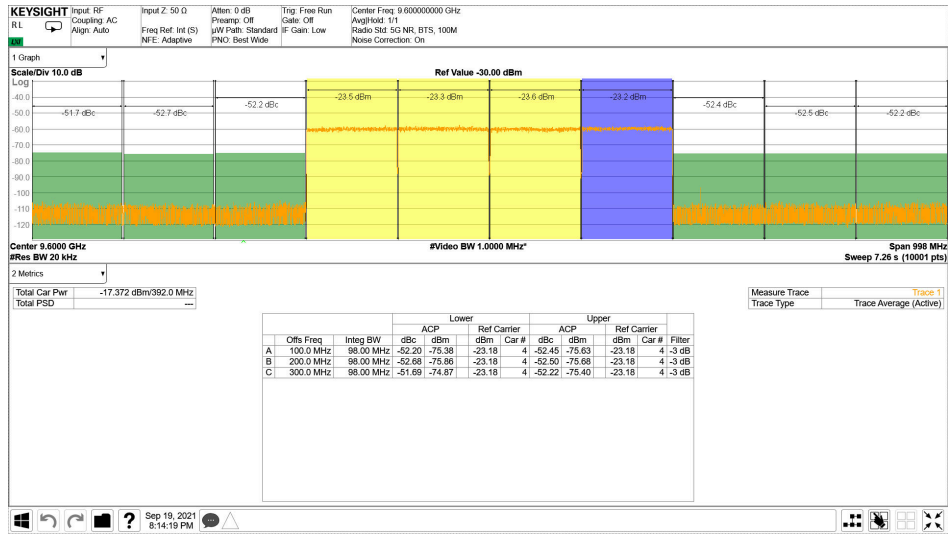


Includes PCB and cable losses.

**Figure 6-273. TX NR100 MHz Output Spectrum at 9.61 GHz**

### 6.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS,  $f_{\text{DAC}} = 11796.48$  MSPS (8x interpolation), Mixed mode, 1<sup>st</sup> Nyquist zone output, PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{OUT}} = -1$  dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6GHz matching

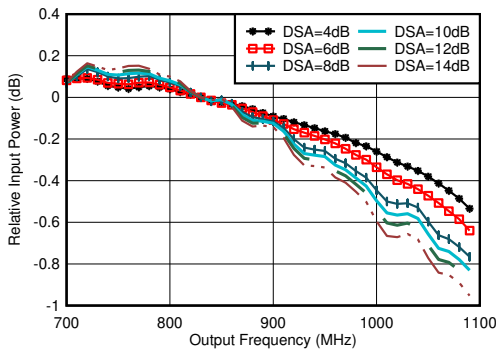


Includes PCB and cable losses.

Figure 6-274. TX 4xNR100 MHz Output Spectrum at 9.61 GHz

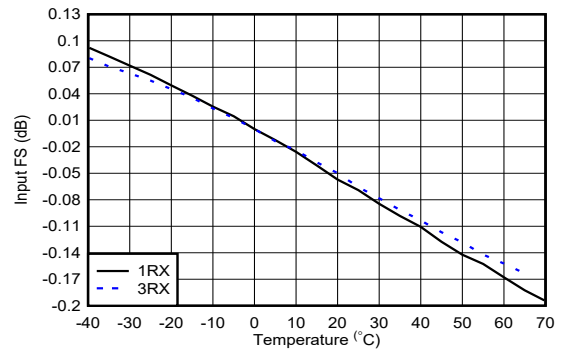
### 6.12.8 RX Typical Characteristics at 800 MHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 4 dB.



With 0.8 GHz matching, normalized to 830 MHz

Figure 6-275. RX In-Band Gain Flatness for Channel 1RX,  $f_{\text{IN}} = 830$  MHz

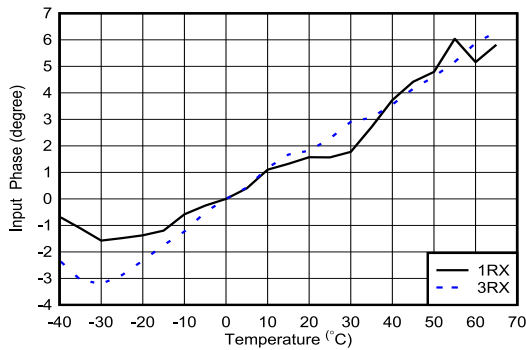


With 0.8 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

Figure 6-276. RX Input Fullscale vs Temperature and Channel at 800 MHz

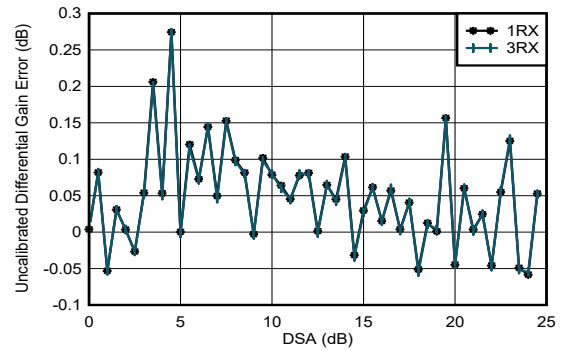
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 0.8 GHz matching, normalized to phase at  $25^\circ\text{C}$

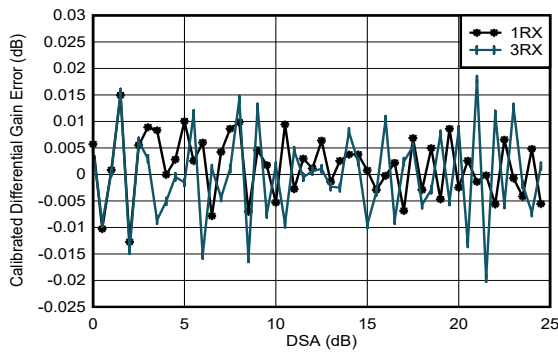
**Figure 6-277. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 0.8\text{ GHz}$**



With 0.8 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

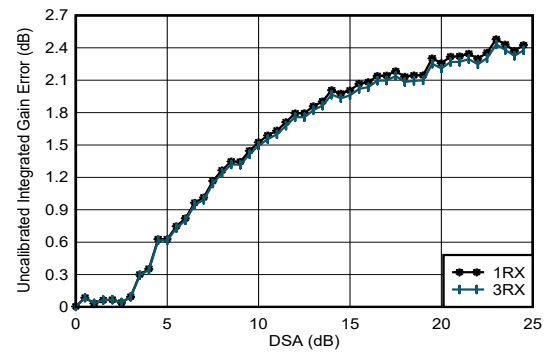
**Figure 6-278. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz**



With 0.8 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

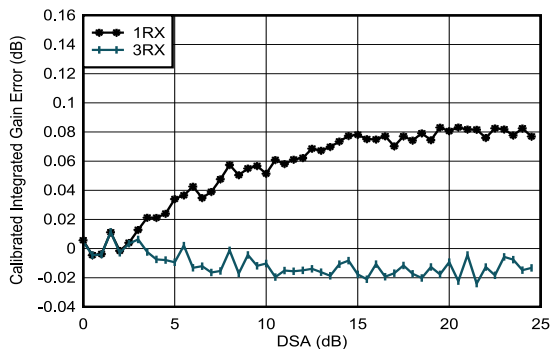
**Figure 6-279. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz**



With 0.8 GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

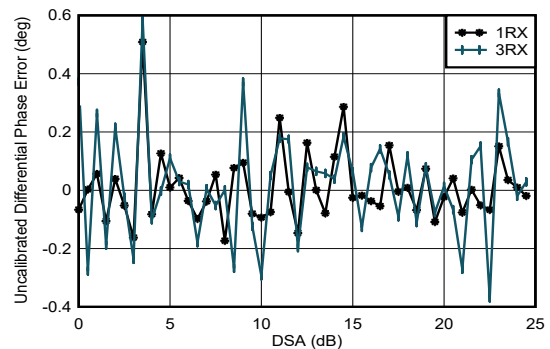
**Figure 6-280. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz**



With 0.8 GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-281. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz**



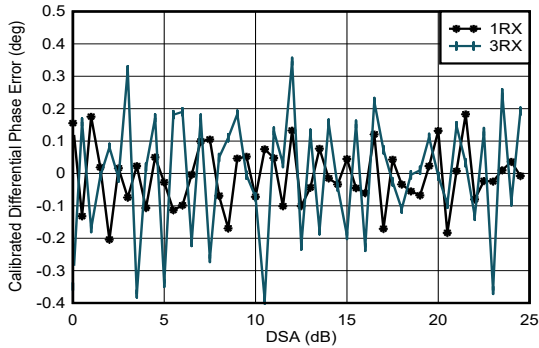
With 0.8 GHz matching

Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-282. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz**

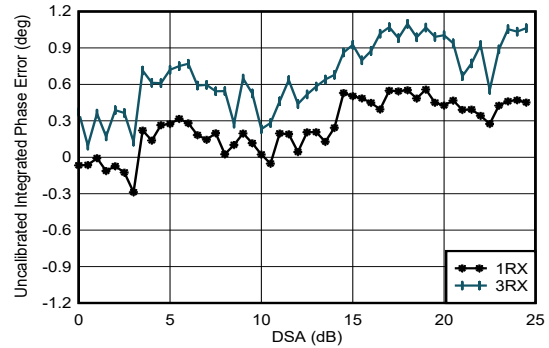
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



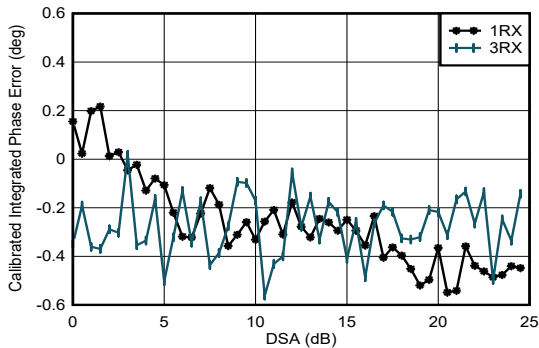
With 0.8 GHz matching  
Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

**Figure 6-283. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz**



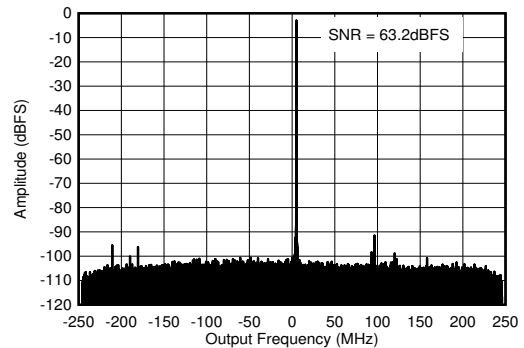
With 0.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-284. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz**



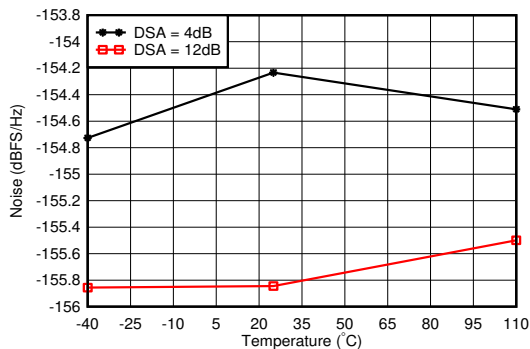
With 0.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-285. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz**



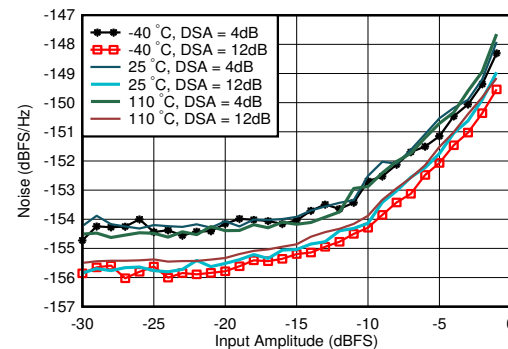
With 0.8 GHz matching,  $f_{\text{IN}} = 840\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$

**Figure 6-286. RX Output FFT at 0.8 GHz**



With 0.8 GHz matching, 12.5-MHz offset from tone

**Figure 6-287. RX Noise Spectral Density vs Temperature at 0.8 GHz**

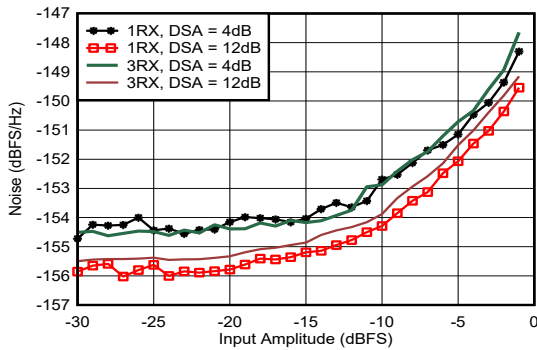


With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 6-288. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz**

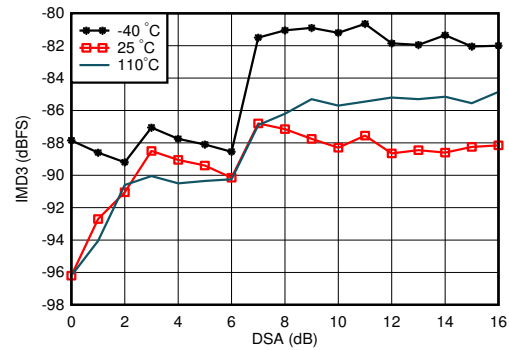
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



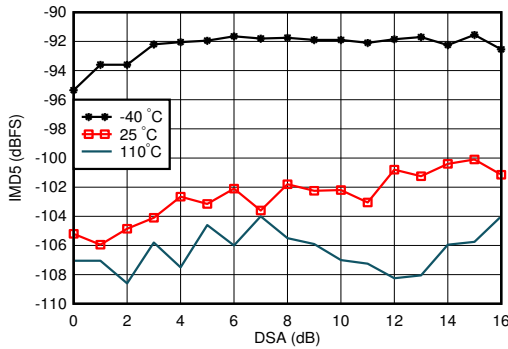
With 0.8 GHz matching, 12.5-MHz offset from tone

**Figure 6-289. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz**



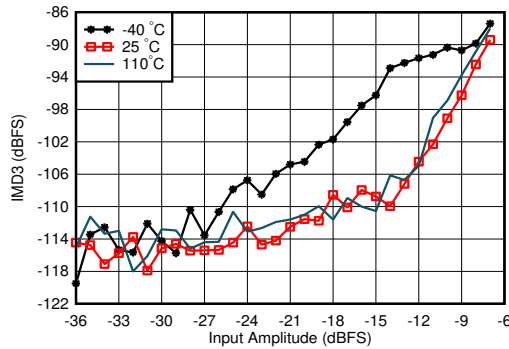
A. With 0.8 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-290. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz**



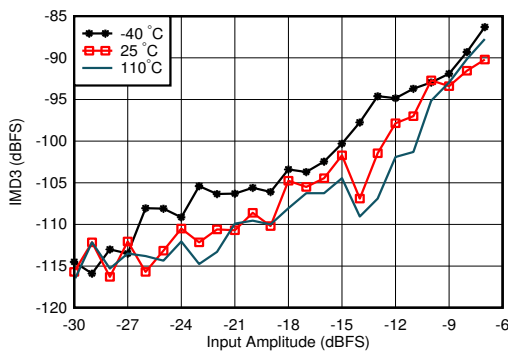
With 0.8 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-291. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz**



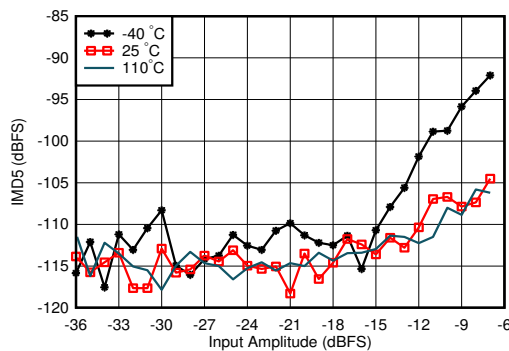
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 6-292. RX IMD3 vs Input Level and Temperature at 0.8 GHz**



With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-293. RX IMD3 vs Input Level and Temperature at 0.8 GHz**



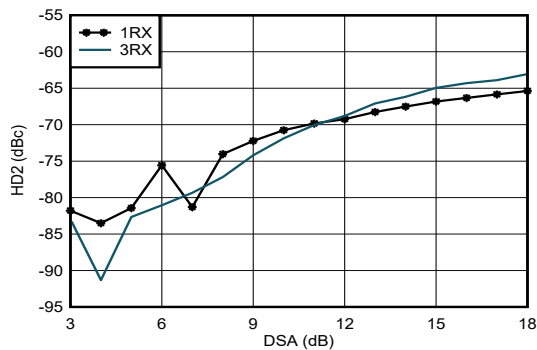
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-294. RX IMD5 vs Input Level and Temperature at 0.8 GHz**



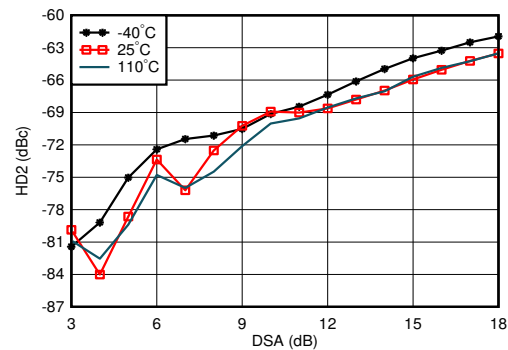
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



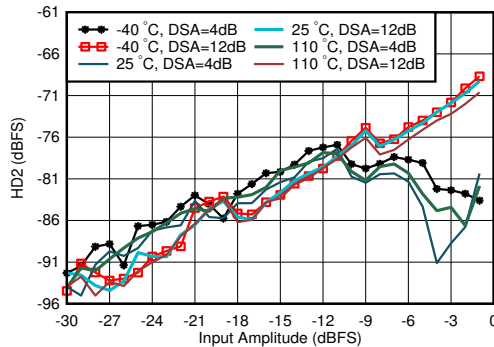
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-295. RX HD2 vs DSA Setting and Channel at 0.8 GHz



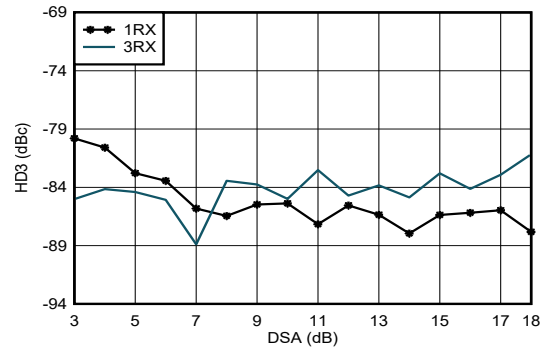
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-296. RX HD2 vs DSA Setting and Temperature at 0.8 GHz



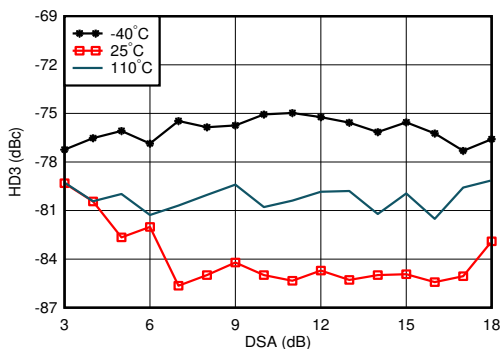
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-297. RX HD2 vs Input Level and Temperature at 0.8 GHz



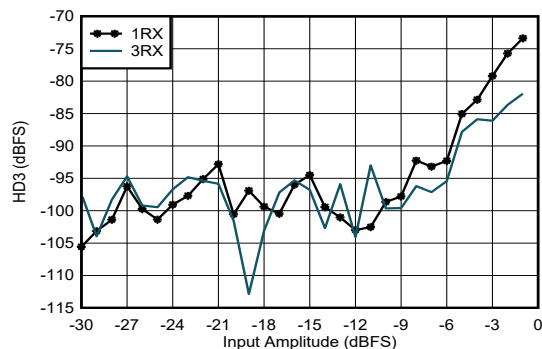
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-298. RX HD3 vs DSA Setting and Channel at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-299. RX HD3 vs DSA Setting and Temperature at 0.8 GHz

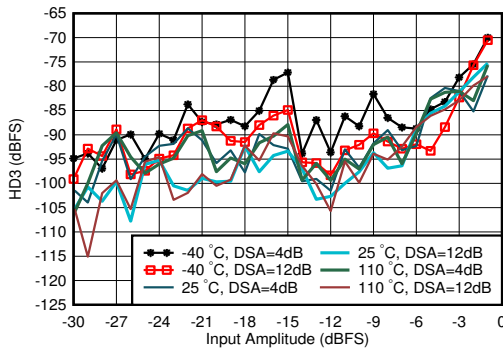


With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-300. RX HD3 vs Input Level and Channel at 0.8 GHz

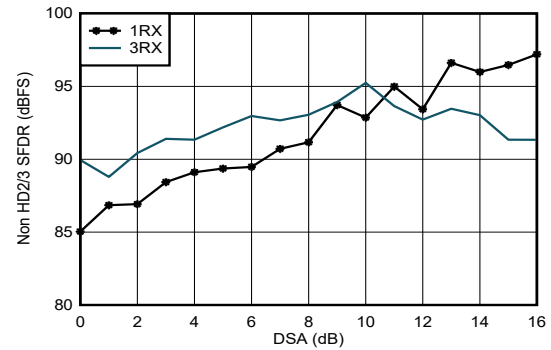
### 6.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



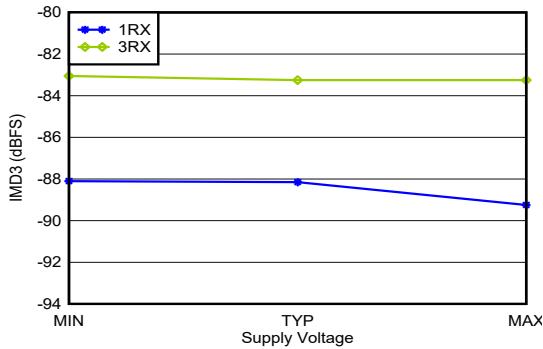
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-301. RX HD3 vs Input Level and Temperature at 0.8 GHz**



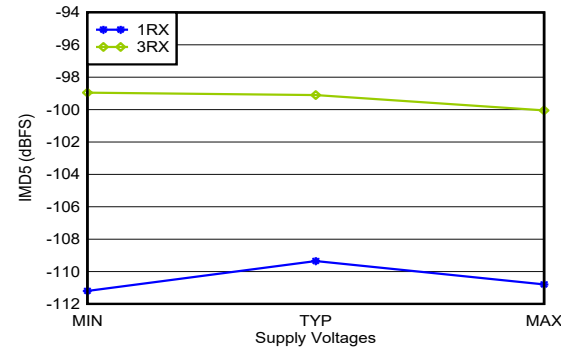
With 0.8 GHz matching

**Figure 6-302. RX Non-HD2/3 vs DSA Setting at 0.8 GHz**



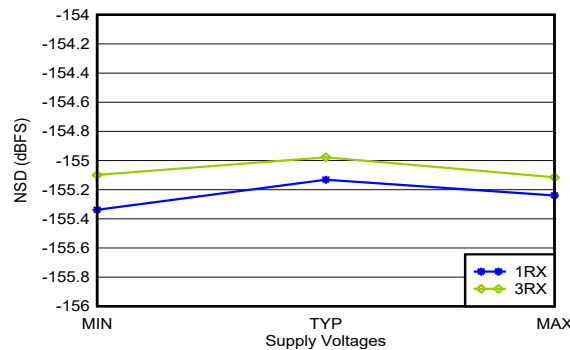
With 0.8 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-303. RX IMD3 vs Supply and Channel at 0.8 GHz**



With 0.8 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-304. RX IMD5 vs Supply and Channel at 0.8 GHz**

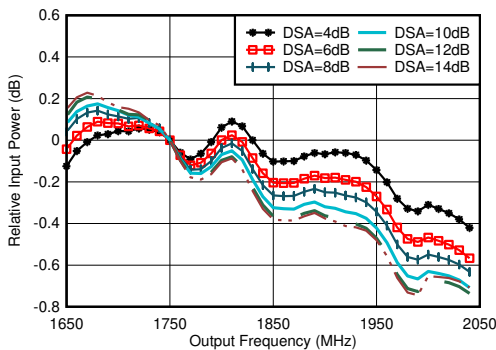


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-305. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz**

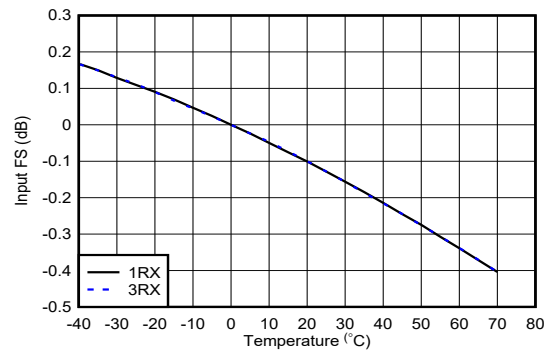
### 6.12.9 RX Typical Characteristics at 1.75-1.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



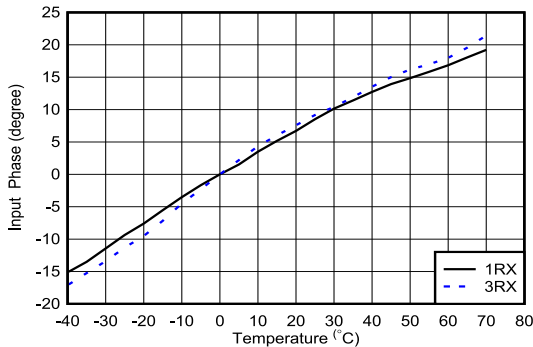
With 1.8 GHz matching, normalized to 1.75 GHz

**Figure 6-306. RX In-Band Gain Flatness,  $f_{IN} = 1750\text{ MHz}$**



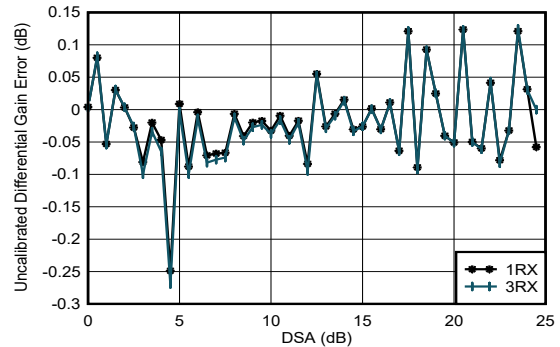
With 1.8 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

**Figure 6-307. RX Input Fullscale vs Temperature and Channel at 1.75 GHz**



With 2.6 GHz matching, normalized to phase at  $25^\circ\text{C}$

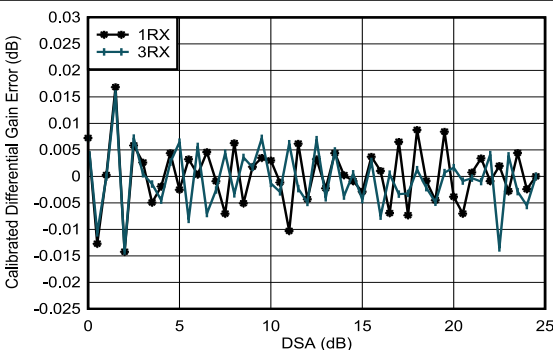
**Figure 6-308. RX Input Phase vs Temperature and DSA at  $f_{IN} = 1.75\text{ GHz}$**



With 1.8 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

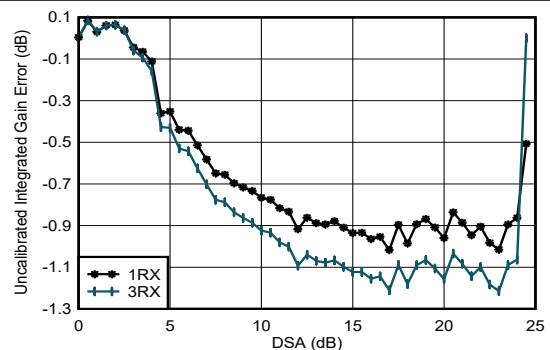
**Figure 6-309. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

**Figure 6-310. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz**



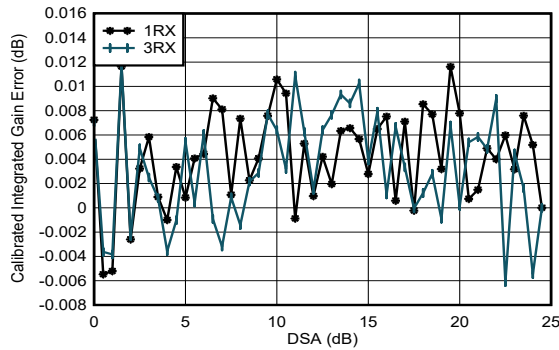
With 1.8 GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-311. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz**

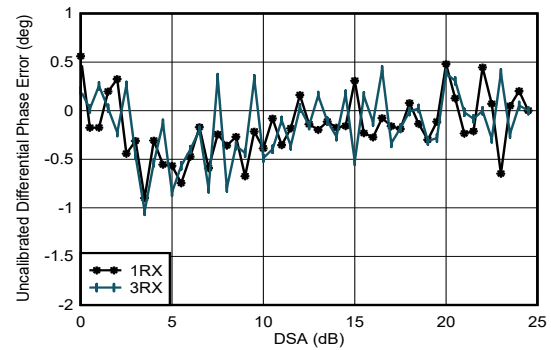
### 6.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



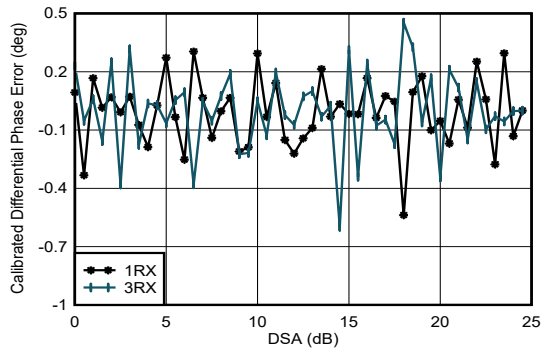
With 1.8 GHz matching  
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-312. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz**



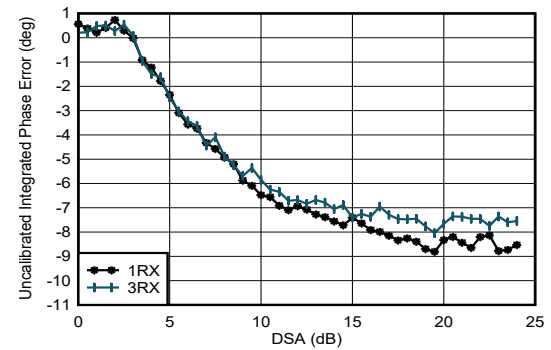
With 1.8 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-313. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz**



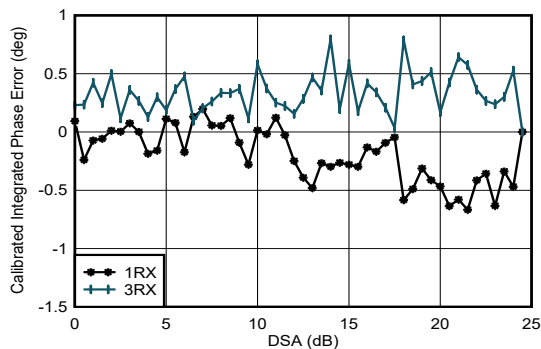
With 1.8 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-314. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz**



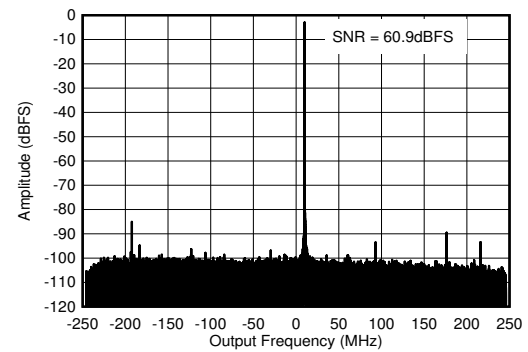
With 1.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-315. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-316. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz**

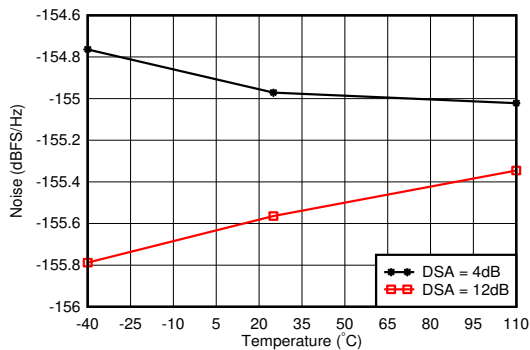


With 1.8 GHz matching,  $f_{IN} = 2610\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

**Figure 6-317. RX Output FFT at 1.75 GHz**

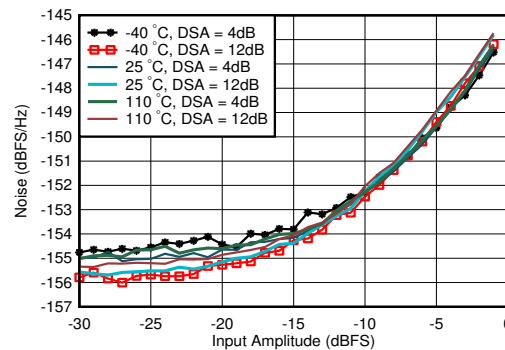
### 6.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



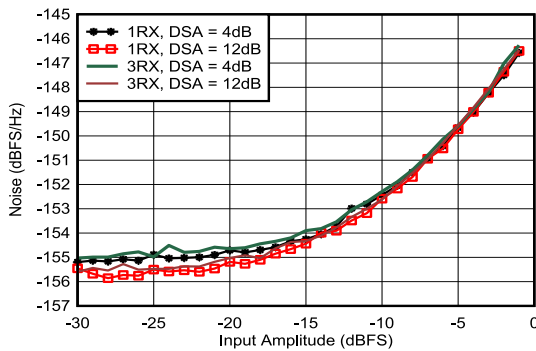
With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 6-318. RX Noise Spectral Density vs Temperature at 1.75 GHz



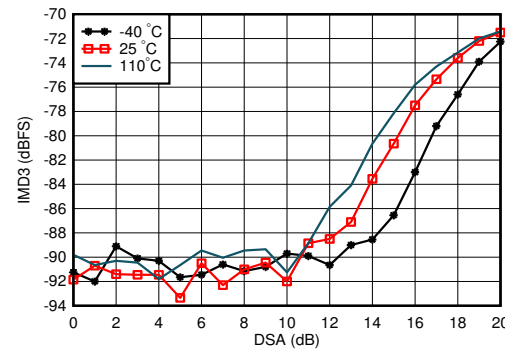
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 6-319. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



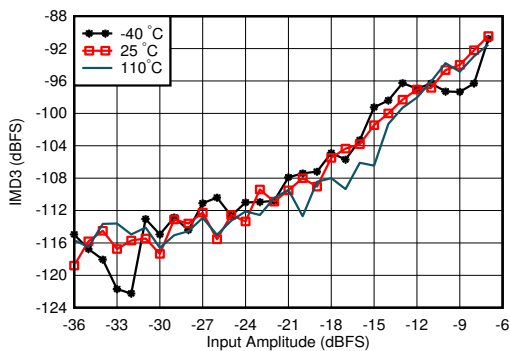
With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 6-320. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz



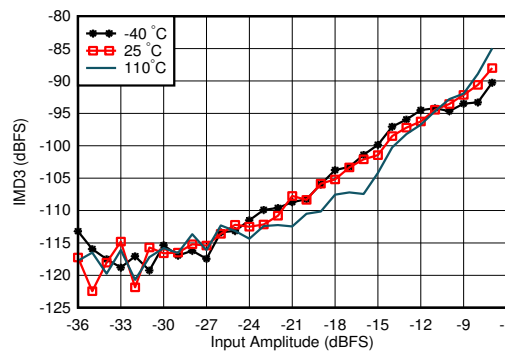
With 1.8 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

Figure 6-321. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 6-322. RX IMD3 vs Input Level and Temperature at 1.75 GHz

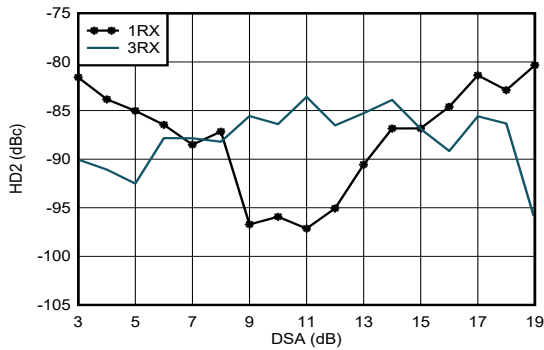


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 6-323. RX IMD3 vs Input Level and Temperature at 1.75 GHz

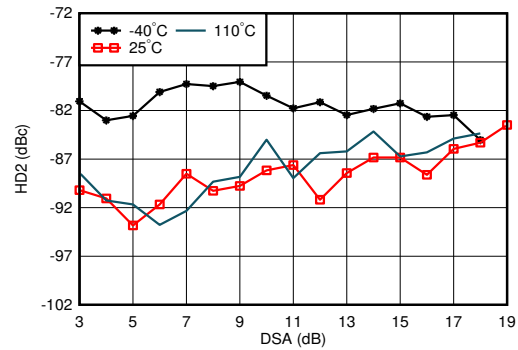
### 6.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



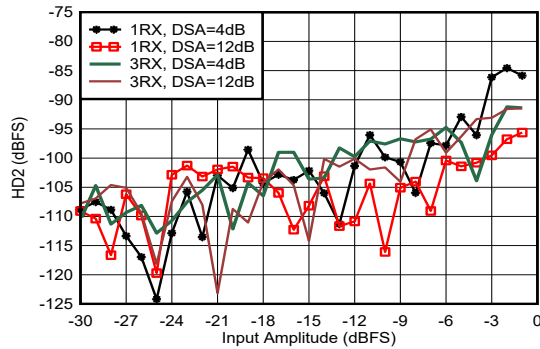
With 1.8 GHz matching,  $f_{in} = 1900\text{ MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-324. RX HD2 vs DSA Setting and Channel at 1.9 GHz



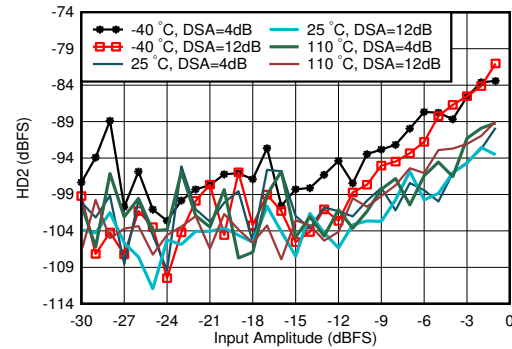
With 1.8 GHz matching,  $f_{in} = 1900\text{ MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-325. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



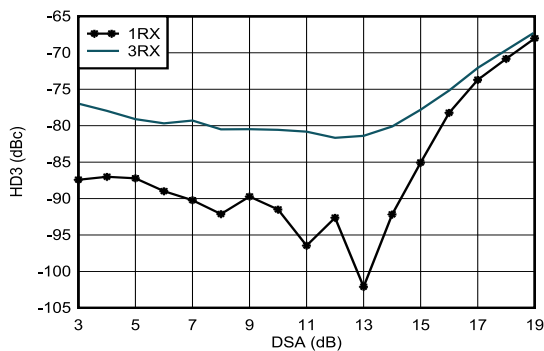
With 1.8 GHz matching,  $f_{in} = 1900\text{ MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-326. RX HD2 vs Input Amplitude and Channel at 1.9 GHz



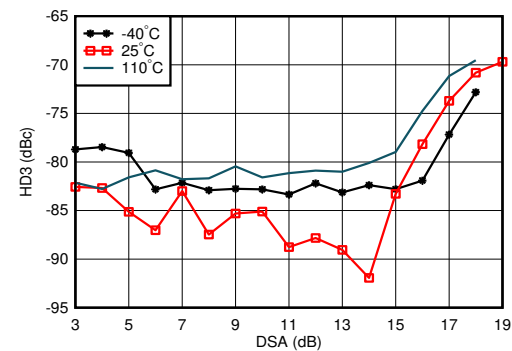
With 1.8 GHz matching,  $f_{in} = 1900\text{ MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 6-327. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz



With 1.8 GHz matching,  $f_{in} = 1900\text{ MHz}$ , DDC bypass mode (TI only mode for characterization)

Figure 6-328. RX HD3 vs DSA Setting and Channel at 1.9 GHz

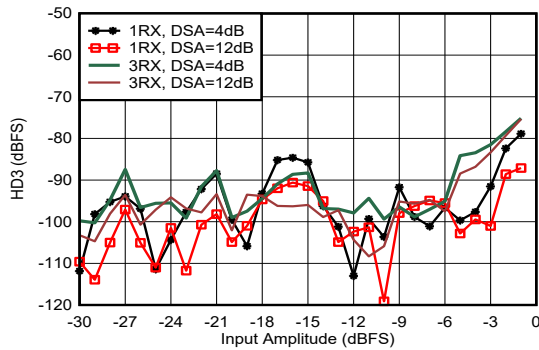


With 1.8 GHz matching,  $f_{in} = 1900\text{ MHz}$ , DDC bypass mode (TI only mode for characterization)

Figure 6-329. RX HD3 vs DSA Setting and Temperature at 1.9 GHz

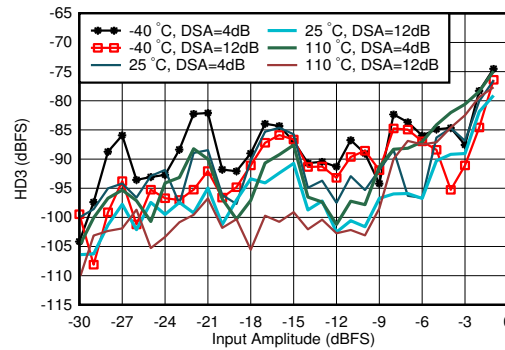
### 6.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



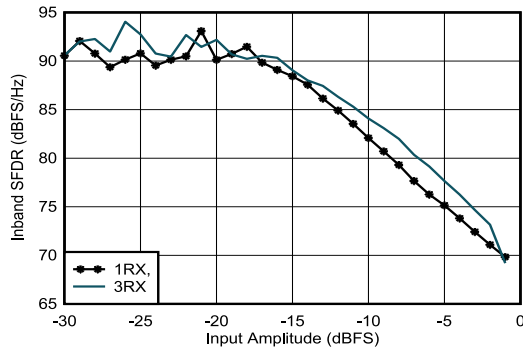
With 1.8 GHz matching,  $f_{in} = 1900\text{ MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 6-330. RX HD3 vs Input Level and Channel at 1.9 GHz**



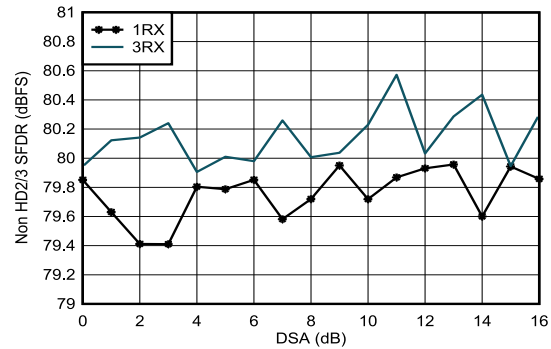
With 1.8 GHz matching,  $f_{in} = 1900\text{ MHz}$ , DDC bypass mode (TI only mode for characterization)

**Figure 6-331. RX HD3 vs Input Level and Temperature at 1.9 GHz**



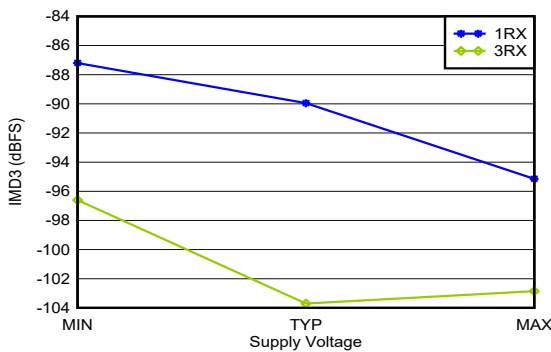
With 1.8 GHz matching, decimated by 3

**Figure 6-332. RX In-Band SFDR ( $\pm 400\text{ MHz}$ ) vs Input Amplitude at 1.75 GHz**



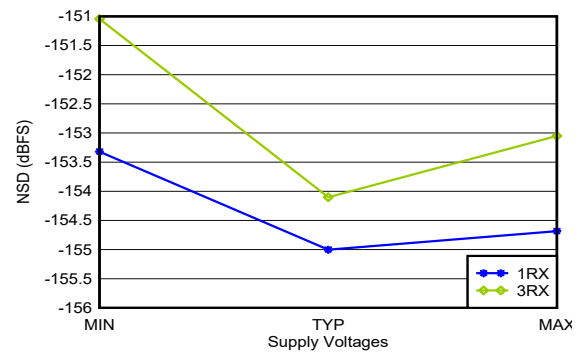
With 1.8 GHz matching

**Figure 6-333. RX Non-HD2/3 vs DSA Setting at 1.75 GHz**



With 1.8 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-334. RX IMD3 vs Supply and Channel at 1.75 GHz**

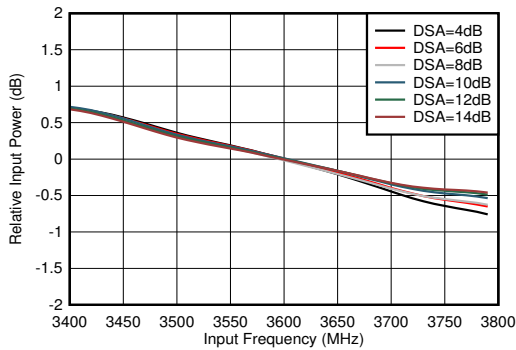


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-335. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz**

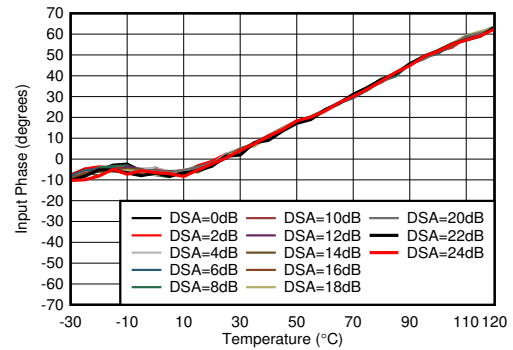
### 6.12.10 RX Typical Characteristics at 3.5 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



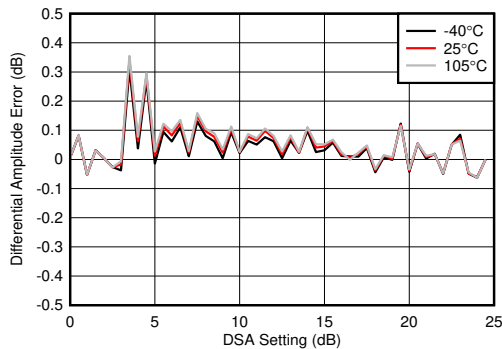
With 3.6 GHz matching, normalized to 3.6 GHz

**Figure 6-336. RX In-Band Gain Flatness,  $f_{\text{IN}} = 3600 \text{ MHz}$**



With 3.6 GHz matching, normalized to phase at  $25^\circ\text{C}$

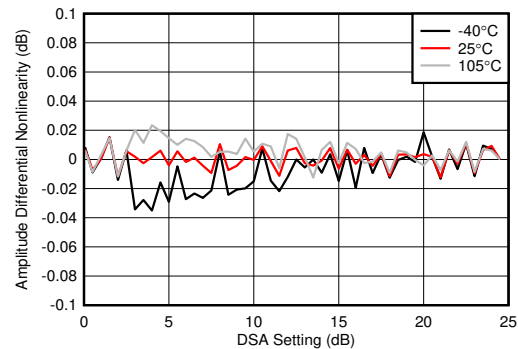
**Figure 6-337. RX Input Phase vs Temperature at 3.6 GHz**



With 3.6 GHz matching

$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

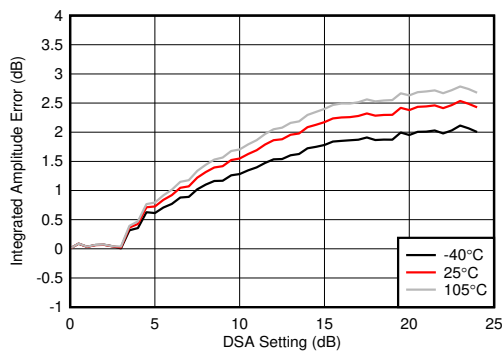
**Figure 6-338. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

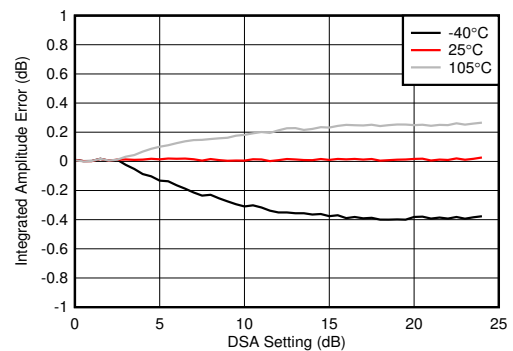
**Figure 6-339. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

**Figure 6-340. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching

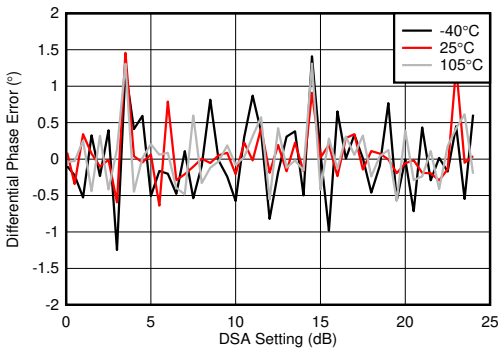
$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

**Figure 6-341. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz**



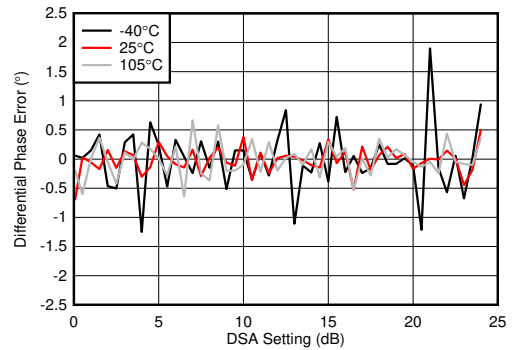
**6.12.10 RX Typical Characteristics at 3.5 GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



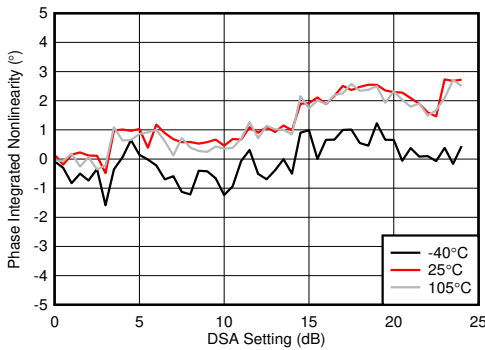
With 3.6 GHz matching  
Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

**Figure 6-342. RX Uncalibrated Differential Phase Error vs DSA Setting at 3.6 GHz**



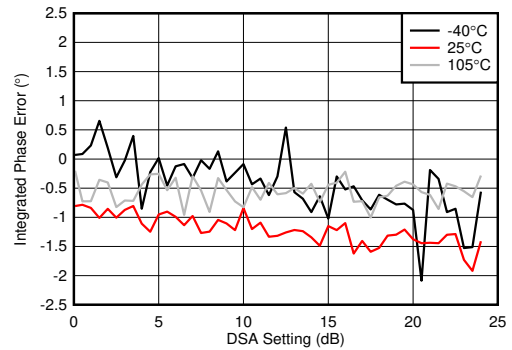
With 3.6 GHz matching  
Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

**Figure 6-343. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz**



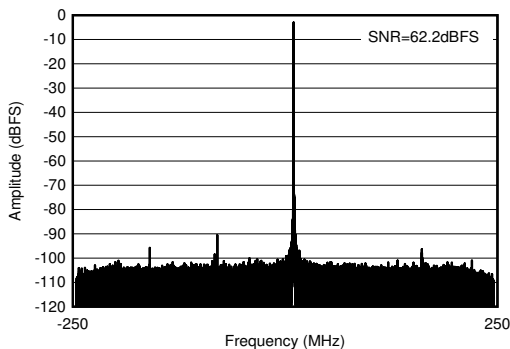
With 3.6 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-344. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz**



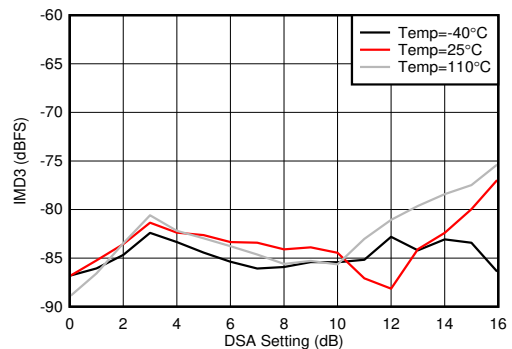
With 3.6 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-345. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz**



With 3.6 GHz matching,  $f_{\text{IN}} = 3610 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$

**Figure 6-346. RX Output FFT at 3.6 GHz**

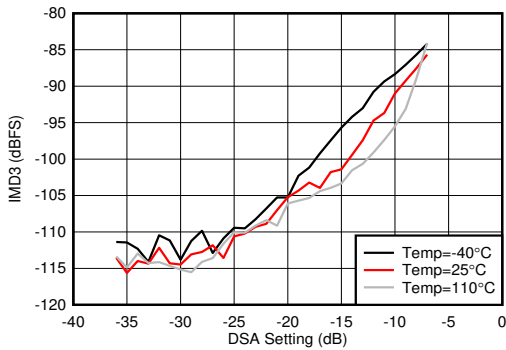


With 3.5 GHz matching, each tone at  $-7 \text{ dBFS}$ , 20-MHz tone spacing

**Figure 6-347. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz**

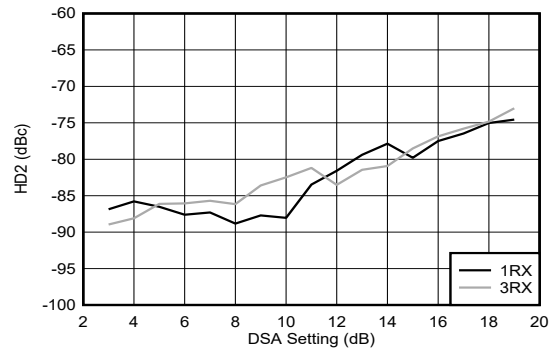
**6.12.10 RX Typical Characteristics at 3.5 GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



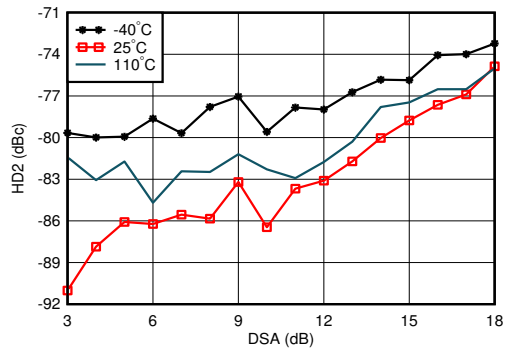
With 3.5 GHz matching, 20-MHz tone spacing

**Figure 6-348. RX IMD3 vs Input Level and Temperature at 3.6 GHz**



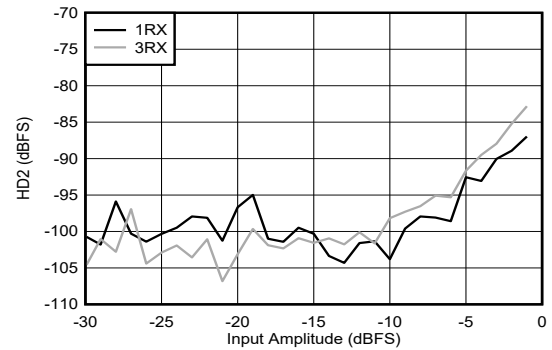
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-349. RX HD2 vs DSA Setting and Channel at 3.6 GHz**



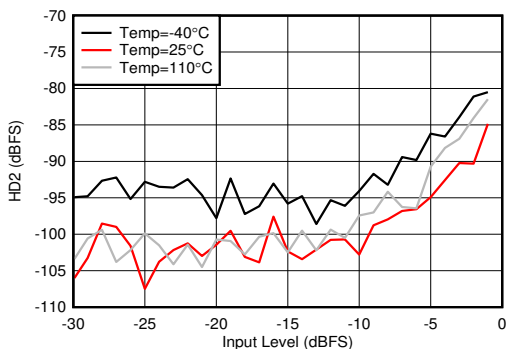
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-350. RX HD2 vs DSA Setting and Temperature at 3.6 GHz**



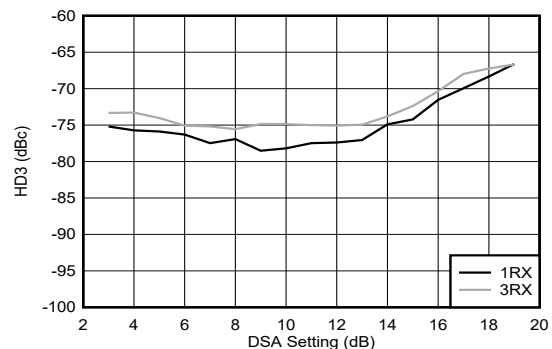
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-351. RX HD2 vs Input Level and Channel at 3.6 GHz**



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-352. RX HD2 vs Input Level and Temperature at 3.6 GHz**

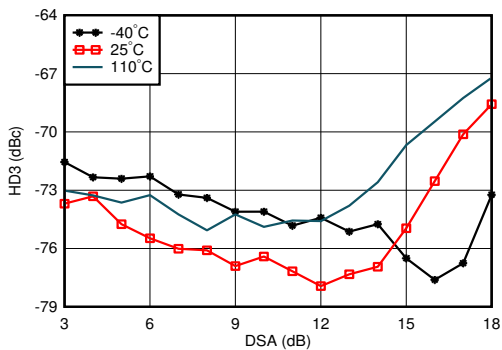


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-353. RX HD3 vs DSA Setting and Channel at 3.6 GHz**

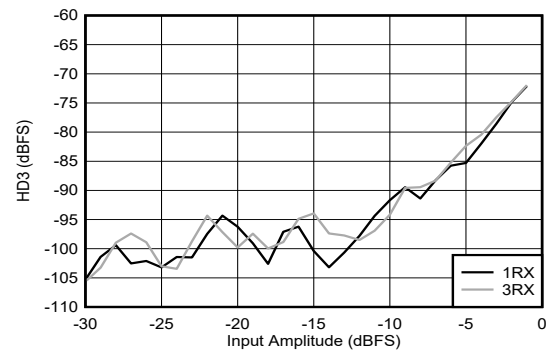
### 6.12.10 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



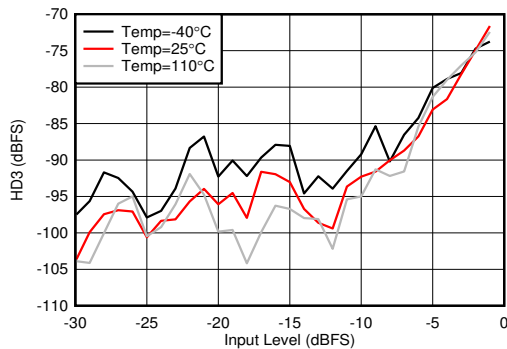
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-354. RX HD3 vs DSA Setting and Temperature at 3.6 GHz



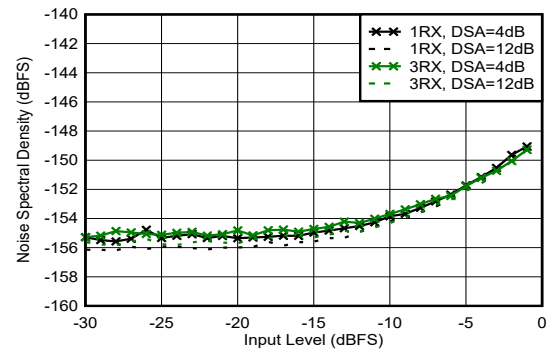
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-355. RX HD3 vs Input Level and Channel at 3.6 GHz



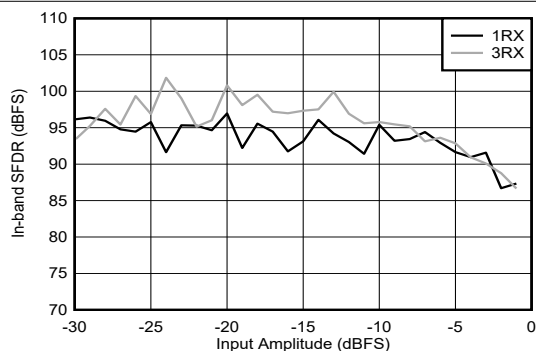
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 6-356. RX HD3 vs Input Level and Temperature at 3.6 GHz



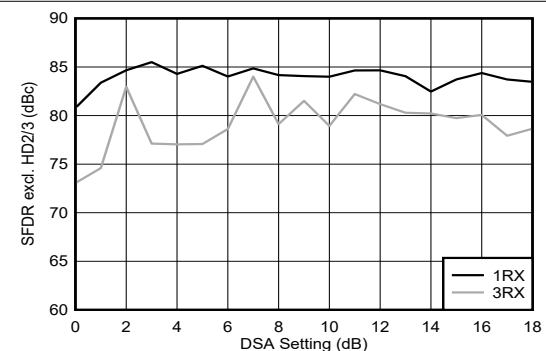
With 3.5 GHz matching, 12.5-MHz offset from tone

Figure 6-357. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



With 3.5 GHz matching

Figure 6-358. RX In-Band SFDR ( $\pm 200\text{ MHz}$ ) vs Input Level and Channel at 3.6 GHz

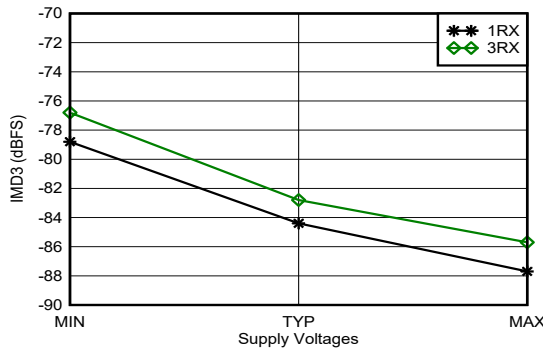


With 3.5 GHz matching

Figure 6-359. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz

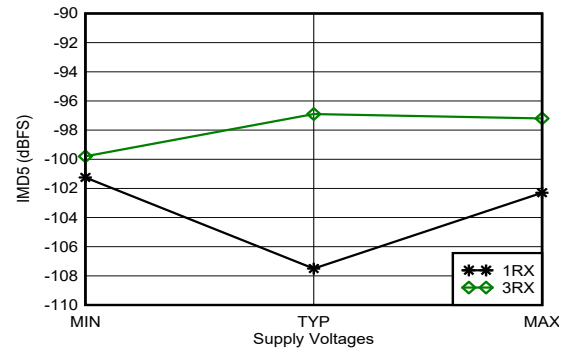
### 6.12.10 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



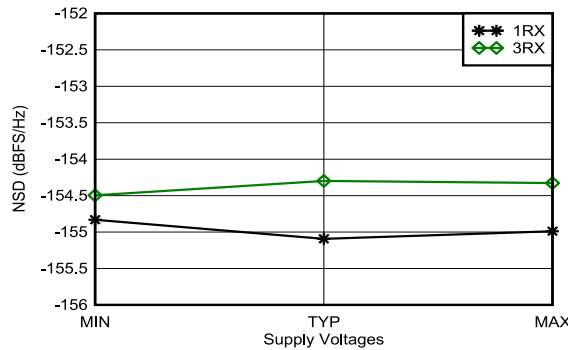
With 3.6 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-360. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz**



With 3.6 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-361. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz**

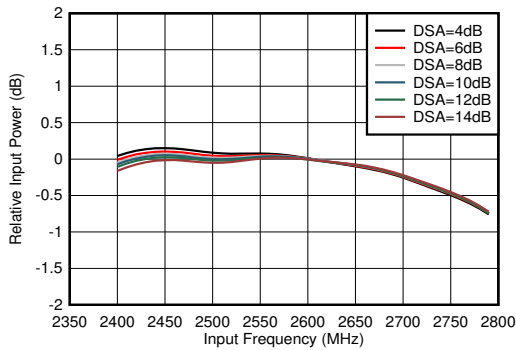


With 3.6 GHz matching, tone at  $-20\text{ dBFS}$ , 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-362. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz**

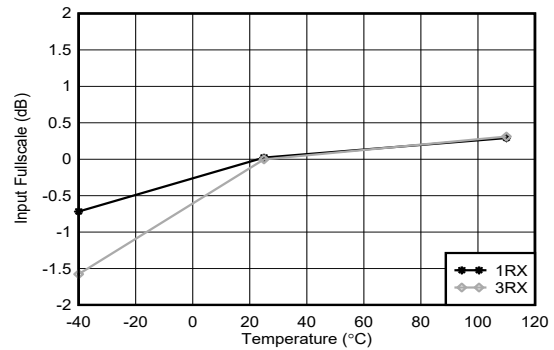
### 6.12.11 RX Typical Characteristics at 2.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



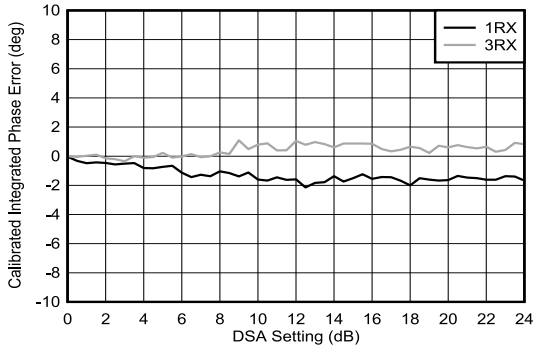
With matching, normalized to power at 2.6 GHz for each DSA setting

**Figure 6-363. RX Inband Gain Flatness,  $f_{\text{IN}} = 2600 \text{ MHz}$**



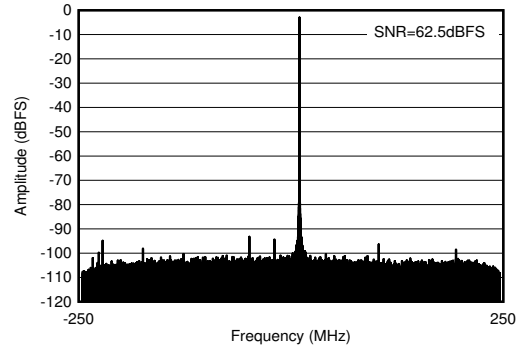
With 2.6 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

**Figure 6-364. RX Input Fullscale vs Temperature and Channel at 2.6 GHz**



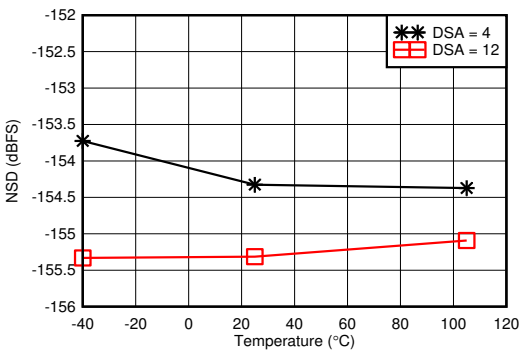
With 2.6 GHz matching  
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

**Figure 6-365. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz**



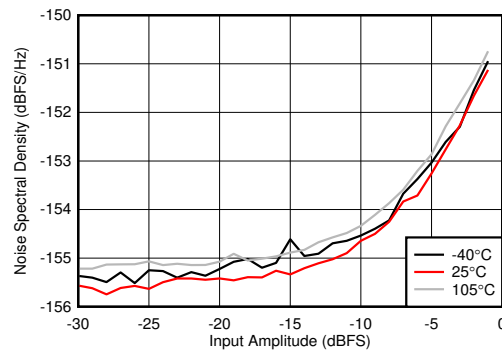
With 2.6 GHz matching,  $f_{\text{IN}} = 2610 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$

**Figure 6-366. RX Output FFT at 2.6 GHz**



With 2.6 GHz matching, 12.5-MHz offset from tone

**Figure 6-367. RX Noise Spectral Density vs Temperature at 2.6 GHz**

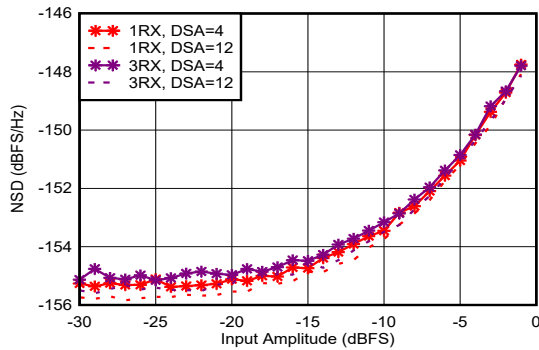


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 6-368. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz**

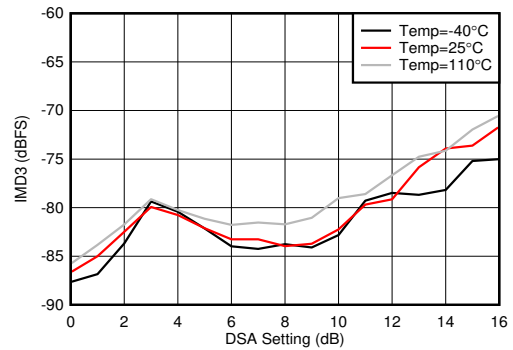
### 6.12.11 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



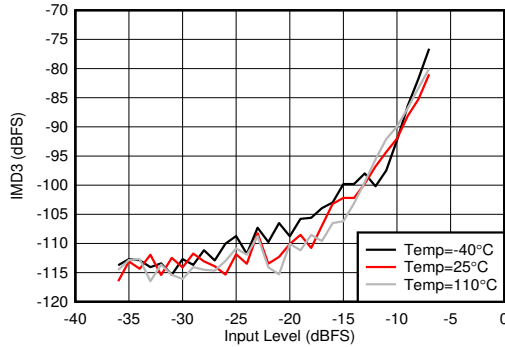
With 2.6 GHz matching, 12.5-MHz offset from tone

**Figure 6-369. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz**



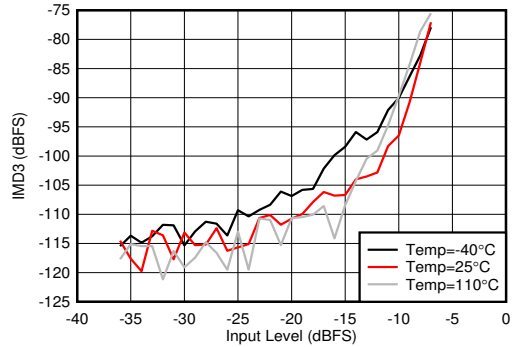
With 2.6 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-370. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz**



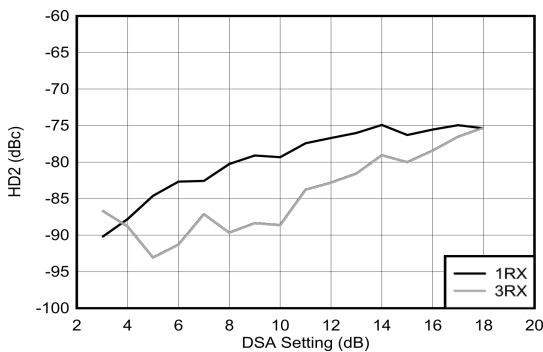
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 6-371. RX IMD3 vs Input Level and Temperature at 2.6 GHz**



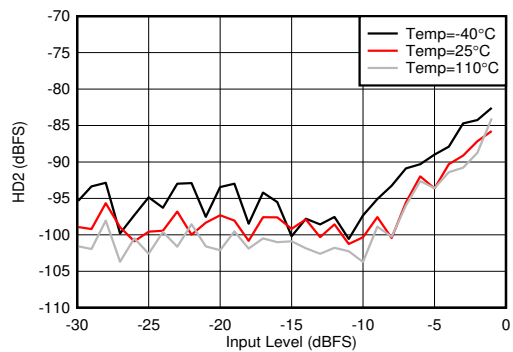
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-372. RX IMD3 vs Input Level and Temperature at 2.6 GHz**



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-373. RX HD2 vs DSA Setting and Channel at 2.6 GHz**

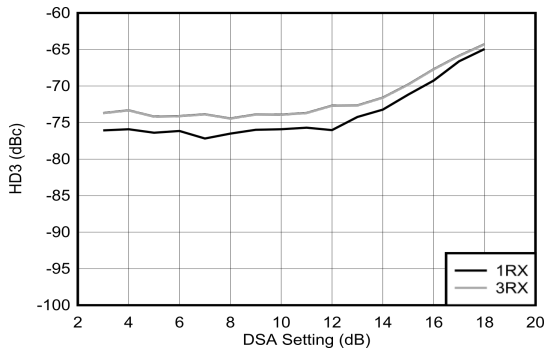


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-374. RX HD2 vs Input Level and Temperature at 2.6 GHz**

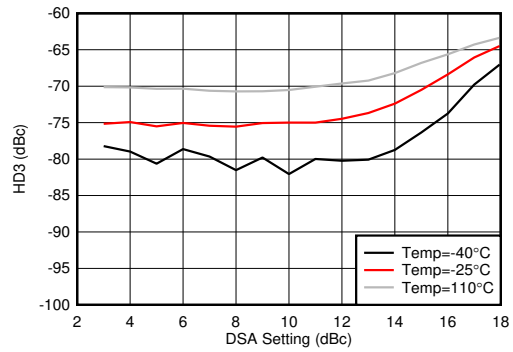
### 6.12.11 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



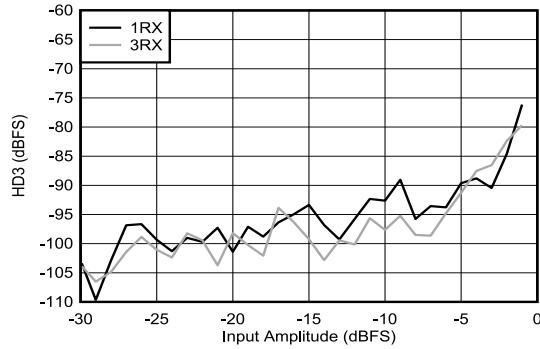
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-375. RX HD3 vs DSA Setting and Channel at 2.6 GHz**



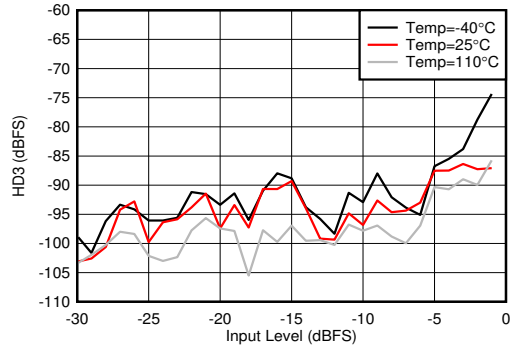
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-376. RX HD3 vs DSA Setting and Temperature at 2.6 GHz**



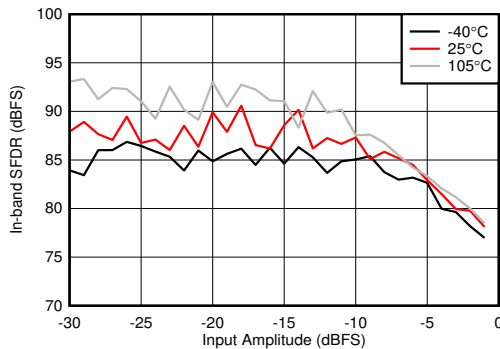
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-377. RX HD3 vs Input Level and Channel at 2.6 GHz**



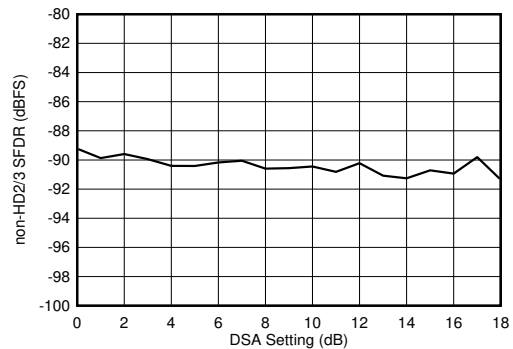
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-378. RX HD3 vs Input Level and Temperature at 2.6 GHz**



With 2.6 GHz matching, decimate by 4

**Figure 6-379. RX In-Band SFDR ( $\pm 300\text{ MHz}$ ) vs Input Amplitude and Temperature at 2.6 GHz**

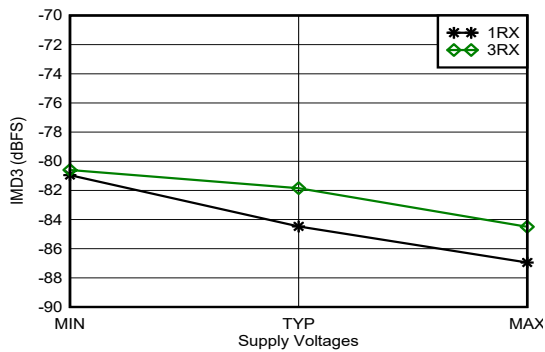


With 2.6 GHz matching

**Figure 6-380. RX Non-HD2/3 vs DSA Setting at 2.6 GHz**

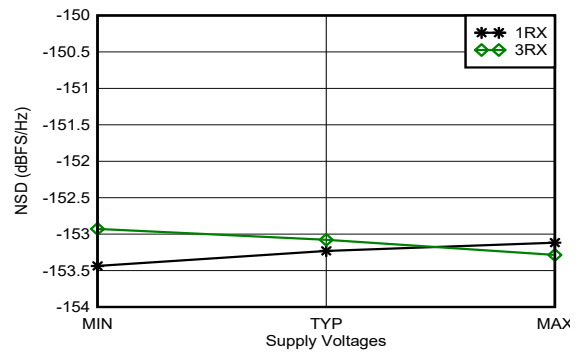
### 6.12.11 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 2.6 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-381. RX IMD3 vs Supply and Channel at 2.6 GHz



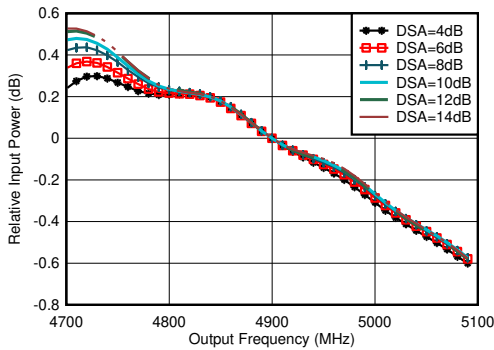
With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 6-382. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz



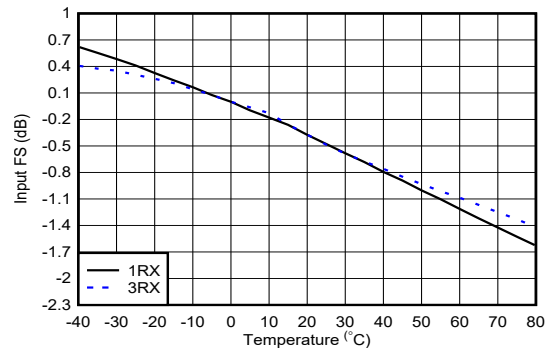
### 6.12.12 RX Typical Characteristics at 4.9 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



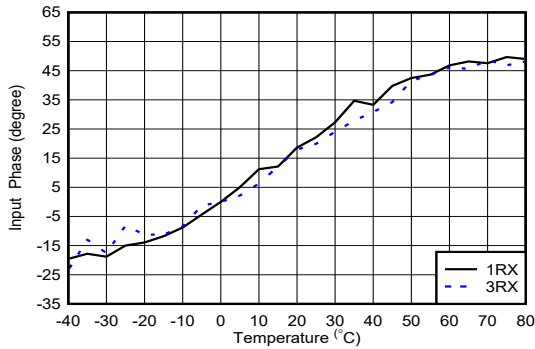
With matching, normalized to power at 4.9GHz for each DSA setting

**Figure 6-383. RX Inband Gain Flatness,  $f_{IN} = 4900\text{ MHz}$**



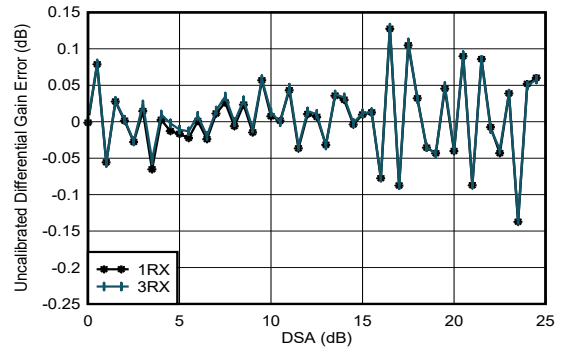
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

**Figure 6-384. RX Input Fullscale vs Temperature and Channel at 4.9 GHz**



With 4.9 GHz matching, normalized to phase at 25°C

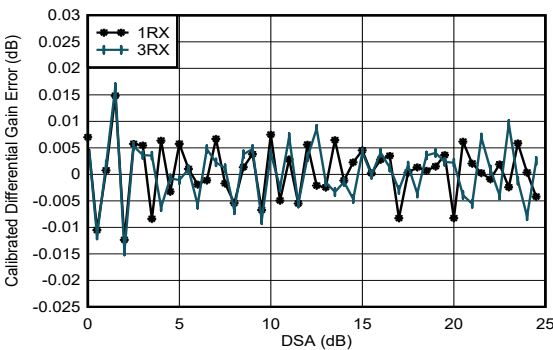
**Figure 6-385. RX Input Phase vs Temperature and DSA at  $f_{OUT} = 4.9\text{ GHz}$**



With 4.9 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

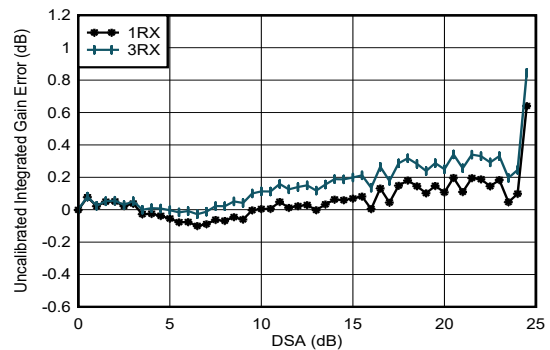
**Figure 6-386. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching

Differential Amplitude Error =  $P_{IN}(\text{DSA Setting} - 1) - P_{IN}(\text{DSA Setting}) + 1$

**Figure 6-387. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz**



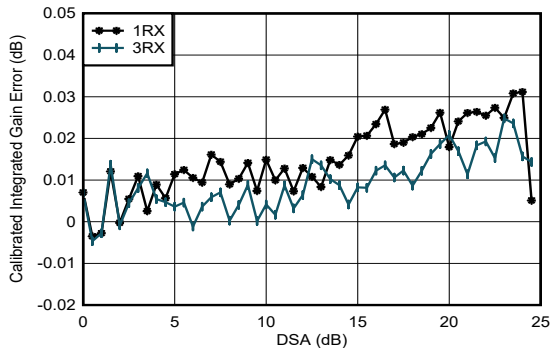
With 4.9 GHz matching

Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-388. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz**

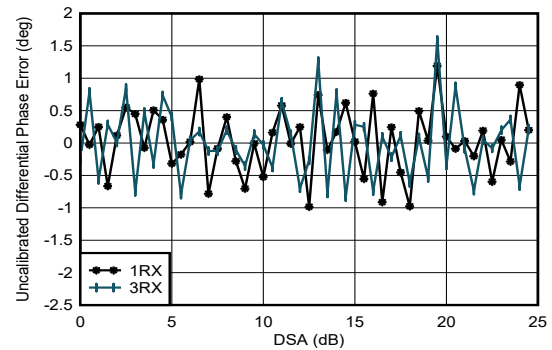
### 6.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



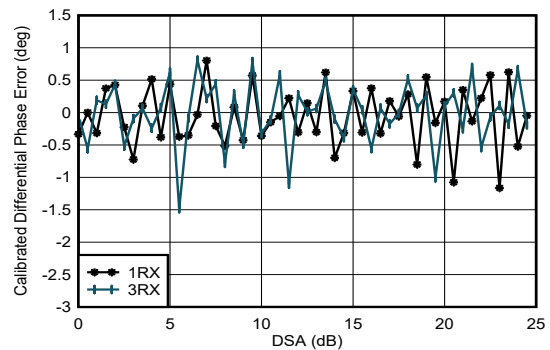
With 4.9 GHz matching  
Integrated Amplitude Error =  $P_{IN}(\text{DSA Setting}) - P_{IN}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

**Figure 6-389. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz**



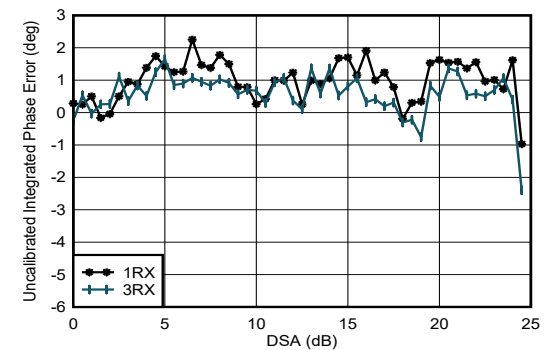
With 4.9 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-390. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz**



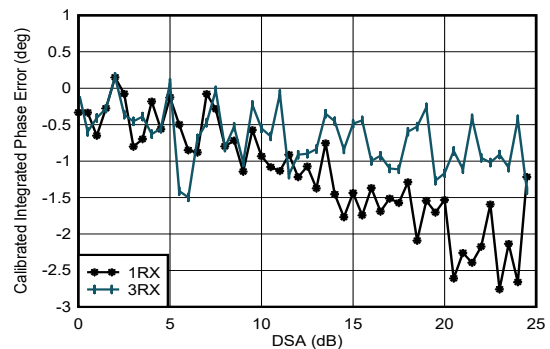
With 4.9 GHz matching  
Differential Phase Error =  $\text{Phase}_{IN}(\text{DSA Setting} - 1) - \text{Phase}_{IN}(\text{DSA Setting})$

**Figure 6-391. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz**



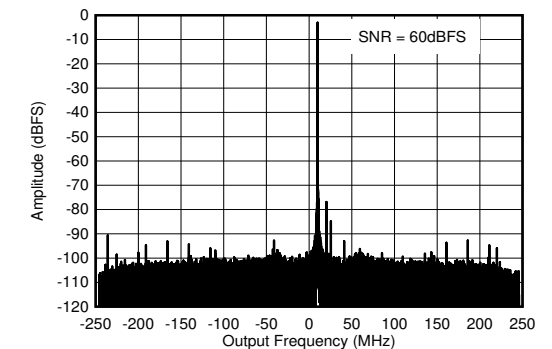
With 4.9 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-392. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching  
Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

**Figure 6-393. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz**

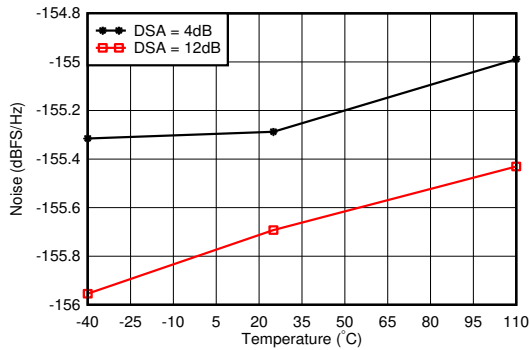


With 4.9 GHz matching,  $f_{IN} = 4910\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$

**Figure 6-394. RX Output FFT at 4.9 GHz**

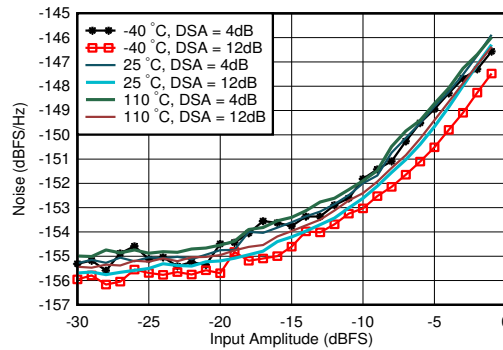
### 6.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



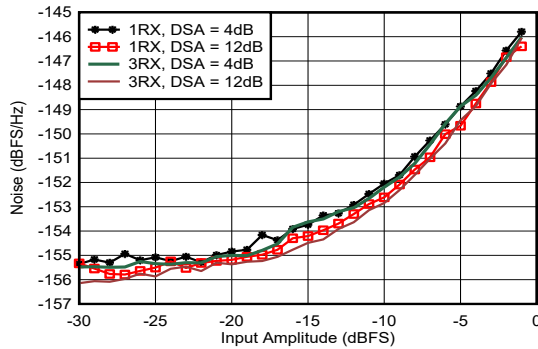
With 4.9 GHz matching, 12.5-MHz offset from tone

**Figure 6-395. RX Noise Spectral Density vs Temperature at 4.9 GHz**



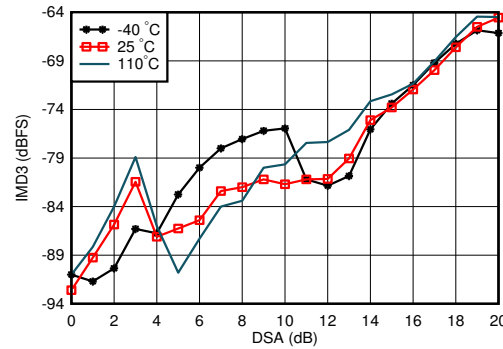
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

**Figure 6-396. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz**



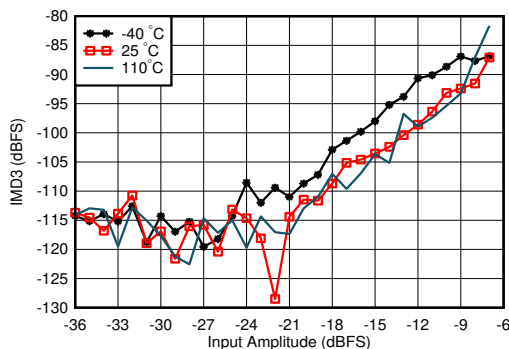
With 4.9 GHz matching, 12.5-MHz offset from tone

**Figure 6-397. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz**



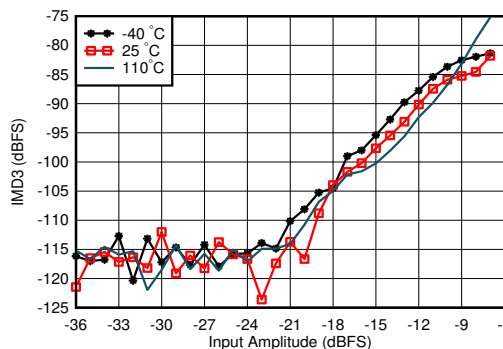
With 4.9 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

**Figure 6-398. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz**



With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

**Figure 6-399. RX IMD3 vs Input Level and Temperature at 4.9 GHz**

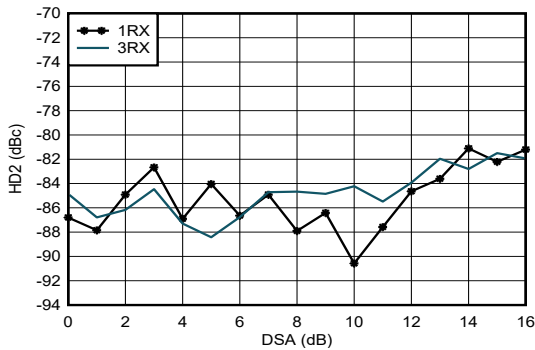


With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

**Figure 6-400. RX IMD3 vs Input Level and Temperature at 4.9 GHz**

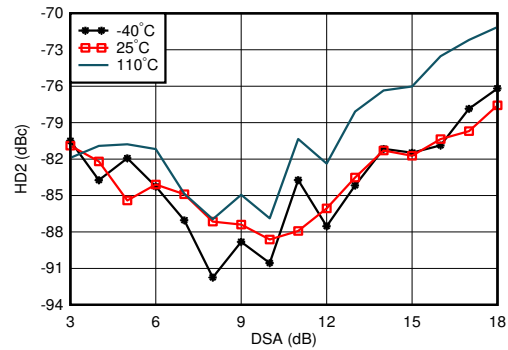
**6.12.12 RX Typical Characteristics at 4.9 GHz (continued)**

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



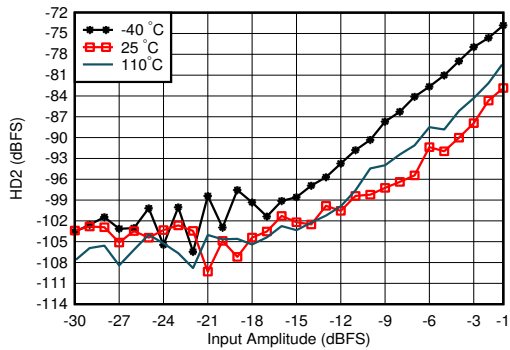
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-401. RX HD2 vs DSA Setting and Channel at 4.9 GHz**



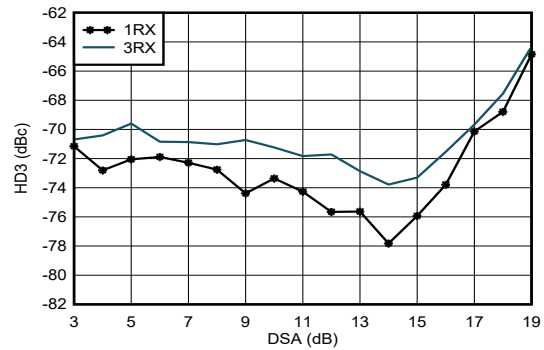
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-402. RX HD2 vs DSA and Temperature at 4.9 GHz**



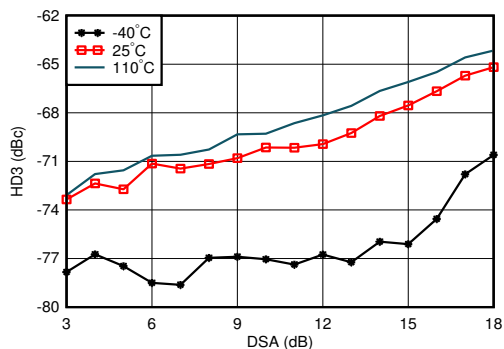
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

**Figure 6-403. RX HD2 vs Input Level and Temperature at 4.9 GHz**



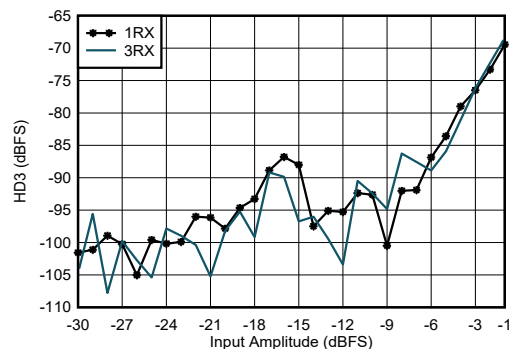
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-404. RX HD3 vs DSA Setting and Channel at 4.9 GHz**



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-405. RX HD3 vs DSA Setting and Temperature at 4.9 GHz**

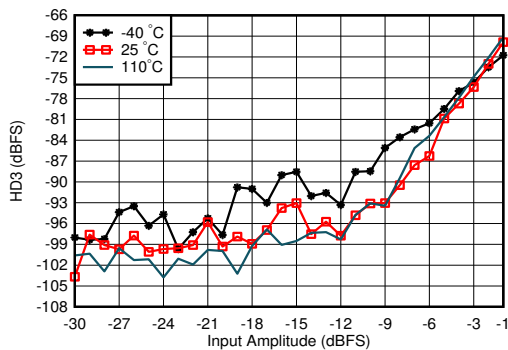


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-406. RX HD3 vs Input Level and Channel at 4.9 GHz**

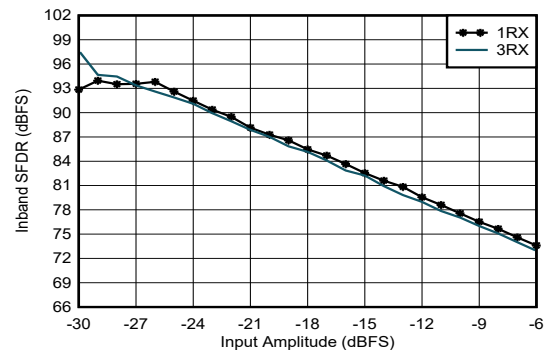
### 6.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with  $f_{REF} = 491.52\text{ MHz}$ ,  $A_{IN} = -3\text{ dBFS}$ , DSA setting = 4 dB.



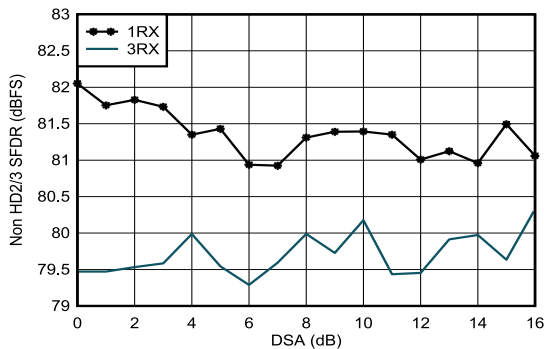
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

**Figure 6-407. RX HD3 vs Input Level and Temperature at 4.9 GHz**



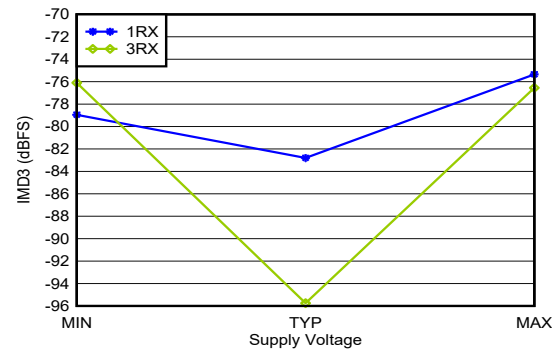
With 4.9 GHz matching, decimate by 3

**Figure 6-408. RX In-Band SFDR ( $\pm 400\text{ MHz}$ ) vs Input Amplitude and Channel at 4.9 GHz**



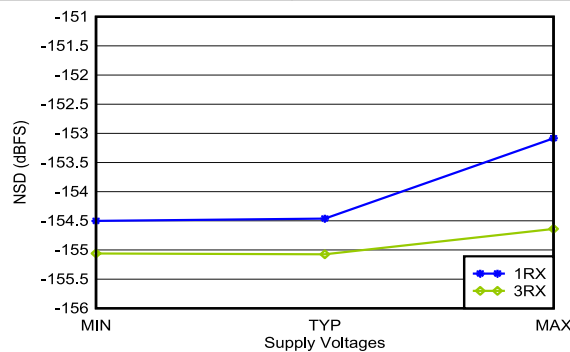
With 4.9 GHz matching

**Figure 6-409. RX Non-HD2/3 vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-410. RX IMD3 vs Supply and Channel at 4.9 GHz**



With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

**Figure 6-411. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz**

### 6.12.13 RX Typical Characteristics at 8.1 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 8.1 GHz matching.

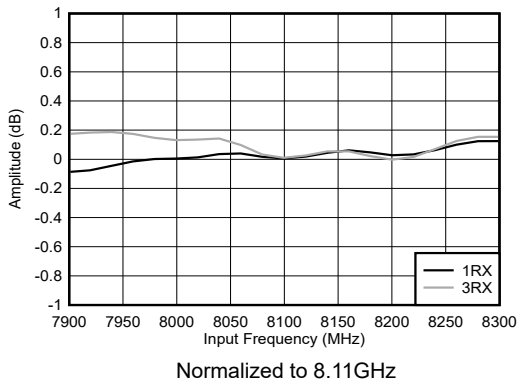


Figure 6-412. RX Amplitude vs Frequency and Channel

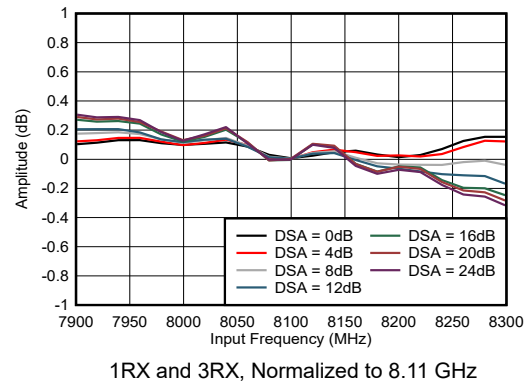


Figure 6-413. RX Amplitude vs Frequency and DSA Setting

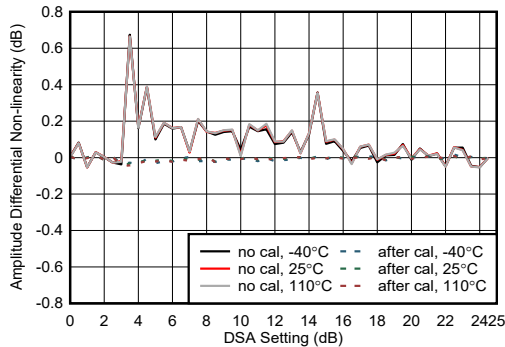


Figure 6-414. RX Amplitude Differential Nonlinearity at 8.1 GHz

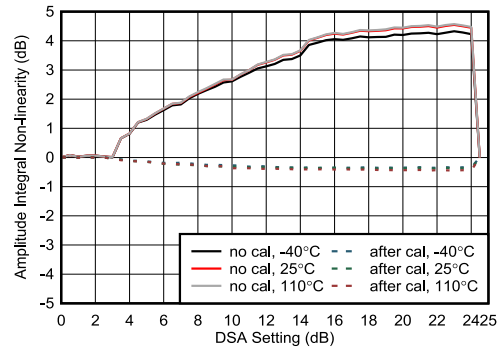


Figure 6-415. RX Amplitude Integrated Nonlinearity at 8.1 GHz

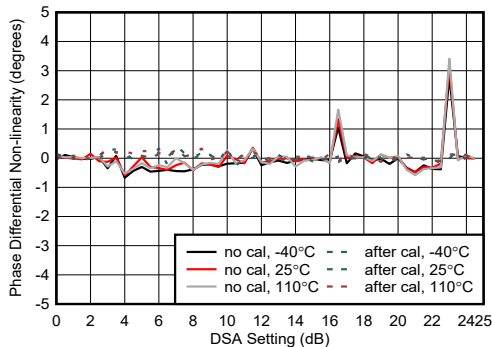


Figure 6-416. RX Phase Differential Nonlinearity at 8.1 GHz

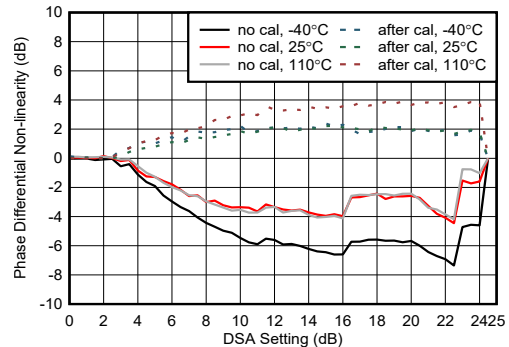


Figure 6-417. RX Phase Differential Nonlinearity at 8.1 GHz

### 6.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), External clock mode with  $f_{\text{CLK}} = 11796.48\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB, 8.1 GHz matching.

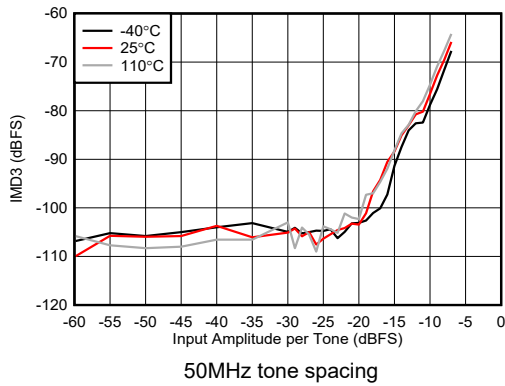


Figure 6-418. RX IMD3 vs Input Amplitude at 8.1 GHz

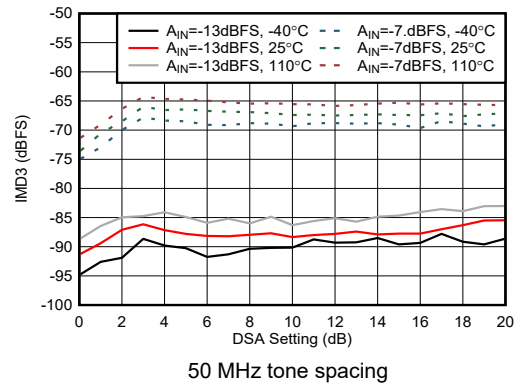


Figure 6-419. RX IMD3 vs DSA Setting at 8.1 GHz

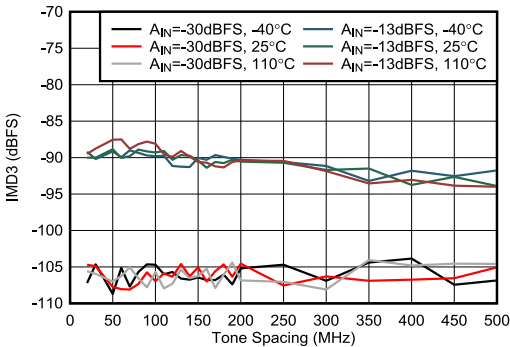


Figure 6-420. RX IMD3 vs Tone Spacing at 8.1 GHz

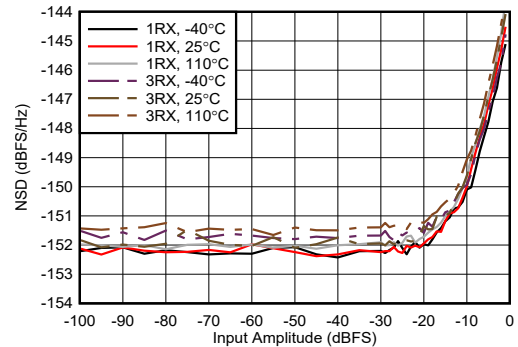


Figure 6-421. RX NSD vs Digital Amplitude at 8.1 GHz

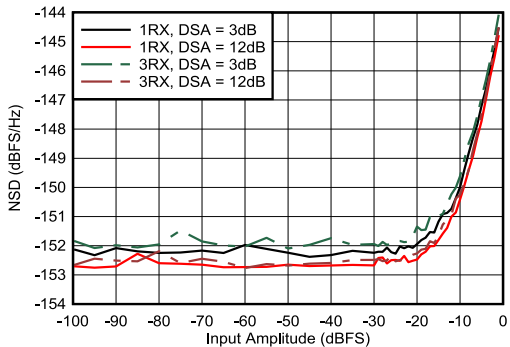


Figure 6-422. RX NSD vs Digital Amplitude at 8.1 GHz

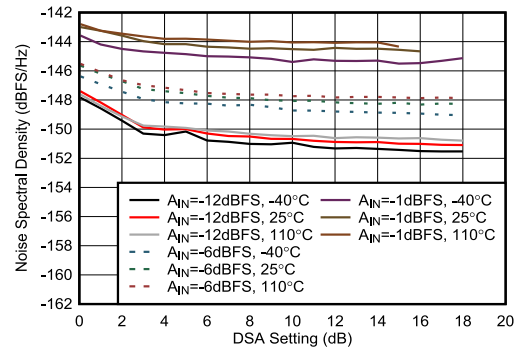


Figure 6-423. RX NSD vs DSA Setting at 8.1 GHz

### 6.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 8.1 GHz matching.

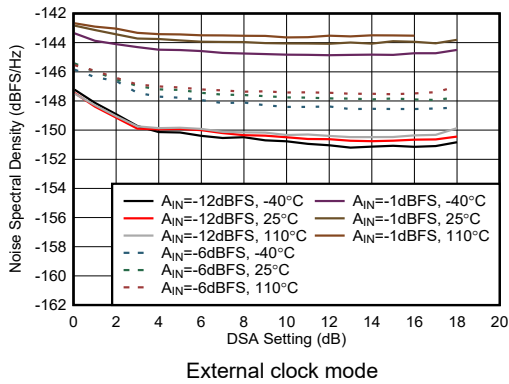


Figure 6-424. RX NSD vs DSA Setting at 8.1 GHz

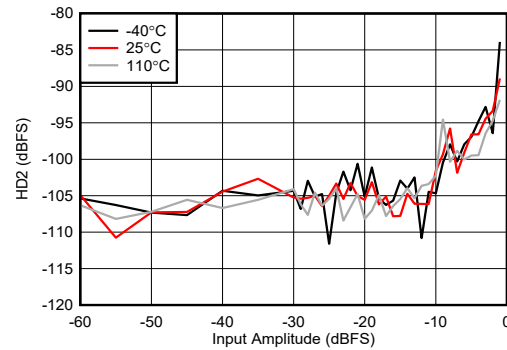


Figure 6-425. RX HD2 vs Digital Amplitude at 8.1 GHz

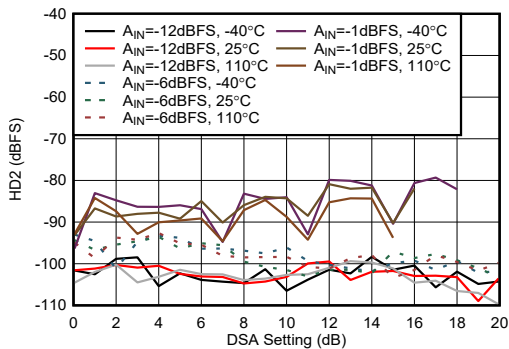


Figure 6-426. RX HD2 vs DSA Setting at 8.1 GHz

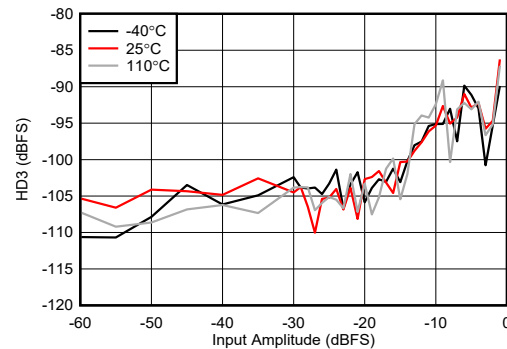


Figure 6-427. RX HD3 vs Digital Amplitude at 8.1 GHz

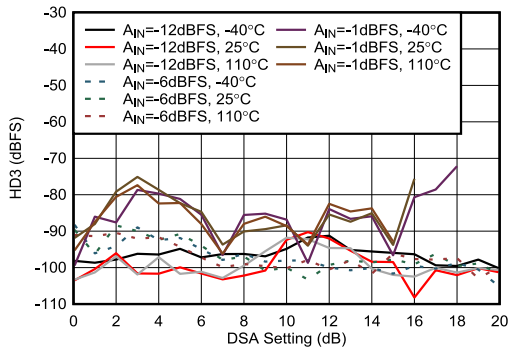


Figure 6-428. RX HD3 vs DSA Setting at 8.1 GHz

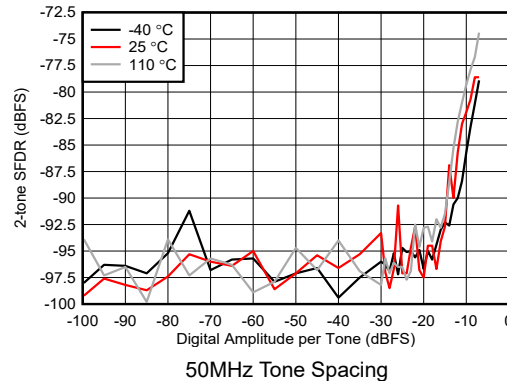
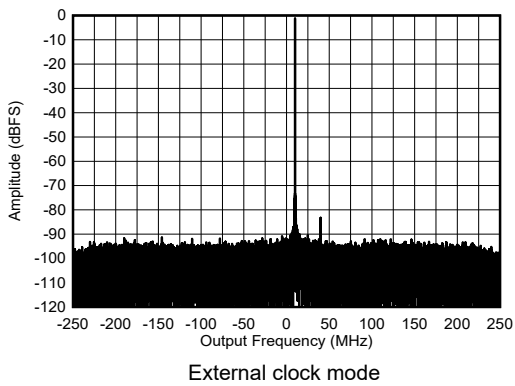


Figure 6-429. RX 2-tone SFDR vs Digital Amplitude at 8.1 GHz

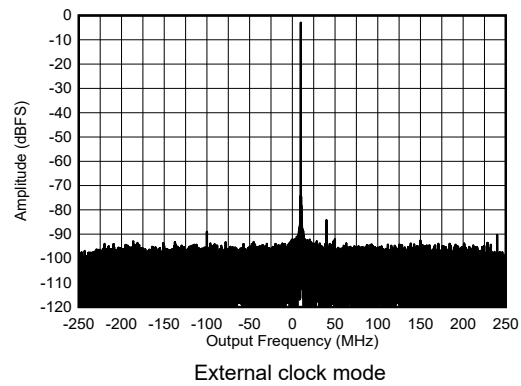


### 6.12.13 RX Typical Characteristics at 8.1 GHz (continued)

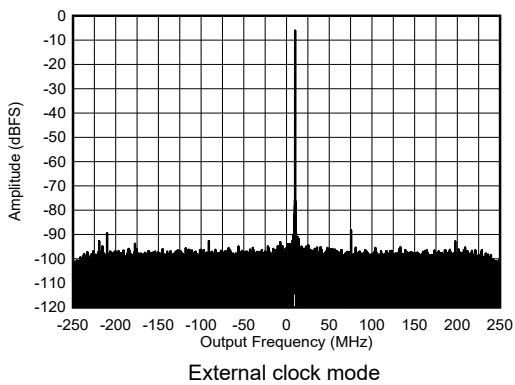
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 8.1 GHz matching.



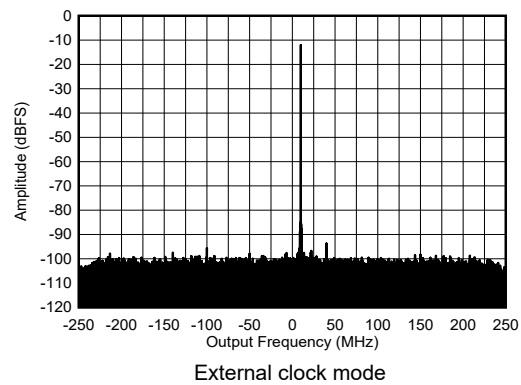
**Figure 6-430. RX Single Tone Output FFT at 8.1 GHz, -1 dBFS**



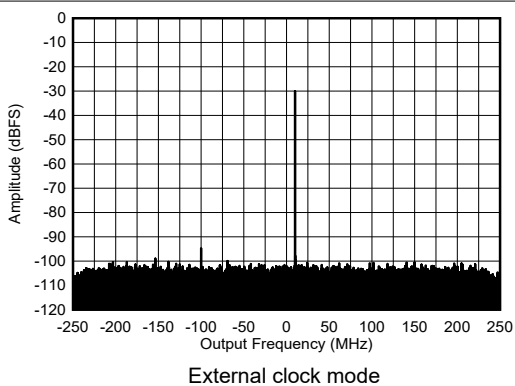
**Figure 6-431. RX Single Tone Output FFT at 8.1 GHz, -3 dBFS**



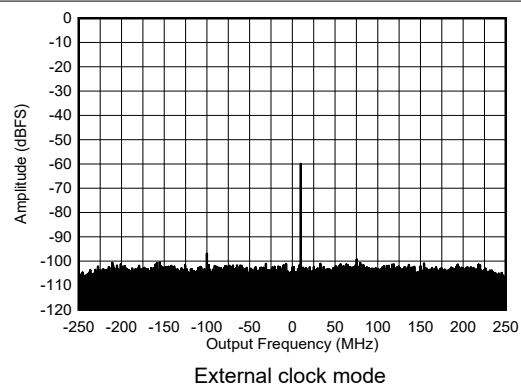
**Figure 6-432. RX Single Tone Output FFT at 8.1 GHz, -6 dBFS**



**Figure 6-433. RX Single Tone Output FFT at 8.1 GHz, -12 dBFS**



**Figure 6-434. RX Single Tone Output FFT at 8.1 GHz, -30 dBFS**



**Figure 6-435. RX Single Tone Output FFT at 8.1 GHz, -60 dBFS**

### 6.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 8.1 GHz matching.

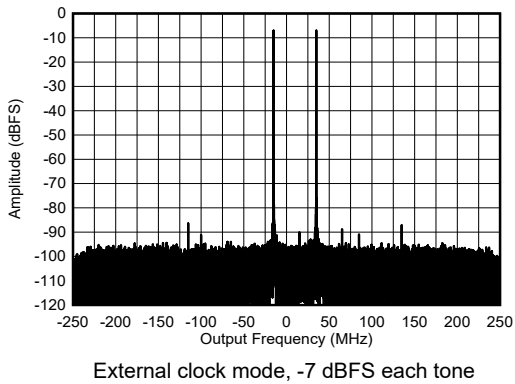


Figure 6-436. RX Dual Tone Output FFT at 8.11 GHz

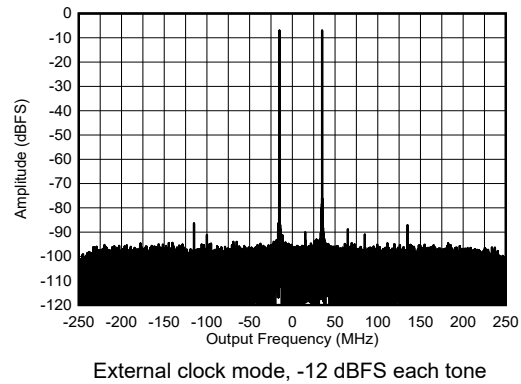


Figure 6-437. RX Dual Tone Output FFT at 8.11 GHz

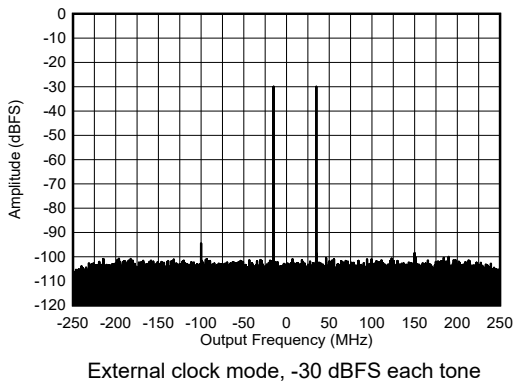


Figure 6-438. RX Dual Tone Output FFT at 8.11 GHz

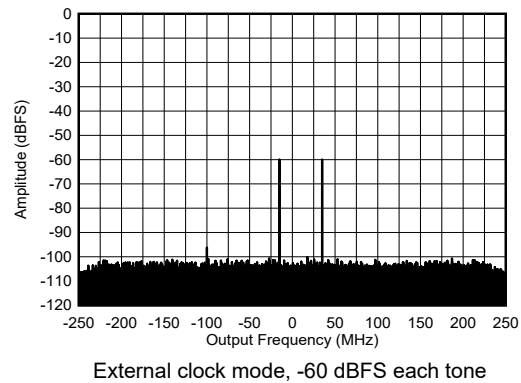


Figure 6-439. RX Dual Tone Output FFT at 8.11 GHz

### 6.12.14 RX Typical Characteristics at 9.6 GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

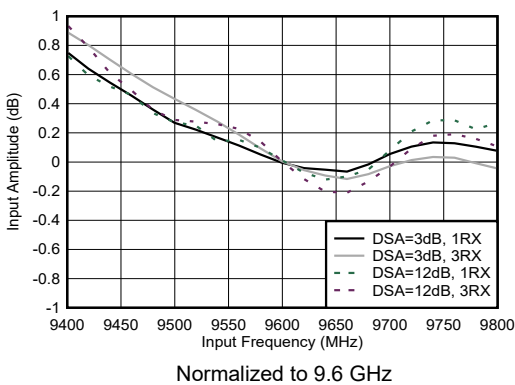


Figure 6-440. RX Input Amplitude vs Frequency

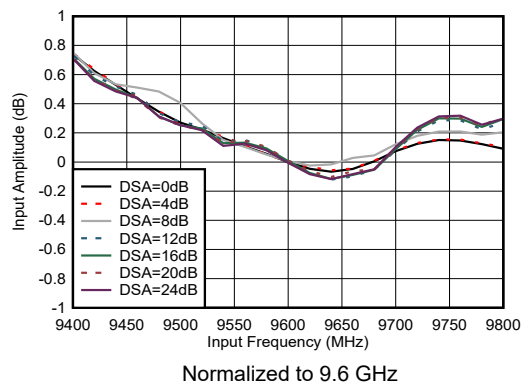


Figure 6-441. RX Input Amplitude vs Frequency at 9.6 GHz

### 6.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48$  MHz,  $A_{\text{IN}} = -3$  dBFS, DSA setting = 3 dB, 9.6 GHz matching.

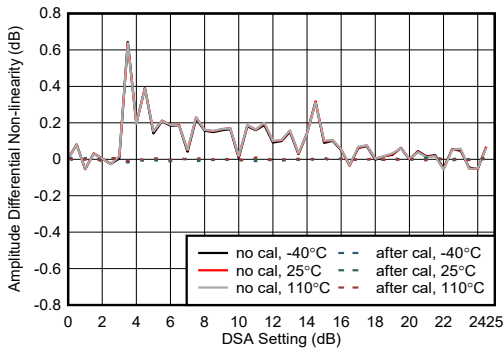


Figure 6-442. RX Amplitude Differential Non-linearity at 9.6 GHz

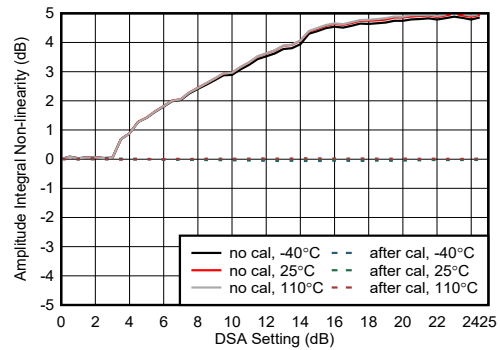


Figure 6-443. RX Amplitude Integrated Non-linearity at 9.6 GHz

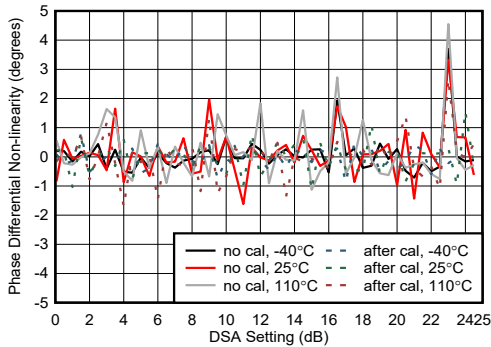


Figure 6-444. RX Phase Differential Non-linearity at 9.6 GHz

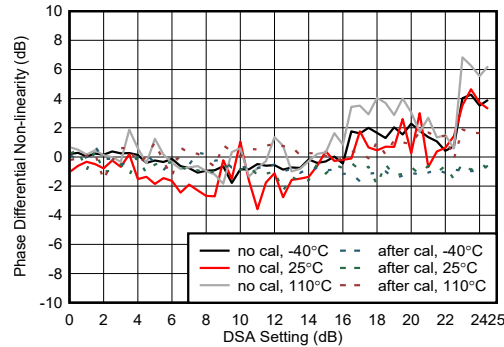


Figure 6-445. RX Phase Integrated Non-linearity at 9.6 GHz

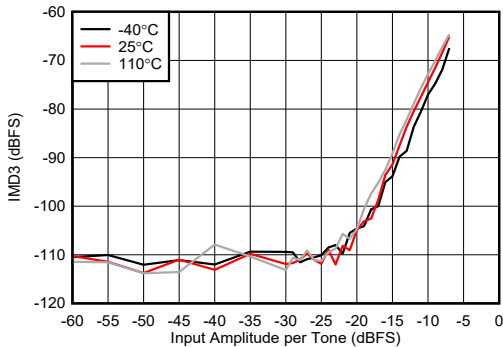


Figure 6-446. RX IMD3 vs Digital Amplitude at 9.6 GHz

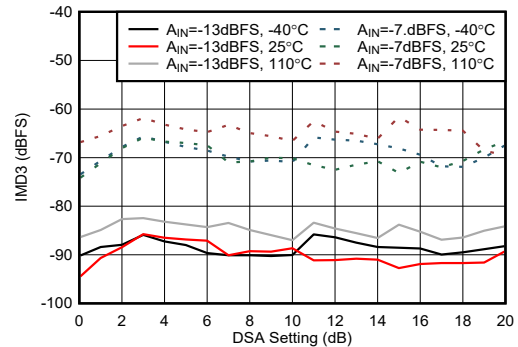


Figure 6-447. RX IMD3 vs DSA Setting at 9.6 GHz

### 6.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

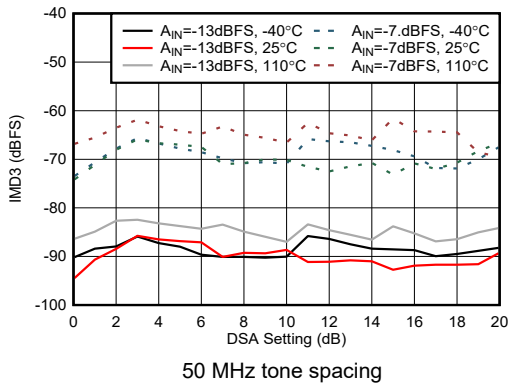


Figure 6-448. RX IMD3 vs DSA Setting at 9.6 GHz

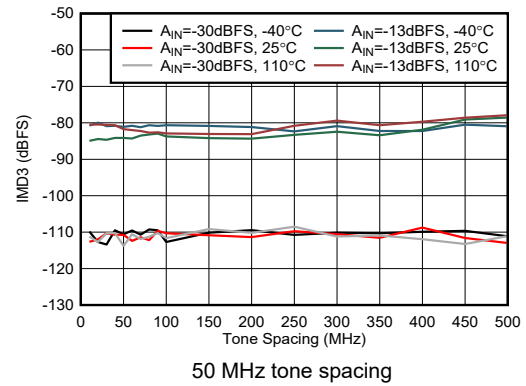


Figure 6-449. RX IMD3 vs Tone Spacing at 9.6 GHz

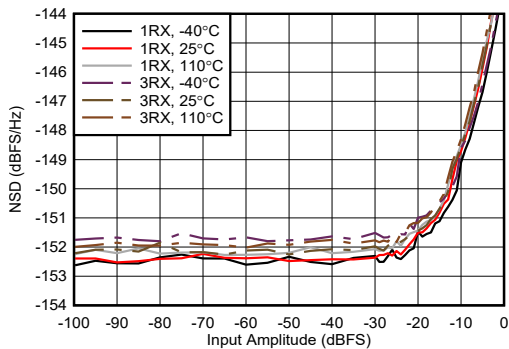


Figure 6-450. RX NSD vs Digital Amplitude at 9.6 GHz

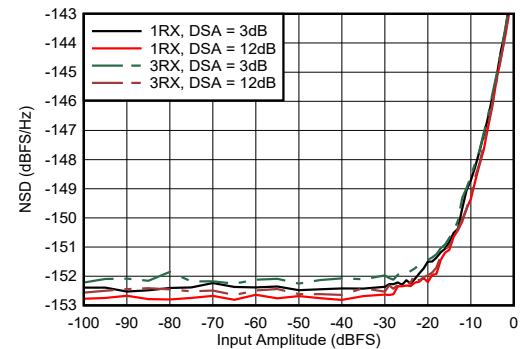


Figure 6-451. RX NSD vs Digital Amplitude at 9.6 GHz

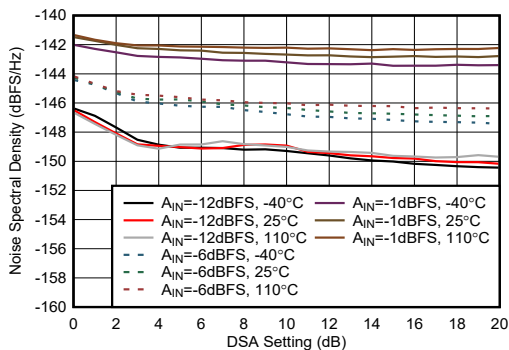


Figure 6-452. RX NSD vs DSA Setting at 9.6 GHz

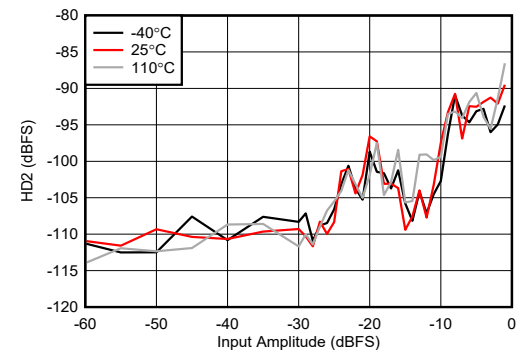


Figure 6-453. RX HD2 vs Digital Level at 9.6 GHz

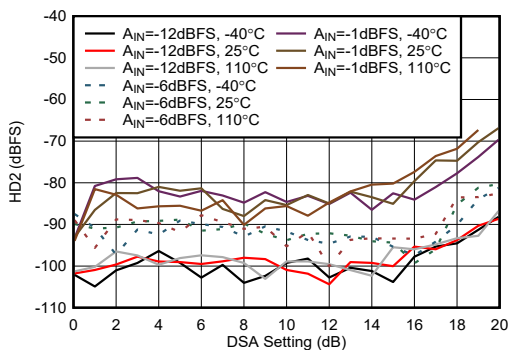


Figure 6-454. RX HD2 vs DSA Setting at 9.6 GHz

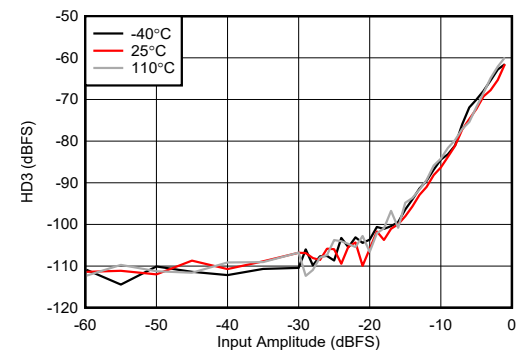


Figure 6-455. RX HD3 vs Digital Level at 9.6 GHz

### 6.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.

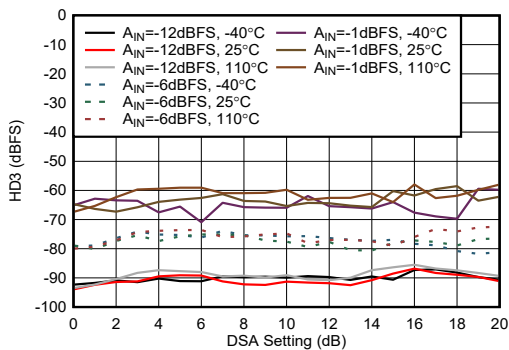
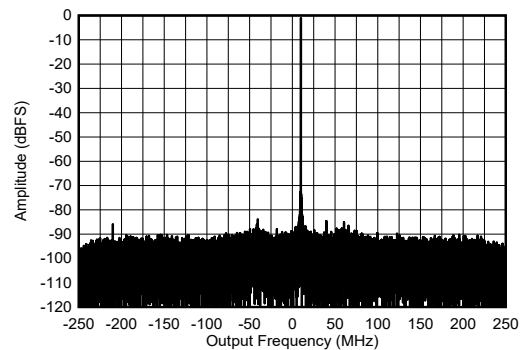
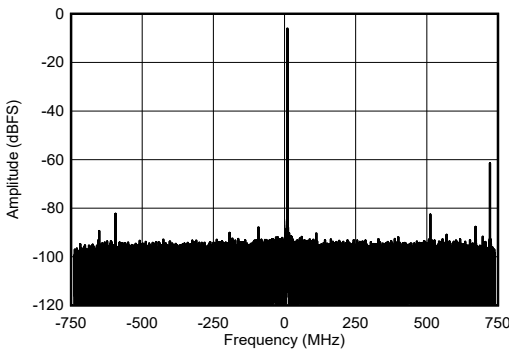


Figure 6-456. RX HD3 vs DSA Setting at 9.6 GHz



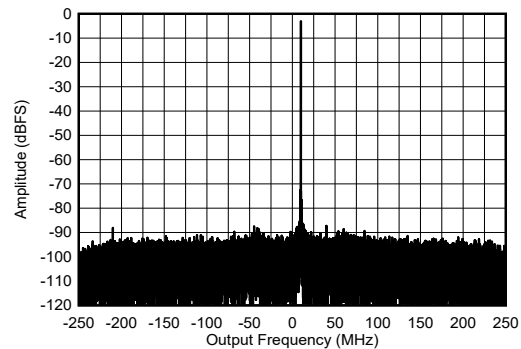
-1 dBFS

Figure 6-457. RX Single Tone Output FFT at 9.61 GHz



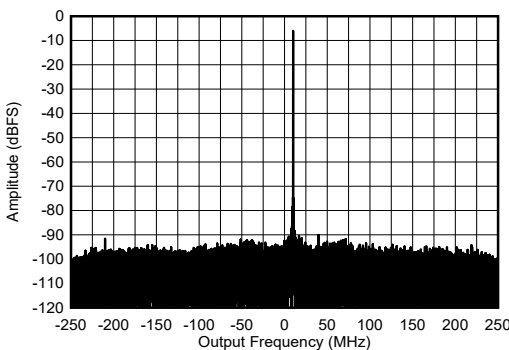
-6 dBFS

Figure 6-458. RX Single Tone Output FFT at 9.61 GHz



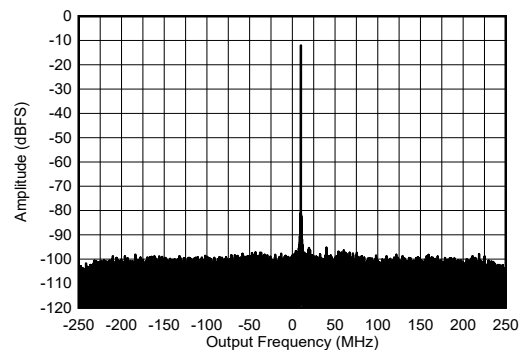
-3 dBFS

Figure 6-459. RX Single Tone Output FFT at 9.61 GHz



-6 dBFS

Figure 6-460. RX Single Tone Output FFT at 9.61 GHz

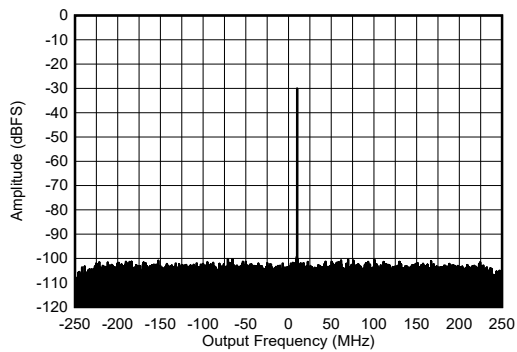


-12 dBFS

Figure 6-461. RX Single Tone Output FFT at 9.61 GHz

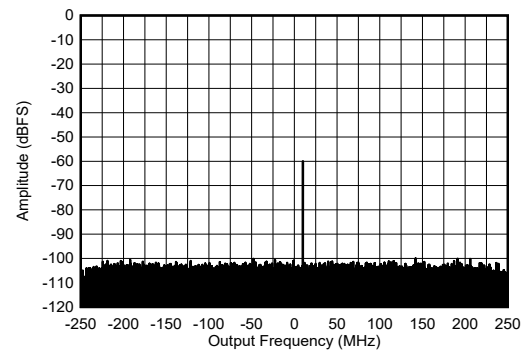
### 6.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with  $f_{\text{CLK}} = 11796.48 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB, 9.6 GHz matching.



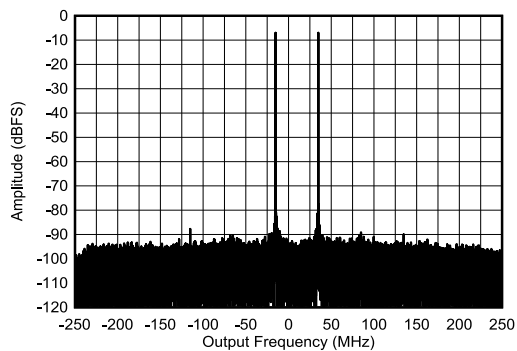
-30 dBFS

Figure 6-462. RX Single Tone Output FFT at 9.61 GHz



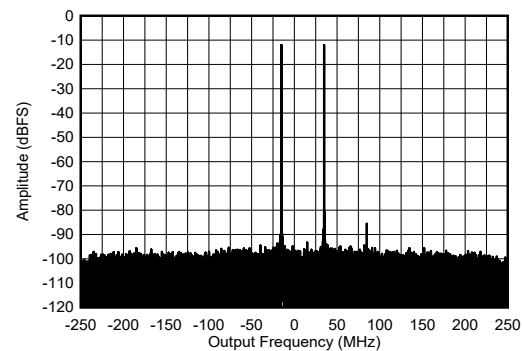
-60 dBFS

Figure 6-463. RX Single Tone Output FFT at 9.61 GHz



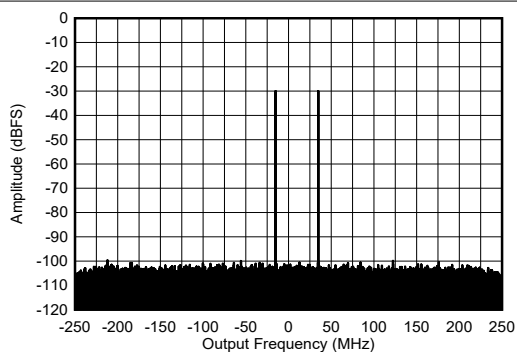
9.585 and 9.635 GHz, -7 dBFS each tone

Figure 6-464. RX Two Tone Output FFT at 9.61 GHz



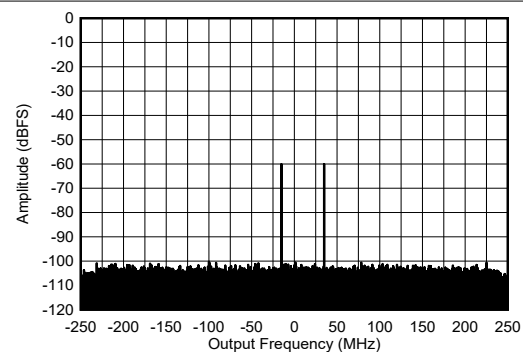
9.585 and 9.635 GHz, -12 dBFS each tone

Figure 6-465. RX Two Tone Output FFT at 9.61 GHz



9.585 and 9.635 GHz, -30 dBFS each tone

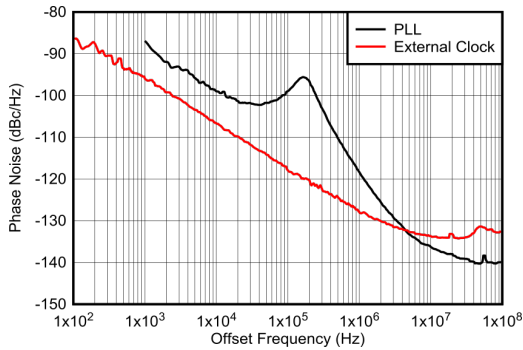
Figure 6-466. RX Two Tone Output FFT at 9.61 GHz



9.585 and 9.635 GHz, -60 dBFS each tone

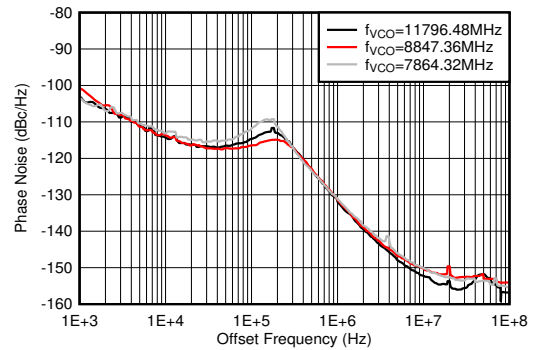
Figure 6-467. RX Two Tone Output FFT at 9.61 GHz

**6.12.15 PLL and Clock Typical Characteristics**



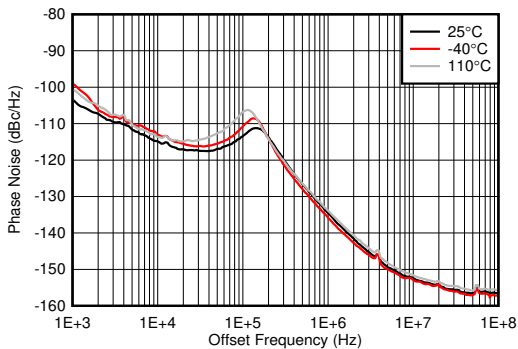
measured at TX output, normalized to 12 GHz by  $20 \times \log_{10}(12\text{GHz}/F_{\text{OUT}})$

**Figure 6-468. Phase Noise vs Offset Frequency for PLL and External Clock at 12 GHz**



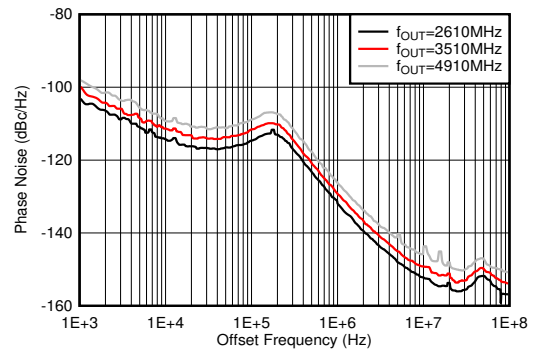
PLL enabled,  $f_{\text{REF}} = 491.52$  MSPS, measured at TX output

**Figure 6-469. Phase Noise vs Offset Frequency and  $f_{\text{VCO}}$  at  $f_{\text{OUT}} = 2610$  MHz**



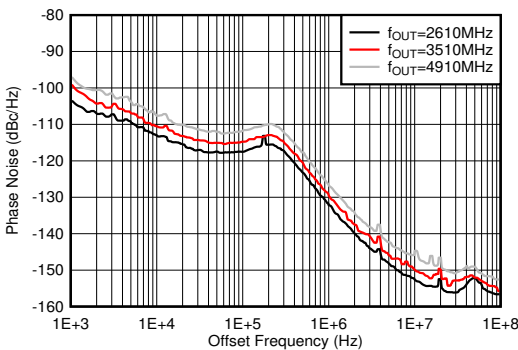
PLL enabled,  $f_{\text{VCO}} = 11796.48$  MHz,  $f_{\text{REF}} = 491.52$  MSPS, measured at TX output

**Figure 6-470. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at  $f_{\text{OUT}} = 1910$  MHz**



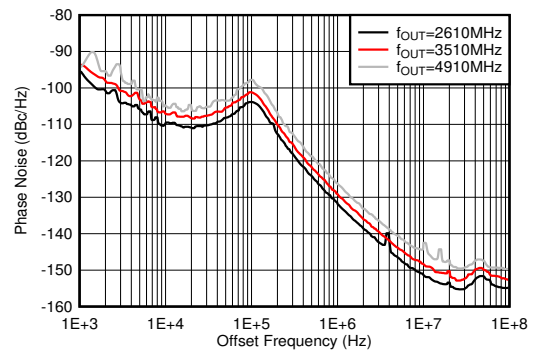
PLL enabled,  $f_{\text{VCO}} = 11796.48$  MHz,  $f_{\text{REF}} = 491.52$  MSPS, measured at TX output

**Figure 6-471. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{\text{OUT}}$  at 25°C**



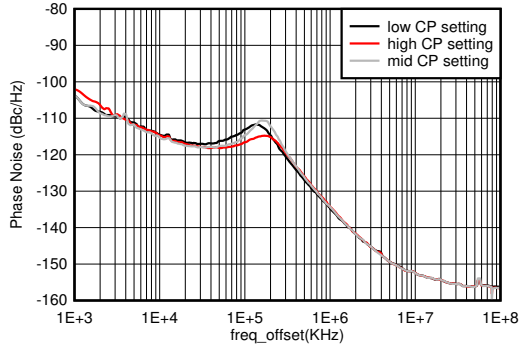
PLL enabled,  $f_{\text{VCO}} = 11796.48$  MHz,  $f_{\text{REF}} = 491.52$  MSPS, measured at TX output

**Figure 6-472. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{\text{OUT}}$  at -40°C**



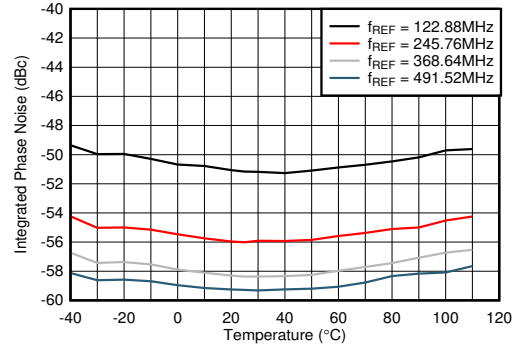
PLL enabled,  $f_{\text{VCO}} = 11796.48$  MHz,  $f_{\text{REF}} = 491.52$  MSPS, measured at TX output

**Figure 6-473. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{\text{OUT}}$  at 110°C**



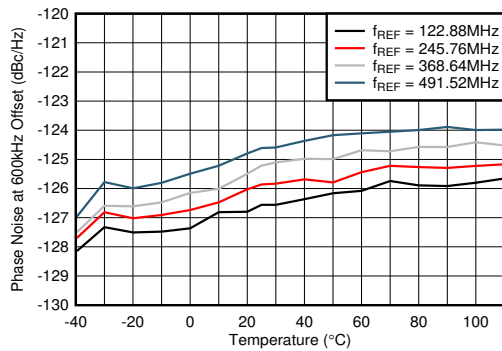
PLL enabled,  $f_{VCO} = 11796.48$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-474. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at  $f_{OUT} = 2.6$  GHz**



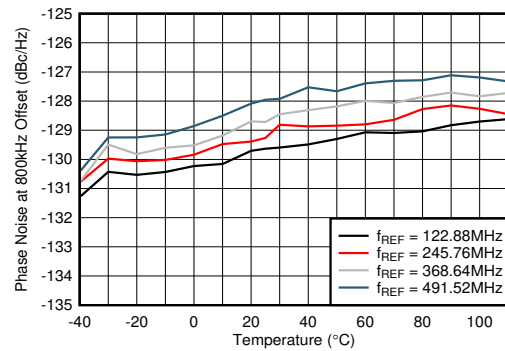
PLL enabled,  $f_{VCO} = 11796.48$  MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at TX output

**Figure 6-475. Integrated Phase Noise for 12-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



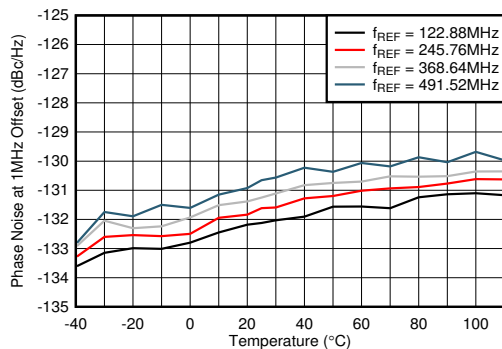
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at TX output

**Figure 6-476. Phase Noise for 12-GHz VCO at 600 kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



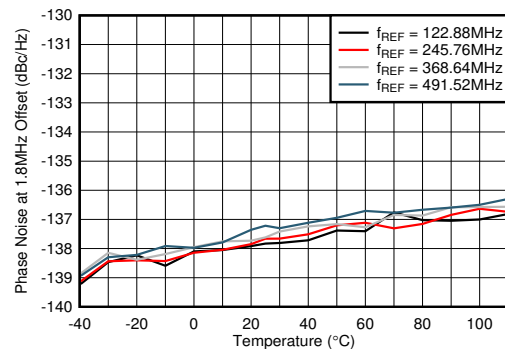
A. PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at TX output

**Figure 6-477. Phase Noise for 12-GHz VCO at 800 kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at TX output

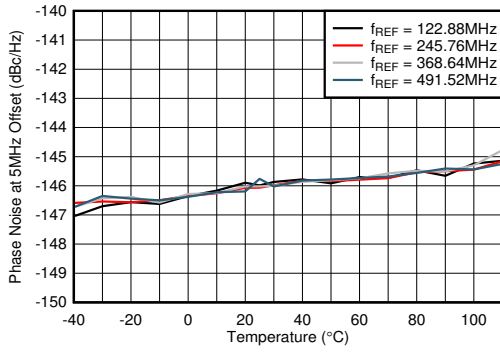
**Figure 6-478. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at TX output

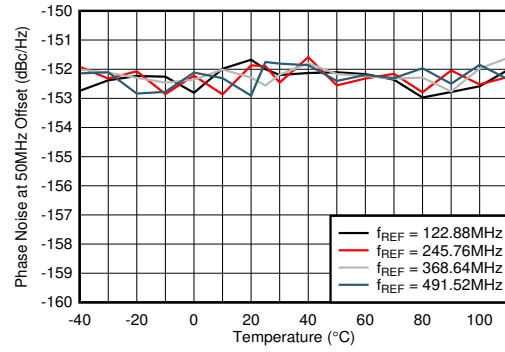
**Figure 6-479. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**





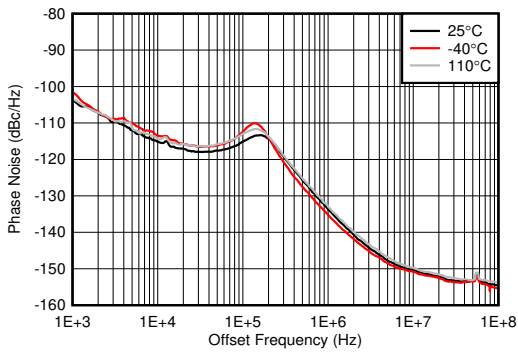
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at TX output

**Figure 6-480. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



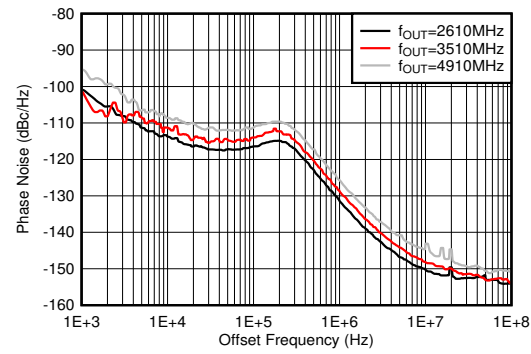
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at TX output

**Figure 6-481. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



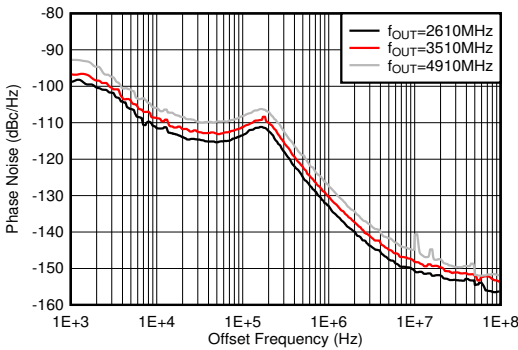
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-482. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**



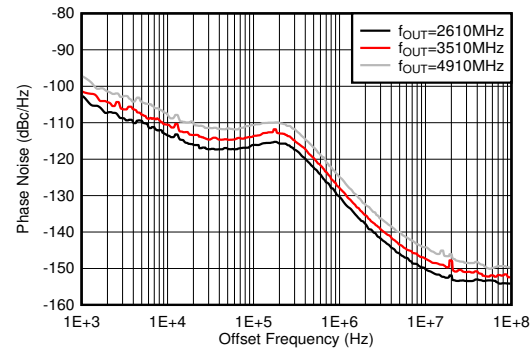
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-483. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 25°C**



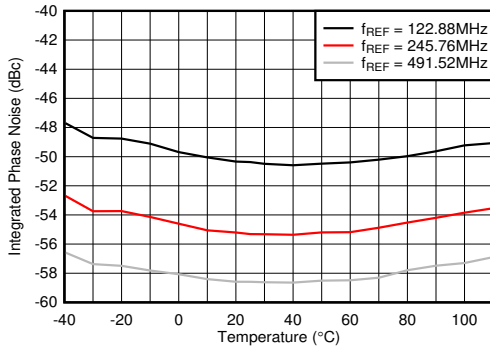
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-484. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at -40°C**



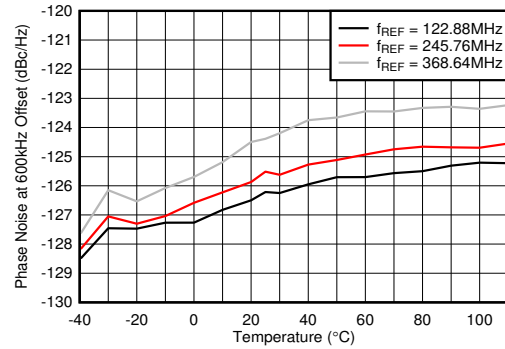
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-485. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 110°C**



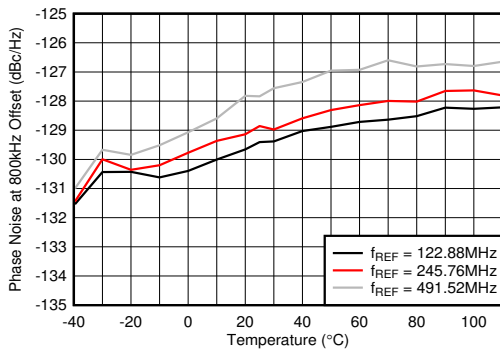
PLL enabled,  $f_{VCO} = 9830.4$  MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at TX output

**Figure 6-486. Integrated Phase Noise for 10-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



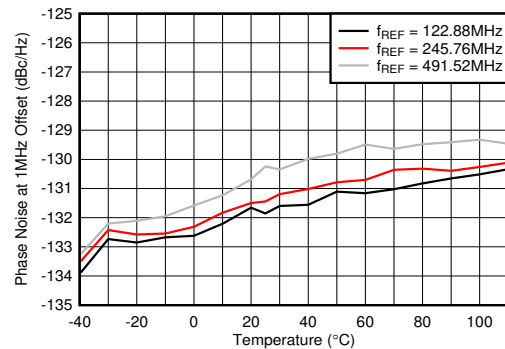
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at TX output

**Figure 6-487. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



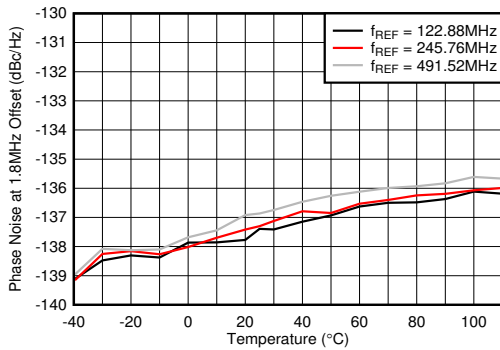
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at TX output

**Figure 6-488. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



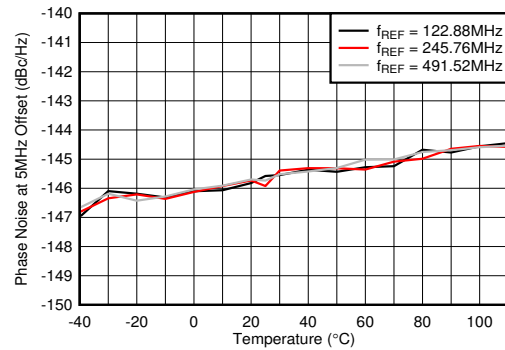
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at TX output

**Figure 6-489. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



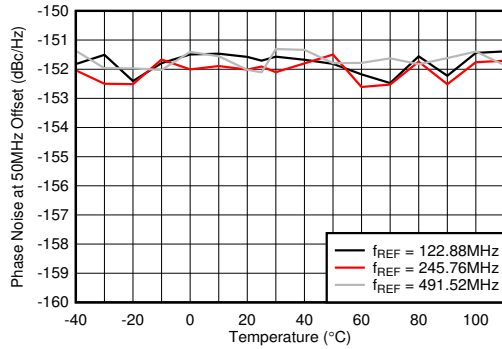
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at TX output

**Figure 6-490. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



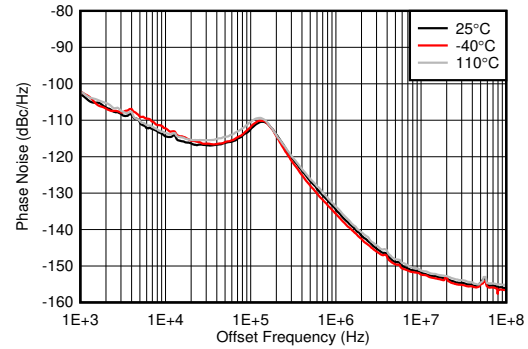
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at TX output

**Figure 6-491. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



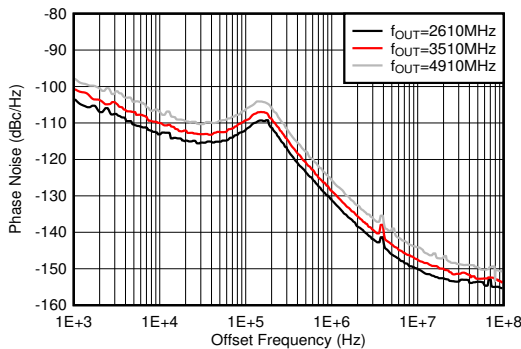
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at TX output

**Figure 6-492. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



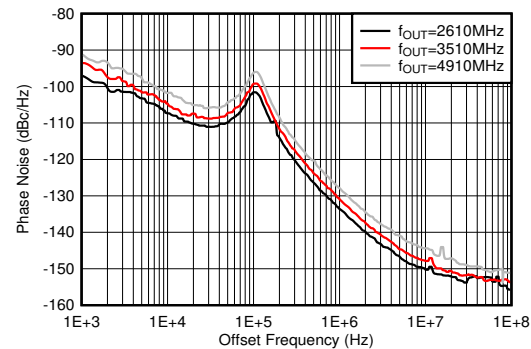
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-493. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**



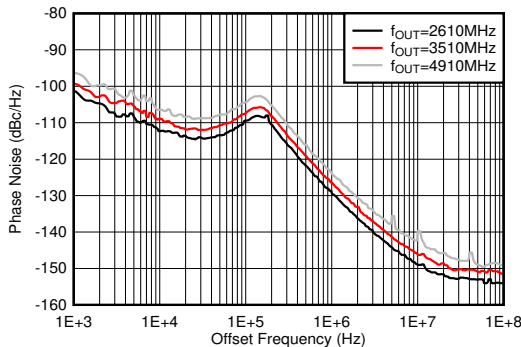
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-494. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 25°C**



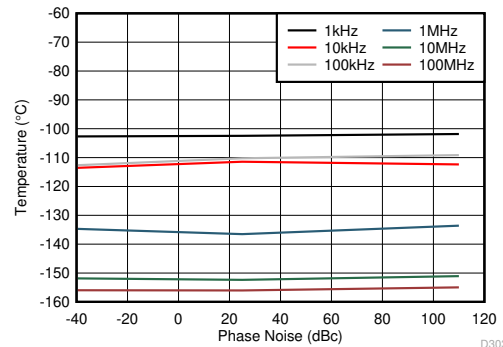
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-495. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at -40°C**



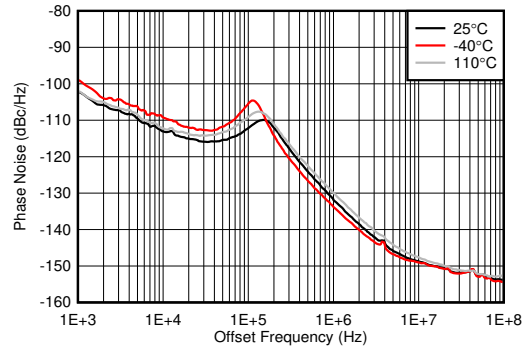
PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-496. Phase Noise for 9-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 110°C**



PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS, minimum LPF BW, measured at TX output

**Figure 6-497. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at  $f_{OUT} = 2.6$  GHz**



PLL enabled,  $f_{VCO} = 7864.32$  MHz,  $f_{REF} = 491.52$  MSPS, measured at TX output

**Figure 6-498. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**

## 7 Device and Documentation Support

### 7.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 7.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 7.3 Trademarks

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### 7.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 7.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7953IABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7953I	<a href="#">Samples</a>
AFE7953IALK	ACTIVE	FCBGA	ALK	400	90	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7953 SNPB	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

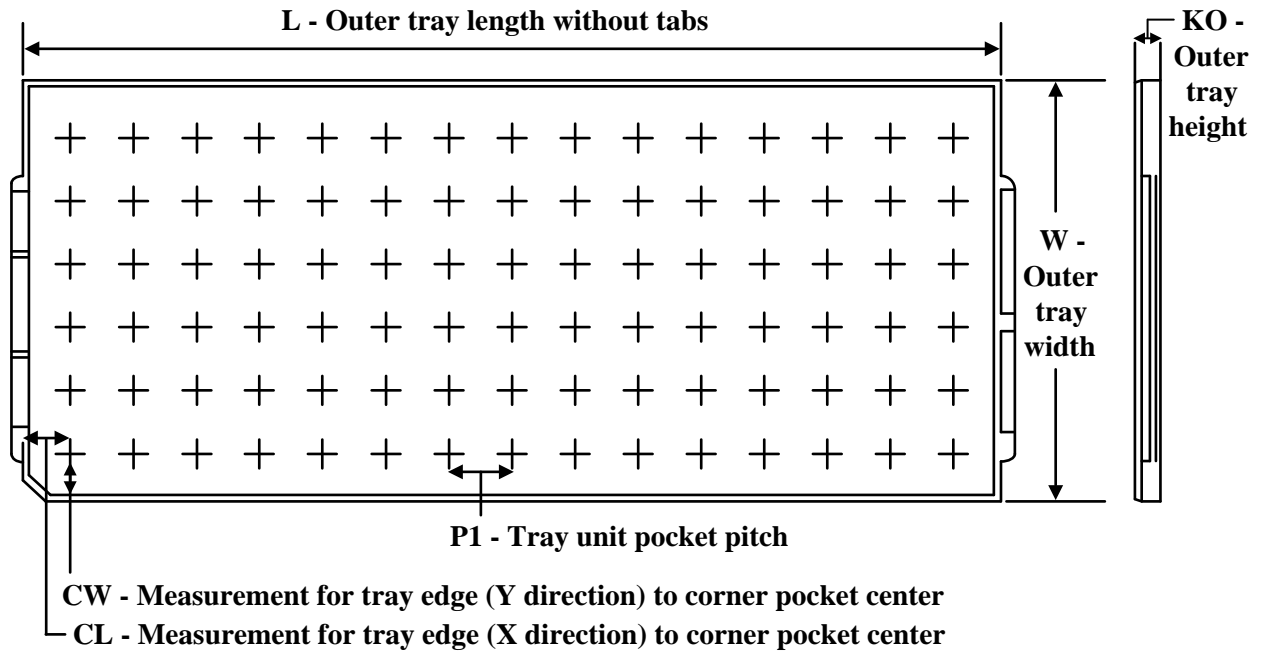
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TRAY**


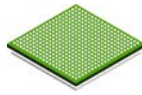
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7953IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7953IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7953IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7953IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2



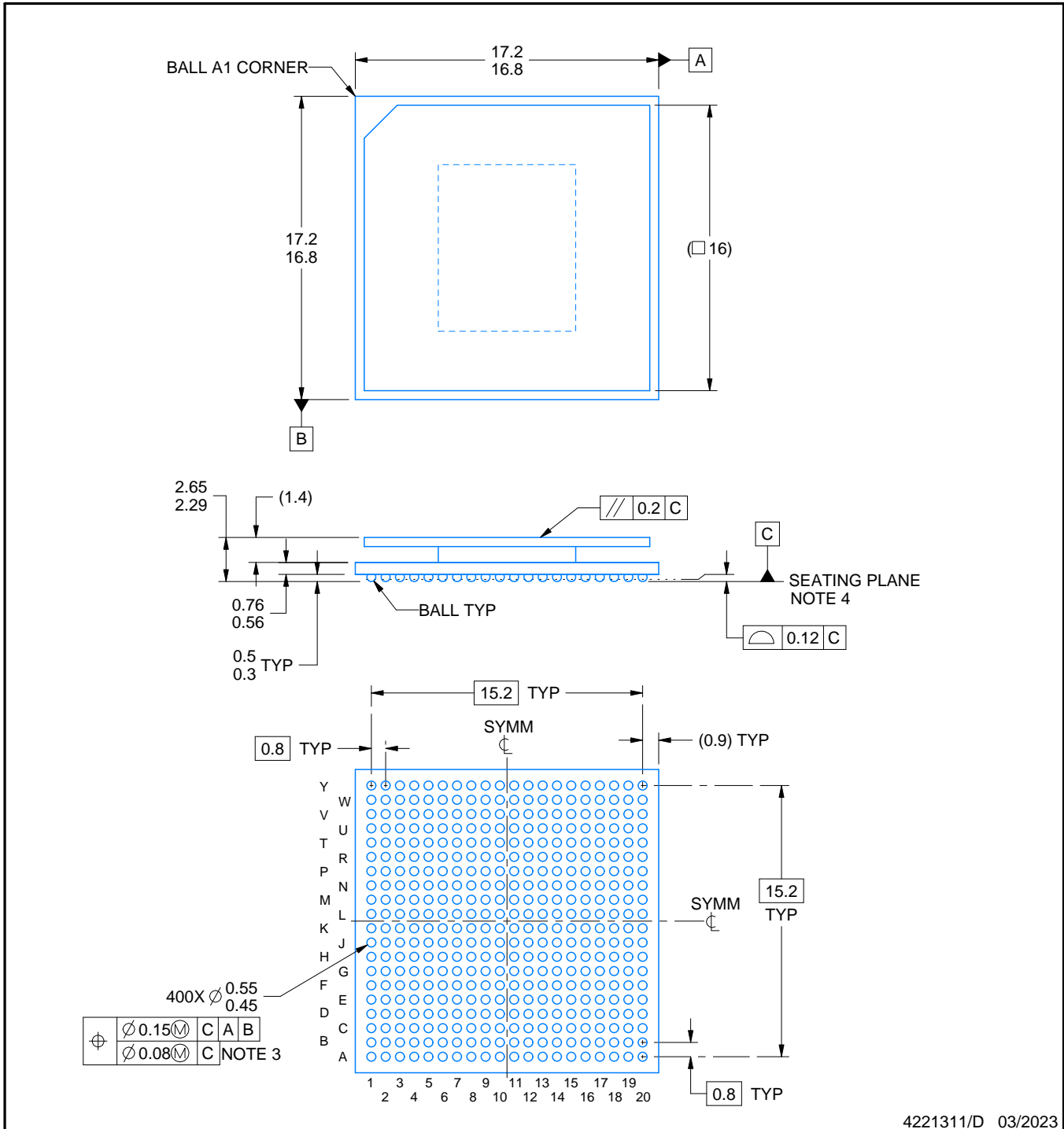
# ABJ0400A



# PACKAGE OUTLINE

FCBGA - 2.65 mm max height

BALL GRID ARRAY



4221311/D 03/2023

## NOTES:

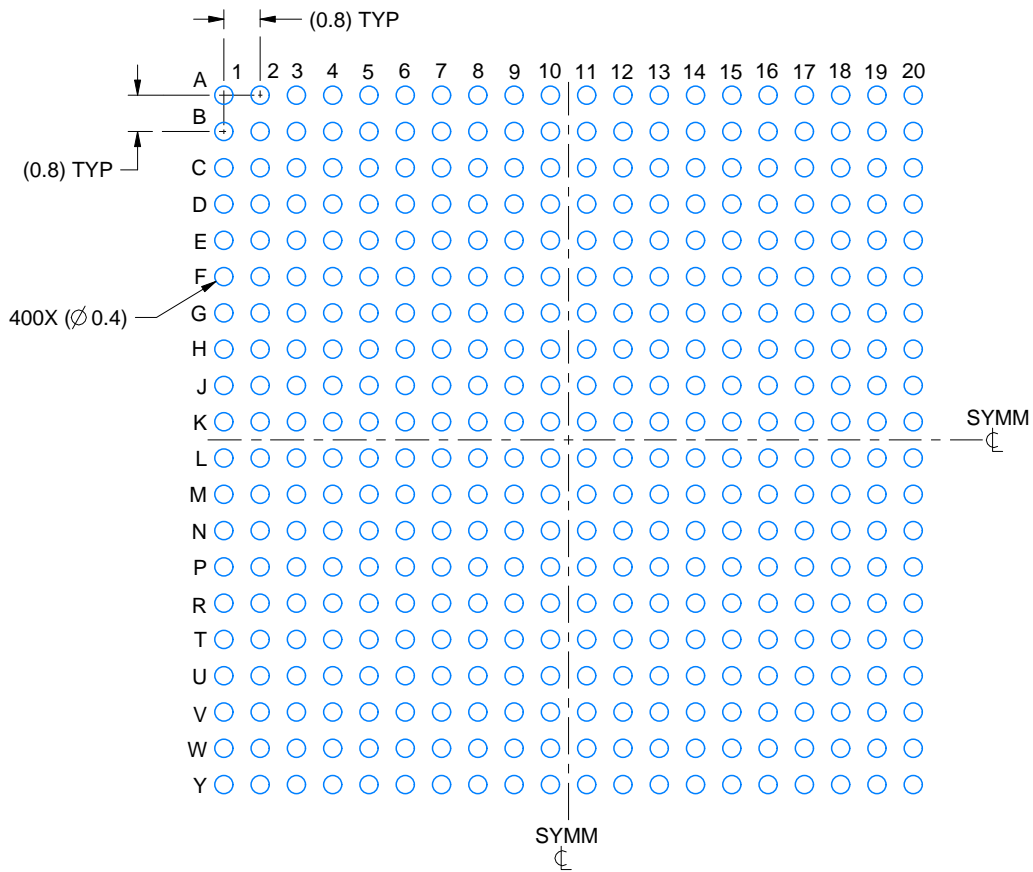
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
- Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
- The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

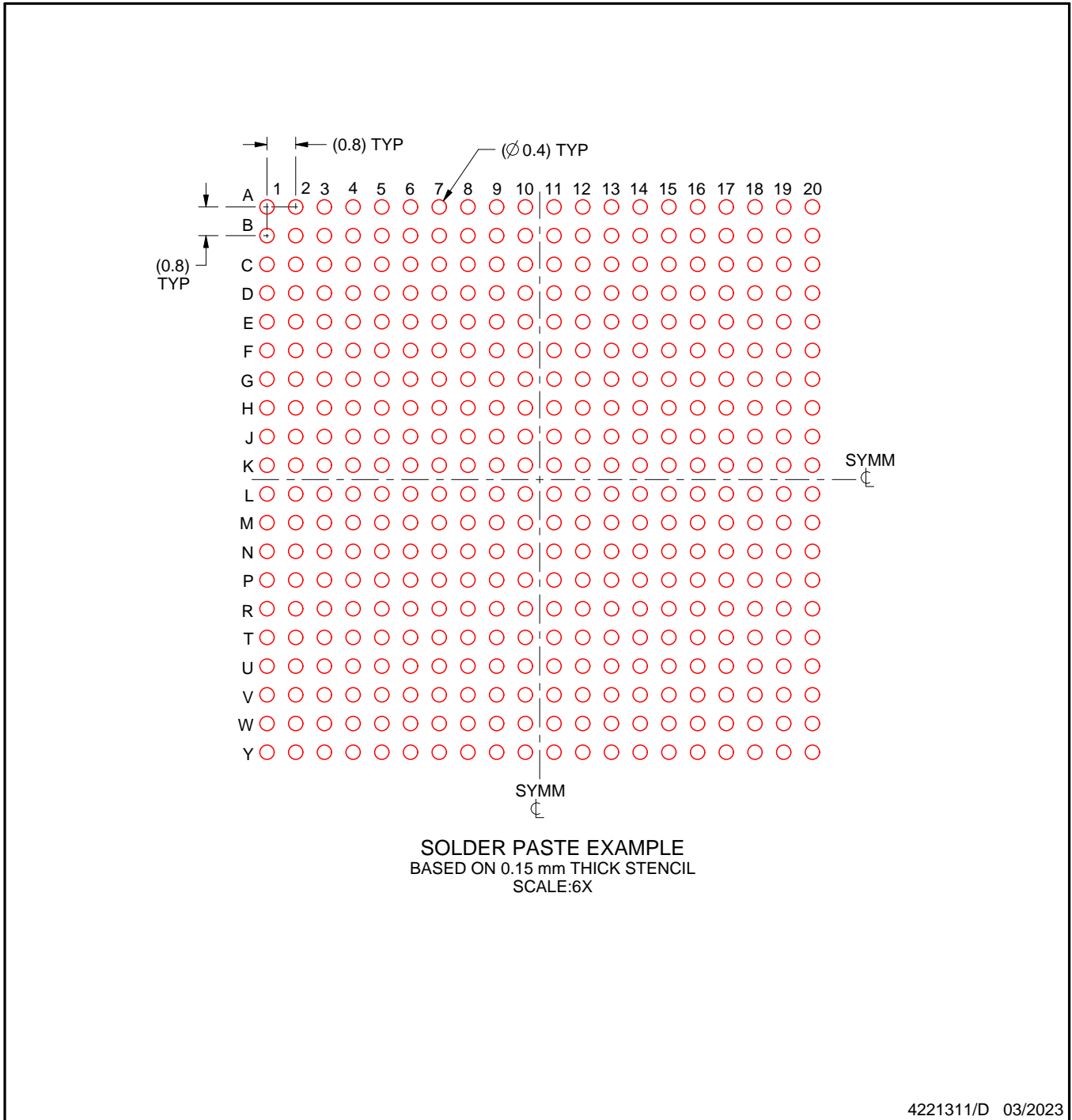
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

## ABJ0400A

## FCBGA - 2.65 mm max height

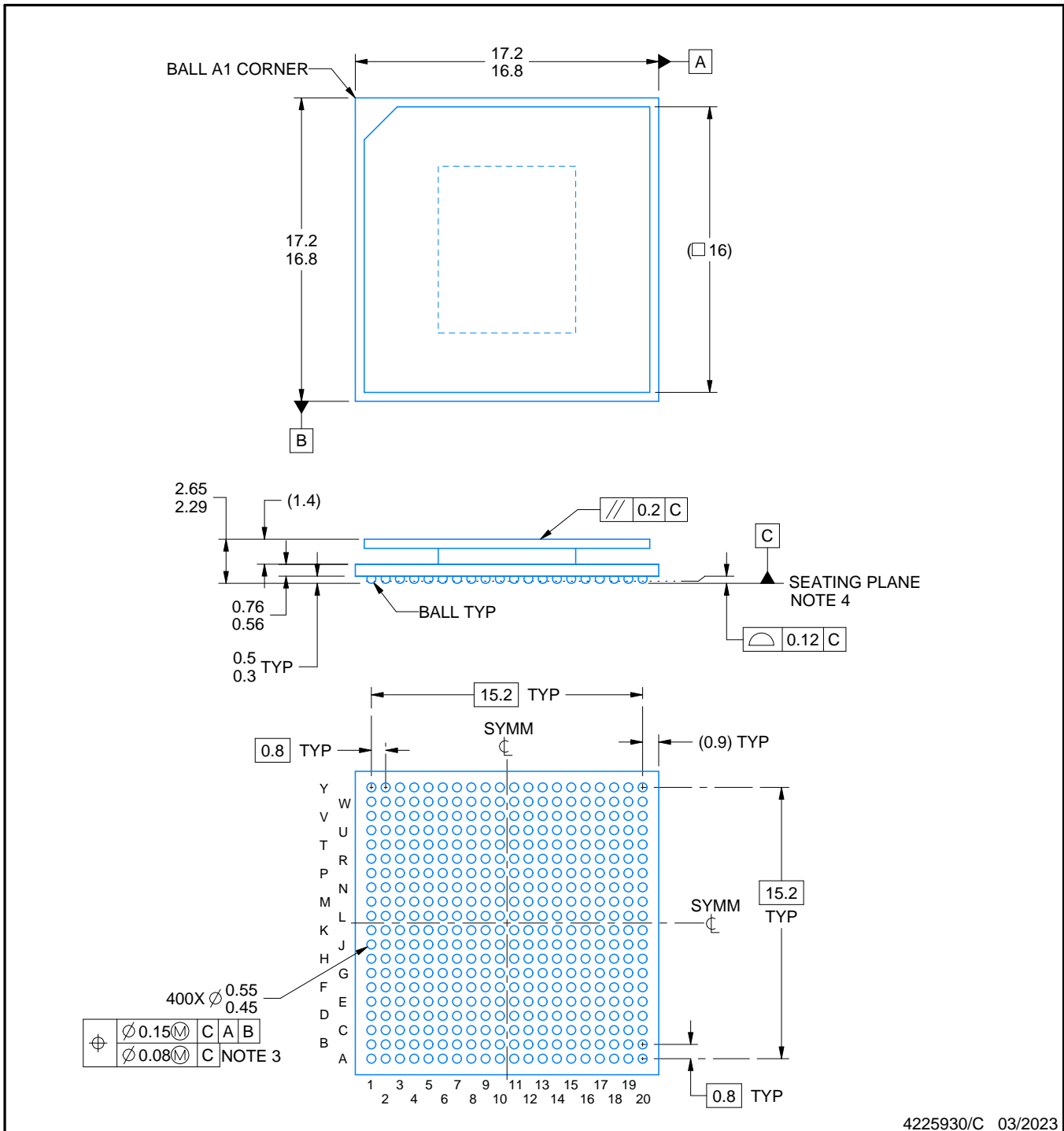
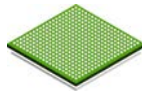
BALL GRID ARRAY



4221311/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



NOTES:

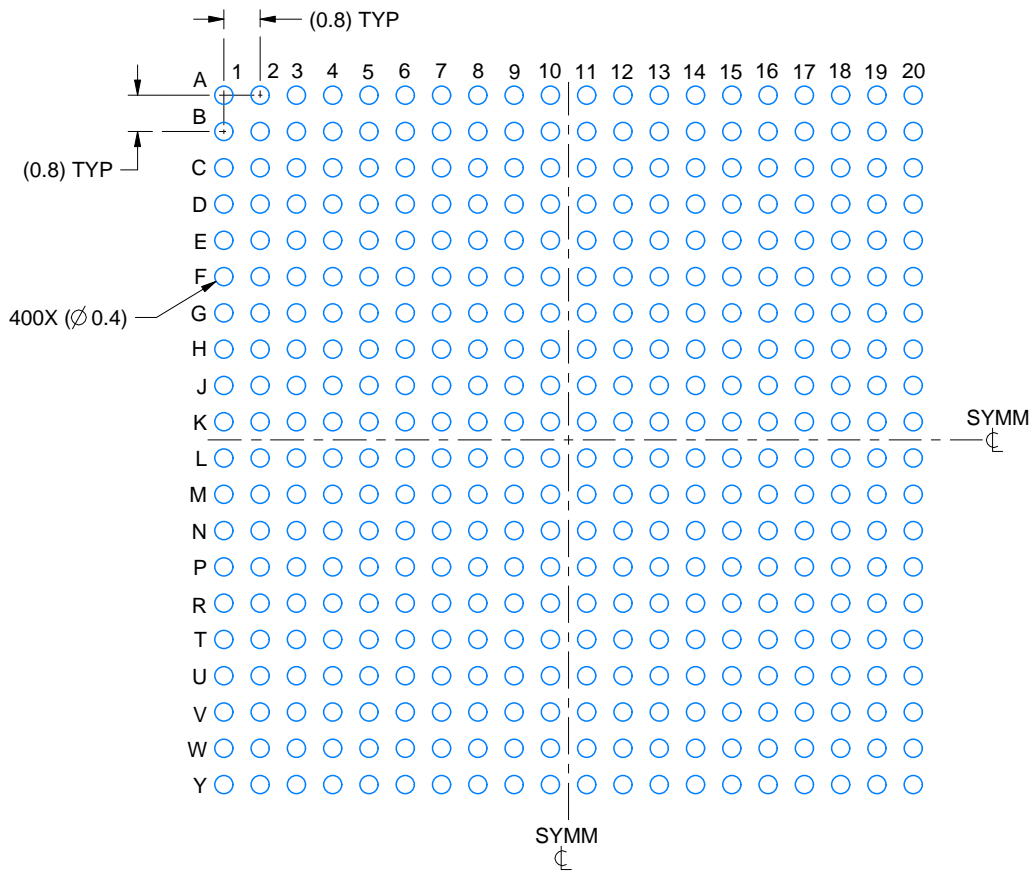
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

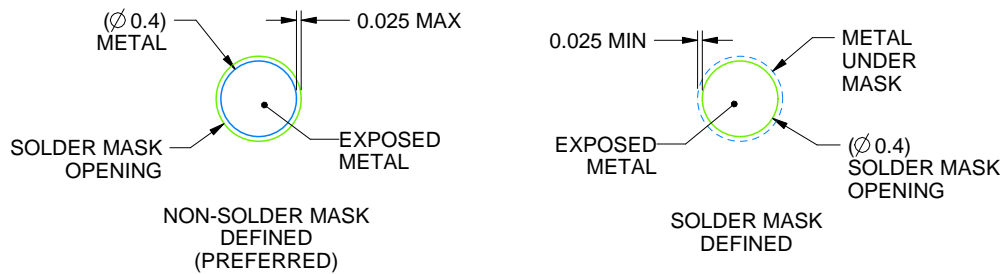
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

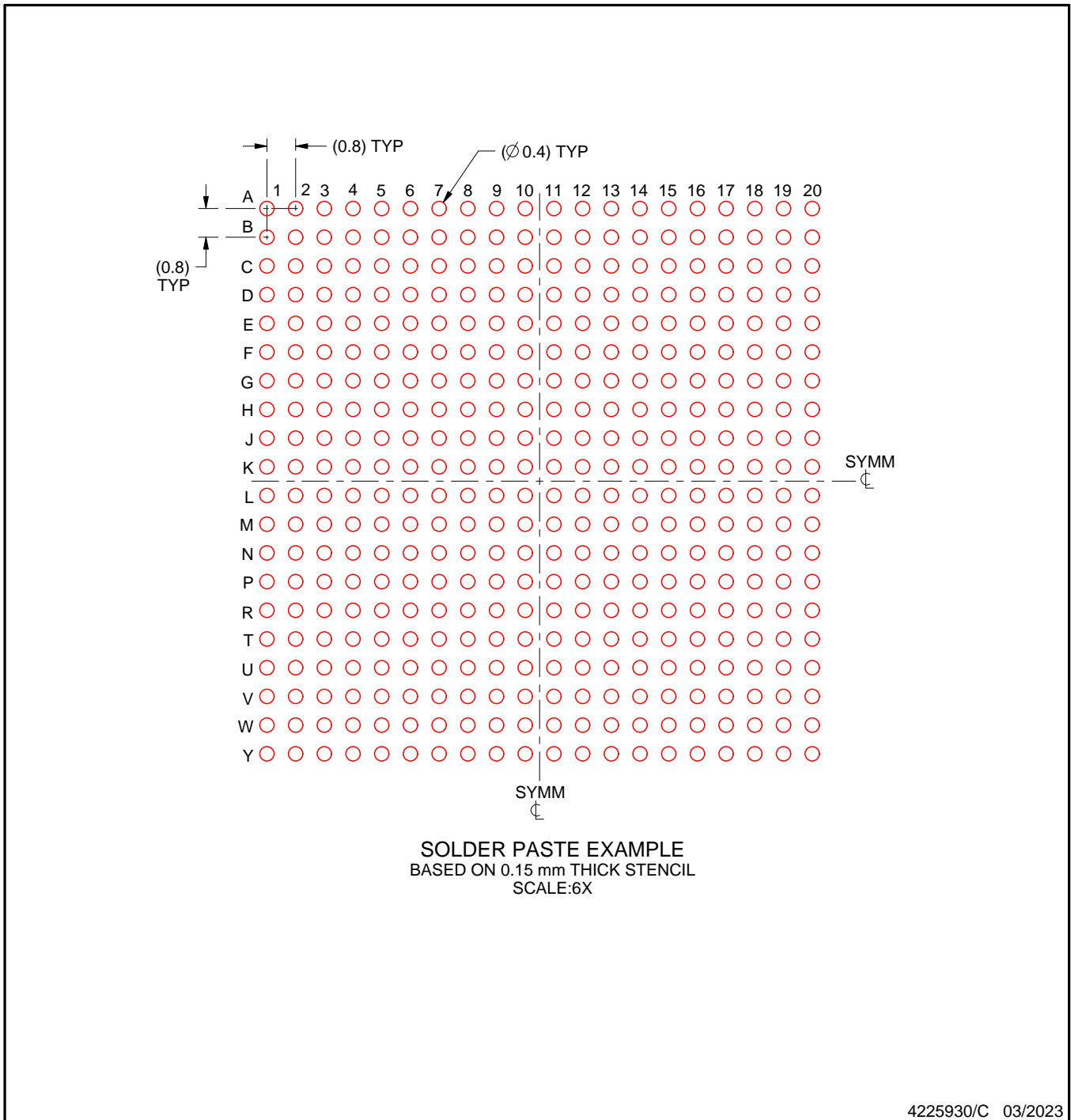
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

## ALK0400A

## FCBGA - 2.65 mm max height

BALL GRID ARRAY



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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