AMC130M03 3-Channel, 64-kSPS, Simultaneous-Sampling, 16-Bit, Reinforced Isolated Delta-Sigma ADC With Integrated DC/DC Converter

1 Features

- Three isolated, simultaneous-sampling ΔΣ ADCs with differential inputs
- Single-supply operation (3.3 V or 5 V) with integrated DC/DC converter
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Programmable data rate up to 64 kSPS
- Programmable gain up to 128
- Low-drift internal voltage reference
- Internal temperature sensor
- 4-wire SPI interface with cyclic redundancy check (CRC)
- Safety-related certifications:
  - 7070-V_{PEAK} reinforced isolation per DIN EN IEC 60747-17 (VDE 0884-17)
  - 5000-V_{RMS} isolation for 1 minute per UL1577
- Package: 20-pin, wide-body SOIC
- Operating temperature range: –40°C to +125°C

2 Applications

- Electricity meters: Commercial and residential
- Circuit breakers
- EV charging stations
- Battery management systems

3 Description

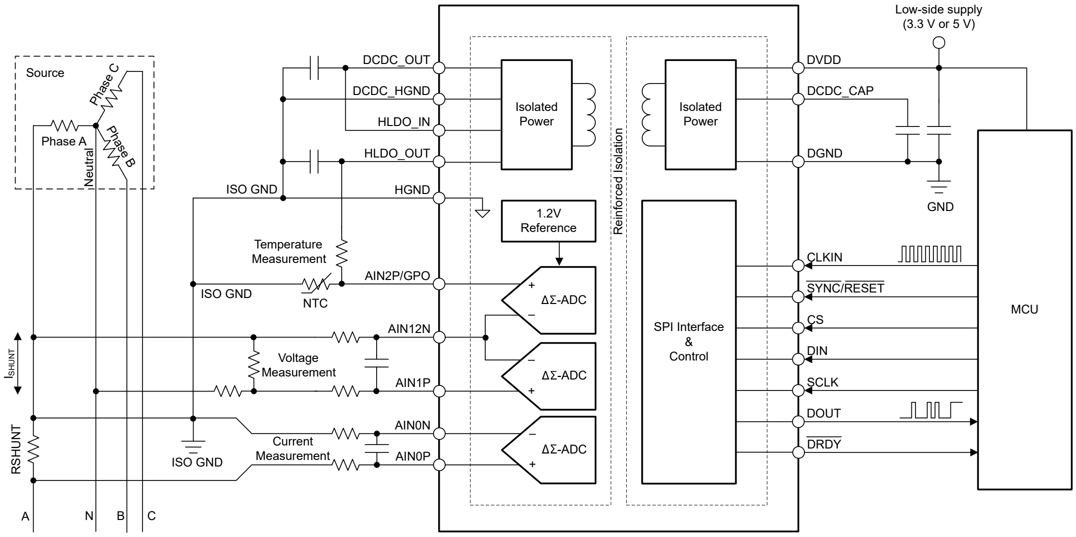
The AMC130M03 is a precision three-channel, data- and power-isolated, simultaneous-sampling, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The AMC130M03 offers wide dynamic range, low power, and energy-measurement-specific features, making the device designed for energy metering and power metrology applications. The ADC inputs can be directly interfaced to a resistor-divider network or a shunt-current sensor because of the device high input impedance.

The AMC130M03 features a fully integrated isolated DC/DC converter that allows single-supply operation from the low-side of the device. The reinforced capacitive isolation barrier is certified according to VDE V 0884-17 and UL1577. This isolation barrier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage, making the AMC130M03 an excellent choice for polyphase energy metering applications using shunt current sensors.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AMC130M03	DFM (SOIC, 20)	12.8 mm × 10.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application of the AMC130M03 in Energy Metering

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 1, 2023 to September 11, 2023 (from Revision * (May 2023) to Revision A (September 2023)) **Page**

- Changed device status from *Advance Information* to *Production Data* 1

5 Pin Configuration and Functions

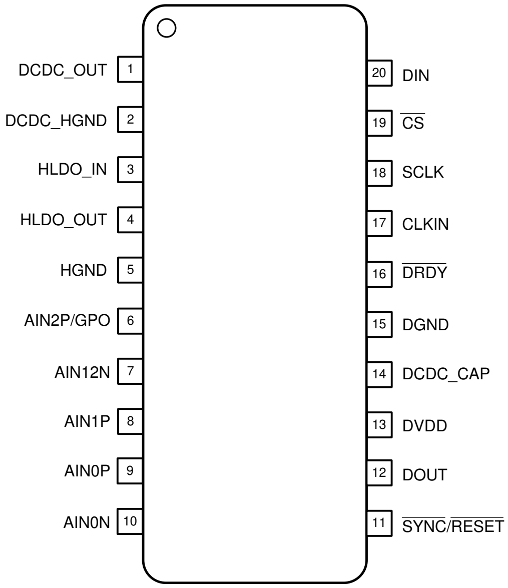


Figure 5-1. DFM Package, 20-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION(1)
NO.	NAME		
1	DCDC_OUT	Supply	High-side output of the DC/DC converter. Connect this pin to the HLDO_IN pin.(2)
2	DCDC_HGND	Supply	High-side ground reference for the DC/DC converter. Connect this pin to the HGND pin.(2)
3	HLDO_IN	Supply	Input of the high-side low-dropout (LDO) regulator. Connect this pin to the DCDC_OUT pin.(2)
4	HLDO_OUT	Supply	Output of the high-side LDO.(2)
5	HGND	Supply	High-side analog signal ground. Connect this pin to the DCDC_HGND pin.
6	AIN2P/GPO	Analog input	Positive analog input 2, or general-purpose output.
7	AIN12N	Analog input	Negative analog input 1 and 2.
8	AIN1P	Analog input	Positive analog input 1.
9	AIN0P(3)	Analog input	Positive analog input 0.
10	AIN0N(3)	Analog input	Negative analog input 0.
11	$\overline{\text{SYNC}}/\overline{\text{RESET}}$	Digital input	Conversion synchronization or system reset; active low.
12	DOUT	Digital output	Serial data output.
13	DVDD	Supply	Low-side analog and digital power supply.(2)
14	DCDC_CAP	Supply	Low-side input of the DC/DC converter, internally connected to the output of the primary-side LDO.(2)
15	DGND	Supply	Low-side analog and digital ground.(2)
16	$\overline{\text{DRDY}}$	Digital output	Data ready; active low.
17	CLKIN	Digital input	Main clock input.
18	SCLK	Digital input	Serial data clock.
19	$\overline{\text{CS}}$	Digital input	Chip select; active low.
20	DIN	Digital input	Serial data input.

(1) See the *Unused Inputs and Outputs* section for details on how to connect unused pins.
(2) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(3) Use AIN0P and AIN0N for the measurement with the most stringent precision requirements.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	DVDD to DGND	–0.3	6.5	V
	DCDC_CAP to DGND	–0.3	3.5	
Analog input voltage	AINxP, AINxN	HGND – 1.6	HGND + 2.7	V
Digital input voltage	$\overline{\text{CS}}$, CLKIN, DIN, SCLK, $\overline{\text{SYNC}}/\overline{\text{RESET}}$	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, all pins except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
V_{DVDD}	Low-side power supply	DVDD to GND	3	3.3	5.5	V
ANALOG INPUTS						
V_{AINxP}, V_{AINxN}	Absolute input voltage (1)	Gain = 1, 2, or 4	HGND – 1.3		HGND + 2.7	V
		Gain = 8, 16, 32, 64, or 128	HGND – 1.3		HGND + 0.9	
V_{IN}	Differential input voltage	$V_{IN} = V_{AINxP} – V_{AINxN}$	$–V_{REF}$ / Gain		V_{REF} / Gain	V
EXTERNAL CLOCK SOURCE						
N_{DIV}	Clock divider ratio	Signal at CLKIN is divided by N_{DIV} to generate modulator clock	2		12	
f_{CLKIN}	External clock frequency at CLKIN pin	High-resolution mode	$1.4 \cdot N_{DIV}$	$4.096 \cdot N_{DIV}$	$4.1 \cdot N_{DIV}$	MHz
		Low-power mode	$1.4 \cdot N_{DIV}$	$2.048 \cdot N_{DIV}$	$2.05 \cdot N_{DIV}$	
	Duty cycle		40%	50%	60%	
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) The subscript "x" signifies the channel. For example, the positive analog input to channel 0 is named AIN0P. See the *Pin Configuration and Functions* section for the pin names.

6.4 Thermal Information

THERMAL METRIC(1)		DFM (SOIC)	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	17.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	50.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.0	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.0	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive peak isolation voltage(2)	At AC voltage	1700	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage(2)	At AC voltage (sine wave)	1200	V_{RMS}
		At DC voltage	1700	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	7070	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (4)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
		Method b2, at routine test (100% production)(7), $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, t_{ini} = t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5 V_{PP} at 1 MHz	~4.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500 V at T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This device is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

6.6 Safety-Related Certifications

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs.
Reinforced insulation	Single protection
Certificate number: Pending	File number: E181974

6.7 Safety Limiting Values

Safety limiting (1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure ofthe I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheatthe die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 73.5°C/W, DVDD = 5.5 V, T_J = 150°C, T_A = 25°C			309	mA
		$R_{\theta JA}$ = 73.5°C/W, DVDD = 3.3 V, T_J = 150°C, T_A = 25°C			472	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 73.5°C/W, T_J = 150°C, T_A = 25°C			1700	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$ is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum low-side voltage.

6.8 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C and DVDD = 3.0 V to 5.5V; typical specifications are at T_A = 25°C, DVDD = 3.3 V, and for channel 0; all specifications are at f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, high-resolution mode, all channels enabled, global-chop mode disabled, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
I_{IB}	Input bias current	AINxP = AINxN = HGND; I_{IB} = (I_{IBP} + I_{IBN}) / 2, Gain = 1, 2, or 4		0.65	0.9	µA
		AINxP = AINxN = HGND; I_{IB} = (I_{IBP} + I_{IBN}) / 2, Gain = 8 to 128	–1.0	–0.65		
TCI_{IB}	Input bias current drift		–1	±0.35	1 (3)	nA/°C
I_{IO}	Input offset current	I_{IO} = I_{IBP} – I_{IBN}		±15		nA
R_{IN}	Single-ended input impedance	AINxN = HGND, gain = 1, 2, or 4		250		kΩ
		AINxN = HGND, gain = 8 to 128		0.5		MΩ
Z_{IND}	Differential input impedance	(AINxN + AINxP) / 2 = HGND, Gain = 1, 2, or 4		275		kΩ
		(AINxN + AINxP) / 2 = HGND, Gain = 8 to 128		1		MΩ
ADC CHARACTERISTICS						
	Resolution		16			Bits
	Gain settings		1, 2, 4, 8, 16, 32, 64, 128			
f_{DATA}	Data rate	High-resolution mode, f_{CLKIN} = 8.192 MHz, N_{DIV} = 2	250		64k	SPS
		Low-power mode, f_{CLKIN} = 4.096 MHz, N_{DIV} = 2	125		32k	
	SPI start-up time	Measured from supplies at 90% to SPI interface ready to accept data		0.3		ms
	Converter start-up time	Measured from DCDC enable bit set to first $\overline{DRDY}$ falling edge with data settled to 0.1% (CLKIN running)		1.0		ms
ADC PERFORMANCE						
INL	Integral nonlinearity	End-point fit		6		ppm of FSR
E_O	Offset error (input referred)	Channel 0,1, external short, T_A = 25°C	–100	±100	330	µV
		Channel 2, external short, T_A = 25°C	–100	±125	330	
		Global-chop mode, channel 0, 1, default global-chop delay, external short, T_A = 25°C (2)	–100	6	100	
		Global-chop mode, channel 2, default global-chop delay, external short, T_A = 25°C (2)	–120	42	120	
TCE_O	Offset error drift vs temperature	Channel 0, 1, external short	–0.5	±0.1	0.5 (3)	µV/°C
		Channel 2, external short	–0.5	±0.2	0.5 (3)	
		Global-chop mode channel 0, 1, external short	–0.3	±0.1	0.3 (3)	
		Global-chop mode channel 2, external short	–0.3	±0.1	0.3 (3)	
E_G	Gain error	Channel 0, T_A = 25°C, end-point fit	–0.2	±0.025	0.2	%
		Channel 1, 2, T_A = 25°C, end-point fit	–1	±0.1	1	
TCE_G	Gain error drift vs temperature	Including internal reference error		8	25 (3)	ppm/°C

6.8 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C and DVDD = 3.0 V to 5.5V; typical specifications are at T_A = 25°C, DVDD = 3.3 V, and for channel 0; all specifications are at f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, high-resolution mode, all channels enabled, global-chop mode disabled, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \leq V_{IN} \leq V_{CM\ max}$		110		dB
		f_{IN} = 50 Hz or 60 Hz, $V_{CM\ min} \leq V_{IN} \leq V_{CM\ max}$, $V_{AINP} = V_{AINN}$		110		
E_N	Input-referred noise			10		μV_{RMS}
	Crosstalk	From one channel to any one of the other channels; f_{IN} = 50 Hz or 60 Hz at AINxP while AINxN = HGND		–120		dB
THD	Total harmonic distortion	f_{IN} = 50 Hz or 60 Hz (up to 5 harmonics), V_{IN} = –0.5 dBFS		–102	–94 (3)	dB
SFDR	Spurious-free dynamic range	f_{IN} = 50 Hz or 60 Hz, V_{IN} = –0.5 dBFS		105		dB
CMTI	Common-mode transient immunity		100	150		V/ns
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Internal reference voltage			1.2		V
TEMPERATURE SENSOR						
	Voltage	Internal temperature sensor, T_A = 25°C, gain = 8		80.5		mV
	Temperature coefficient	Internal temperature sensor, T_A = 25°C, gain = 8		265		µV/°C
	Temperature measurement error	Internal temperature sensor, T_A = 25°C, gain = 8		±3		°C
		Internal temperature sensor, across temperature, gain = 8		±5		
	Input impedance	External temperature sensor, T_A = 25°C, gain = 1, 2, or 4		8		MΩ
TUE	Total unadjusted error (4)	External temperature sensor, T_A = 25°C, gain = 1		0.3		% FSR
DIGITAL INPUTS/OUTPUTS						
V_{IL}	Logic input level, low		DGND		0.2 DVDD	V
V_{IH}	Logic input level, high		0.8 DVDD		DVDD	V
V_{OL}	Logic output level, low	I_{OL} = –1 mA			0.2 DVDD	V
V_{OH}	Logic output level, high	I_{OH} = 1 mA	0.8 DVDD			V
I_{IN}	Input current	DGND < $V_{Digital\ Input}$ < DVDD	–1		1	µA
C_{IN}	Input capacitance			1		pF
C_{LOAD}	Output load capacitance			15	30	pF
HIGH-SIDE DIGITAL OUTPUT						
R_{GPO}	High-side GPO output impedance	Driving 0		100		Ω
		Driving 1		115		
I_{GPO}	High-side GPO load current				1	mA
POWER SUPPLY						
I_{DVDD}	Low-side supply current(1)	High-resolution mode		19.5	24	mA
		Low-power mode, f_{CLKIN} = 4.096 MHz		16	21	
		Standby mode, all channels disabled, no clock applied		160	210	µA

6.8 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C and DVDD = 3.0 V to 5.5V; typical specifications are at T_A = 25°C, DVDD = 3.3 V, and for channel 0; all specifications are at f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS, high-resolution mode, all channels enabled, global-chop mode disabled, and gain = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Power dissipation	High-resolution mode		64		mW
		Low-power mode, f_{CLKIN} = 4.096 MHz		53		
		Standby mode, all channels disabled, no clock applied		525		µW
V_{DCDC_OUT}	DC/DC output voltage	DCDC_OUT to HGND, all channels enabled, T_A = 25°C		3.0		V
V_{HLDO_OUT}	High-side LDO output voltage	HLDO_OUT to HGND, no external load, any channel enabled	2.6	2.9	3.2	V
		HLDO_OUT to HGND, 1-mA external load on HLDO_OUT,any channel enabled	2.4	2.8	3.1	
I_H	High-side supply current for auxiliary circuitry	Load connected from HLDO_OUT to HGND			1	mA

(1) Currents measured with SPI idle.
(2) See global-chop mode section for details.
(3) Specified by design and characterization, not production tested.
(4) Total unadjusted error (TUE) includes gain error, offset error and INL. Typically, gain error dominates the TUE.

6.9 Timing Requirements

over operating ambient temperature range, DOUT load: 20 pF || 100 kΩ (unless otherwise noted)

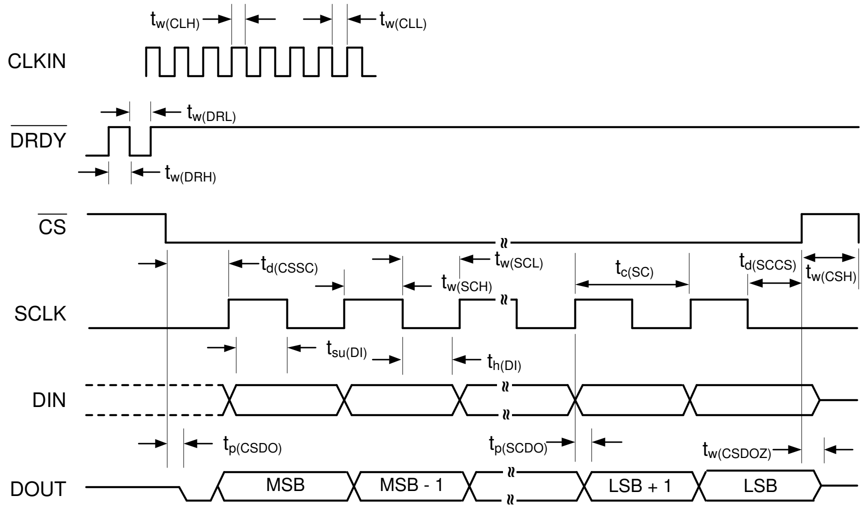
		MIN	MAX	UNIT
3.0 V ≤ DVDD ≤ 5.5 V				
$t_{w(CLL)}$	Pulse duration, CLKIN low	49		ns
$t_{w(CLH)}$	Pulse duration, CLKIN high	49		ns
$t_{c(SC)}$	SCLK period	40		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	20		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	20		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{\text{CS}}$ falling edge	16		ns
$t_{d(SCCS)}$	Delay time, $\overline{\text{CS}}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{\text{CS}}$ high	15		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling egde	5		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	8		ns
$t_{w(SYL)}$	Pulse duration, $\overline{\text{SYNC/RESET}}$ low for synchronization	1	2047	t_{CLKIN}
$t_{w(RSL)}$	Pulse duration, $\overline{\text{SYNC/RESET}}$ low to generate device reset	2048		t_{CLKIN}
$t_{su(SY)}$	Setup time, $\overline{\text{SYNC/RESET}}$ valid before CLKIN falling edge	10		ns

6.10 Switching Characteristics

over operating ambient temperature range, DOUT load: 20 pF || 100 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
3.0 V ≤ DVDD ≤ 5.5 V						
$t_{p(CSDO)}$	Propagation delay time, $\overline{\text{CS}}$ falling edge to DOUT driven				50	ns
$t_{p(SCDO)}$	Progapation delay time, SCLK rising edge to valid new DOUT				20	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{\text{CS}}$ rising edge to DOUT high impedance				75	ns
$t_{w(DRH)}$	Pulse duration, $\overline{\text{DRDY}}$ high			4		t_{CLKIN}
$t_{w(DRL)}$	Pulse duration, $\overline{\text{DRDY}}$ low			4		t_{CLKIN}
t_{POR}	Power-on-reset time	Measured from supplies at 90%		250		µs
	SPI timeout		32768			t_{CLKIN}
t_{REGACQ}	Register default acquisition time			5		µs

6.11 Timing Diagrams



SPI settings are CPOL = 0 and CPHA = 1. $\overline{\text{CS}}$ transitions must take place when SCLK is low.

Figure 6-1. SPI Timing Diagram

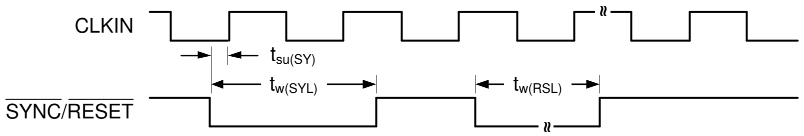


Figure 6-2. $\overline{\text{SYNC}}/\overline{\text{RESET}}$ Timing Requirements

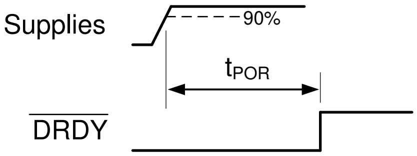


Figure 6-3. Power-On-Reset Timing

6.12 Typical Characteristics

for channel 0 at T_A = 25°C, DVDD = 3.3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS (OSR = 1024 and clock divider N_{DIV} = 2), high-resolution mode, with all channels enabled, global-chop mode disabled, and gain = 1 (unless otherwise noted)

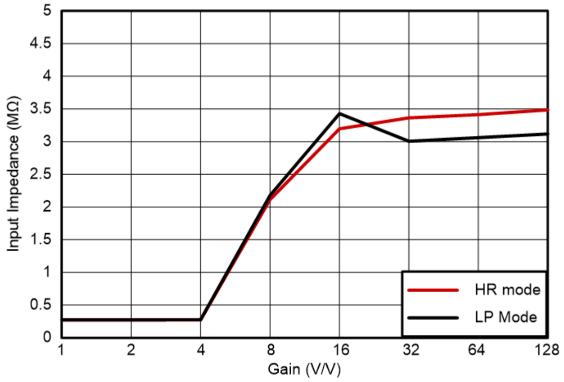


Figure 6-4. Input Impedance vs Gain

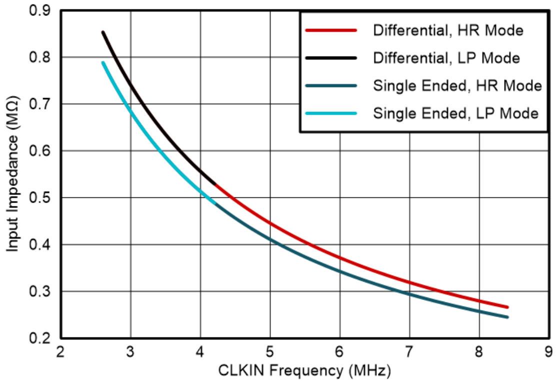


Figure 6-5. Input Impedance vs CLKIN Frequency

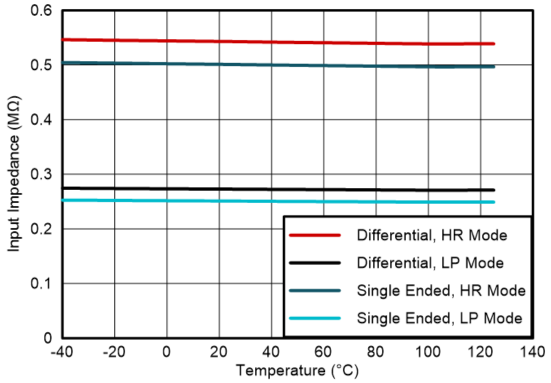


Figure 6-6. Input Impedance vs Temperature

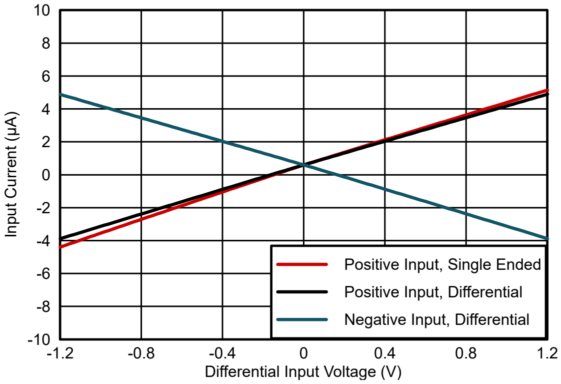


Figure 6-7. Input Current vs Differential Input Voltage

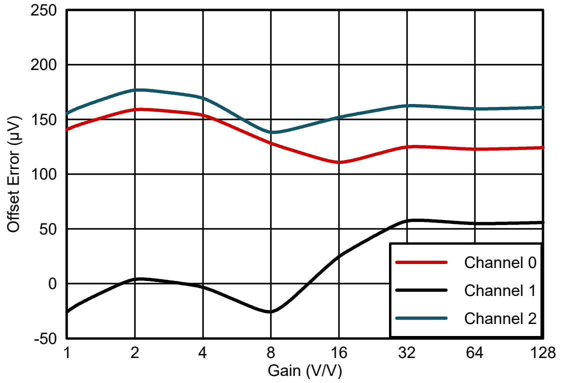


Figure 6-8. Offset Error vs Gain

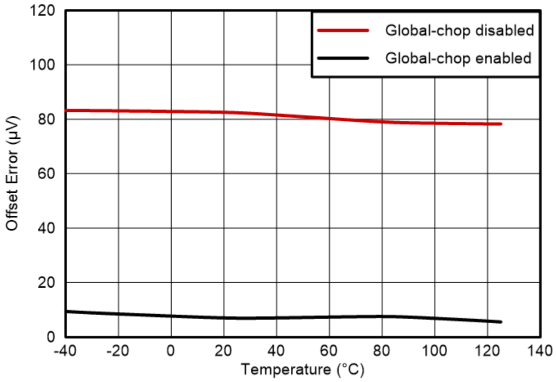
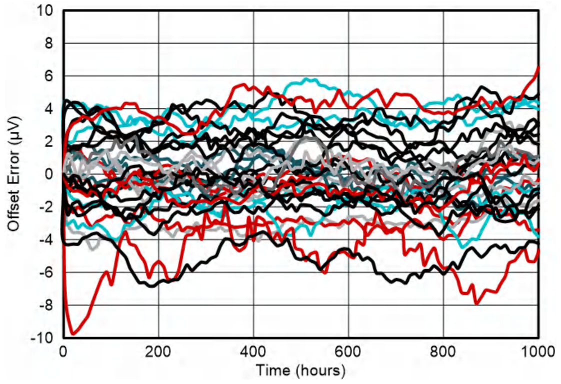


Figure 6-9. Offset Error vs Temperature

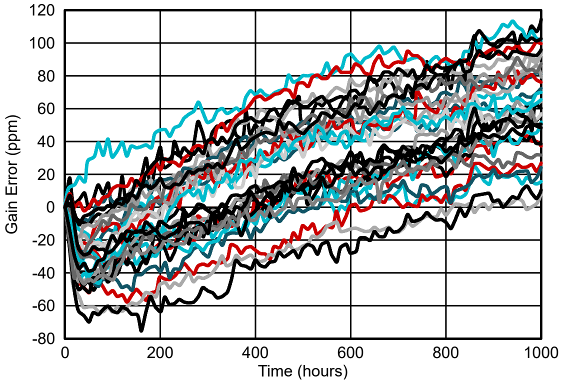
6.12 Typical Characteristics (continued)

for channel 0 at T_A = 25°C, DVDD = 3.3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS (OSR = 1024 and clock divider N_{DIV} = 2), high-resolution mode, with all channels enabled, global-chop mode disabled, and gain = 1 (unless otherwise noted)



30 units, 85°C

Figure 6-10. Offset Error vs Time



30 units, 85°C

Figure 6-11. Gain Error vs Time

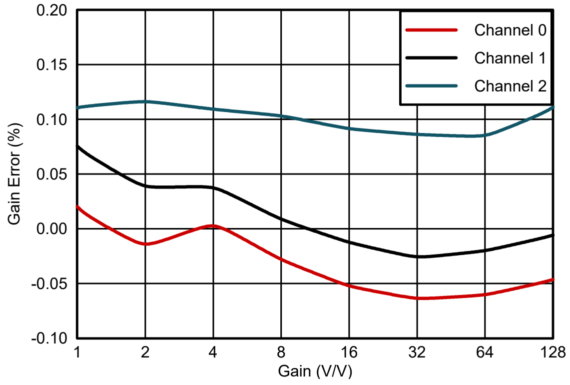


Figure 6-12. Gain Error vs Gain

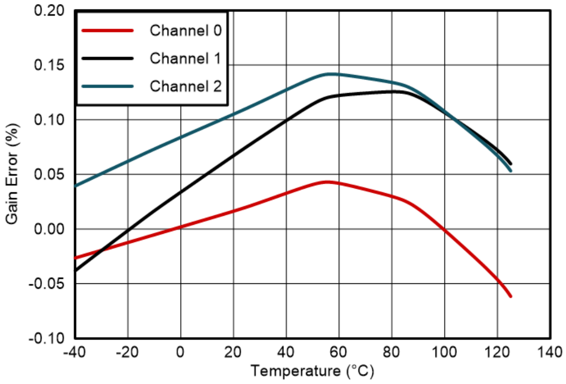
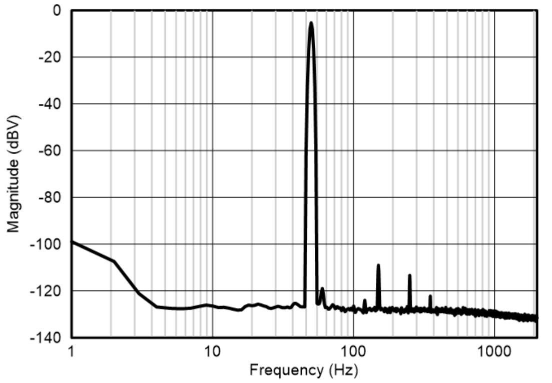
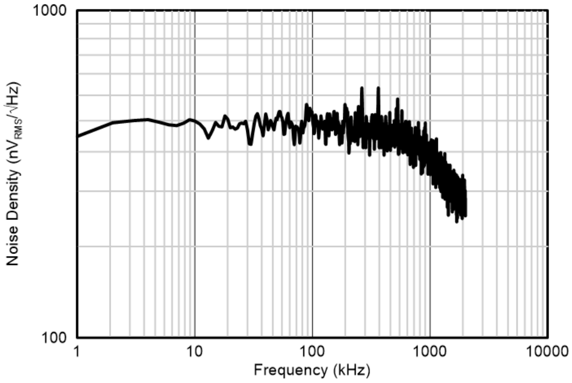


Figure 6-13. Gain Error vs Temperature



Averaged FFT, frequency bin width equals 1 Hz

Figure 6-14. Frequency Spectrum With 50-Hz Input Signal



Averaged FFT, frequency bin width equals 1 Hz

Figure 6-15. Noise Spectral Density vs Frequency

6.12 Typical Characteristics (continued)

for channel 0 at T_A = 25°C, DVDD = 3.3 V, f_{CLKIN} = 8.192 MHz, data rate = 4 kSPS (OSR = 1024 and clock divider N_{DIV} = 2), high-resolution mode, with all channels enabled, global-chop mode disabled, and gain = 1 (unless otherwise noted)

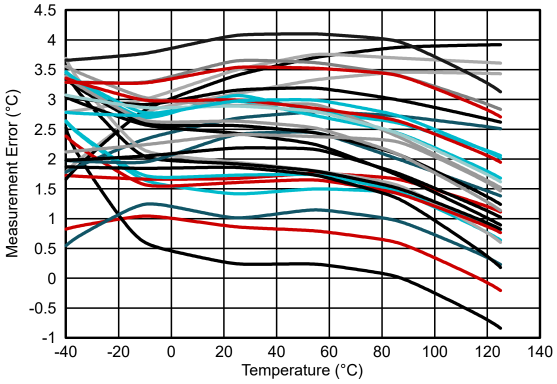


Figure 6-16. Internal Temperature Sensor Accuracy vs Temperature (Without Calibration)

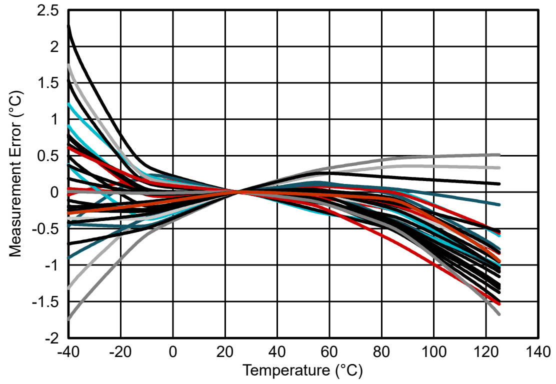


Figure 6-17. Internal Temperature Sensor Accuracy vs Temperature (With Calibration)

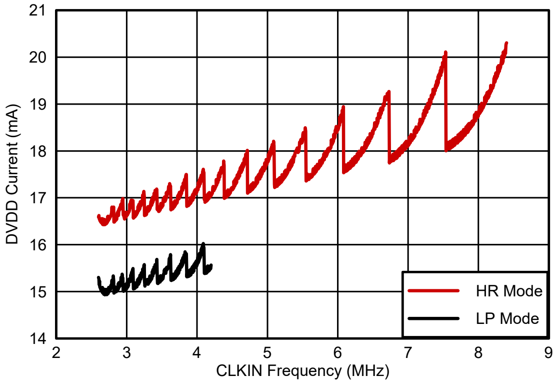


Figure 6-18. DVDD Current vs CLKIN Frequency

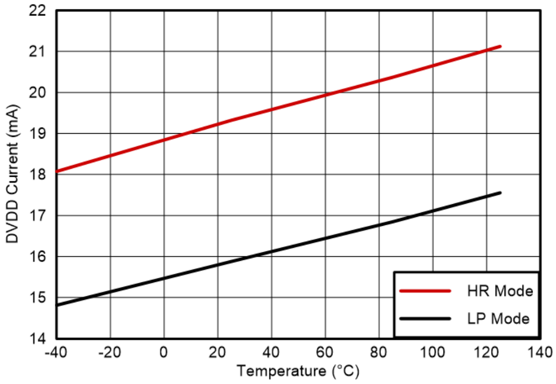


Figure 6-19. DVDD Current vs Temperature

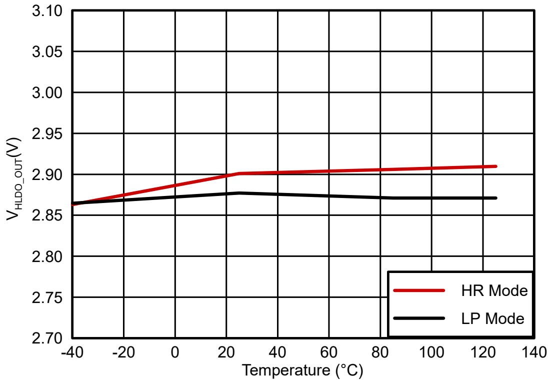


Figure 6-20. HLDO Output Voltage vs Temperature

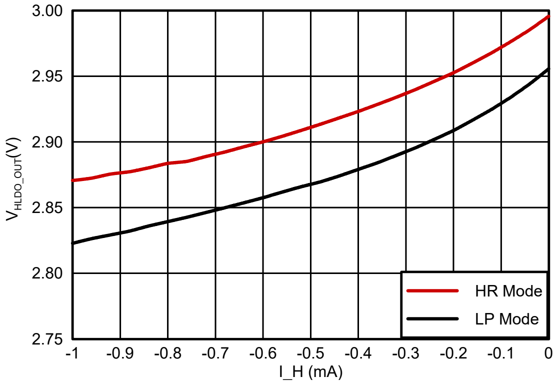


Figure 6-21. HLDO Output Voltage vs Load Current

7 Parameter Measurement Information

7.1 Noise Measurements

Adjust the data rate and gain to optimize the AMC130M03 noise performance. When averaging is increased by reducing the data rate, noise drops correspondingly. Table 7-1 summarizes the AMC130M03 noise performance using the 1.2-V internal reference and a 3.3-V power supply at the DVDD pin. Data are representative of typical noise performance at T_A = 25°C when f_{CLKIN} = 8.192 MHz. The clock divider is configured to the default setting (that is, the CLK_SEL[1:0] bits in the CLOCK register are set to 00b), thus the modulator clock frequency (f_{MOD}) is equal to f_{CLKIN} / 2. The data shown are typical input-referred noise results with the analog inputs shorted together and taking an average of multiple readings on channel 0. A minimum 1 second of consecutive readings are used to calculate the RMS noise for each reading. Table 7-2 lists the effective resolution calculated from the noise data. Equation 1 calculates effective resolution. V_{REF} corresponds to the internal 1.2-V reference. In global-chop mode, noise improves by a factor of $\sqrt{2}$.

Noise performance scales with the OSR and gain settings, but is independent from the configured power mode. Thus, the device exhibits the same noise performance in different power modes when selecting the same OSR and gain settings. However, the data rate at the OSR settings scales based on the applied clock frequency for the different power modes.

$$\text{Effective Resolution} = \log_2\left(\frac{2 \times V_{REF}}{\text{Gain} \times V_{RMS}}\right) \tag{1}$$

Table 7-1. Noise (μV_{RMS}) at T_A = 25°C, Channel 0

OSR	DATA RATE (kSPS), f_{CLKIN} = 8.192 MHz	GAIN							
		1	2	4	8	16	32	64	128
16384	0.25	36.62	18.31	9.16	4.58	2.29	1.14	0.57	0.51
8192	0.5	36.62	18.31	9.16	4.58	2.29	1.55	1.07	0.92
4096	1	36.62	18.31	9.16	4.58	2.29	1.56	1.53	1.67
2048	2	36.62	18.31	9.16	4.58	2.46	1.68	1.56	1.85
1024	4	36.62	18.31	9.16	4.58	3.39	1.75	2.03	2.86
512	8	36.62	18.31	9.16	6.34	5.15	4.22	4.63	4.36
256	16	36.62	18.31	10.51	8.39	7.10	6.35	5.58	4.75
128	32	36.62	18.31	14.68	10.44	7.75	7.72	8.35	7.87
64	64	77.32	42.11	28.44	16.83	10.89	9.94	9.06	8.99

Table 7-2. Effective Resolution (Bits) at T_A = 25°C, Channel 0

OSR	DATA RATE (kSPS), f_{CLKIN} = 8.192 MHz	GAIN							
		1	2	4	8	16	32	64	128
16384	0.25	16.0	16.0	16.0	16.0	16.0	16.0	16.0	15.2
8192	0.5	16.0	16.0	16.0	16.0	16.0	15.6	15.1	14.3
4096	1	16.0	16.0	16.0	16.0	16.0	15.5	14.6	13.5
2048	2	16.0	16.0	16.0	16.0	15.9	15.4	14.6	13.3
1024	4	16.0	16.0	16.0	16.0	15.4	15.4	14.2	12.7
512	8	16.0	16.0	16.0	15.5	14.8	14.1	13.0	12.1
256	16	16.0	16.0	15.8	15.1	14.4	13.5	12.7	11.9
128	32	16.0	16.0	15.3	14.8	14.2	13.2	12.1	11.2
64	64	14.9	14.8	14.4	14.1	13.7	12.9	12.0	11.0

8 Detailed Description

8.1 Overview

The AMC130M03 is an isolated, low-power, three-channel, simultaneous-sampling, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with a low-drift internal voltage reference and an integrated DC/DC converter that allows the device to be supplied from a single 3.3-V or 5-V voltage supply source on the primary (low) side. The dynamic range, size, feature set, and power consumption are optimized for cost-sensitive applications requiring simultaneous sampling.

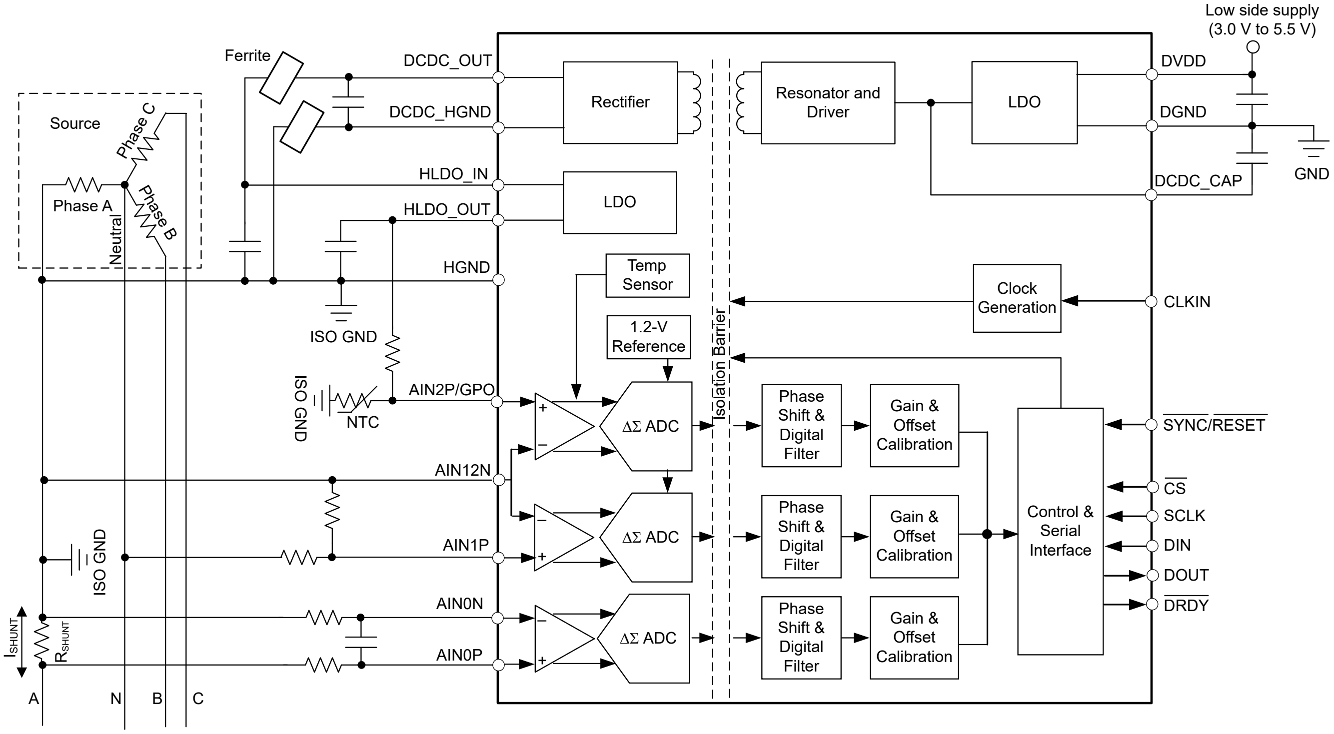
The silicon-dioxide (SiO_2)-based capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note.

An integrated negative charge pump allows absolute input voltages as low as 1.3 V below HGND, which enables measurements of input signals varying around ground with a single-ended power supply. The device features a programmable gain amplifier (PGA) with gains up to 128. An integrated input precharge buffer enabled at gains greater than 4 provides high input impedance at high PGA gain settings. The ADC receives the reference voltage from an integrated 1.2-V reference. The device allows differential input voltages as large as the reference. Two power-scaling modes allow designers to trade power consumption for ADC dynamic range.

Each ADC channel on the AMC130M03 contains a digital decimation filter that demodulates the output of the ΔΣ modulators. The filter enables data rates as high as 64 kSPS per channel in high-resolution mode. The relative phase of the samples can be configured between channels, thus enabling an accurate compensation for the sensor phase response. Offset and gain calibration registers can be programmed to automatically adjust output samples for measured offset and gain errors. The *Functional Block Diagram* provides a detailed diagram of the AMC130M03.

The device communicates via a serial programming interface (SPI)-compatible interface. Several SPI commands and internal registers control the operation of the AMC130M03. Other devices can be added to the same SPI bus by adding discrete $\overline{\text{CS}}$ control lines. The $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin can synchronize conversions between multiple AMC130M03 devices and maintains synchronization with external events.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Isolated DC/DC Converter

The AMC130M03 offers a fully integrated isolated DC/DC converter stage that includes the following components, as illustrated in the *Functional Block Diagram*:

- Low-dropout regulator (LDO) on the primary side to stabilize the supply voltage that drives the primary side of the converter
- Primary full-bridge inverter and drivers
- Laminate-based, air-core transformer for high immunity to magnetic fields
- Secondary full-bridge rectifier
- Secondary LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path

The DC/DC converter uses a spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronous to the operation of the ΔΣ modulator to minimize interference with data transmission and support the high analog performance of the device.

8.3.1.1 DC/DC Converter Failure Detection

A failure in the DC/DC converter is indicated by reading a logic high of the SEC_FAIL bit in the STATUS register. This bit is a latched bit. If any failure of the internal DC/DC converter occurs during device operation, but the DC/DC converter recovers from the failure and operates normally after this instance, the SEC_FAIL bit remains in a logic high state until the STATUS register is read. Reading the status register clears the SEC_FAIL bit. As described in the *Start-Up Behavior After Power-Up* section, use two consecutive STATUS register read commands to verify correct operation of the DC/DC converter at a given point in time (for example, at device power-up).

8.3.2 High-Side Current Drive Capability

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC130M03 and can source up to I_H of additional DC current for external circuitry (such as an active filter, preamplifier, or comparator). Use the HLDO_OUT pin as a power supply for this external circuit. Because of the output impedance at the HLDO_OUT pin, the voltage at HLDO_OUT depends on the magnitude of the drive current and the selected power mode. For operation across all temperatures and power modes, components for the external circuits must operate at a low supply voltage (such as 2.7 V). See the *Clocking and Power Modes* section for details on the available power modes.

8.3.3 Isolation Channel Signal Transmission

The AMC130M03 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the capacitive SiO_2-based isolation barrier. After transmission across the isolation barrier, the modulator output bitstream is decimated using the sinc filter to reconstruct the ADC conversion data, and is then transferred to the digital control so that the data are accessible through the SPI interface. Figure 8-1 depicts the block diagram of an isolation channel. The transmitter modulates the bitstream at TX IN with an internally generated, 480-MHz carrier and sends a burst across the isolation barrier to represent a digital *one* and sends a *no signal* to represent the digital *zero*. The receiver demodulates the signal after advanced signal conditioning and produces the output. The symmetrical design of each isolation channel improves the common-mode transient immunity (CMTI) performance and reduces the radiated emissions caused by the high-frequency carrier.

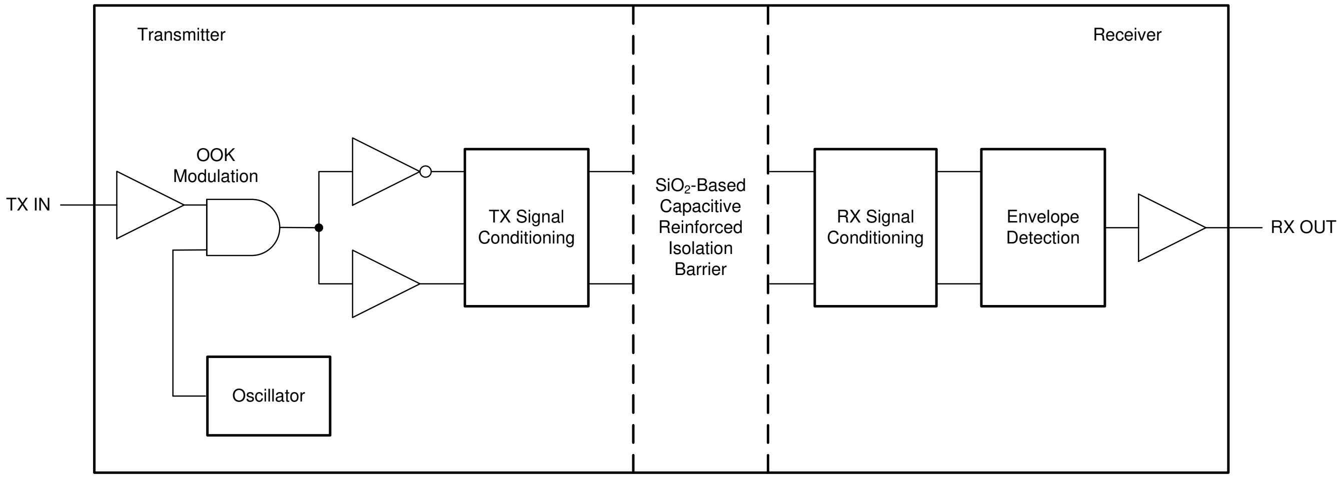


Figure 8-1. Block Diagram of an Isolation Channel

Figure 8-2 shows the concept of the on-off keying scheme.

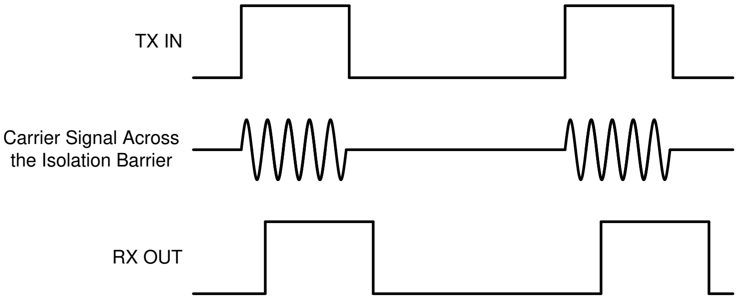


Figure 8-2. OOK-Based Modulation Scheme

8.3.4 Input ESD Protection Circuitry

Basic electrostatic discharge (ESD) circuitry protects the AMC130M03 inputs from ESD and overvoltage events in conjunction with external circuits and assemblies. Figure 8-3 shows a simplified representation of the ESD circuit. The protection for input voltages exceeding V_{HLDO_OUT} can be modeled as a simple diode.

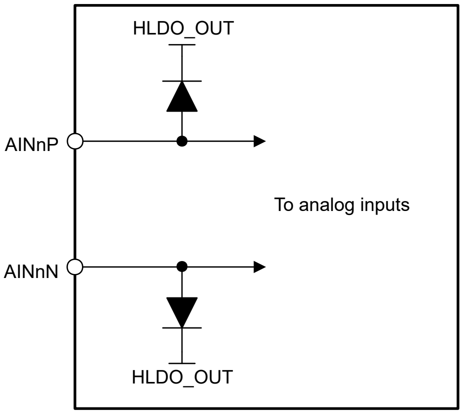


Figure 8-3. Input ESD Protection Circuitry

The AMC130M03 has an integrated negative charge pump that allows for input voltages below HGND with a unipolar supply. Consequently, shunt diodes between the inputs and HGND cannot be used to clamp excessive negative input voltages. Instead, the same diode that clamps overvoltage also clamps undervoltage at the reverse breakdown voltage. Take care to prevent input voltages or currents from exceeding the limits provided in the *Absolute Maximum Ratings* table.

8.3.5 Input Multiplexer

Each channel of the AMC130M03 has a dedicated input multiplexer. The multiplexer controls which signals are routed to the ADC channels. Configure the input multiplexer using the MUXn[1:0] bits in the CHn_CFG register. The input multiplexer allows the following inputs to be connected to the ADC channel:

- The analog input pins corresponding to the given channel
- HGND, which is used for offset calibration
- Positive DC test signal
- Negative DC test signal

See the *Internal Test Signals* section for more information about the test signals. Figure 8-4 shows a diagram of the input multiplexer on the AMC130M03.

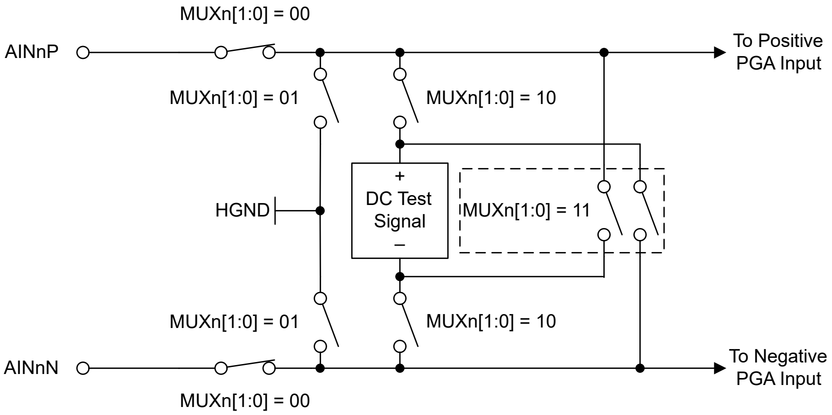


Figure 8-4. Input Multiplexer

8.3.6 Programmable Gain Amplifier (PGA)

Each channel of the AMC130M03 features an integrated programmable gain amplifier (PGA) that provides gains of 1, 2, 4, 8, 16, 32, 64, and 128. The gains for all channels are individually controlled by the PGAGAINx[2:0] bits for each channel in the GAIN register.

Changing the PGA gain scales the differential full-scale input voltage range (FSR) of the ADC. Equation 2 describes the relationship between FSR and gain. Equation 2 uses the internal reference voltage, 1.2 V, as the scaling factor without accounting for gain error caused by tolerance in the reference voltage.

$$FSR = \pm 1.2\ V / Gain \tag{2}$$

Table 8-1 shows the corresponding full-scale ranges for each gain setting.

Table 8-1. Full-Scale Range

GAIN SETTING	FSR
1	±1.2 V
2	±600 mV
4	±300 mV
8	±150 mV
16	±75 mV
32	±37.5 mV
64	±18.75 mV
128	±9.375 mV

The input impedance of the PGA dominates the input impedance characteristics of the AMC130M03. The PGA input impedance for gain settings up to 4 behaves according to Equation 3 without accounting for device tolerance and change over temperature. Minimize the output impedance of the circuit that drives the AMC130M03 inputs to obtain the best possible gain error, INL, and distortion performance.

$$275\ \text{k}\Omega \times 4.096\ \text{MHz} / f_{MOD} \quad (3)$$

where:

- f_{MOD} is the ΔΣ modulator frequency, f_{CLKIN} / N_{DIV}

By default, N_{DIV} = 2. N_{DIV} is set by the programmable clock divider, see the *Clocking and Power Modes* section.

The device uses an input precharge buffer for PGA gain settings of 8 and higher. The input impedance at these gain settings is very high. Specifying the input bias current for these gain settings is therefore more useful.

8.3.7 Voltage Reference

The AMC130M03 uses an internally generated, low-drift, band-gap voltage to supply the reference for the ADC. The reference has a nominal voltage of 1.2 V, allowing the differential input voltage to swing from –1.2 V to 1.2 V. The reference circuitry starts up very quickly to accommodate the fast start-up feature of this device. The device waits until the reference circuitry is fully settled before generating conversion data.

8.3.8 Internal Test Signals

The AMC130M03 features an internal analog test signal that is useful for troubleshooting and diagnosis. A positive or negative DC test signal can be applied to the channel inputs through the input multiplexer. The multiplexer is controlled through the MUXn[1:0] bits in the CHn_CFG register. The test signals are created by internally dividing the reference voltage. The same signal is shared by all channels.

The test signal is nominally 2 / 15 × V_{REF}. The test signal automatically adjusts the voltage level with the gain setting such that the ADC always measures a signal that is 2 / 15 × $V_{Diff\ Max}$. For example, at a gain of 1, this voltage equates to 160 mV. At a gain of 2, this voltage is 80 mV.

8.3.9 Clocking and Power Modes

An LVCMOS clock must be provided at the CLKIN pin continuously when the AMC130M03 is running in normal operation. The frequency of the clock can be scaled in conjunction with the power mode to provide a tradeoff between power consumption and dynamic range.

The PWR[1:0] bits in the CLOCK register allow the device to be configured in one of two power modes: high-resolution (HR) or low-power (LP) mode. Changing the PWR[1:0] bits scales the internal bias currents to achieve the expected power levels. The external clock frequency must follow the guidance provided in the *Recommended Operating Conditions* table corresponding to the intended power mode for the device to perform according to the specification.

The main clock must be externally provided at the CLKIN pin. As shown in Figure 8-5, a user-programmable clock divider divides the main clock to derive the internal modulator clock (MOD_CLK). By default, the main clock provided at the CLKIN pin is divided by N_{DIV} = 2 to generate a 50% duty cycle internal modulator clock. As listed in Table 8-2, the divider ratio N_{DIV} can be changed to values of 4, 8, and 12 using the CLK_DIV[1:0] bits in the CLOCK register.

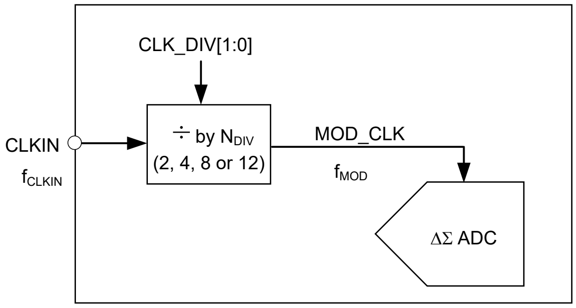


Figure 8-5. Programmable Clock Divider Block Diagram

Table 8-2. Modulator Clock Divider Selection

CLK_DIV[1:0]	N_{DIV} FOR MOD_CLK AT ALL CHANNELS
00b	2
01b	4
10b	8
11b	12

The clock frequency range of the internal DC/DC converter must be synchronized with the modulator clock to minimize interference. To optimize the DC/DC converter internal clock, the actual frequency value of the modulator clock must be written to the DCDC_CTRL register immediately after device power-up. The modulator clock frequency is a result of the frequency provided at the CLKIN pin and the selected divider ratio (for example, if a 4-MHz clock frequency is provided at the CLKIN pin, and the divider ratio is set to 4, then the frequency of the modulator clock MOD_CLK is 1 MHz). The correct modulator clock frequency value must be configured in the DCDC_CTRL register, as given in Table 8-3, by writing to the DCDC_FREQ[3:0] register bits immediately after start-up.

An example calculation is:

- Main clock: f_{CLKIN} = 8.192 MHz
- Divider ratio: N_{DIV}= 4
- Resulting modulator clock: f_{CLKIN} / N_{DIV} = 2.048 MHz
- Modulator clock frequency is within the range: 1.926 MHz to 2.051 MHz; see Table 8-3
- Required DCDC_FREQ[3:0] bit setting: 1000b; see Table 8-3

Table 8-3. Modulator Clock Frequency Range Selection for DC/DC Synchronization

MODULATOR CLOCK FREQUENCY (MHz)	DCDC_FREQ[3:0] BIT SETTING
3.768 MHz to 4.100 MHz	0000b
3.366 MHz to 3.768 MHz	0001b
3.041 MHz to 3.366 MHz	0010b
2.773 MHz to 3.041 MHz	0011b
2.549 MHz to 2.773 MHz	0100b
2.358 MHz to 2.549 MHz	0101b
2.194 MHz to 2.358 MHz	0110b
2.051 MHz to 2.194 MHz	0111b
1.926 MHz to 2.051 MHz	1000b
1.815 MHz to 1.926 MHz	1001b
1.716 MHz to 1.815 MHz	1010b
1.627 MHz to 1.716 MHz	1011b
1.547 MHz to 1.627 MHz	1100b
1.475 MHz to 1.547 MHz	1101b
1.409 MHz to 1.475 MHz	1110b
1.400 MHz to 1.409 MHz	1111b

8.3.10 ΔΣ Modulator

The AMC130M03 uses a delta-sigma (ΔΣ) modulator to convert the analog input voltage to a one's density modulated digital bitstream. The ΔΣ modulator oversamples the input voltage at a frequency many times greater than the output data rate. The modulator frequency, f_{MOD}, of the AMC130M03 is derived from the main clock frequency (provided at the CLKIN pin) with the user-programmable clock divider; see the *Clocking and Power Modes* section.

The output of the modulator is fed back to the modulator input through a digital-to-analog converter (DAC) as a means of error correction. This feedback mechanism shapes the modulator quantization noise in the frequency domain to make the noise more dense at higher frequencies and less dense in the band of interest. The digital decimation filter following the ΔΣ modulator significantly attenuates the out-of-band modulator quantization noise, allowing the device to provide excellent dynamic range.

8.3.11 Digital Filter

The ΔΣ modulator bitstream feeds into a digital filter. The digital filter is a linear-phase, finite impulse response (FIR), low-pass, sinc-type filter that attenuates the out-of-band quantization noise of the ΔΣ modulator. The digital filter demodulates the output of the ΔΣ modulator by averaging. The data passing through the filter are decimated and downsampled to reduce the rate at which data come out of the modulator (f_{MOD}) to the output data rate (f_{DATA}). The decimation factor is defined as per Equation 4 and is called the *oversampling ratio (OSR)*.

$$OSR = f_{MOD} / f_{DATA} \tag{4}$$

The OSR is configurable and set by the OSR[2:0] bits in the CLOCK register. By setting the OSR[2:0] bits, the OSR can be configured in values ranging from 128 to 16384 in binary steps. In addition, the OSR can be configured to a value of 64 by setting the TURBO bit in the CLOCK register (turbo mode). Therefore in total, there are nine OSR settings in the AMC130M03, allowing nine different data rate settings for any given main clock frequency. Table 8-4 lists the OSR settings and the corresponding output data rates for the nominal CLKIN frequencies mentioned, assuming the programmable clock divider is set to N_{DIV} = 2.

The OSR determines the amount of averaging of the modulator output in the digital filter and, therefore, also the filter bandwidth. The filter bandwidth directly affects the noise performance of the ADC because lower bandwidth results in lower noise, whereas higher bandwidth results in higher noise. See Table 7-1 for the noise specifications for various OSR settings.

The device must be in standby mode when changing the OSR. Setting the OSR[2:0] bits to a new value while the ADC is generating conversion data can result in unexpected behavior of the ADC output.

Table 8-4. OSR Settings and Data Rates for Nominal Main Clock Frequencies

POWER MODE	NOMINAL MAIN CLOCK FREQUENCY	f_{MOD}(1)	OSR	OUTPUT DATA RATE
High-resolution (HR)	8.192 MHz	4.096 MHz	64	64 kSPS
			128	32 kSPS
			256	16 kSPS
			512	8 kSPS
			1024	4 kSPS
			2048	2 kSPS
			4096	1 kSPS
			8192	500 SPS
			16384	250 SPS
Low-power (LP)	4.096 MHz	2.048 MHz	64	32 kSPS
			128	16 kSPS
			256	8 kSPS
			512	4 kSPS
			1024	2 kSPS
			2048	1 kSPS
			4096	500 SPS
			8192	250 SPS
			16384	125 SPS

(1) Programmable clock divider is set to N_{DIV} = 2.

8.3.11.1 Digital Filter Implementation

Figure 8-6 shows the digital filter implementation of the AMC130M03. The modulator bitstream feeds two parallel filter paths: a sinc^3 filter and a fast-settling filter path.

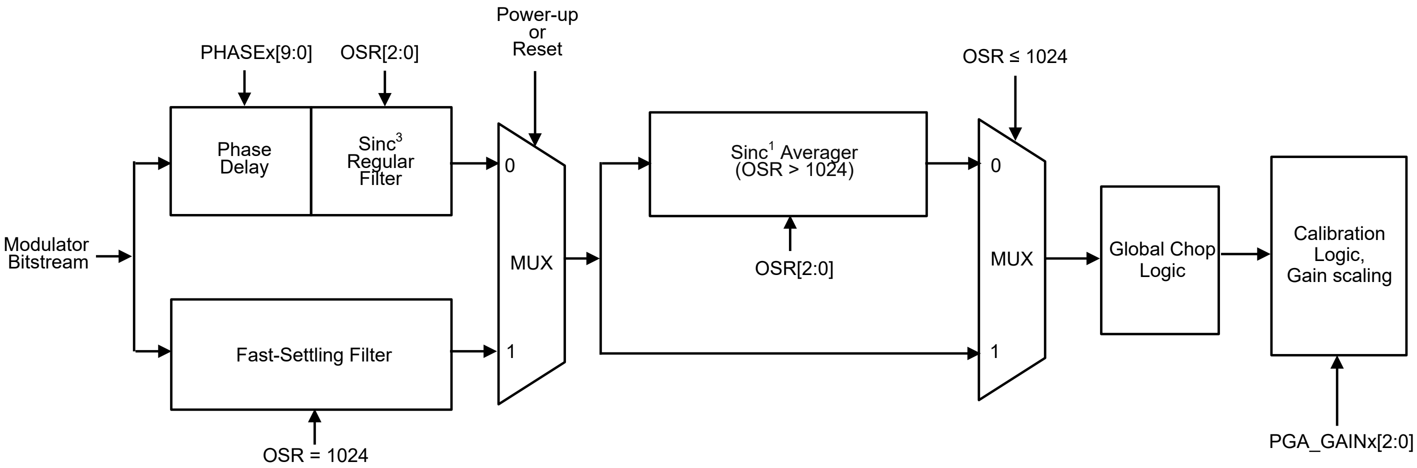


Figure 8-6. Digital Filter Implementation

8.3.11.1.1 Fast-Settling Filter

At power-up or after a device reset, the AMC130M03 selects the fast-settling filter to allow for settled output data generation with minimal latency. The fast-settling filter has the characteristic of a first-order sinc filter (sinc^1).

After two conversions, the device switches to and remains in the sinc^3 filter path until the next time the device is powered down or reset.

The fast-settling filter exhibits wider bandwidth and less stop-band attenuation than the sinc^3 filter. Consequently, the noise performance when using the fast-settling filter is not as high as with the sinc^3 filter. The first two samples available from the AMC130M03 after a supply ramp or reset have the noise performance and frequency response corresponding to the fast-settling filter, whereas subsequent samples have the noise performance and frequency response consistent with the sinc^3 filter. See the *Start-Up Behavior After Power-Up* section for more details regarding the start-up capabilities of the AMC130M03.

8.3.11.1.2 SINC^3 and SINC^3 + SINC^1 Filter

The AMC130M03 selects the sinc^3 filter path two conversions after power-up or device reset. For OSR settings of 64 to 1024, the sinc^3 filter output directly feeds into the global-chop and calibration logic. For OSR settings of 2048 and higher, the sinc^3 filter is followed by a sinc^1 filter. The sinc^3 filter operates at a fixed OSR of 1024 in this case while the sinc^1 filter implements the additional OSRs of 2 to 16. Thus, when an OSR of 4096 (for example) is selected, the sinc^3 filter operates at an OSR of 1024 and the sinc^1 filter operates at an OSR of 4.

The filter has infinite attenuation at integer multiples of the data rate except for integer multiples of f_{MOD}. As with all digital filters, the digital filter response of the AMC130M03 repeats at integer multiples of the modulator frequency, f_{MOD}. The data rate and filter notch frequencies scale with f_{MOD}.

When possible, plan frequencies for unrelated periodic processes in the application for integer multiples of the data rate such that any parasitic effect on data acquisition is effectively canceled by the notches of the digital filter. Avoid frequencies near integer multiples of f_{MOD} whenever possible because tones in these bands can alias to the band of interest.

The sinc^3 and sinc^3 + sinc^1 filters for a given channel require time to settle after a channel is enabled, the channel multiplexer or gain setting is changed, or a resynchronization event occurs. See the *Synchronization* section for more details on resynchronization. Table 8-5 lists the settling times of the sinc^3 and sinc^3 + sinc^1 filters for each OSR setting. The AMC130M03 does not gate unsettled data. Therefore, the host must account for the filter settling time and disregard unsettled data if any are read. Wait for the duration of the settling times listed in Table 8-5 plus one additional conversion cycle before the data that was read can be considered valid.

Table 8-5. Digital Filter Settling Times

OSR (OVERALL)	OSR (SINC^3)	OSR (SINC^1)	SETTLING TIME, detailed (t_{CLKIN})	SETTLING TIME, total (t_{CLKIN})
64	64	N/A	3 × 64 + 44 + 4	240
128	128	N/A	3 × 128 + 44 + 4	432
256	256	N/A	3 × 256 + 44 + 4	816
512	512	N/A	3 × 512 + 44 + 4	1584
1024	1024	N/A	3 × 1024 + 44 + 4	3120
2048	1024	2	6 × 1024 + 44 + 4	6192
4096	1024	4	10 × 1024 + 44 + 4	10288
8192	1024	8	18 × 1024 + 44 + 4	18480
16384	1024	16	34 × 1024 + 44 + 4	34864

8.3.11.2 Digital Filter Characteristic

Equation 5 calculates the z-domain transfer function of a sinc^3 filter that is used for OSRs of 1024 and lower.

$$\left|H(z)\right| = \left|\frac{1 - Z^{-N}}{N\left(1 - Z^{-1}\right)}\right|^3 \tag{5}$$

where:

- N is the OSR

Equation 6 calculates the transfer function of a sinc^3 filter in terms of the continuous-time frequency parameter *f*.

$$
H(f)\,\Big| = \left| \frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)} \right|^3 \tag{6}
$$

where:

- N is the OSR

Figure 8-7 and Figure 8-8 show the digital filter response of the fast-settling filter and the sinc^3 filter for OSRs of 1024 and lower. Figure 8-9 and Figure 8-10 show the digital filter response of the sinc^3 + sinc^1 filter for an OSR of 4096.

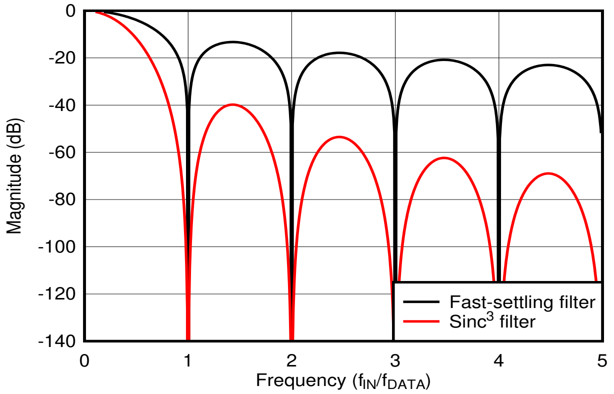


Figure 8-7. Fast-Settling and Sinc^3 Digital Filter Response

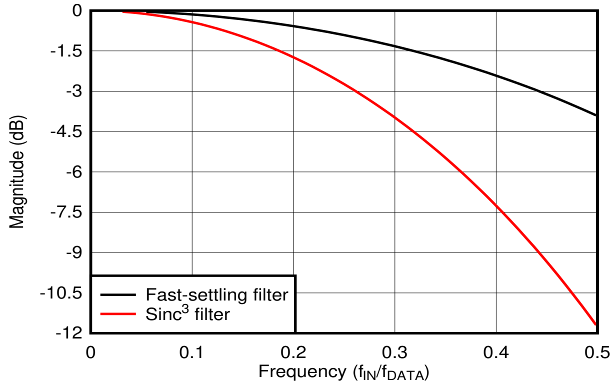


Figure 8-8. Fast-Settling and Sinc^3 Digital Filter Response, Pass-Band Detail

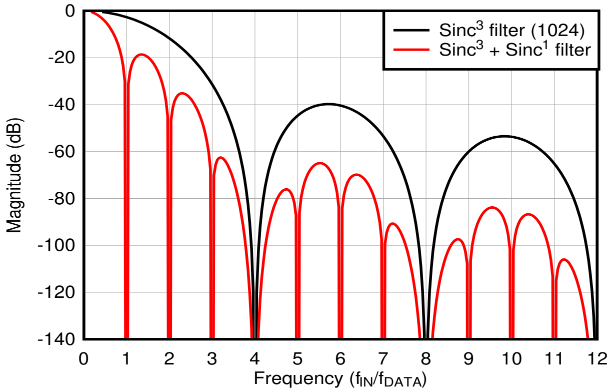


Figure 8-9. Digital Filter Response for OSR = 4096 as a Combination of Sinc^3 + Sinc^1

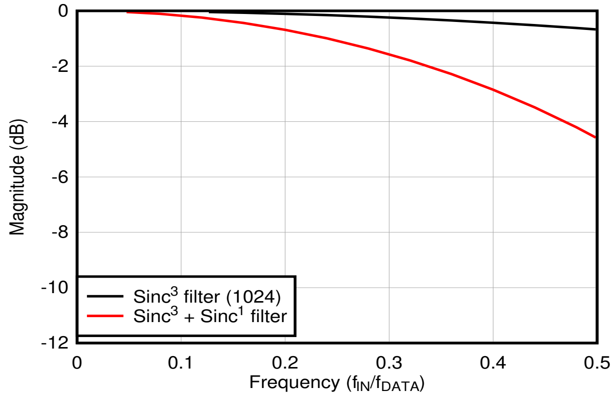


Figure 8-10. Sinc^3 + Sinc^1 Digital Filter Response at OSR = 4096, Pass-Band Detail

8.3.12 Channel Phase Calibration

The AMC130M03 allows fine adjustment of the sample phase between channels by using channel phase calibration. This feature is helpful when different channels are measuring the outputs of different types of sensors that have different phase responses. For example, in power metrology applications, voltage can be measured by a voltage divider, whereas current is measured using a current transformer that exhibits a phase difference between the input and output signals. The differences in phase between the voltage and current measurement must be compensated to measure the power and related parameters accurately.

The phase setting of the different channels is configured by the PHASEn[9:0] bits in the CHn_CFG register corresponding to the channel whose phase adjustment is desired. The register value is a 10-bit, two's-complement value corresponding to the number of modulator clock cycles of phase offset compared to a reference phase of zero degrees.

The mechanism for achieving phase adjustment derives from the ΔΣ architecture. The ΔΣ modulator produces samples continuously at the modulator frequency, f_{MOD}. These samples are filtered and decimated to the output data rate by the digital filter. The ratio between f_{MOD} and the data rate is the oversampling ratio (OSR). Each conversion result corresponds to an OSR number of modulator samples provided to the digital filter. When the different channels of the AMC130M03 have no programmed phase offset between them, the modulator clock cycles corresponding to the conversion results of the different channels are aligned in the time domain. Figure 8-11 shows an example scenario where the voltage input to channel 1 has no phase offset from channel 0.

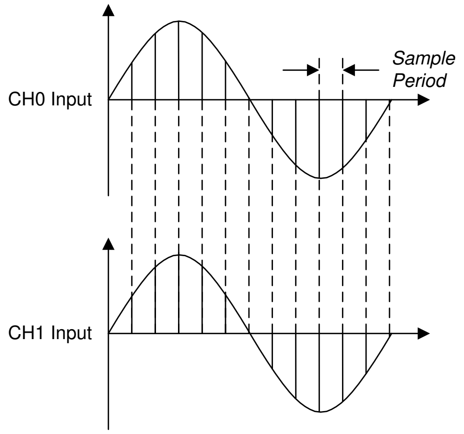


Figure 8-11. Two Channel Outputs With Equal Phase Settings

However, the sample period of one channel can be shifted with respect to another. If the inputs to both channels are sinusoids of the same frequency and the samples for these channels are retrieved by the host at the same time, the effect is that the phase of the channel with the modified sample period appears *shifted*. Figure 8-12 shows how the period corresponding to the samples are shifted between channels. Figure 8-13 illustrates how the samples appear as having generated a phase shift when retrieved by the host.

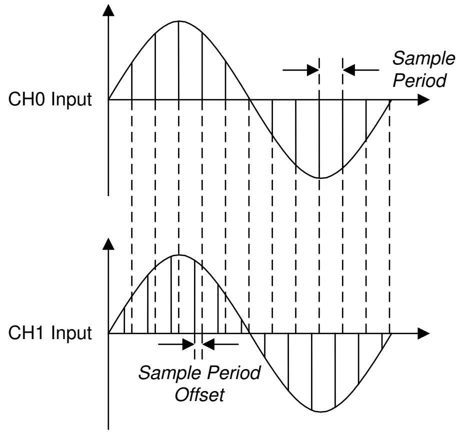


Figure 8-12. Channel 1 With a Positive Sample Phase Shift With Respect to Channel 0

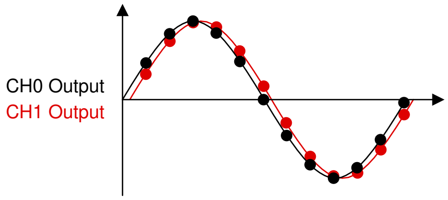


Figure 8-13. Channels 1 and 0 From the Perspective of the Host

The valid setting range is from –OSR / 2 to (OSR / 2) – 1, except for OSRs greater than 1024, where the phase calibration setting is limited to –512 to 511. If a value outside of –OSR / 2 and (OSR / 2) – 1 is programmed, the device internally clips the value to the nearest limit. For example, if the OSR setting is programmed to 128 and the PHASEn[9:0] bits are programmed to 0001100100b corresponding to 100 modulator clock cycles, the device sets the phase of the channel to 63 because that value is the upper limit of phase calibration for that OSR setting. Table 8-6 gives the range of phase calibration settings for various OSR settings.

Table 8-6. Phase Calibration Setting Limits for Different OSR Settings

OSR SETTING	PHASE OFFSET RANGE (t_{MOD})	PHASEn[9:0] BITS RANGE
64	–32 to 31	11 1110 0000b to 00 0001 1111b
128	–64 to 63	11 1100 0000b to 00 0011 1111b
256	–128 to 127	11 1000 0000b to 00 0111 1111b
512	–256 to 255	11 0000 0000b to 00 1111 1111b
1024	–512 to 511	10 0000 0000b to 01 1111 1111b
2048	–512 to 511	10 0000 0000b to 01 1111 1111b
4096	–512 to 511	10 0000 0000b to 01 1111 1111b
8192	–512 to 511	10 0000 0000b to 01 1111 1111b
16384	–512 to 511	10 0000 0000b to 01 1111 1111b

Follow these steps to create a phase shift larger than half the sample period for OSRs less than 2048:

- Create a phase shift corresponding to an integer number of sample periods by modifying the indices between channel data in software
- Use the phase calibration function of the AMC130M03 to create the remaining fractional sample period phase shift

For example, to create a phase shift of 2.25 samples between channels 0 and 1, create a phase shift of two samples by aligning sample N in the channel 0 output data stream with sample N+2 in the channel 1 output data stream in the host software. Make the remaining 0.25 sample adjustment using the AMC130M03 phase calibration function.

The phase calibration settings of the channels affect the timing of the data-ready interrupt signal, $\overline{\text{DRDY}}$. See the *Data Ready ($\overline{\text{DRDY}}$)* section for more details regarding how phase calibration affects the $\overline{\text{DRDY}}$ signal.

8.3.13 Calibration Registers

The calibration registers allow for automatic computation of calibrated ADC conversion results from preprogrammed values. The host can rely on the device to automatically correct for system gain and offset after the error correction terms are programmed into the corresponding device registers. The measured calibration coefficients must be stored in external nonvolatile memory and programmed into the registers each time the AMC130M03 powers up because the AMC130M03 registers are volatile.

The offset calibration registers are used to correct for system offset error, otherwise known as *zero error*. Offset error corresponds to the ADC output when the input to the system is zero. The AMC130M03 corrects for offset errors by subtracting the contents of the OCALn[23:0] register bits in the CHn_OCAL_MSB and CHn_OCAL_LSB registers from the conversion result for that channel before being output. There are separate CHn_OCAL_MSB and CHnOCAL_LSB registers for each channel, which allows separate offset calibration coefficients to be programmed for each channel. The contents of the OCALn[23:0] bits are interpreted by the device as 24-bit, two's-complement values.

The gain calibration registers are used to correct for system gain error. Gain error corresponds to the deviation of gain of the system from the ideal value. The AMC130M03 corrects for gain errors by multiplying the ADC conversion result by the value given by the contents of the GCALn[23:0] register bits in the CHn_GCAL_MSB and CHn_GCAL_LSB registers before being output. There are separate CHn_GCAL_MSB and CHn_GCAL_LSB registers for each channel, which allows separate gain calibration coefficients to be programmed for each channel. The contents of the GCALn[23:0] bits are interpreted by the device as 24-bit unsigned values corresponding to linear steps ranging from gains of 0 to $2 – (1 / 2^{23})$. Table 8-7 describes the relationship between the GCALn[23:0] bit values and the gain calibration factor.

Table 8-7. GCALn[23:0] Bit Mapping

GCALn[23:0] VALUE	GAIN CALIBRATION FACTOR
000000h	0
000001h	1.19×10^{-7}
800000h	1
FFFFFEh	$2 – 2.38 \times 10^{-7}$
FFFFFFh	$2 – 1.19 \times 10^{-7}$

The calibration registers do not need to be enabled because these registers are always in use. The OCALn[23:0] bits have a default value of 000000h resulting in no offset correction. Similarly, the GCALn[23:0] bits default to 800000h resulting in a gain calibration factor of 1.

Figure 8-14 shows a block diagram illustrating the mechanics of the calibration registers on one channel of the AMC130M03.

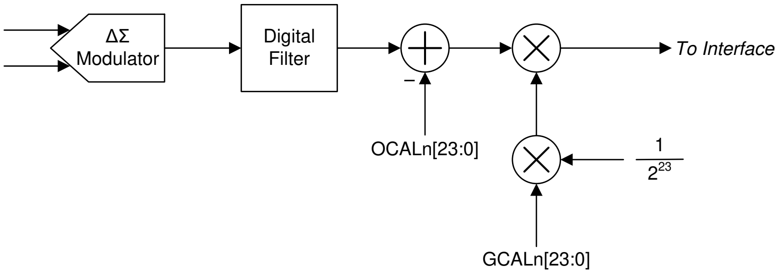


Figure 8-14. Calibration Block Diagram

8.3.14 Register Map CRC

The AMC130M03 performs a CRC on the device register map as a means to check for unintended changes to the registers. Enable the register map CRC by setting the REG_CRC_EN bit in the MODE register. When enabled, the device constantly calculates the register map CRC using each bit in the writable register space. The register addresses covered by the register map CRC on the AMC130M03 are 02h through 31h. The CRC is calculated beginning with the MSB of register 02h and ending with the LSB of register 31h using the polynomial selected in the CRC_TYPE bit in the MODE register.

The calculated CRC is a 16-bit value and is stored in the REGMAP_CRC register. The REG_MAP bit in the STATUS register is set to flag the host if the register map CRC changes, including changes resulting from register writes. The bit is cleared by reading the STATUS register, or by the STATUS register being output as a response to the NULL command.

The CRC calculation is initialized with the seed value of FFFFh.

8.3.15 Temperature Sensor

The AMC130M03 offers an integrated temperature sensor that is multiplexed with the AIN2P input of the voltage channel. The TS_EN bit in the CH2_CFG register selects the temperature sensor mode for the ADC channel connected to the AIN2P input of the AMC130M03. If the TS_EN bit is 0b the ADC measures the voltage between the AIN2P and AIN12N pins (channel 2 input). If the TS_EN bit is 1b, the ADC for this channel is in temperature sensor measurement mode.

Do not use the temperature sensor measurement mode and the global-chop mode at the same time on the AMC130M03. When the TS_EN bit in the CH2_CFG register is set to 1b, the GC_EN bit in the GLOBAL_CHOP_CFG register must be set to 0b.

There are two options for the temperature sensor measurement: internal and external temperature sensor mode. Use the TS_SEL bit in the CH2_CFG register to configure the internal or external temperature measurement mode. If the TS_SEL bit in the CH2_CFG register is set to 0b, the internal temperature sensor mode is selected. In this mode, the ADC on channel 2 measures the internal temperature sensor. Set the TS_SEL bit in the CH2_CFG register to 1b to select the external temperature sensor mode. In external temperature sensor mode, the ADC on channel 2 measures the voltage between the AIN2P and AIN12N pins for sensing an external temperature sensor, such as a positive (PTC) or negative temperature coefficient (NTC) element. This mode is very similar to the generic ADC measurement of a voltage between the AIN2P and AIN12N pins (channel 2 input); however, the conversion rate is reduced as explained in this section, with the benefit of increasing the input impedance.

Temperature readings follow the same process as the analog inputs for starting and reading conversion results; however, the conversion rate for temperature measurements is reduced by a factor of 32 in comparison to the other ADC channels. The benefit is a significantly increased input impedance. New temperature readings are available at channel 2 at every 32nd falling edge of $\overline{\text{DRDY}}$, and new conversion results at channel 0 and channel 1 are available at every falling edge of $\overline{\text{DRDY}}$. The DRDY2 bit in the STATUS register is set to high when a new temperature reading is available.

8.3.15.1 Internal Temperature Sensor

Set the TS_EN bit in the CH2_CFG register to 1b, and the TS_SEL bit in the CH2_CFG register to 0b to select the internal temperature sensor mode. Set the PGAGAIN2[2:0] bits in the GAIN register to 011b (gain of 8) when using the internal temperature sensor. As shown in Figure 8-15, the temperature sensor is comprised of two internal diodes with one diode having eight times the current density of the other. The difference in current density of the diodes yields a differential output voltage that is proportional to absolute temperature. The temperature sensor reading is converted by the ADC.

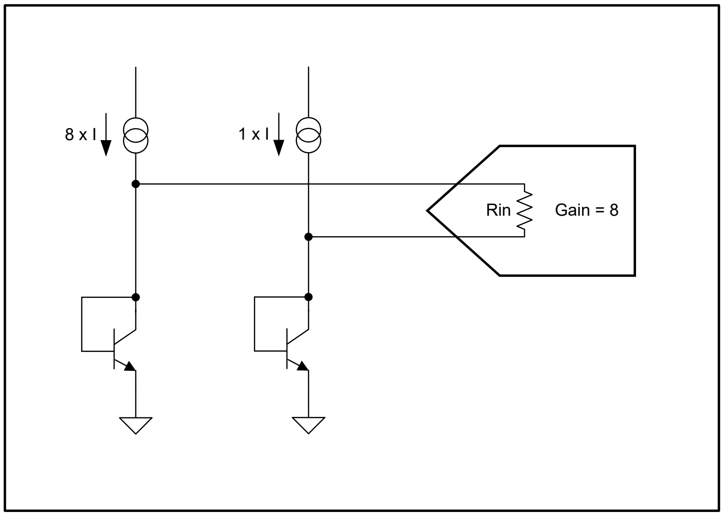


Figure 8-15. Internal Temperature Sensor Block Diagram

For internal temperature sensor mode, use Equation 7 to calculate the device temperature from the ADC conversion result on channel 2.

$$Temperature\ (°C) = 25°C + \frac{ConversionResult(mV) - 80.45\ mV}{0.277\ mV}\ °C \quad (7)$$

8.3.15.2 External Temperature Sensor

Set the TS_EN bit in the CH2_CFG register to 1b, and the TS_SEL bit in the CH2_CFG register to 1b to select the external temperature sensor mode. Set the PGAGAIN2[2:0] bits in the GAIN register to 000b (gain of 1) when using the external temperature sensor. In this mode, the ADC for channel 2 measures the voltage between the AIN2P and AIN12N pins (channel 2 input), as shown in Figure 8-16, for sensing an external temperature sensor (such as a PTC or NTC element).

The PTC or NTC element is powered from the secondary (high-side) supply that is generated by the onboard DC/DC converter and therefore exhibits supply variations. As shown in Figure 8-16, to eliminate supply variations and enable a ratiometric measurement, the ADC reference input for channel 2 in external temperature sensor mode is connected to a voltage Vref_R derived from the secondary (high-side) supply HLDO_OUT using a resistor divider R1 and R2. This reference selection is different from the internal temperature sensor mode and the normal ADC conversion mode, because in both modes the ADC is measured with respect to the internal reference V_{REF} of 1.2 V. R1 and R2 are selected so that Vref_R is also typically 1.2 V.

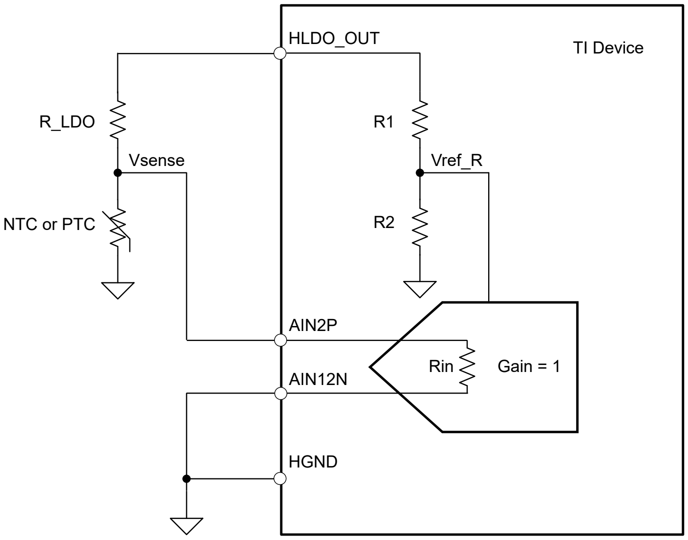


Figure 8-16. External Temperature Sensor Measurement Block Diagram

Equation 8 and Equation 9 determine the external temperature by measuring the temperature-dependent resistance of the NTC or PTC element, assuming a gain of 1.

$$ConversionResult = \frac{Vsens}{Vref\_R} = \frac{R_{NTC}}{R_{NTC} + R_{LDO}} \cdot \frac{R_1 + R_2}{R_2} \tag{8}$$

$$R_1 = 320\ k\Omega,\ R_2 = 240\ k\Omega,\ \frac{R_1 + R_2}{R_2} = 2.33 \tag{9}$$

In Equation 8, *ConversionResult* is expressed in units ranging from 0 (zero-scale) to 1.0 (full-scale). To obtain *ConversionResult* from the decimal ADC code, divide the ADC code by 2^{23}.

$$ConversionResult = ADC\_CODE / 2^{23} \tag{10}$$

Equation 8 can be transformed into Equation 11, which calculates the temperature-dependent resistance of the NTC or PTC element from the ADC conversion result on channel 2.

$$R_{NTC} = \frac{R_{LDO} \cdot ConversionResult}{\frac{R_1 + R_2}{R_2} - ConversionResult} = \frac{R_{LDO} \cdot ConversionResult}{2.33 - ConversionResult} \tag{11}$$

Equation 11 illustrates that the measurement of the NTC or PTC resistance is independent from the secondary (high-side) supply voltage and is therefore ratiometric, eliminating any errors from variation of the supply voltage.

8.3.15.3 Clock Selection for Temperature Sensor Operation

The modulator clock MOD_CLK for each ADC is derived from the external clock provided at the CLKIN pin by a user-controlled programmable clock divider, as described in the *Clocking and Power Modes* section. By default, the clock provided at the CLKIN pin is divided by N_{DIV} = 2 to generate a 50% duty cycle internal modulator clock MOD_CLK. The divider ratio N_{DIV} can be changed to values of 4, 8, and 12 using the CLK_DIV[1:0] bits in the CLOCK register.

When in temperature sensor mode, MOD_CLK is further divided by a factor of 32 and used as the modulator clock for channel 2 that converts the temperature readings on channel 2. However, the modulators on channel 0 and channel 1 are still controlled by the undivided MOD_CLK, as defined by the CLK_DIV[1:0] bits in the CLOCK register.

Table 8-8 shows the MOD_CLK for each ADC channel when operating in temperature sensor mode and in normal mode.

Table 8-8. Modulator Clock Selection for Normal ADC Mode and Temperature Sensor Mode

TS_EN	CLK_DIV[1:0]	N_{DIV} FOR MOD_CLK		
		CHANNEL 0	CHANNEL 1	CHANNEL 2
		AIN0N, AIN0P	AIN12N, AIN1P	AIN12N, AIN2P
0b	00b	2	2	2
0b	01b	4	4	4
0b	10b	8	8	8
0b	11b	12	12	12
1b	00b	2	2	64
1b	01b	4	4	128
1b	10b	8	8	256
1b	11b	12	12	384

As explained in the *Temperature Sensor* section, the ADC conversion rate is reduced for the temperature sensor mode by a factor 32.

8.3.16 General-Purpose Digital Output (GPO)

The AIN2P/GPO pin can be configured as a general-purpose output by setting the GPO_EN bit in the CFG register to 1b. The GPO pin uses logic levels based on the HLDO_OUT supply. See the *Electrical Characteristics* table for details regarding the logic high and low levels.

Use the GPO_DAT bit in the CFG register to drive a logic high or low level on the AIN2P/GPO pin when configured as a digital output. The GPO output is push-pull. The value written to the GPO_DAT bit is ignored when the AIN2P/GPO is configured as an analog input.

8.4 Device Functional Modes

Figure 8-17 shows a state diagram depicting the major functional modes of the AMC130M03 and the transitions between them.

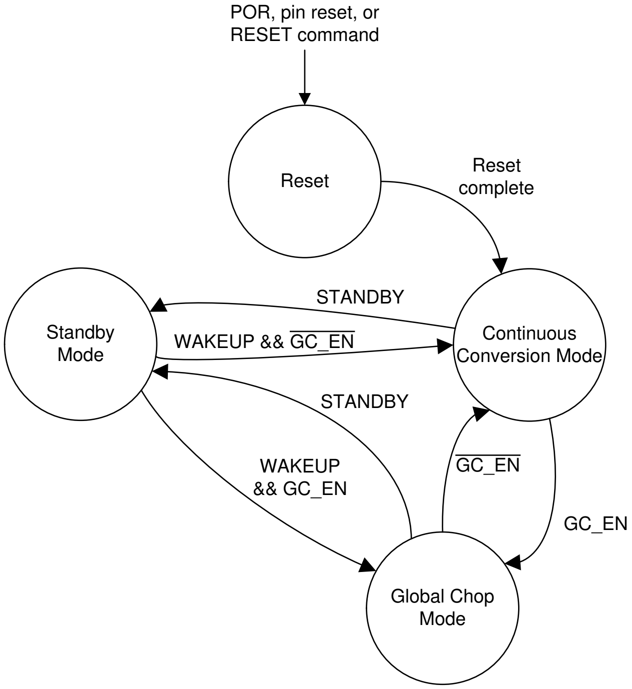


Figure 8-17. State Diagram Depicting Device Functional Modes

8.4.1 Power-Up and Reset

The AMC130M03 is reset in one of three ways: by a power-on reset (POR), by the $\overline{\text{SYNC/RESET}}$ pin, or by a RESET command. After a reset occurs, the configuration registers are reset to the default values. Therefore, the DC/DC converter is disabled when a reset occurs. The internal DC/DC converter must be enabled after any type of reset for the device to begin generating conversion data, such as the power-on-reset, or a reset using a RESET command, or a reset using the $\overline{\text{SYNC/RESET}}$ pin.

8.4.1.1 Power-On Reset

Power-on reset (POR) is the reset that occurs when a valid supply voltage is first applied. The POR process requires t_{POR} from when the supply voltages reach 90% of the nominal value. Internal circuitry powers up and the registers are set to the default state during this time. The $\overline{\text{DRDY}}$ pin transitions from low to high immediately after t_{POR}, indicating the SPI interface is ready for communication. The device ignores any SPI communication before this point.

See the *Start-Up Behavior After Power-Up* section for a recommended procedure to ensure a correct start-up behavior at power-up.

8.4.1.2 $\overline{\text{SYNC/RESET}}$ Pin

The $\overline{\text{SYNC/RESET}}$ pin is an active low, dual-function pin that generates a reset if the pin is held low longer than $t_{w(RSL)}$. The device maintains a reset state until $\overline{\text{SYNC/RESET}}$ is returned high. The host must wait for at least t_{REGACQ} after $\overline{\text{SYNC/RESET}}$ is brought high before communicating with the device with SPI. Follow the procedure described in the *Start-Up Behavior After a Pin Reset or RESET Command* section after the device is reset.

8.4.1.3 RESET Command

The AMC130M03 can be reset with the SPI RESET command (0011h).

The device communicates in frames of a fixed length. See the *SPI Communication Frames* section for details regarding SPI data framing on the AMC130M03. The RESET command is transmitted in the first word of the data frame on DIN, but the command is not latched and executed by the device until the entire frame is complete. Terminating the frame early causes the RESET command to be ignored. Five words are required to complete a frame on the AMC130M03.

A reset occurs immediately after the command is latched. The host must wait for t_{REGACQ} before communicating with the device to make sure the registers have assumed the default settings. Follow the procedure described in the *Start-Up Behavior After a Pin Reset or RESET Command* section after the device is reset.

8.4.2 Start-Up Behavior After Power-Up

The AMC130M03 does not generate conversion data automatically after power-up because the integrated DC/DC converter is disabled initially. For the ADC to operate, the DC/DC converter must be enabled after power-up, and a stable supply voltage at the HLDO_OUT pin must be established that serves as the power supply for the circuitry on the secondary (high) side.

A recommended procedure for powering up the AMC130M03 is described in this section. Figure 8-18 depicts a timing diagram for the device behavior when this recommended sequence is used. Figure 8-19 provides a flow diagram that displays the recommended sequence in a graphical form.

Follow these steps to ensure a correct start-up behavior at power-up:

- Power up the DVDD supply.
- The transition of $\overline{\text{DRDY}}$ from low to high indicates a valid supply voltage on the primary side is established, and also indicates the SPI interface is ready for communication.
- Configure the clock divider by setting the CLK_DIV[1:0] bits in the CLOCK register as needed.
- Configure the modulator clock frequency by setting the DCDC_FREQ[3:0] bits in the DCDC_CTRL register; see the *Clocking and Power Modes* section for details.
- Enable the DC/DC converter by setting the DCDC_EN bit in the DCDC_CTRL register to 1b.
- Configure all other registers of the AMC130M03 before the external clock is applied to the CLKIN pin.
- Provide the main clock at the CLKIN input to start operation of the integrated DC/DC converter, and to make sure that the secondary power supply at the HLDO_OUT pin is generated.
- The transition of the SEC_FAIL bit in the STATUS register from high to low indicates that the secondary power supply at the HLDO_OUT pin is established and the ADC conversion data output is valid. Confirm device operation by reading the SEC_FAIL bit, and verify that this bit is set to 0b, before reading any conversion data from the ADC. There are two options for reading the SEC_FAIL bit in the STATUS register: sending a NULL command results in a response including the STATUS word, or sending a register read command to read the STATUS register. The SEC_FAIL bit is a latched bit; therefore, at least two read commands are required to confirm that this bit transitioned from high to low; the first read command clears the logic high value that is latched during device power-up. Use the second read command to verify that the SEC_FAIL bit is set to 0b, indicating that the secondary supply is valid. If the SEC_FAIL bit still reads 1b as a result of the second read command, continue reading the SEC_FAIL bit until this bit reads 0b before reading any conversion data from the ADC.

Regarding the conversion data after power-up, pay attention to the following:

- The high-to-low transition of $\overline{\text{DRDY}}$ indicates that new conversion data are available. As given in Figure 8-18, ADC data are only valid if the SEC_FAIL reads 0b during the conversion period. The first two conversion results shown in Figure 8-18, represent invalid data.
- When the ADC generates valid data, the digital filter must settle, as described in the *SINC^3 and SINC^3 + SINC^1 Filter* section. Two subsequent conversion results illustrated in Figure 8-18 are unsettled (assuming OSR equals 1024), and the last conversion result shown provides valid and settled data.
- For best control of the conversion timing, especially in a system where multiple devices of the AMC130M03 are used, trigger a synchronization using the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin before the host collects conversion data from the ADC. See the *Synchronization* section for more details regarding how to synchronize the device.

In Figure 8-18, t_{POR_SEC} is the time from enabling the DC/DC converter to the first falling edge of the SEC_FAIL bit, which indicates that the secondary power supply at the HLDO_OUT pin is stable. t_{POR_DVDD} is the time from DVDD supply at 90% to $\overline{\text{DRDY}}$ first rising edge.

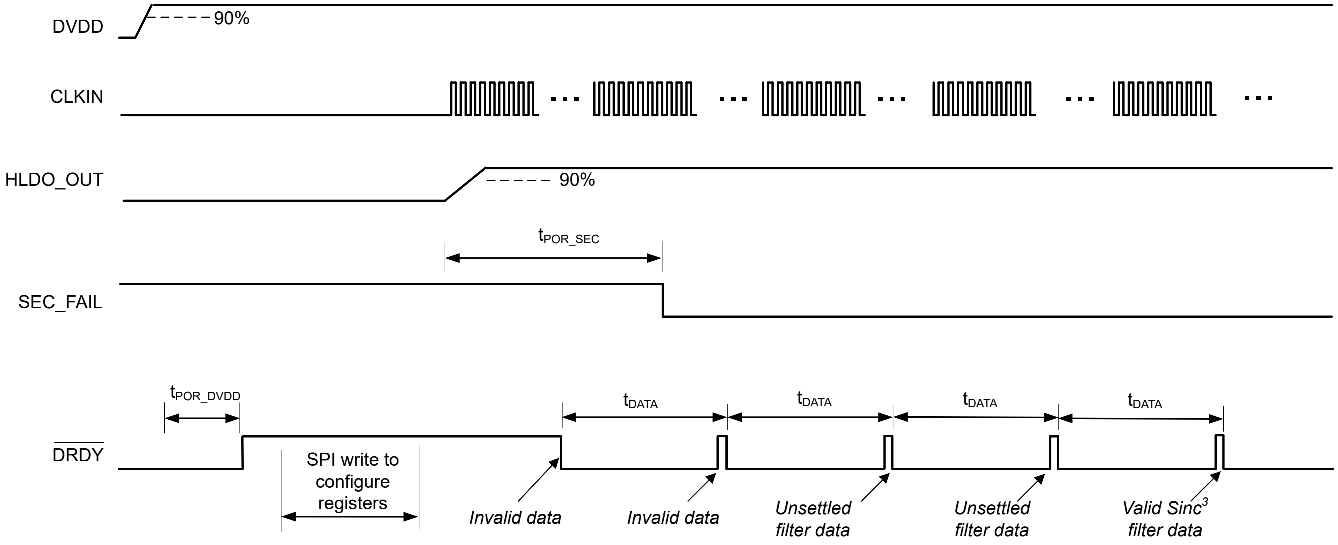


Figure 8-18. Start-Up Behavior at Power-Up and Settling Times, OSR = 1024

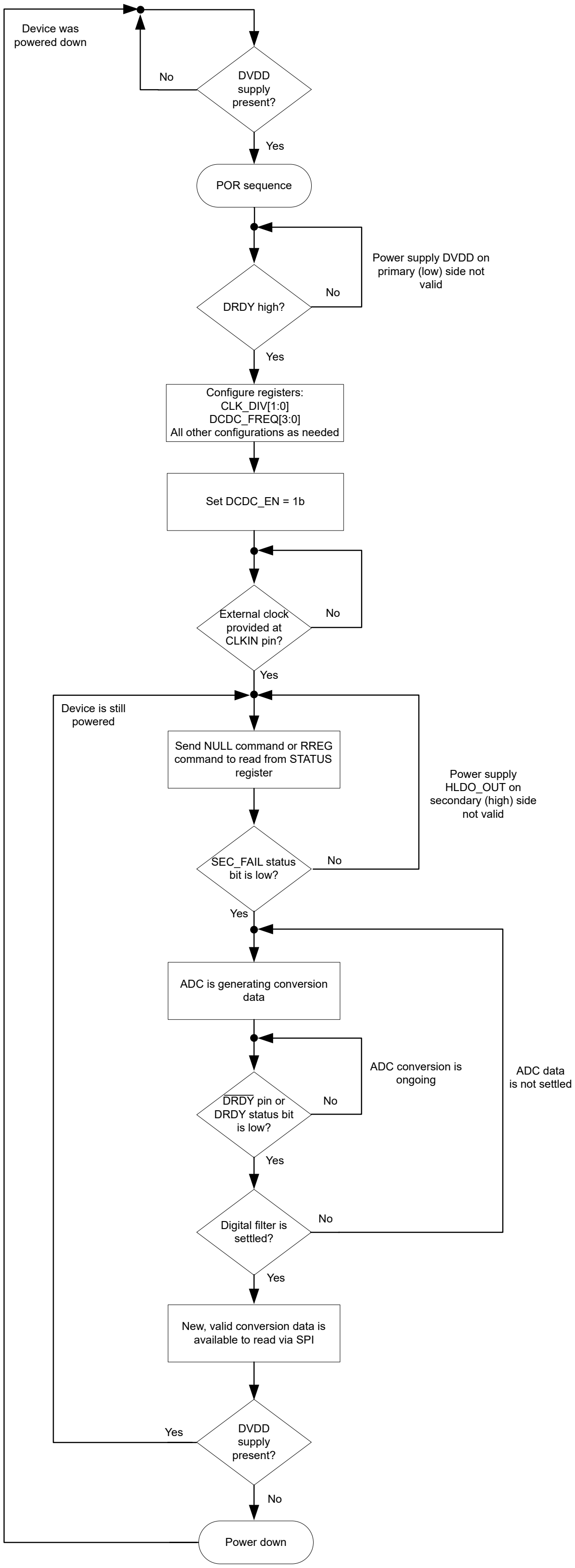


Figure 8-19. Flow Diagram for Start-Up Procedure at Power-Up

8.4.3 Start-Up Behavior After a Pin Reset or RESET Command

Sending a RESET command or executing a pin reset using the SYNC/RESET pin disables the DC/DC converter by resetting the DCDC_EN bit to 0b. Therefore, the start-up process following a RESET command or a pin reset using the SYNC/RESET pin is similar to what occurs after power up. However, there is no t_{POR_DVDD} in the case of a command or pin reset because the DVDD supply is already ramped.

Figure 8-20 shows the behavior after a pin reset using the SYNC/RESET pin. A reset is only generated if the SYNC/RESET pin is held low longer than $t_{w(RSL)}$. If the pin is held low for a duration less then $t_{w(RSL)}$ but greater than a CLKIN period, a synchronization occurs instead of a reset.

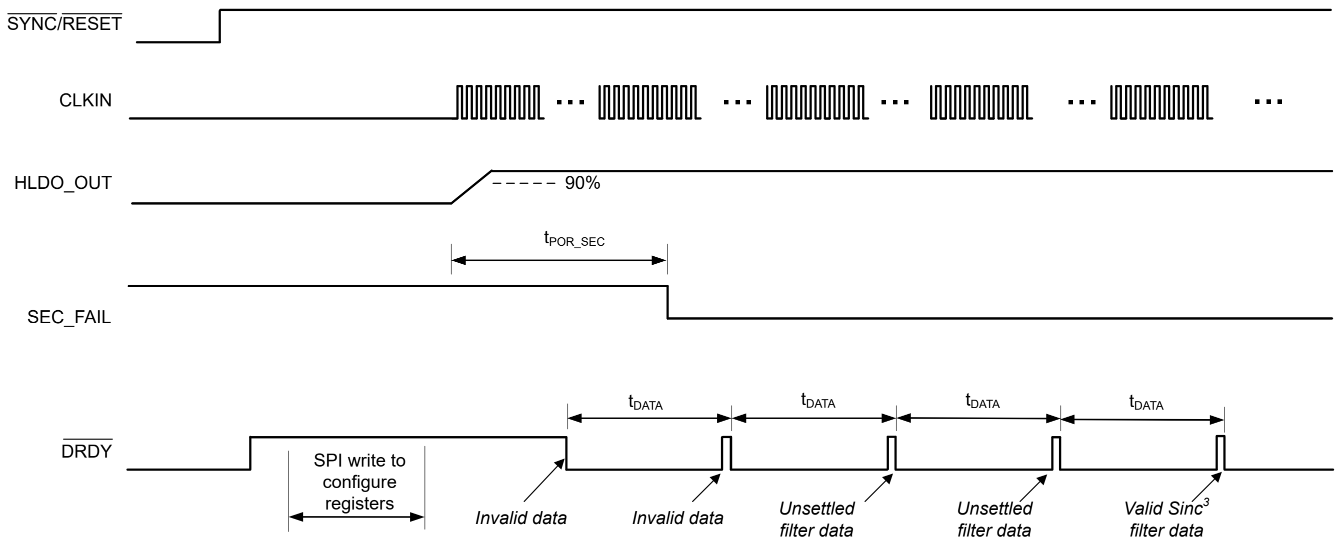


Figure 8-20. Start-Up Behavior After a Pin Reset and Settling Times

As shown in Figure 8-20, follow the same sequence for configuring the device and reading the SEC_FAIL bit in the STATUS register as described in the *Start-Up Behavior After Power-Up* section to receive valid conversion data after a RESET command or a pin reset using the SYNC/RESET pin.

8.4.4 Start-Up Behavior After a Pause in CLKIN

A pause in the clock signal provided at the CLKIN pin causes the power supply generated by the DC/DC converter on the secondary (high) side to drop and can prevent the ADC circuit on the secondary side from operating. The DC/DC converter is automatically re-enabled when the clock at the CLKIN pin resumes, and the AMC130M03 registers do not need to be reconfigured. However, the supply voltage on the secondary (high) side is not stable until the SEC_FAIL bit in the STATUS register is set to 0b.

Follow the same sequence for reading the SEC_FAIL bit in the STATUS register as described in the *Start-Up Behavior After Power-Up* section to receive valid conversion data after the clock has been paused and re-started at the CLKIN pin.

8.4.5 Synchronization

Synchronization can be performed by the host to make sure the ADC conversions are synchronized to an external event. For example, synchronization can realign the data capture to the expected timing of the host if a glitch on the clock causes the host and device to become out of synchronization.

The SYNC/RESET pin is a multifunction digital input pin that allows the host to synchronize conversions to an external event or to reset the device. See the *SYNC/RESET Pin* section for more details regarding how the device is reset.

Provide a negative pulse on the SYNC/RESET pin with a duration less than $t_{w(RSL)}$ but greater than a CLKIN period to trigger synchronization. The device internally compares the leading negative edge of the SYNC/RESET pulse to the internal clock that tracks the data rate. The internal data rate clock has timing equivalent to the DRDY pin if configured to assert with a phase calibration setting of 0b. If the negative edge on SYNC/RESET aligns with the internal data rate clock, the device is determined to be synchronized and therefore no action is taken. If there is misalignment, the digital filters on the device are reset to be synchronized with the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pulse.

Figure 8-21 shows the behavior after a synchronization pulse on the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin for OSR = 1024. As explained in the *SINC^3 and SINC^3 + SINC^1 Filter* section, because of the settling of the digital filter, the first two conversion results are unsettled data and must be ignored.

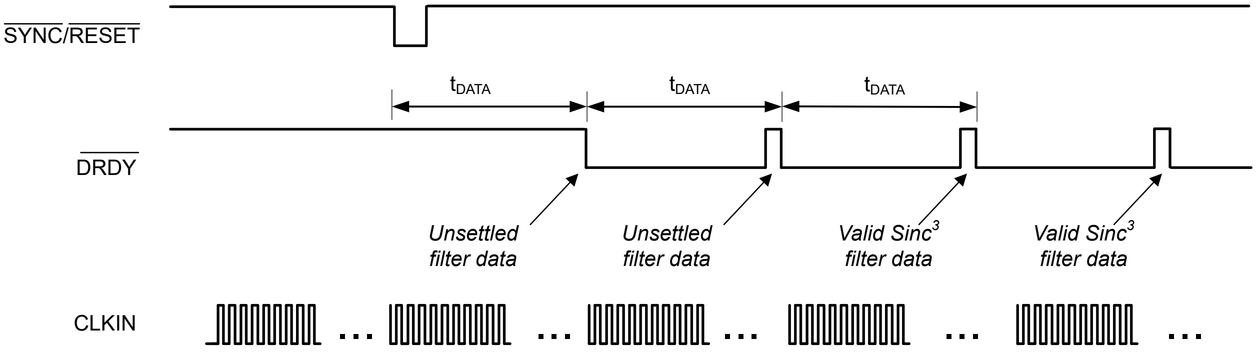


Figure 8-21. Synchronization Timing for OSR = 1024

In global-chop mode, conversions are always immediately restarted at the falling edge of the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ pin.

The phase calibration settings on all channels are retained during synchronization. Thus, channels with non-zero phase calibration settings generate conversion results less than a data rate period after the synchronization event occurs. However, the results are not settled until the respective channels have at least three conversion cycles for the sinc^3 filter to settle.

8.4.6 Conversion Modes

There are two ADC conversion modes on the AMC130M03: continuous-conversion and global-chop mode. Continuous-conversion mode is a mode where ADC conversions are generated constantly by the ADC at a rate defined by f_{MOD} / OSR. Global-chop mode differs from continuous-conversion mode because global-chop periodically chops (or swaps) the inputs, which reduces system offset errors at the cost of settling time between the points when the inputs are swapped. In either continuous-conversion or global-chop mode, there are two power modes that provide flexible options to scale power consumption with bandwidth and dynamic range. The *Power Modes* section discusses these power modes in further detail.

8.4.6.1 Continuous-Conversion Mode

Continuous-conversion mode is the mode in which ADC data are generated constantly at the rate of f_{MOD} / OSR. New data are indicated by a $\overline{\text{DRDY}}$ falling edge at this rate. Continuous-conversion mode is intended for measuring AC signals because this mode allows for higher output data rates than global-chop mode.

8.4.6.2 Global-Chop Mode

The AMC130M03 incorporates a global-chop mode option to reduce offset error and offset drift inherent to the device resulting from mismatch in the internal circuitry to very low levels. When global-chop mode is enabled by setting the GC_EN bit in the GLOBAL_CHOP_CFG register, the device uses the conversion results from two consecutive internal conversions taken with opposite input polarity to cancel the device offset voltage. Conversion n is taken with normal input polarity. The device then reverses the internal input polarity for conversion $\overline{n + 1}$. The average of two consecutive conversions (n and $\overline{n + 1}$, $\overline{n + 1}$ and $n + 2$, and so on) yields the final offset compensated result.

Figure 8-22 shows a block diagram of the global-chop mode implementation. The combined PGA and ADC internal offset voltage is modeled as V_{OFS}. Only this device-inherent offset voltage is reduced by global-chop mode. Offset in the external circuitry connected to the analog inputs is not affected by global-chop mode.

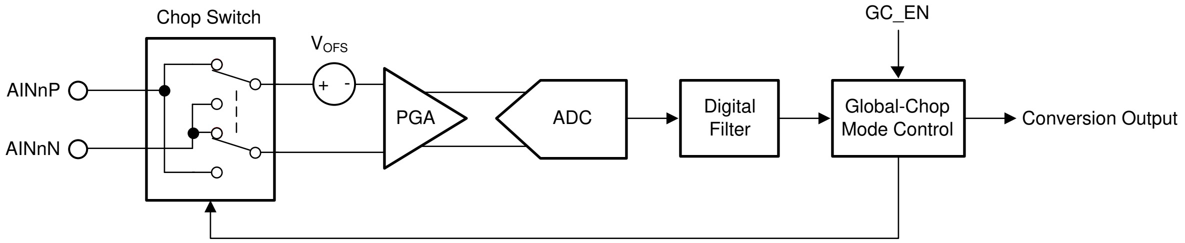


Figure 8-22. Global-Chop Mode Implementation

The conversion period in global-chop mode differs from the conversion time when global-chop mode is disabled (t_{DATA} = OSR × t_{MOD}). Figure 8-23 shows the conversion timing for an ADC channel using global-chop mode.

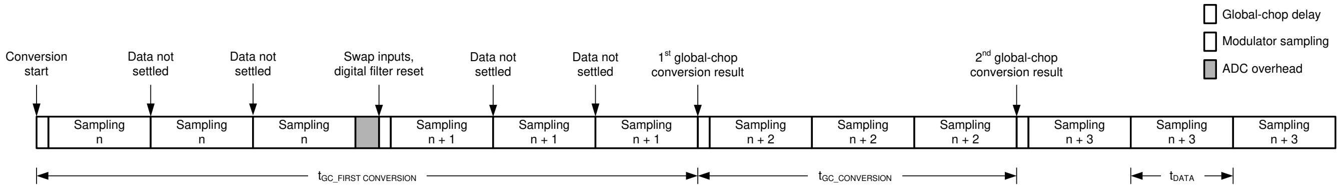


Figure 8-23. Conversion Timing With Global-Chop Mode Enabled

Every time the device swaps the input polarity, the digital filter is reset. The ADC then always takes three internal conversions to produce one settled global-chop conversion result.

The AMC130M03 provides a programmable delay (t_{GC_DLY}) between the end of the previous conversion period and the beginning of the subsequent conversion period after the input polarity is swapped. This delay allows external input circuitry to settle because the chopping switches interface directly with the analog inputs. The GC_DLY[3:0] bits in the GLOBAL_CHOP_CFG register configure the delay after chopping the inputs. The global-chop delay is selected in terms of modulator clock periods from 2 to 65,536 × t_{MOD}.

The effective conversion period in global-chop mode follows Equation 12. A $\overline{\text{DRDY}}$ falling edge is generated each time a new global-chop conversion becomes available to the host.

The conversion process of all ADC channels in global-chop mode is restarted in the following two conditions so that all channels start sampling at the same time:

- Falling edge of the $\overline{\text{SYNC/RESET}}$ pin
- Change of the OSR setting

The conversion period of the first conversion after the ADC channels are reset is considerably longer than the conversion period of all subsequent conversions mentioned in Equation 12 because the device must first perform two fully settled internal conversions with the input polarity swapped. The conversion period for the first conversion in global-chop mode follows Equation 13.

$$t_{GC\_CONVERSION} = t_{GC\_DLY} + 3 \times OSR \times t_{MOD} \quad (12)$$

$$t_{GC\_FIRST\_CONVERSION} = t_{GC\_DLY} + 3 \times OSR \times t_{MOD} + t_{GC\_DLY} + 3 \times OSR \times t_{MOD} + 44 \times t_{MOD} \quad (13)$$

Using global-chop mode reduces the ADC noise listed in Table 7-1 at a given OSR by a factor of $\sqrt{2}$ because two consecutive internal conversions are averaged to yield one global-chop conversion result. The DC test signal cannot be measured in global-chop mode.

Phase calibration is automatically disabled in global-chop mode.

8.4.7 Power Modes

In both continuous-conversion and global-chop mode, there are two selectable power modes that allow scaling of power with bandwidth and performance: high-resolution (HR) mode and low-power (LP) mode. The mode is selected by the PWR[1:0] bits in the CLOCK register. Changing the PWR[1:0] bits scales the internal bias currents to achieve the expected power levels. See the *Recommended Operating Conditions* table for restrictions on the CLKIN frequency for each power mode.

8.4.8 Standby Mode

Standby mode is a low-power state in which all channels are disabled, and the reference and other non-essential circuitry are powered down. This mode differs from completely powering down the device because the device retains the register settings. Set the DCDC_EN bit in the DCDC_CTRL register to 0b to disable the DC/DC converter before entering standby mode. Enter standby mode by sending the STANDBY command (0022h). Stop toggling CLKIN when the device is in standby mode to minimize device power consumption. Exit standby mode by sending the WAKEUP command (0033h).

8.5 Programming

8.5.1 Serial Interface

The AMC130M03 uses an SPI-compatible interface to configure the device and retrieve conversion data. The device always acts as an SPI peripheral; SCLK and CS are inputs to the interface. The interface operates in SPI mode 1, where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the controller and peripheral on SCLK falling edges. The interface is full-duplex, meaning data can be sent and received simultaneously by the interface. The device includes the typical SPI signals: SCLK, CS, DIN, and DOUT. In addition, there are two other digital pins that provide functionality. The DRDY pin serves as a flag to the host to indicate new conversion data are available. The SYNC/RESET pin is a dual-function pin that allows synchronization of conversions to an external event and allows for a hardware device reset.

8.5.1.1 Chip Select (CS)

The CS pin is an active low input signal that selects the device for communication. The device ignores any communication and DOUT is high impedance when CS is held high. Hold CS low for the duration of a communication frame to ensure proper communication. The interface is reset each time CS is taken high.

8.5.1.2 Serial Data Clock (SCLK)

The SCLK pin is an input that serves as the serial clock for the interface. Output data on the DOUT pin transitions on the rising edge of SCLK and input data on DIN are latched on the falling edge of SCLK.

8.5.1.3 Serial Data Input (DIN)

The DIN pin is the peripheral in, controller out (PICO) pin for the device. Serial commands are shifted in through the DIN pin by the device with each SCLK falling edge when the CS pin is low.

8.5.1.4 Serial Data Output (DOUT)

The DOUT pin is the peripheral out, controller in (POCI) pin for the device. The device shifts out command responses and ADC conversion data serially with each rising SCLK edge when the CS pin is low. This pin assumes a high-impedance state when CS is high.

8.5.1.5 Data Ready (DRDY)

The DRDY pin is an active-low output that indicates when new conversion data are ready in conversion mode. Connect the DRDY pin to an input on the host to trigger periodic data retrieval in conversion mode. The period between each DRDY falling edge is the data rate period.

The timing of DRDY with respect to the sampling of a given channel on the AMC130M03 depends on the phase calibration setting of the channel and the state of the DRDY_SEL[1:0] bits in the MODE register. Setting the DRDY_SEL[1:0] bits to 00b configures DRDY to assert when the channel with the largest positive phase calibration setting, or the most lagging, has a new conversion result. When the bits are 01b, the device asserts

DRDY each time any channel data are ready. Finally, setting the bits to either 10b or 11b configures the device to assert DRDY when the channel with the most negative phase calibration setting, or the most leading, has new conversion data. Changing the DRDY_SEL[1:0] bits has no effect on DRDY behavior in global-chop mode because phase calibration is automatically disabled in global-chop mode.

The timing of the first DRDY assertion after channels are enabled or after a synchronization pulse is provided depends on the phase calibration setting. If the channel that causes DRDY to assert has a phase calibration setting less than zero, the first DRDY assertion can be less than one sample period from the channel being enabled or the occurrence of the synchronization pulse. However, DRDY asserts in the next sample period if the phase setting puts the output timing too close to the beginning of the sample period.

Table 8-9 lists the phase calibration setting boundary at which DRDY either first asserts within a sample period, or in the next sample period. If the setting for the channel configured to control DRDY assertion is greater than the value listed in Table 8-9 for each OSR, DRDY asserts for the first time within a sample period of the channel being enabled or the synchronization pulse. If the phase setting value is equal to or more negative than the value in Table 8-9, DRDY asserts in the following sample period. See the *Synchronization* section for more information about synchronization.

Table 8-9. Phase Setting First DRDY Assertion Boundary

OSR	PHASE SETTING BOUNDARY	PHASEn[9:0] BIT SETTING BOUNDARY
128	–19	3EDh
256	–83	3ADh
512	–211	32Dh
1024	–467	22Dh
>1024	None	N/A

The DRDY_HIZ bit in the MODE register configures the state of the DRDY pin when deasserted. By default the bit is 0b, meaning the pin is actively driven high using a push-pull output stage. When the bit is 1b, DRDY behaves like an open-drain digital output. Use a 10-kΩ pullup resistor to pull the pin high when DRDY is not asserted.

The DRDY_FMT bit in the MODE register determines the format of the DRDY signal. When the bit is 0b, new data are indicated by DRDY changing from high to low and remaining low until either all conversion data are shifted out of the device, or remaining low and going high briefly before the next time DRDY transitions low. When the DRDY_FMT bit is 1b, new data are indicated by a short negative pulse on the DRDY pin. If the host does not read conversion data after the DRDY pulse when DRDY_FMT is 1b, the device skips a conversion result and does not provide another DRDY pulse until the second following instance when data are ready because of how the pulse is generated. See the *Collecting Data for the First Time or After a Pause in Data Collection* section for more information about the behavior of DRDY when data are not consistently read.

8.5.1.6 Conversion Synchronization or System Reset (SYNC/RESET)

The SYNC/RESET pin is a multifunction digital input pin that serves primarily to allow the host to synchronize conversions to an external process or to reset the device. See the *Synchronization* section for more details regarding the synchronization function. See the *SYNC/RESET Pin* section for more details regarding how the device is reset.

8.5.1.7 SPI Communication Frames

SPI communication on the AMC130M03 is performed in frames. Each SPI communication frame consists of several words. The word size is configurable as either 16, 24, or 32 bits by programming the WLENGTH[1:0] bits in the MODE register.

The interface is full duplex, meaning that the interface is capable of transmitting data on DOUT while simultaneously receiving data on DIN. The input frame that the host sends on DIN always begins with a command. The first word on the output frame that the device transmits on DOUT always begins with the response to the command that was sent in the previous input frame.

The number of words in a command depends on the command provided. For most commands, there are five words in a frame. On DIN, the host provides the command, the command CRC if input CRC is enabled or a word of zeros if input CRC is disabled, and three additional words of zeros. Simultaneously on DOUT, the device outputs the response from the previous frame command, three words of ADC data representing the three ADC channels, and a CRC word. If one or several of the ADC channels are disabled, this frame structure of five words still applies, and the data of disabled channels reads all zeros. Figure 8-24 shows a typical command frame structure.

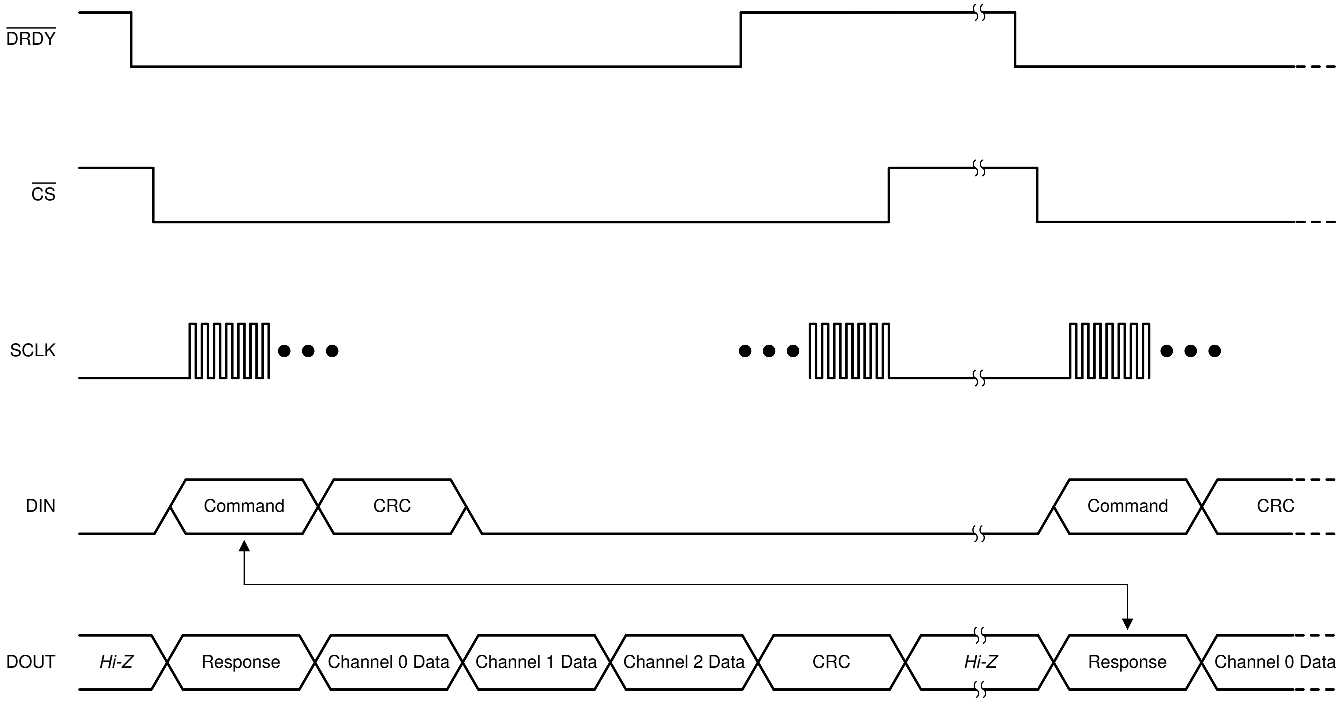


Figure 8-24. Typical Communication Frame

There are some commands that require more than five words. In the case of a read register (RREG) command where multiple registers are read, the response to the command contains the acknowledgment of the command followed by the register contents requested, which can require a larger frame depending on how many registers are read. See the *RREG* section for more details on the RREG command.

In the case of a write register (WREG) command where multiple registers are written, the frame extends to accommodate the additional data. See the *WREG* section for more details on the WREG command.

See the *Commands* section for a list of all valid commands and the corresponding responses on the AMC130M03.

Under special circumstances, a data frame can be shortened by the host. See the *Short SPI Frames* section for more information about artificially shortening communication frames.

8.5.1.8 SPI Communication Words

An SPI communication frame with the AMC130M03 is made of words. Words on DIN can contain commands, register settings during a register write, or a CRC of the input data. Words on DOUT can contain command responses, register settings during a register read, ADC conversion data, or the CRC of the output data.

Words can be 16, 24, or 32 bits. The word size is configured by the WLENGTH[1:0] bits in the MODE register. The device defaults to a 24-bit word size. Commands, responses, CRC, and registers always contain 16 bits of actual data. These words are always most significant bit (MSB) aligned, and therefore the least significant bits (LSBs) are zero-padded to accommodate 24- or 32-bit word sizes. ADC conversion data are nominally 16 bits. If the 24 bit word size is used, the eight LSBs of ADC conversion data are zero-padded. There are two options for 32-bit communication available for ADC data that are configured by the WLENGTH[1:0] bits in the MODE register. Either the ADC data can be LSB padded with zeros or the data can be MSB sign extended.

8.5.1.9 Short SPI Frames

The SPI frame can be shortened to only send commands and receive responses if the ADCs are disabled and no ADC data are being output by the device. Read out all expected output data words from each sample period if the ADCs are enabled. Reading all data output with each frame ensures predictable $\overline{\text{DRDY}}$ pin behavior. If reading out all data on each output data period is not feasible, see the *Collecting Data for the First Time or After a Pause in Data Collection* section on how to begin reading data again after a pause from when the ADCs were last enabled.

A short frame is not possible when using the RESET command. A full frame must be provided for a device reset to take place when providing the RESET command.

8.5.1.10 Communication Cyclic Redundancy Check (CRC)

The AMC130M03 features a cyclic redundancy check (CRC) engine on both input and output data to mitigate SPI communication errors. The CRC word is 16 bits wide for either input or output CRC. Coverage includes all words in the SPI frame where the CRC is enabled, including zero-padded or sign-extended bits.

CRC on the SPI input is optional and can be enabled and disabled by writing the RX_CRC_EN bit in the MODE register. Input CRC is disabled by default. The device checks the provided input CRC against the CRC generated based on the input data. A CRC error occurs if the CRC words do not match. The device does not execute any commands, except for the WREG command, if the input CRC check fails. A WREG command always executes even when the CRC check fails. The device sets the CRC_ERR bit in the STATUS register for all cases of a CRC error. The response on the output in the SPI frame following the frame where the CRC error occurred is that of a NULL command, which means the STATUS register plus the conversion data are output in the following SPI frame. The CRC_ERR bit is cleared when the STATUS register is output.

Output CRC is not optional and always appears at the end of the output frame. The host can ignore the data if output CRC is not used.

There are two types of CRC polynomials available: CCITT CRC and ANSI CRC (CRC-16). The CRC setting determines the algorithm for both the input and output CRC. The CRC type is programmed by the CRC_TYPE bit in the MODE register. Table 8-10 lists the details of the two CRC types.

The CRC calculation is initialized with the seed value of FFFFh to detect errors in the event that DIN or DOUT are stuck low.

Table 8-10. CRC Types

CRC TYPE	POLYNOMIAL	BINARY POLYNOMIAL
CCITT CRC	$x^{16} + x^{12} + x^5 + 1$	0001 0000 0010 0001
ANSI CRC	$x^{16} + x^{15} + x^2 + 1$	1000 0000 0000 0101

8.5.1.11 SPI Timeout

The AMC130M03 features an SPI timeout as a means to recover SPI communication, especially in situations where $\overline{\text{CS}}$ is permanently tied low. Enable the SPI timeout using the TIMEOUT bit in the MODE register. When enabled, the entire SPI frame (first SCLK to last SCLK) must complete in 2^{15} MCLK cycles, otherwise the SPI logic resets. When a timeout happens, the device starts interpreting the data starting with the next SCLK as a new SPI frame.

8.5.2 ADC Conversion Data Format

The device provides conversion data for each channel at the data rate set by the OSR bits in the CLOCK register. The time when data are available relative to $\overline{\text{DRDY}}$ asserting is determined by the channel phase calibration setting and the DRDY_SEL[1:0] bits in the MODE register when in continuous-conversion mode. All data are available immediately following $\overline{\text{DRDY}}$ assertion in global-chop mode. The conversion status of all channels is available as the DRDY[2:0] bitsin the STATUS register. The STATUS register content is automatically output as the response to the NULL command.

Conversion data are 16 bits. The LSBs are zero padded when operating with a 24-bit or 32-bit word size.

Data are given in binary two's complement format. Use Equation 14 to calculate the size of one code (LSB).

$$1\ \text{LSB} = (2.4 / \text{Gain}) / 2^{16} = +\text{FSR} / 2^{15} \tag{14}$$

A positive full-scale input $V_{IN} \geq +\text{FSR} – 1\ \text{LSB} = 1.2 / \text{Gain} – 1\ \text{LSB}$ produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq –\text{FSR} = –1.2 / \text{Gain}$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

Table 8-11 summarizes the ideal output codes for different input signals.

Table 8-11. Ideal Output Code versus Input Signal

INPUT SIGNAL ($V_{IN} = V_{AINP} – V_{AINN}$)	IDEAL OUTPUT CODE
$\geq$ FSR $(2^{15} – 1) / 2^{15}$	7FFFh
FSR / 2^{15}	0001h
0	0000h
–FSR / 2^{15}	FFFFh
$\leq$ –FSR	8000h

Figure 8-25 shows the mapping of the analog input signal to the output codes.

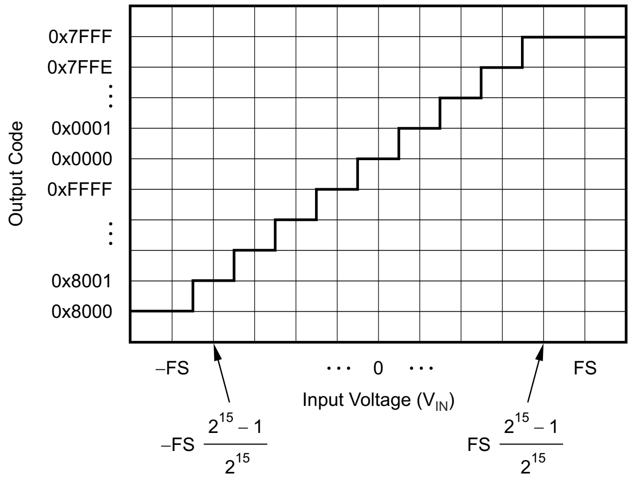


Figure 8-25. Code Transition Diagram

8.5.3 Commands

Table 8-12 contains a list of all valid commands, a short description of the functionality, the binary command word, and the expected response that appears in the following frame.

Table 8-12. Command Definitions

COMMAND	DESCRIPTION	COMMAND WORD	RESPONSE
NULL	No operation	0000 0000 0000 0000	STATUS register
RESET	Reset the device	0000 0000 0001 0001	1111 1111 0010 0011
STANDBY	Place the device into standby mode	0000 0000 0010 0010	0000 0000 0010 0010
WAKEUP	Wake the device from standby mode to conversion mode	0000 0000 0011 0011	0000 0000 0011 0011
LOCK	Lock the interface such that only the NULL, UNLOCK, and RREG commands are valid	0000 0101 0101 0101	0000 0101 0101 0101
UNLOCK	Unlock the interface after the interface is locked	0000 0110 0101 0101	0000 0110 0101 0101
RREG	Read *nnn nnnn* plus 1 registers beginning at address *a aaaa a*	101*a aaaa annn nnnn*	*dddd dddd dddd dddd* or 111*a aaa annn nnnn* (1)
WREG	Write *nnn nnnn* plus 1 registers beginning at address *a aaaa a*	011*a aaaa annn nnnn*	010*a aaaa ammm mmmm* (2)

(1) When *nnn nnnn* is 0, the response is the requested register data *dddd dddd dddd dddd*. When *nnn nnnn* is greater than 0, the response begins with 111*a aaaa annn nnnn*, followed by the register data.

(2) In this case, *mmm mmmm* represents the number of registers that are actually written minus one. This value can be less than *nnn nnnn* in some cases.

8.5.3.1 NULL (0000 0000 0000 0000)

The NULL command is the *no-operation* command that results in no registers read or written, and the state of the device remains unchanged. The intended use case for the NULL command is to read conversion data from the ADC. The command response for the NULL command is the contents of the STATUS register. Any invalid command also gives the NULL response.

8.5.3.2 RESET (0000 0000 0001 0001)

The RESET command resets the ADC to the register defaults. The command is latched by the device at the end of the frame. A reset occurs immediately after the command is latched. The host must wait for t_{REGACQ} after reset before communicating with the device to make sure the registers have assumed the default settings. The device sends an acknowledgment of FF23h when the ADC is properly reset. The device responds with 0011h if the command word is sent but the frame is not completed, and therefore, the device is not reset. See the *RESET Command* section for more information regarding the operation of the reset command. Figure 8-26 illustrates a properly sent RESET command frame.

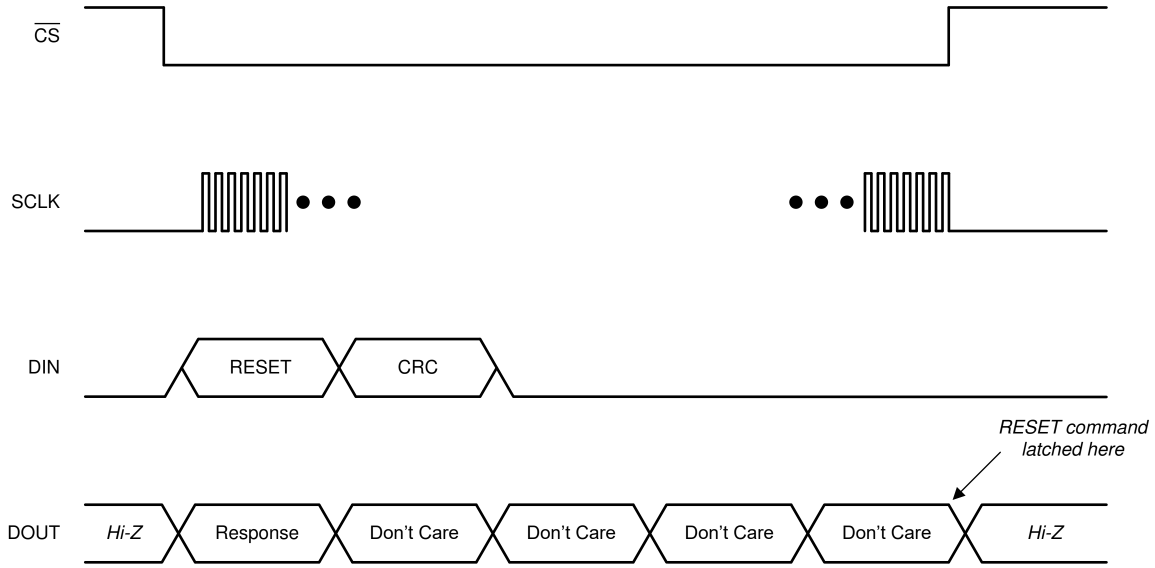


Figure 8-26. RESET Command Frame

8.5.3.3 STANDBY (0000 0000 0010 0010)

The STANDBY command places the device in a low-power standby mode. The command is latched by the device at the end of the frame. The device enters standby mode immediately after the command is latched. Set the DCDC_EN bit in the DCDC_CTRL register to 0b to disable the DC/DC converter before entering standby mode. See the *Standby Mode* section for more information. This command has no effect if the device is already in standby mode.

8.5.3.4 WAKEUP (0000 0000 0011 0011)

The WAKEUP command returns the device to conversion mode from standby mode. This command has no effect if the device is already in conversion mode.

Set the DCDC_EN bit in the DCDC_CTRL register to 1b to enable the DC/DC converter after sending the WAKEUP command.

8.5.3.5 LOCK (0000 0101 0101 0101)

The LOCK command locks the interface, preventing the device from accidentally latching unwanted commands that can change the state of the device. When the interface is locked, the device only responds to the NULL, RREG, and UNLOCK commands. The device continues to output conversion data even when locked.

8.5.3.6 UNLOCK (0000 0110 0101 0101)

The UNLOCK command unlocks the interface if previously locked by the LOCK command.

8.5.3.7 RREG (101a aaaa annn nnnn)

The RREG command reads the device registers. The binary format of the command word is 101*a aaaa annn nnnn*, where *a aaaa a* is the binary address of the register to begin reading and *nnn nnnn* is the unsigned binary number of consecutive registers to read minus one. There are two cases for reading registers on the AMC130M03. When reading a single register (*nnn nnnn* = 000 0000b), the device outputs the register contents in the command response word of the following frame. If multiple registers are read using a single command (*nnn nnnn* > 000 0000b), the device outputs the requested register data sequentially in order of addresses.

8.5.3.7.1 Reading a Single Register

Read a single register from the device by specifying *nnn nnnn* as zero in the RREG command word. As with all SPI commands on the AMC130M03, the response occurs on the output in the frame following the command. Instead of a unique acknowledgment word, the response word is the contents of the register whose address is specified in the command word. Figure 8-27 shows an example of reading a single register.

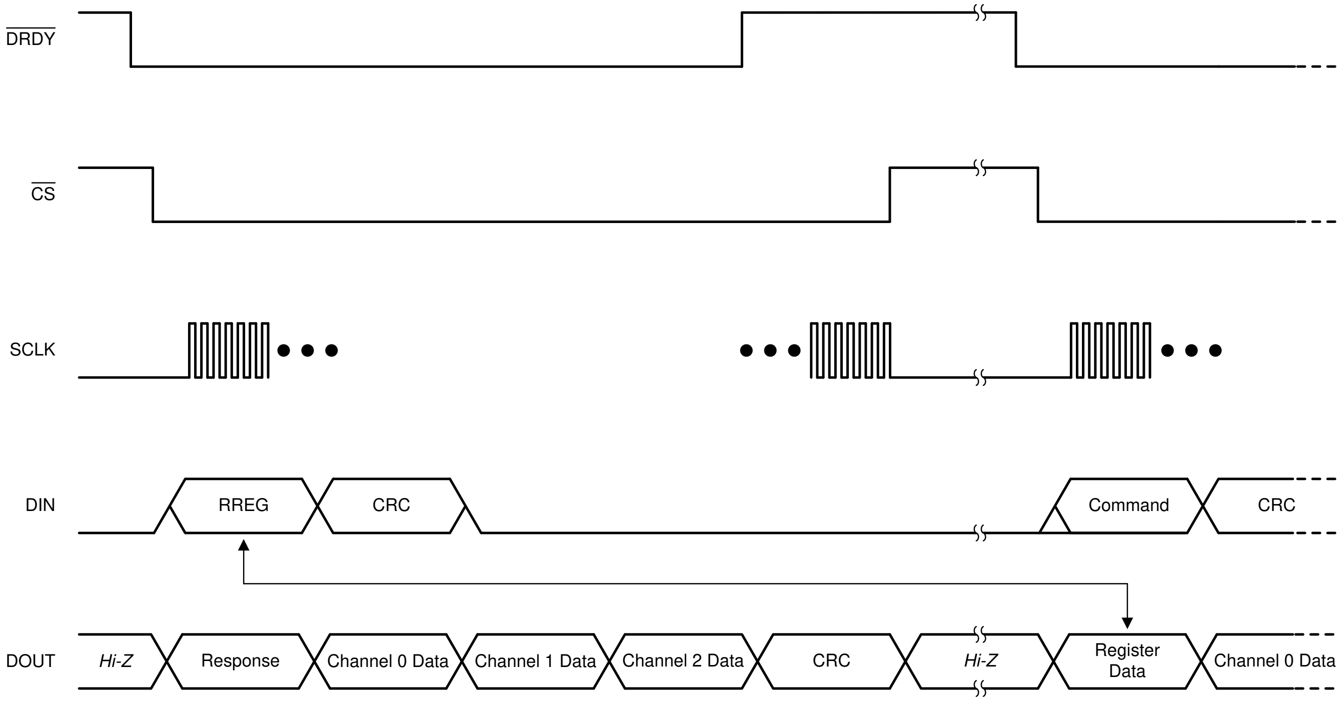


Figure 8-27. Reading a Single Register

8.5.3.7.2 Reading Multiple Registers

Multiple registers are read from the device when *nnn nnnn* is specified as a number greater than zero in the RREG command word. As with all SPI commands on the AMC130M03, the response occurs on the output in the frame following the command. Instead of a single acknowledgment word, the response spans multiple words to shift out all requested registers. Continue toggling SCLK to accommodate outputting the entire data stream. ADC conversion data are not output in the frame following an RREG command to read multiple registers. Figure 8-28 shows an example of reading multiple registers.

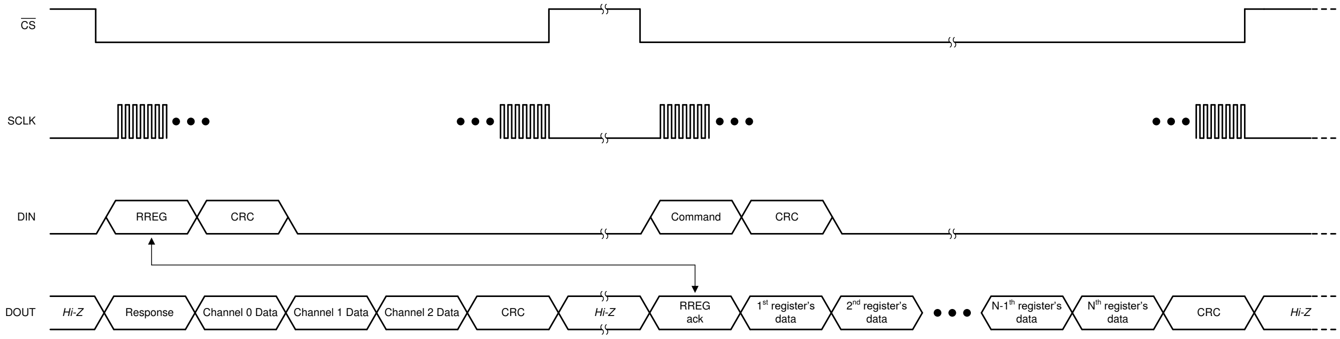


Figure 8-28. Reading Multiple Registers

8.5.3.8 WREG (011a aaaa annn nnnn)

The WREG command allows writing an arbitrary number of contiguous device registers. The binary format of the command word is 011*a aaaa annn nnnn*, where *a aaaa a* is the binary address of the register to begin writing and *nnn nnnn* is the unsigned binary number of consecutive registers to write minus one. Send the data to be written immediately following the command word. Write the intended contents of each register into individual words, MSB aligned.

If the input CRC is enabled, write this CRC after the register data. The registers are written to the device as they are shifted into DIN. Therefore, a CRC error does not prevent an erroneous value from being written to a register. An input CRC error during a WREG command sets the CRC_ERR bit in the STATUS register.

The device ignores writes to read-only registers or to out-of-bounds addresses. Gaps in the register map address space are still included in the parameter *nnn nnnn*, but are not writeable so no change is made to them. The response to the WREG command that occurs in the following frame appears as 010*a aaaa ammm mmmm*, where *mmm mmmm* is the number of registers actually written minus one. This number can be checked by the host against *nnn nnnn* to make sure the expected number of registers are written.

Figure 8-29 shows a typical WREG sequence. In this example, the number of registers to write is larger than the number of ADC channels and, therefore, the frame is extended beyond the ADC channels and output CRC word. Make sure all ADC data and output CRC are shifted out during each transaction where new data are available.

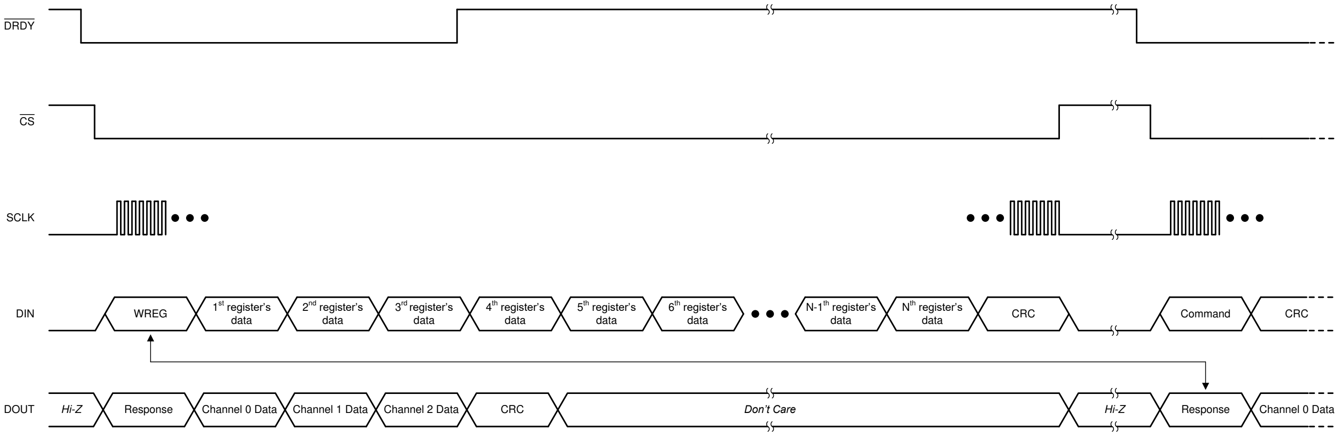


Figure 8-29. Writing Registers

8.5.4 ADC Output Buffer and FIFO Buffer

As shown in Figure 8-30, the AMC130M03 has two internal data buffers per ADC channel holding conversion data: an *ADC output buffer* and a *FIFO buffer*. Each buffer can only hold one conversion result at a time. The data output on DOUT is always from the FIFO buffer.

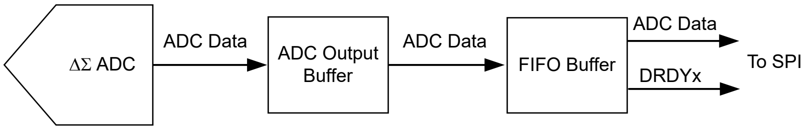


Figure 8-30. ADC Data Output Buffer Structure

Whenever an ADC channel generates new conversion data, the ADC output buffer for that channel is updated immediately with the new data. However, updating the FIFO buffer depends on the previous conversion data retrieval by the host. There are three scenarios:

- If conversion data (N) stored in the FIFO buffer has already been read by the host at the time that new conversion data (N+1) become available, then the FIFO buffer is updated with the new conversion data

(N+1). In this case, data in both the ADC output buffer and the FIFO buffer are updated at the same time (that is, both buffers now hold the same conversion data N+1).

- If conversion data (N) stored in the FIFO buffer has *not* yet been read by the host when new conversion data (N+1) become available, then the FIFO buffer is *not* updated and still holds the previous conversion data (N), while the ADC output buffer now holds the new conversion data (N+1). In this case, data content is different between the ADC output buffer (N+1) and the FIFO buffer (N). After the host reads conversion data N from the FIFO buffer, the FIFO buffer is updated with the conversion data N+1. The host can then retrieve conversion data N+1.
- A special scenario exists if conversion data (N) stored in the FIFO buffer has *not* been read by the host, but *two* new conversion data already became available in the meantime (that is, the ADC output buffer is updated with conversion data N+2). In this case, the FIFO buffer is updated with conversion result N+2 at the same time the ADC output buffer is updated with conversion result N+2 (that is, both buffers now hold the same conversion data N+2). That means, conversion data N and N+1 are lost and cannot be retrieved by the host anymore.

Table 8-13 summarizes the ADC output buffer and FIFO buffer operation when new conversion data (N+1) are available.

Table 8-13. New Conversion Data Available: Operation of the ADC Output Buffer and FIFO Buffer

SPI HISTORY	NEW CONVERSION DATA AVAILABLE AT TIME $t = t_S$	ADC OUTPUT BUFFER CONTENT ($t < t_S$)	FIFO BUFFER CONTENT ($t < t_S$)	ADC OUTPUT BUFFER CONTENT ($t > t_S$)	FIFO BUFFER CONTENT ($t > t_S$)
FIFO data N has been read by the host	N+1	N	N	N+1	N+1
FIFO data N has not yet been read by the host	N+1	N	N	N+1	N
FIFO data N has not yet been read by the host	N+2	N+1	N	N+2	N+2

The following three examples illustrate the behavior of the ADC output and FIFO buffer using a simplified notation to indicate which conversion data is stored in each buffer: [number of sample in the ADC output buffer | number of sample in the FIFO buffer].

Example 1: Host reads conversion results as soon as the results become available

- When the first conversion (result 1) completes, this result is placed both in the ADC output buffer and the FIFO buffer [1 | 1].
- If the host reads conversion result 1 immediately after the conversion completes, the content of the buffers stays at [1 | 1]. The host can read conversion result 1 from the FIFO buffer multiple times if needed before conversion result 2 completes.
- When conversion result 2 completes, the result is again placed into both the ADC output buffer and the FIFO buffer [2 | 2].
- If the host reads the result before the third conversion completes, result 2 is read out and the buffers stay at [2 | 2].

Example 2: Host misses reading one conversion result

- When the first conversion (result 1) completes, the result is placed both in the ADC output buffer and the FIFO buffer [1 | 1].
- If the host misses reading result 1 from the FIFO buffer before the second conversion completes, then the ADC output buffer holds result 2, and the FIFO buffer still holds result 1 [2 | 1].
- If the host now reads data before the third conversion completes, result 1 is read. The content of the buffers then updates to [2 | 2].
- Another conversion data read request by the host shifts out result 2 on DOUT. The buffers stay at [2 | 2].
- Now when the third conversion completes, both buffers update with result 3 [3 | 3].

Example 3: Host misses reading two consecutive conversion results

- When the first conversion (result 1) completes, the result is placed both in the ADC output buffer and the FIFO buffer [1 | 1].

- If the host misses reading result 1 from the FIFO buffer before the second conversion completes, then the ADC output buffer holds result 2, and the FIFO buffer still holds result 1 [2 | 1].
- Now if the third conversion completes and the host still did not retrieve data from the FIFO buffer, then result 3 overwrites the data in both the ADC output and FIFO buffer [3 | 3].
- In this case, both conversion result 1 and result 2 are lost and cannot be read anymore by the host.

Resulting from the internal structure of the ADC, including the ADC output buffer and the FIFO buffer, the DRDY pin behaves as described:

- If conversion data are read by the host every time new conversion data become available, then DRDY follows the format described in the *Data Ready (DRDY)* section, depending on the DRDY_FMT bit in the MODE register: When the DRDY_FMT bit is 0b, new data are indicated by DRDY changing from high to low and remaining low until either all conversion data are shifted out of the device, or remaining low and going high briefly before the next time DRDY transitions low. When the DRDY_FMT bit is 1b, new data are indicated by a short negative pulse on the DRDY pin.
- If the DRDY_FMT bit is 0b and the host does not read conversion data from the FIFO buffer before the next conversion completes, then DRDY remains low and goes high briefly before the next time DRDY transitions low (indicating a new conversion).
- If the DRDY_FMT bit is 1b and the host does not read conversion data from the FIFO buffer before the next conversion completes, then the device skips one DRDY pulse and does not provide another DRDY pulse until the second following instance when data are ready. Therefore, if the DRDY_FMT bit is 1b and the host does not read conversion data at all, the DRDY pin toggles at a rate which is half the conversion rate.

8.5.5 Collecting Data for the First Time or After a Pause in Data Collection

Take special precaution when collecting data for the first time or when beginning to collect data again after a pause. As explained in the *ADC Output Buffer and FIFO Buffer* section, the device contains a first-in-first-out (FIFO) buffer in addition to the ADC output buffer. When the host is reading each consecutive sample from the device, both buffers are updated each time new data are generated, so the DRDY flag in the STATUS register is cleared with each read. However, if data are not read for a period of time, previous samples can be lost as explained in the *ADC Output Buffer and FIFO Buffer* section. Either strobe the SYNC/RESET pin to resynchronize conversions and clear the buffers, or quickly read two data packets when data are read for the first time or after a gap in reading data. This process ensures predictable DRDY pin behavior. See the *Synchronization* section for information about the synchronization feature. These methods do not need to be employed if each channel data is read for each output data period from when the ADC is enabled.

Figure 8-31 shows an example of how to collect data after a period of the ADC running, but where no data are being retrieved. In this instance, the SYNC/RESET pin clears the internal buffers and realigns the AMC130M03 output data with the host.

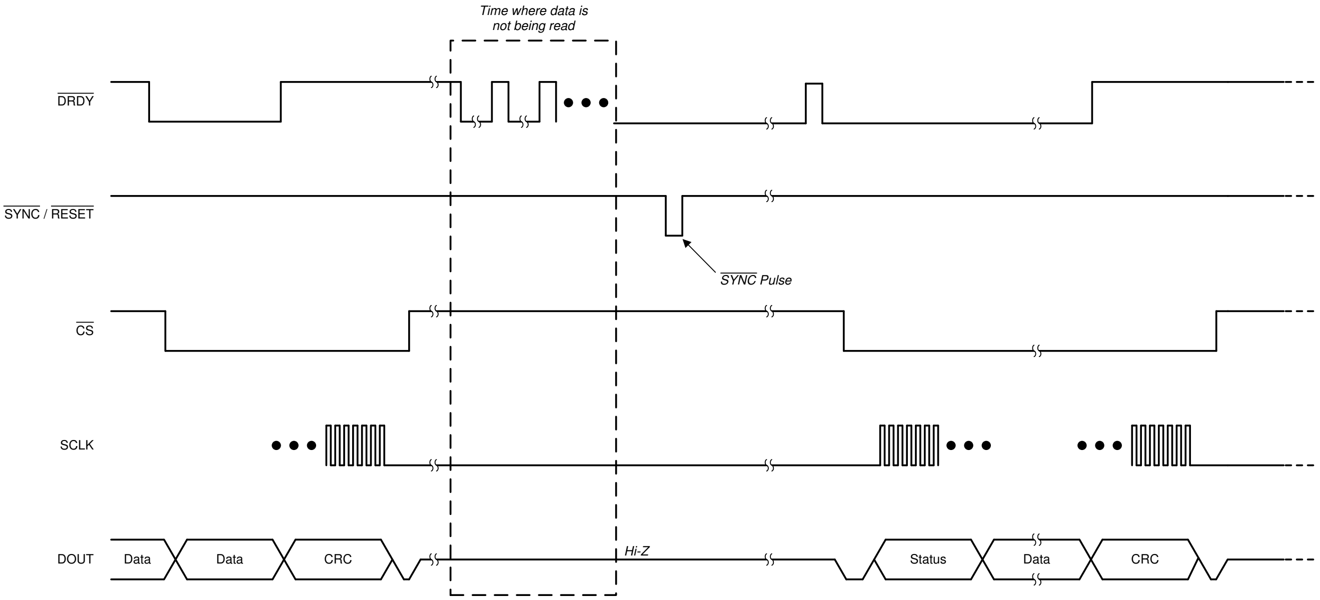


Figure 8-31. Collecting Data After a Pause Using the $\overline{\text{SYNC}}/\overline{\text{RESET}}$ Pin

Another functionally equivalent method for clearing the FIFO after a pause in collecting data is to begin by reading two samples in quick succession. Figure 8-32 shows this method. This example shows that when the DRDY_FMT bit in the MODE register is set to 0b, $\overline{\text{DRDY}}$ is a level output. There is a very narrow pulse on $\overline{\text{DRDY}}$ immediately after the first set of data are shifted out of the device. This pulse can be too narrow for some microcontrollers to detect. Therefore, do not rely upon this pulse but instead immediately read out the second data set after the first data set. The host operates synchronous to the device after the second word is read from the device.

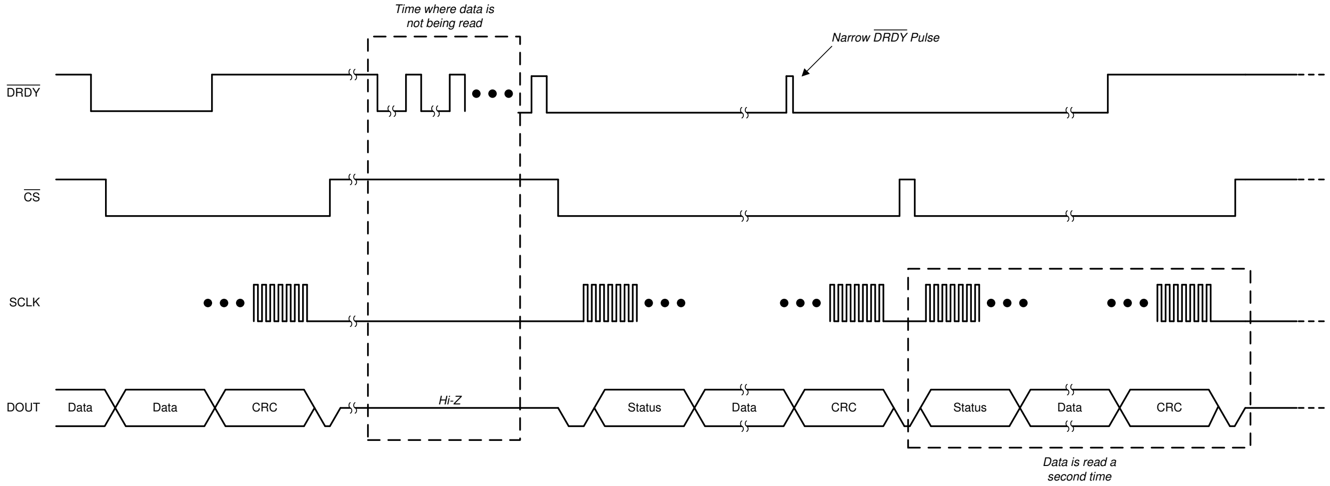


Figure 8-32. Collecting Data After a Pause by Reading Data Twice

8.6 AMC130M03 Registers

Table 8-14 lists the memory-mapped registers for the AMC130M03 registers. All register offset addresses not listed in Table 8-14 should be considered as reserved locations and the register contents should not be modified.

Table 8-14. Register Map

Address	Acronym	Reset	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	ID	Xb	RESERVED				CHANCNT[3:0]			
			RESERVED							
01h	STATUS	0540h	LOCK	F_RESYNC	REG_MAP	CRC_ERR	CRC_TYPE	RESET	WLENGTH[1:0]	
			FUSE_FAIL	SEC_FAIL	RESERVED			DRDY2	DRDY1	DRDY0
02h	MODE	0510h	RESERVED		REG_CRC_EN	RX_CRC_EN	CRC_TYPE	RESET	WLENGTH[1:0]	
			RESERVED			TIMEOUT	DRDY_SEL[1:0]		DRDY_HiZ	DRDY_FMT
03h	CLOCK	070Eh	RESERVED					CH2_EN	CH1_EN	CH0_EN
			CLK_DIV[1:0]		TURBO	OSR[2:0]			PWR[1:0]	
04h	GAIN	0000h	RESERVED					PGAGAIN2[2:0]		
			RESERVED	PGAGAIN1[2:0]			RESERVED	PGAGAIN0[2:0]		
06h	CFG	0600h	RESERVED	GPO_EN	GPO_DAT	GC_DLY[3:0]				GC_EN
			RESERVED							
09h	CH0_CFG	0000h	PHASE0[9:0]							
			PHASE0[9:0]		RESERVED				MUX0[1:0]	
0Ah	CH0_OCAL_MSB	0000h	OCAL0_MSB[15:0]							
			OCAL0_MSB[15:0]							
0Bh	CH0_OCAL_LSB	0000h	OCAL0_LSB[7:0]							
			RESERVED							
0Ch	CH0_GCAL_MSB	8000h	GCAL0_MSB[15:0]							
			GCAL0_MSB[15:0]							
0Dh	CH0_GCAL_LSB	0000h	GCAL0_LSB[7:0]							
			RESERVED							
0Eh	CH1_CFG	0000h	PHASE1[9:0]							
			PHASE1[9:0]		RESERVED				MUX1[1:0]	
0Fh	CH1_OCAL_MSB	0000h	OCAL1_MSB[15:0]							
			OCAL1_MSB[15:0]							
10h	CH1_OCAL_LSB	0000h	OCAL1_LSB[7:0]							
			RESERVED							
11h	CH1_GCAL_MSB	8000h	GCAL1_MSB[15:0]							
			GCAL1_MSB[15:0]							
12h	CH1_GCAL_LSB	0000h	GCAL1_LSB[7:0]							
			RESERVED							
13h	CH2_CFG	0000h	PHASE2[9:0]							
			PHASE2[9:0]		TS_SEL	TS_EN	RESERVED	TS_CHOP	MUX2[1:0]	
14h	CH2_OCAL_MSB	0000h	OCAL2_MSB[15:0]							
			OCAL2_MSB[15:0]							
15h	CH2_OCAL_LSB	0000h	OCAL2_LSB[7:0]							
			RESERVED							
16h	CH2_GCAL_MSB	8000h	GCAL2_MSB[15:0]							
			GCAL2_MSB[15:0]							
17h	CH2_GCAL_LSB	0000h	GCAL2_LSB[7:0]							
			RESERVED							
31h	DCDC_CTRL	0000h	RESERVED				DCDC_FREQ[3:0]			
			RESERVED							DCDC_EN
3Eh	REGMAP_CRC	0000h	REG_CRC[15:0]							
			REG_CRC[15:0]							

Complex bit access types are encoded to fit into small table cells. Table 8-15 shows the codes that are used for access types in this section.

Table 8-15. AMC130M03 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

8.6.1 ID Register (Address = 00h) [Reset = 23XXh]

Return to the Summary Table.

Figure 8-33. ID Register

15	14	13	12	11	10	9	8
RESERVED				CHANCNT[3:0]			
R-0010b				R-0011b			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-X							

Table 8-16. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R	0010b	Reserved Always reads 0010b
11:8	CHANCNT[3:0]	R	0011b	Channel count Always reads 0011b
7:0	RESERVED	R	X	Reserved Values are subject to change without notice.

8.6.2 STATUS Register (Address = 01h) [Reset = 0540h]

Return to the Summary Table.

Figure 8-34. STATUS Register

15	14	13	12	11	10	9	8
LOCK	F_RESYNC	REG_MAP	CRC_ERR	CRC_TYPE	RESET	WLENGTH[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-1b	R-01b	

7	6	5	4	3	2	1	0
FUSE_FAIL	SEC_FAIL	RESERVED			DRDY2	DRDY1	DRDY0
R-0b	R-1b	R-000b			R-0b	R-0b	R-0b

Table 8-17. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LOCK	R	0b	SPI interface lock indicator Indicates the SPI interface is locked by the lock command. The bit is reset to 0b by the unlock command. 0b = Unlocked 1b = Locked
14	F_RESYNC	R	0b	ADC resynchronization indicator This bit is set each time the ADC resynchronizes. This bit is cleared by reading the STATUS register, either by executing the NULL command or a RREG command accessing the STATUS register. 0b = No resynchronization occurred 1b = Resynchronization occurred
13	REG_MAP	R	0b	Register map CRC fault indicator Indicates a register map CRC fault occurred. This bit is cleared by reading the STATUS register, either by executing the NULL command or a RREG command accessing the STATUS register. 0b = No register map CRC fault occurred 1b = Register map CRC fault occurred
12	CRC_ERR	R	0b	SPI input CRC error indicator Indicates a SPI input CRC fault occurred. This bit is cleared by reading the STATUS register, either by executing the NULL command or a RREG command accessing the STATUS register. 0b = No CRC error 1b = Input CRC error occurred
11	CRC_TYPE	R	0b	CRC type indicator Indicates the CRC type. This bit is cleared by a device reset. 0b = 16-bit CCITT 1b = 16-bit ANSI
10	RESET	R	1b	Reset status indicator The device reset indicator is triggered by the $\overline{\text{RESET}}$ pin, power-on-reset or the RESET command. This bit is cleared by writing 0b to the RESET bit in the MODE register. 0b = Not reset 1b = Reset occurred
9:8	WLENGTH[1:0]	R	01b	Data word length indicator Indicates the data word frame length. This bit is cleared by a device reset. 00b = 16 bit 01b = 24 bits 10b = 32 bits; zero padding 11b = 32 bits; MSB sign extension
7	FUSE_FAIL	R	0b	Fuse parity fault indicator Indicates a fault of the internal memory. This bit is cleared by reading the STATUS register, either by executing the NULL command or a RREG command accessing the STATUS register. If the physical fault persists, the indicator is set again automatically. 0b = Fuse parity OK 1b = Fuse parity not OK
6	SEC_FAIL	R	1b	High-side supply fault indicator Indicates a fault of the high-side output of the DC/DC converter, or a communication error during the data transmission across the isolation barrier. This bit is cleared by reading the STATUS register, either by executing the NULL command or a RREG command accessing the STATUS register. 0b = High-side supply OK 1b = High-side supply not OK
5:3	RESERVED	R	000b	Reserved Always reads 000b
2	DRDY2	R	0b	Channel 2 ADC data available indicator 0b = No new data available 1b = New data are available
1	DRDY1	R	0b	Channel 1 ADC data available indicator 0b = No new data available 1b = New data are available

Table 8-17. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	DRDY0	R	0b	Channel 0 ADC data available indicator 0b = No new data available 1b = New data are available

8.6.3 MODE Register (Address = 02h) [Reset = 0510h]

Return to the Summary Table.

Figure 8-35. MODE Register

15	14	13	12	11	10	9	8
RESERVED		REG_CRC_EN	RX_CRC_EN	CRC_TYPE	RESET	WLENGTH[1:0]	
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-01b	

7	6	5	4	3	2	1	0
RESERVED			TIMEOUT	DRDY_SEL[1:0]		DRDY_HiZ	DRDY_FMT
R/W-000b			R/W-1b	R/W-00b		R/W-0b	R/W-0b

Table 8-18. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	RESERVED	R/W	00b	Reserved Always write 00b
13	REG_CRC_EN	R/W	0b	Register map CRC enable 0b = Disabled 1b = Enabled
12	RX_CRC_EN	R/W	0b	SPI input CRC enable 0b = Disabled 1b = Enabled
11	CRC_TYPE	R/W	0b	SPI input and output, register map CRC type 0b = 16-bit CCITT 1b = 16-bit ANSI
10	RESET	R/W	1b	Reset Write 0b to clear the RESET bit in the STATUS register 0b = No reset 1b = Reset occurred
9:8	WLENGTH[1:0]	R/W	01b	Data word length selection 00b = 16 bits 01b = 24 bits 10b = 32 bits; LSB zero padding 11b = 32 bits; MSB sign extension
7:5	RESERVED	R/W	000b	Reserved Always write 000b
4	TIMEOUT	R/W	1b	SPI timeout enable 0b = Disabled 1b = Enabled
3:2	DRDY_SEL[1:0]	R/W	00b	$\overline{\text{DRDY}}$ pin signal source selection 00b = Most lagging enabled channel 01b = Logic OR of all the enabled channels 10b = Most leading enabled channel 11b = Most leading enabled channel
1	DRDY_HiZ	R/W	0b	$\overline{\text{DRDY}}$ pin state when conversion data are not available 0b = Logic high 1b = High impedance
0	DRDY_FMT	R/W	0b	$\overline{\text{DRDY}}$ signal format when conversion data are available 0b = Logic low 1b = Low pulse with a fixed duration

8.6.4 CLOCK Register (Address = 03h) [Reset = 070Eh]

Return to the Summary Table.

Figure 8-36. CLOCK Register

15	14	13	12	11	10	9	8
RESERVED					CH2_EN	CH1_EN	CH0_EN
R/W-00000b					R/W-1b	R/W-1b	R/W-1b

7	6	5	4	3	2	1	0
CLK_DIV[1:0]		TURBO	OSR[2:0]			PWR[1:0]	
R/W-00b		R/W-0b	R/W-011b			R/W-10b	

Table 8-19. CLOCK Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved Always write 00000b
10	CH2_EN	R/W	1b	Channel 2 ADC enable 0b = Disabled 1b = Enabled
9	CH1_EN	R/W	1b	Channel 1 ADC enable 0b = Disabled 1b = Enabled
8	CH0_EN	R/W	1b	Channel 0 ADC enable 0b = Disabled 1b = Enabled
7:6	CLK_DIV[1:0]	R/W	00b	Clock divider ratio selection 00b = Divide by 2 01b = Divide by 4 10b = Divide by 8 11b = Divide by 12
5	TURBO	R/W	0b	Turbo mode (OSR = 64) Selects oversampling ratio 64 by setting this bit to 1b. The OSR[2:0] bits are ignored if this bit is set to 1b. 0b = Disabled 1b = Enabled
4:2	OSR[2:0]	R/W	011b	Modulator oversampling ratio selection 000b = 128 001b = 256 010b = 512 011b = 1024 100b = 2048 101b = 4096 110b = 8192 111b = 16384
1:0	PWR[1:0]	R/W	10b	Power mode selection 00b = Reserved. Do not use. 01b = Low power 10b = High resolution 11b = Reserved. Do not use.

8.6.5 GAIN Register (Address = 04h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-37. GAIN Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="5">RESERVED</td><td colspan="3">PGAGAIN2[2:0]</td></tr>
<tr><td colspan="5">R/W-00000b</td><td colspan="3">R/W-000b</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>RESERVED</td><td colspan="3">PGAGAIN1[2:0]</td><td>RESERVED</td><td colspan="3">PGAGAIN0[2:0]</td></tr>
<tr><td>R/W-0b</td><td colspan="3">R/W-000b</td><td>R/W-0b</td><td colspan="3">R/W-000b</td></tr>
</table>

Table 8-20. GAIN Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	RESERVED	R/W	00000b	Reserved Always write 00000b
10:8	PGAGAIN2[2:0]	R/W	000b	PGA gain selection for channel 2 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128
7	RESERVED	R/W	0b	Reserved Always write 0b
6:4	PGAGAIN1[2:0]	R/W	000b	PGA gain selection for channel 1 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128
3	RESERVED	R/W	0b	Reserved Always write 0b
2:0	PGAGAIN0[2:0]	R/W	000b	PGA gain selection for channel 0 000b = 1 001b = 2 010b = 4 011b = 8 100b = 16 101b = 32 110b = 64 111b = 128

8.6.6 CFG Register (Address = 06h) [Reset = 0600h]

Return to the Summary Table.

Figure 8-38. CFG Register

15	14	13	12	11	10	9	8
RESERVED	GPO_EN	GPO_DAT	GC_DLY[3:0]				GC_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0011b				R/W-0b
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R/W-00000000b							

Table 8-21. CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0b	Reserved Always write 0b
14	GPO_EN	R/W	0b	Digital output enable Enables digital output (GPO) functionality at AIN2P pin. 0b = Digital output disabled 1b = Digital output enabled
13	GPO_DAT	R/W	0b	Digital output data Digital output (GPO) data if GPO_EN = 1b. 0b = Zero output 1b = One output
12:9	GC_DLY[3:0]	R/W	0011b	Global-chop delay selection Delay in modulator clock periods before measurement begins. 0000b = 2 0001b = 4 0010b = 8 0011b = 16 0100b = 32 0101b = 64 0110b = 128 0111b = 256 1000b = 512 1001b = 1024 1010b = 2048 1011b = 4096 1100b = 8192 1101b = 16384 1110b = 32768 1111b = 65536
8	GC_EN	R/W	0b	Global-chop enable 0b = Disabled 1b = Enabled
7:0	RESERVED	R/W	00000000b	Reserved Always write 00000000b

8.6.7 CH0_CFG Register (Address = 09h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-39. CH0_CFG Register

15	14	13	12	11	10	9	8
PHASE0[9:0]							
R/W-0000000000b							

7	6	5	4	3	2	1	0
PHASE0[9:0]		RESERVED				MUX0[1:0]	
R/W-0000000000b		R-0000b				R/W-00b	

Table 8-22. CH0_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASE0[9:0]	R/W	0000000000b	Channel 0 phase delay selection Phase delay in modulator clock cycles provided in twos complement format.
5:2	RESERVED	R	0000b	Reserved Always reads 0000b
1:0	MUX0[1:0]	R/W	00b	Channel 0 input selection Input multiplexer for channel 0 00b = AIN0P and AIN0N 01b = AIN0 disconnected (ADC inputs shorted) 10b = DC diagnostic signal 11b = AC diagnostic signal

8.6.8 CH0_OCAL_MSB Register (Address = 0Ah) [Reset = 0000h]

Return to the Summary Table.

Figure 8-40. CH0_OCAL_MSB Register

15	14	13	12	11	10	9	8
OCAL0_MSB[15:0]							
R/W-0000000000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OCAL0_MSB[15:0]							
R/W-0000000000000000b							

Table 8-23. CH0_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCAL0_MSB[15:0]	R/W	0000000000000000b	Channel 0 offset calibration register bits [23:8] Value provided in twos complement format.

8.6.9 CH0_OCAL_LSB Register (Address = 0Bh) [Reset = 0000h]

Return to the Summary Table.

Figure 8-41. CH0_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCAL0_LSB[7:0]							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-00000000b							

Table 8-24. CH0_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCAL0_LSB[7:0]	R/W	00000000b	Channel 0 offset calibration register bits [7:0] Value provided in twos complement format.
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.10 CH0_GCAL_MSB Register (Address = 0Ch) [Reset = 8000h]

Return to the Summary Table.

Figure 8-42. CH0_GCAL_MSB Register

15	14	13	12	11	10	9	8
GCAL0_MSB[15:0]							
R/W-1000000000000000b							
7	6	5	4	3	2	1	0
GCAL0_MSB[15:0]							
R/W-1000000000000000b							

Table 8-25. CH0_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCAL0_MSB[15:0]	R/W	1000000000000000b	Channel 0 gain calibration register bits [23:8] Unsigned number for the gain range from 0.0 to 2.0 x (2^{24} – 1) / 2^{24}

8.6.11 CH0_GCAL_LSB Register (Address = 0Dh) [Reset = 0000h]

Return to the Summary Table.

Figure 8-43. CH0_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCAL0_LSB[7:0]							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-00000000b							

Table 8-26. CH0_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCAL0_LSB[7:0]	R/W	00000000b	Channel 0 gain calibration register bits [7:0] Unsigned number for the gain range from 0.0 to 2.0 x (2^{24} – 1) / 2^{24}
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.12 CH1_CFG Register (Address = 0Eh) [Reset = 0000h]

Return to the Summary Table.

Figure 8-44. CH1_CFG Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">PHASE1[9:0]</td></tr>
<tr><td colspan="8">R/W-0000000000b</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">PHASE1[9:0]</td><td colspan="4">RESERVED</td><td colspan="2">MUX1[1:0]</td></tr>
<tr><td colspan="2">R/W-0000000000b</td><td colspan="4">R-0000b</td><td colspan="2">R/W-00b</td></tr>
</table>

Table 8-27. CH1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASE1[9:0]	R/W	0000000000b	Channel 1 phase delay selection Phase delay in modulator clock cycles provided in twos complement format.
5:2	RESERVED	R	0000b	Reserved Always reads 0000b
1:0	MUX1[1:0]	R/W	00b	Channel 1 input selection Input multiplexer for channel 1 00b = AIN1P and AIN12N 01b = AIN1 disconnected (ADC inputs shorted) 10b = DC diagnostic signal 11b = AC diagnostic signal

8.6.13 CH1_OCAL_MSB Register (Address = 0Fh) [Reset = 0000h]

Return to the Summary Table.

Figure 8-45. CH1_OCAL_MSB Register

15	14	13	12	11	10	9	8
OCAL1_MSB[15:0]							
R/W-0000000000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OCAL1_MSB[15:0]							
R/W-0000000000000000b							

Table 8-28. CH1_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCAL1_MSB[15:0]	R/W	0000000000000000b	Channel 1 offset calibration register bits [23:8] Value provided in twos complement format.

8.6.14 CH1_OCAL_LSB Register (Address = 10h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-46. CH1_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCAL1_LSB[7:0]							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-00000000b							

Table 8-29. CH1_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCAL1_LSB[7:0]	R/W	00000000b	Channel 1 offset calibration register bits [7:0] Value provided in twos complement format.
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.15 CH1_GCAL_MSB Register (Address = 11h) [Reset = 8000h]

Return to the Summary Table.

Figure 8-47. CH1_GCAL_MSB Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">GCAL1_MSB[15:0]</td></tr>
<tr><td colspan="8">R/W-1000000000000000b</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">GCAL1_MSB[15:0]</td></tr>
<tr><td colspan="8">R/W-1000000000000000b</td></tr>
</table>

Table 8-30. CH1_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCAL1_MSB[15:0]	R/W	1000000000000000b	Channel 1 gain calibration register bits [23:8] Unsigned number for the gain range from 0.0 to 2.0 x $(2^{24} – 1) / 2^{24}$

8.6.16 CH1_GCAL_LSB Register (Address = 12h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-48. CH1_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCAL1_LSB[7:0]							
R/W-00000000b							
7	6	5	4	3	2	1	0
RESERVED							
R-00000000b							

Table 8-31. CH1_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCAL1_LSB[7:0]	R/W	00000000b	Channel 1 gain calibration register bits [7:0] Unsigned number for the gain range from 0.0 to 2.0 x $(2^{24} – 1) / 2^{24}$
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.17 CH2_CFG Register (Address = 13h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-49. CH2_CFG Register

15	14	13	12	11	10	9	8
PHASE2[9:0]							
R/W-0000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PHASE2[9:0]		TS_SEL	TS_EN	RESERVED	TS_CHOP	MUX2[1:0]	
R/W-0000000000b		R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-00b	

Table 8-32. CH2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15:6	PHASE2[9:0]	R/W	0000000000b	Channel 2 phase delay selection Phase delay in modulator clock cycles provided in twos complement format.
5	TS_SEL	R/W	0b	Temperature sensor input selection Selects between internal and external temperature sensor. 0b = Internal sensor 1b = External sensor
4	TS_EN	R/W	0b	Temperature sensor measurement mode enable 0b = Temperature sensor disabled 1b = Temperature sensor enabled
3	RESERVED	R	0b	Reserved Always reads 0000b
2	TS_CHOP	R/W	0b	Temperature sensor input polarity selection Inverts the temperature sensor inputs. 0b = Temperature sensor inputs are not inverted 1b = Temperature sensor inputs are inverted
1:0	MUX2[1:0]	R/W	00b	Channel 2 input selection Input multiplexer for channel 2 00b = AIN2P and AIN12N 01b = AIN2 disconnected (ADC inputs shorted) 10b = DC diagnostic signal 11b = AC diagnostic signal

8.6.18 CH2_OCAL_MSB Register (Address = 14h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-50. CH2_OCAL_MSB Register

15	14	13	12	11	10	9	8
OCAL2_MSB[15:0]							
R/W-0000000000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OCAL2_MSB[15:0]							
R/W-0000000000000000b							

Table 8-33. CH2_OCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	OCAL2_MSB[15:0]	R/W	0000000000000000b	Channel 2 offset calibration register bits [23:8] Value provided in twos complement format.

8.6.19 CH2_OCAL_LSB Register (Address = 15h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-51. CH2_OCAL_LSB Register

15	14	13	12	11	10	9	8
OCAL2_LSB[7:0]							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-00000000b							

Table 8-34. CH2_OCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	OCAL2_LSB[7:0]	R/W	00000000b	Channel 2 offset calibration register bits [7:0] Value provided in twos complement format.
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.20 CH2_GCAL_MSB Register (Address = 16h) [Reset = 8000h]

Return to the Summary Table.

Figure 8-52. CH2_GCAL_MSB Register

15	14	13	12	11	10	9	8
GCAL2_MSB[15:0]							
R/W-1000000000000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GCAL2_MSB[15:0]							
R/W-1000000000000000b							

Table 8-35. CH2_GCAL_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	GCAL2_MSB[15:0]	R/W	1000000000000000b	Channel 2 gain calibration register bits [23:8] Unsigned number for the gain range from 0.0 to 2.0 x (2^{24} – 1) / 2^{24}

8.6.21 CH2_GCAL_LSB Register (Address = 17h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-53. CH2_GCAL_LSB Register

15	14	13	12	11	10	9	8
GCAL2_LSB[7:0]							
R/W-00000000b							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-00000000b							

Table 8-36. CH2_GCAL_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	GCAL2_LSB[7:0]	R/W	00000000b	Channel 2 gain calibration register bits [7:0] Unsigned number for the gain range from 0.0 to 2.0 x $(2^{24} – 1) / 2^{24}$
7:0	RESERVED	R	00000000b	Reserved Always reads 00000000b

8.6.22 DCDC_CTRL Register (Address = 31h) [Reset = 0000h]

Return to the Summary Table.

Figure 8-54. DCDC_CTRL Register

15	14	13	12	11	10	9	8
RESERVED				DCDC_FREQ[3:0]			
R/W-0000b				R/W-0000b			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							DCDC_EN
R/W-0000000b							R/W-0b

Table 8-37. DCDC_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0000b	Reserved Always write 0000b
11:8	DCDC_FREQ[3:0]	R/W	0000b	DC/DC frequency range selection Selects the range of the modulator clock frequency, based on the frequency at the CLKIN pin and clock divider ratio. 0000b = 3.76 MHz to 4.10 MHz 0001b = 3.52 MHz to 3.84 MHz 0010b = 3.30 MHz to 3.59 MHz 0011b = 3.09 MHz to 3.36 MHz 0100b = 2.89 MHz to 3.15 MHz 0101b = 2.71 MHz to 2.95 MHz 0110b = 2.53 MHz to 2.76 MHz 0111b = 2.37 MHz to 2.59 MHz 1000b = 2.22 MHz to 2.42 MHz 1001b = 2.08 MHz to 2.27 MHz 1010b = 1.95 MHz to 2.12 MHz 1011b = 1.82 MHz to 1.99 MHz 1100b = 1.71 MHz to 1.86 MHz 1101b = 1.60 MHz to 1.74 MHz 1110b = 1.50 MHz to 1.63 MHz 1111b = 1.40 MHz to 1.53 MHz
7:1	RESERVED	R/W	0000000b	Reserved Always write 0000000b
0	DCDC_EN	R/W	0b	DC/DC enable Enables the integrated DC/DC converter. 0b = Disabled 1b = Enabled

8.6.23 REGMAP_CRC Register (Address = 3Eh) [Reset = 0000h]

Return to the Summary Table.

Figure 8-55. REGMAP_CRC Register

15	14	13	12	11	10	9	8
REG_CRC[15:0]							
R-0000000000000000b							
7	6	5	4	3	2	1	0
REG_CRC[15:0]							
R-0000000000000000b							

Table 8-38. REGMAP_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	REG_CRC[15:0]	R	0000000000000000b	Register map CRC value

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Unused Inputs and Outputs

Leave any unused analog inputs floating or connected to HGND.

Do not float unused digital inputs because excessive power-supply leakage current can result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND. Leave the DRDY pin unconnected if unused.

9.1.2 Antialiasing

An analog low-pass filter is required in front of each of the channel inputs to prevent out-of-band noise and interference from coupling into the band of interest. Because the AMC130M03 is a delta-sigma ADC, the integrated digital filter provides substantial attenuation for frequencies outside of the band of interest up to the frequencies adjacent to f_{MOD}. Therefore, a single-order RC filter provides sufficient antialiasing protection in the vast majority of applications.

Choosing the values of the resistor and capacitor depends on the desired cutoff frequency, limiting source impedance for the ADC inputs, and providing enough instantaneous charge to the ADC input sampling circuit through the filter capacitor. Figure 9-1 shows the recommended filter component values.

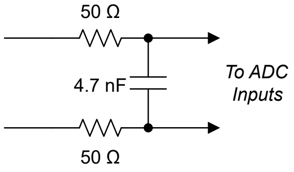


Figure 9-1. Recommended Antialiasing Circuitry

9.1.3 Minimum Interface Connections

Figure 9-2 illustrates how the AMC130M03 can be configured for the minimum number of interface pins. This configuration is useful when using data isolation to minimize the number of isolation channels required or when the microcontroller (MCU) pins are limited.

The CLKIN pin requires an LVCMOS clock that can be either generated by the MCU or created using a local LVCMOS output device. Tie the SYNC/RESET pin to DVDD in hardware if unused. The DRDY pin can be left floating if unused. Connect either SYNC/RESET or DRDY to the MCU to make sure the MCU stays synchronized to ADC conversions. If the MCU provides CLKIN, the CLKIN periods can be counted to determine the sample period rather than forcing synchronization using the SYNC/RESET pin or monitoring the DRDY pin. Synchronization cannot be regained if a bit error occurs on the clock and samples can be missed if the SYNC/RESET or DRDY pins are not used. CS can be tied low in hardware if the AMC130M03 is the only device on the SPI bus. Make sure the data input and output CRC are enabled and are used to guard against faulty register reads and writes if CS is tied low permanently.

During a read operation, if CS is tied low permanently, all data words must be extracted from the device, no SPI word can be skipped.

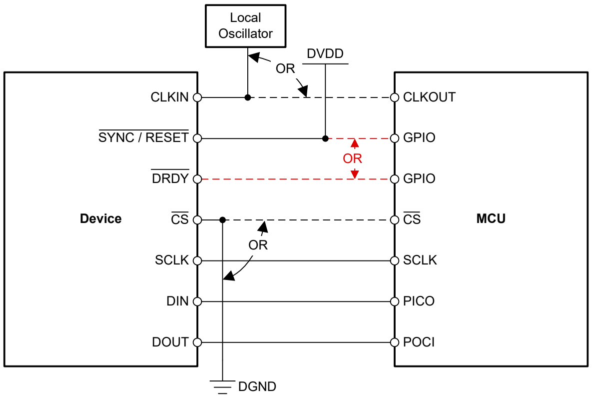


Figure 9-2. Minimum Connections Required to Operate the AMC130M03

9.1.4 Multiple Device Configuration

Multiple AMC130M03 devices can be arranged to scale the number of channels for simultaneous data acquisition. The same clock must be provided to all devices and the $\overline{\text{SYNC/RESET}}$ pins must be strobed simultaneously at least one time to align the sample periods internally between devices. The phase settings of each device can be changed uniquely, but the host must take care to record which channel in the group of devices represents the *zero* phase.

The devices can also share the SPI bus where only the $\overline{\text{CS}}$ pins for each device are unique. Each device can be addressed sequentially by asserting $\overline{\text{CS}}$ for the device that the host wishes to communicate with. The DOUT pin remains high impedance when the $\overline{\text{CS}}$ pin is high, allowing the DOUT lines to be shared between devices as long as no two devices sharing the bus simultaneously have the $\overline{\text{CS}}$ pins low. Figure 9-3 depicts multiple devices configured for simultaneous data acquisition while sharing the SPI bus.

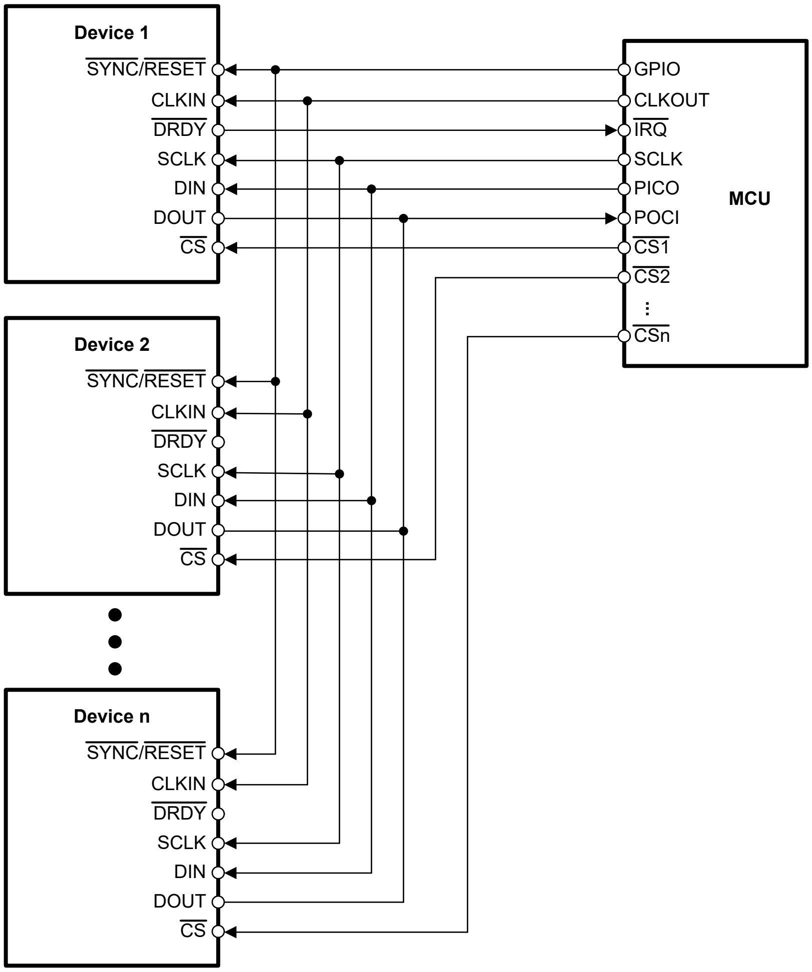


Figure 9-3. Multiple Device Configuration

9.1.5 Calibration

Certain signal chain errors can be corrected through a single room-temperature calibration. The AMC130M03 can store calibration values and uses the values to correct the results in real time. Among the errors that can be corrected in real time with the AMC130M03 are offset error, gain error, and phase error.

Offset calibration is performed by determining the measured output of the signal chain when the input is zero voltage for a voltage channel or zero current for a current channel. The ADC conversion result for zero input can be measured and recorded in external nonvolatile memory for each channel. When the system is deployed, these values can be provided to the CHn_OCAL_MSB and CHn_OCAL_LSB registers for the corresponding channels. The AMC130M03 then subtracts these values from the conversion results prior to providing them to the host.

Similar to offset error correction, system gain error can be determined prior to deployment and can be used to correct the gain error on each channel in real time. Gain error is defined as the percentage difference in the ADC transfer function from the PGA gain corrected ideal value of 1. This error can be determined by measuring the results from both a maximum and minimum input signal, finding the difference between these results, and dividing by the difference between the ideal difference. Equation 15 describes how to calculate gain error.

$$\text{Gain Error} = 1 - \frac{V,I_{\text{Max,Measured}} - V,I_{\text{Min,Measured}}}{V,I_{\text{Max}} - V,I_{\text{Min}}} \tag{15}$$

To correct for gain error, divide each offset-corrected conversion result by the measured gain. The AMC130M03 multiplies each conversion result by the gain calibration factor stored in the CHn_GCAL_MSB and CHn_GCAL_LSB registers according to the method described in the *Calibration Registers* section. The host can program the measured inverted gain values for each channel into these registers to have them automatically corrected for each sample.

The AMC130M03 can also correct for system phase error introduced by sensors. For this design, PCB routing from the shunt to the ADC input (and from the voltage measurement resistive divider) can introduce some phase error into the system. Some designs use a software method for phase correction, but the AMC130M03 can perform this function in real time. The system must first measure the phase relationships between the various channels. Then the AMC130M03 defines one channel as *phase 0*. Subsequently, the PHASEn bits in the CHn_CFG registers corresponding to the various other channels can be edited to correct the phase relationship relative to the phase 0 channels.

9.1.6 Troubleshooting

Table 9-1 lists common issues faced when designing with the AMC130M03 and the corresponding solutions. This list is not comprehensive.

Table 9-1. Troubleshooting Common Issues Using the AMC130M03

ISSUE	POSSIBLE ROOT CAUSE	POSSIBLE SOLUTION
The DRDY pin is toggling at half the expected frequency.	The DRDY_FMT bit is set to 1b and ADC conversion data are not being read. The updates of the conversion data in the FIFO buffer drive the DRDY pin. If the host does not read the conversion data, the data in the FIFO buffer are updated every other conversion. This update causes the DRDY pin to toggle at half the output data rate. See the *ADC Output Buffer and FIFO Buffer* section for a detailed explanation.	Read data after each DRDY falling edge following the recommendations given in the *Collecting Data for the First Time or After a Pause in Data Collection* section.
The F_RESYNC bit is set in the STATUS word even though this bit was already cleared.	The SYNC/RESET pin is being toggled asynchronously to CLKIN.	The SYNC/RESET pin functions as a constant synchronization check, rather than a *convert start* pin. See the *Synchronization* section for more details on the intended usage of the SYNC/RESET pin.
The same ADC conversion data are output multiple times before changing.	The ADC does not recognize the data as being read because not all ADC channel data are read by the host.	Read all data words in the output data frame, including those for channels that are disabled.
The SEC_FAIL bit in the STATUS register is set, even if the power on the secondary side appears to be stable, for example after an SPI write operation.	Writing data to any of the ADC configuration registers on the high side also sets the SEC_FAIL bit until the transmission over the isolation barrier is complete.	Read the SEC_FAIL bit in the STATUS register repeatedly until the bit is cleared to 0b, before reading ADC conversion data.

9.2 Typical Application

This section describes a typical three-phase energy measurement front-end using the AMC130M03. The ADC samples the outputs of resistive current sensors (shunts) and voltage dividers to measure the current and voltage of each leg of the AC mains. The design can achieve high accuracy across a wide input current range (0.05 A–100 A) and supports high sampling frequencies necessary for advanced power-quality features, such as individual harmonic analysis. Using the AMC130M03 to sample the voltages and currents per phase provides designers greater flexibility in the choice of metrology microcontrollers (MCU) when compared to an integrated system-on-a-chip (SoC) and dedicated application-specific products.

Figure 9-4 illustrates the front-end for a three-phase energy measurement design. In this design, one AMC130M03 per phase measures the current and voltage for this respective phase, providing galvanic isolation from phase to phase. This isolation is critical because the voltage level in a typical case can be in the order of 220 V on one phase and –220 V at another phase. If only one ADC for multiple phases is used, a voltage difference in the order of 440 V between two adjacent ADC inputs can appear, potentially destroying the device.

The design also includes a fourth ADC to monitor the current in the neutral line. Assuming the system ground for the metering front-end is connected to the neutral line, this ADC can be a non-isolated device such as the ADS131M02. This fourth device is optional and is typically used if tamper detection is a concern.

RC antialiasing filters are not given in Figure 9-4 for simplicity, but are recommended for all channels.

The microcontroller uses the SPI port to communicate with the four ADC devices, and provides a clock to all ADC devices at the respective CLKIN pins. Four of the microcontroller I/O pins (CS_A, CS_B, CS_C, and CS_D) generate the SPI $\overline{\text{CS}}$ signals. The SCLK, DIN, and DOUT connections are shared between all ADC devices. To simplify the figure, these connections are not shown in detail.

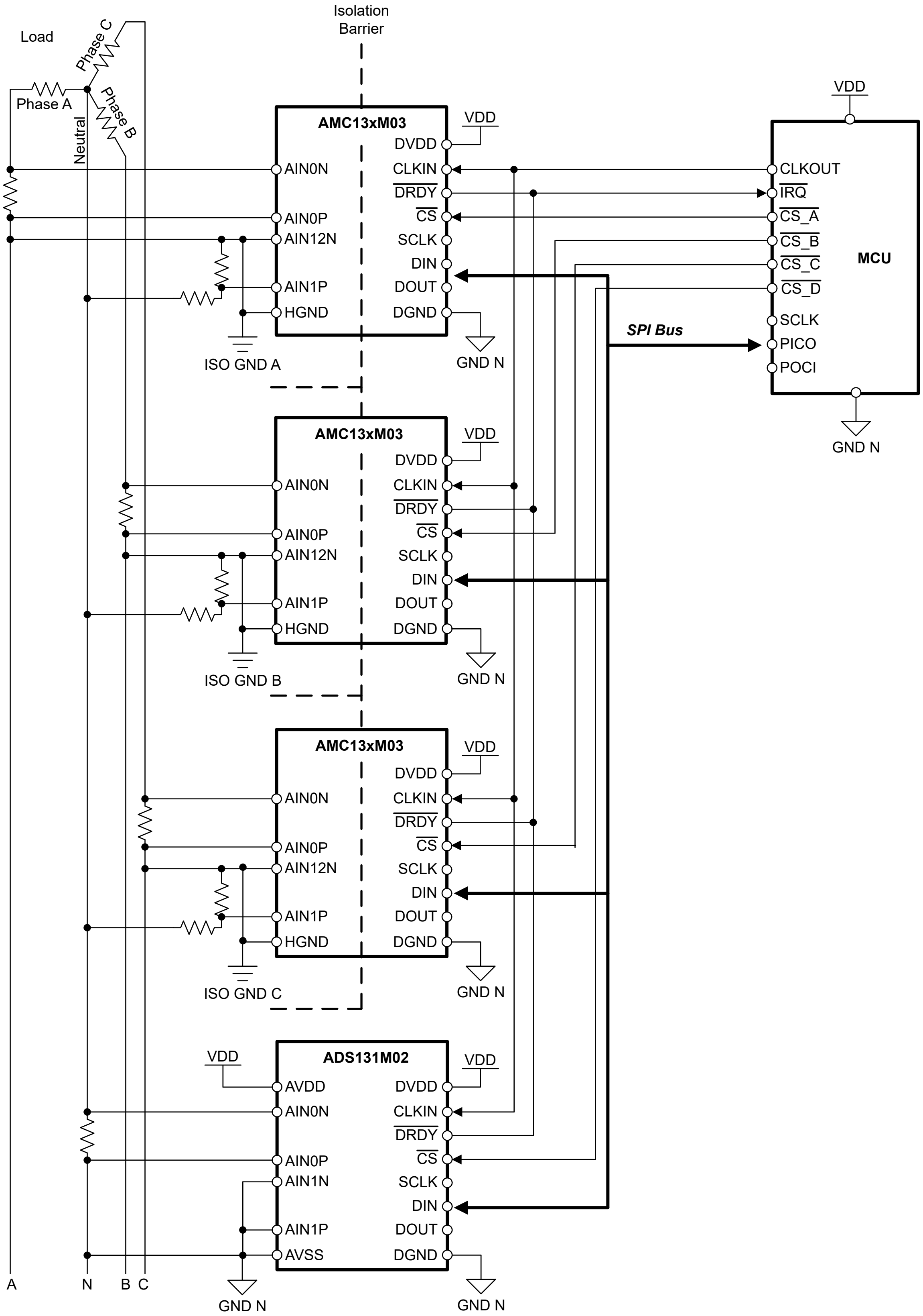


Figure 9-4. 3-Phase Metrology Design Front-End Using the AMC130M03

9.2.1 Design Requirements

Table 9-2 lists the design requirements for a three-phase metrology application.

Table 9-2. Key System Specifications

FEATURES	DESCRIPTION
Number of phases	3 phase (requires measurement of three voltages and three currents)
E-meter accuracy class	Class 0.1
Current sensor	Shunt resistor
Current range	0.05 A–100 A
System nominal frequency	50 Hz or 60 Hz
Measured parameters	• Active, reactive, apparent power, and energy • Root-mean-square (RMS) current and voltage • Power factor • Line frequency

9.2.2 Detailed Design Procedure

Figure 9-5 illustrates phase A of a three-phase energy meter. The other AMC130M03 devices that monitor phases B and C are connected in a similar way. The phase A current, I_{SHUNT}, is sensed with a shunt resistor (R_{SHUNT}) using channel 0 of the ADC (AIN0N, AIN0P). One terminal of the shunt becomes the isolated ground ISO_GND of the circuit and is connected to the ground pin HGND (pin 5) of the isolated side of the AMC130M03. The phase A to neutral voltage V_{PHASEA} is sensed with a resistor divider connected to channel 1, and the AIN12N pin is also connected to the ISO_GND node. The high side of the resistor divider is connected to the neutral line, the mid-point of the resistor divider is connected to the positive ADC input AIN1P, and the low side of the resistor divider (which is sensing the ISO_GND node) is connected to the negative input AIN12N of channel 1; therefore, the negative phase voltage is measured at channel 1. Thus, voltages measured by channel 1 of the AMC130M03 are opposite in sign to the phase voltage V_{PHASEA} and the phase current I_{SHUNT}, which is a classic approach in single-phase and poly-phase metering.

The selection of the shunt resistor value is made based on the manufacturer and current range required for energy measurements. The voltage divider resistors for the voltage channel are selected to make sure the mains voltage is divided down to adhere to the normal input voltage ranges of the AMC130M03.

In this design, the AMC130M03 interacts with an MCU in the following manner:

- The MCU provides the CLKIN clock to the AMC130M03
- When new ADC conversion data are ready, the AMC130M03 asserts the $\overline{\text{DRDY}}$ pin, which alerts the MCU that new samples are available
- After being alerted of new conversion data, the MCU retrieves the voltage and current samples from the AMC130M03 through the SPI interface

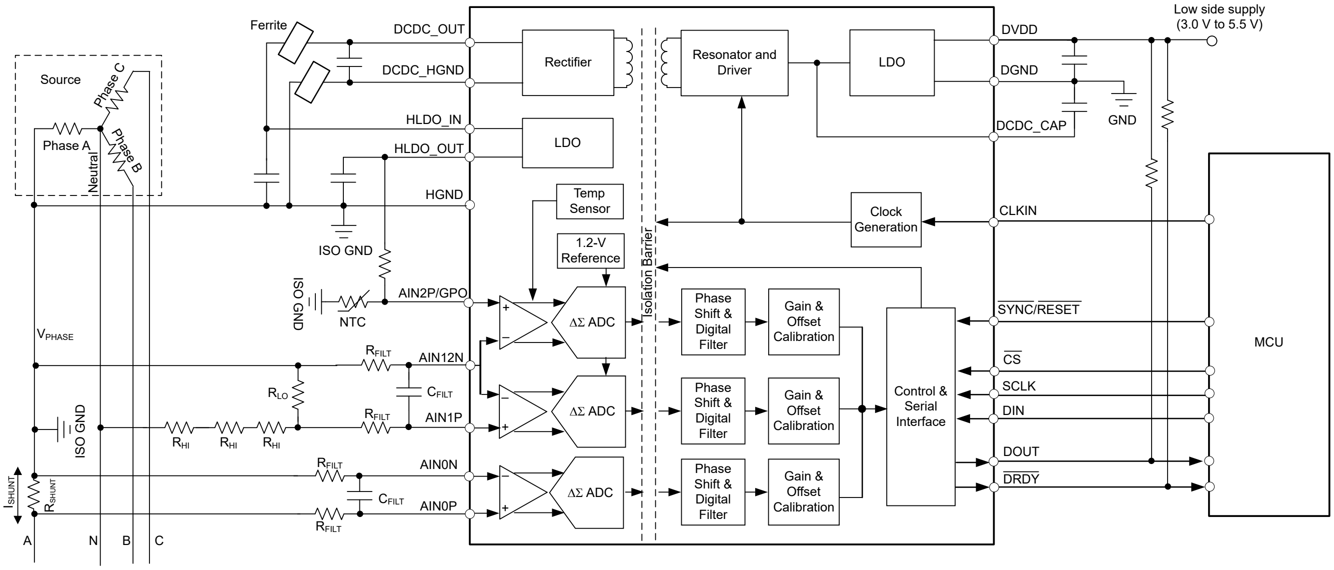


Figure 9-5. Current and Voltage Sensing With the AMC130M03

9.2.2.1 Voltage Measurement

The nominal mains voltage ranges from 100 V to 240 V, so this voltage must be scaled down to be sensed by an ADC. Figure 9-5 shows the analog front-end used for this voltage scaling at the ADC channel 1.

The analog front-end for voltage measurement consists of a voltage divider network (R_{HI} and R_{LO}), and an RC low-pass filter (R_{FILT} and C_{FILT}). Additional protection components (such as spike protection varistors) are usually placed as well, but are not shown in this circuit for simplicity.

Equation 16 shows how to calculate the range of differential voltages fed to the voltage ADC channel for a given mains voltage and the selected voltage divider resistor values.

$$V_{ADC} = \pm V_{RMS} \times \sqrt{2} \times \frac{R_{LO}}{3R_{HI} + R_{LO}} \quad (16)$$

R_{HI} is 300 kΩ and R_{LO} is 750 Ω in a typical design. For a mains voltage of 240 V (as measured between the line and neutral), the input signal to the voltage-sensing ADC has a voltage swing of ±256 mV (182 mV_{RMS}) based on Equation 16 and the selected resistor values. This voltage is well within the ±1.2-V input voltage range that can be sensed by the AMC130M03 for the selected PGA gain value of 1 that is used for the voltage channels. In addition, overvoltages as high as four times the main voltages (up to 1000 V) can also be measured based on the selected combination of resistor values and gain setting.

The finite input impedance of the ADC channel 1 results in a gain error and offset error from the non-ideal voltage division by R_{LO}. The introduction of a resistor in series with the inverting input of the ADC can reduce the offset and gain errors, as explained in the *Isolated Voltage-Measurement Circuit With ±250-mV Input and Differential Output* application note. The value of the additional series resistor is recommended to be in the order of R_{LO}, and the design steps are documented in the *Isolated Voltage-Measurement Circuit With ±250-mV Input and Differential Output* application note.

9.2.2.2 Current Shunt Measurement

The analog front-end for current measurement is different from the analog front-end for voltage measurement. Figure 9-5 shows the analog front-end used for current measurement at the ADC channel 0, which consists of the shunt resistor R_{SHUNT} and an RC low-pass antialiasing filter (R_{FILT} and C_{FILT}).

For a shunt value of 200 µΩ and a maximum current of I_{MAX} = 100 A, the maximum voltage drop across the shunt is $V_{SHUNT} = R_{SHUNT} \times I_{MAX}$ = 200 µΩ × ±100 A = ±20 mV.

To measure this shunt voltage, configure channel 0 of the AMC130M03 for gain = 32, which allows differential voltage measurements of $V_{IN1} = V_{AIN1P} – V_{AIN1N} = ±V_{REF} / 8 = ±1.2\ V / 32 = ±37.5\ mV$. The integrated charge pump in the device allows voltage measurements 1.3 V below HGND while using a unipolar analog power supply. This bipolar voltage measurement capability is important because one side of the shunt is connected to the same ISO_GND potential as the HGND pin of the AMC130M03, which means that the absolute voltage that the device must measure during the current measurement is up to 37.5 mV below HGND.

9.2.2.3 Temperature Measurement

Channel 2 of the AMC130M03 can be configured to measure temperature with an internal or external temperature sensor. Figure 9-5 illustrates an external temperature measurement using a discrete NTC temperature sensing element on channel 2 of the AMC130M03. Place the NTC close to the current-shunt sensor on the PCB if temperature calibration of the shunt measurement is required.

The *External Temperature Sensor* section describes how to operate channel 2 in external temperature sensor mode.

9.2.3 Application Curves

Electromagnetic interference (EMI) testing is common in many applications using the AMC130M03 to verify the system does not produce radiated emissions that exceed the defined levels that can possibly negatively impact other components or circuits in the system. See the *Understanding electromagnetic compliance tests in digital isolators* white paper for a more in-depth description of EMI. The magnitude of acceptable radiation and testing procedure for radiated emissions is put in place by the Comité International Spécial des Perturbations Radio, also known as CISPR. Industrial applications measure according to the CISPR 11 standard, and automotive applications measure to the CISPR 25 standard. For more information on the CISPR standards and the respective magnitudes over frequency, see the *An overview of radiated EMI specifications for power supplies* white paper.

Figure 9-6 and Figure 9-7 show the radiated emissions measurement for the AMC130M03 using the evaluation module available at AMC131M03EVM.

The measurements were done following CISPR 11 requirements, that is in a in a semi-anechoic chamber using a broadband antenna configured for horizontal and vertical polarizations with a 3-meter distance. The ADC is receiving a continuous clock at the CLKIN pin, and is generating conversion results, however there is no SPI communication while the emission profile is characterized.

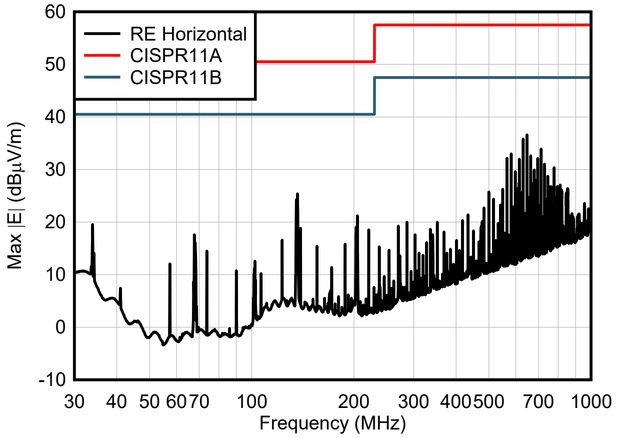


Figure 9-6. AMC130M03 Horizontal Radiated Emission CISPR11 Measurement

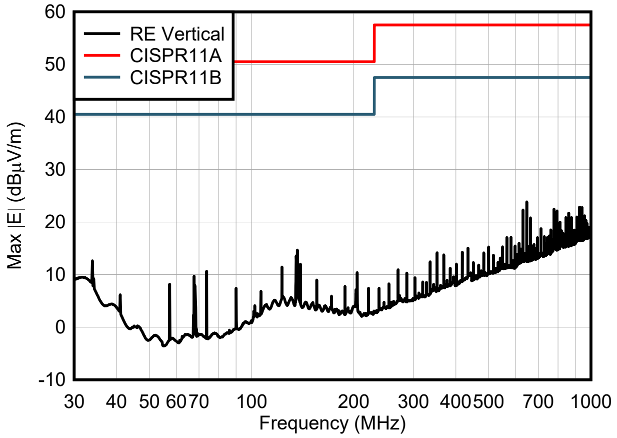


Figure 9-7. AMC130M03 Vertical Radiated Emission CISPR11 Measurement

9.3 Power Supply Recommendations

The AMC130M03 is powered from the low-side power supply (DVDD) with a nominal value of 3.3 V (or 5 V) ± 10%. Place a low-ESR decoupling capacitor of 1 nF (C15 in Figure 9-8) as close as possible to the DVDD pin, followed by a 1-µF capacitor (C16) to filter this power-supply path.

The low-side power supply (DVDD) is the only external supply required to operate the AMC130M03. All internal voltage supplies and secondary (high-side) supplies are generated by the integrated DC/DC converter and the high-side LDO, such as the supply voltage at the output pins, DCDC_OUT and HLDO_OUT.

The primary-side of the DC/DC converter is decoupled with a low-ESR, 100-nF capacitor (C17) positioned close to the device between the DCDC_CAP and DGND pins. Use a 1-µF capacitor (C6) to decouple the high-side in addition to a low-ESR, 1-nF capacitor (C1) placed as close as possible to the device and connected between the DCDC_OUT and DCDC_HGND pins.

For improved EMI performance, place a ferrite bead between the DCDC_OUT and HLDO_IN pins (F1) and the DCDC_HGND and HGND pins (F2), respectively.

For the high-side LDO, use low-ESR capacitors of 1 nF (C11) placed as close as possible to the AMC130M03, followed by a 100-nF decoupling capacitor (C13) between the HLDO_OUT and HGND pins.

The ground reference for the high-side (HGND) is derived from the terminal of the shunt resistor that is connected to the negative input (AIN0N) of the device. For best DC accuracy, use a separate trace to make this connection instead of shorting HGND to AIN0N directly at the device input.

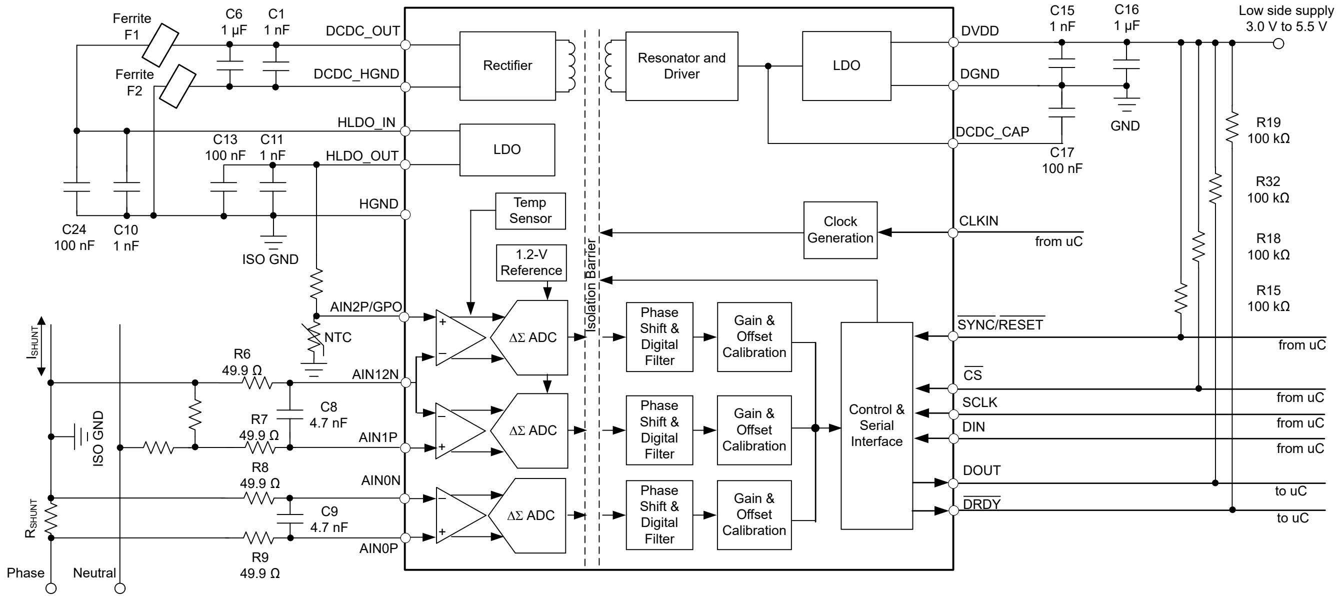


Figure 9-8. Power Supply Decoupling the AMC130M03

Capacitors must provide adequate *effective* capacitance under the applicable DC bias conditions they experience in the application. MLCC capacitors typically exhibit only a fraction of the nominal capacitance under real-world conditions and this factor must be taken into consideration when selecting these capacitors. This problem is especially acute in low-profile capacitors, in which the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

Table 9-3 lists components suitable for use with the AMC130M03. This list is not exhaustive. Other components can exist that are equally suitable (or better), however these listed components have been validated during the development of the AMC130M03.

Table 9-3. Recommended External Components

COMP	DESCRIPTION	PART NUMBER	MANUFACTURER	SIZE (EIA, L x W)
DVDD				
C15	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
C16	1 µF ± 10%, X7R, 25 V	12063C105KAT2A	AVX	1206, 3.2 mm x 1.6 mm
DC/DC CONVERTER				
C17	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C1	1 nF ± 10%, X7R, 50 V	C0603C102K5RACTU	Kemet	0603, 1.6 mm x 0.8 mm
C6	1 µF ± 10%, X7R, 25 V	CGA3E1X7R1E105K080AC	TDK	0603, 1.6 mm x 0.8 mm
F1, F2	Ferrite bead	74269244182	Wurth Elektronik	0402, 1.0 mm x 0.5 mm
HLDO				
C24	100 nF ± 10%, X7R, 50 V	C0603C104K5RACAUTO	Kemet	0603, 1.6 mm x 0.8 mm
C10	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm
C13	100 nF ± 5%, NP0, 50 V	C3216NP01H104J160AA	TDK	1206, 3.2 mm x 1.6 mm
C11	1 nF ± 10%, X7R, 50 V	12065C102KAT2A	AVX	1206, 3.2 mm x 1.6 mm

9.4 Layout

9.4.1 Layout Guidelines

Figure 9-9 illustrates a layout recommendation with the critical placement of the decoupling capacitors. The same component reference designators are used as in the *Power Supply Recommendations* section.

For best EMI performance, do not dedicate a ground plane on the high-side, but connect the ground reference for the high-side (HGND) using individual traces as illustrated in Figure 9-9.

Route digital traces away from all analog inputs and associated components to minimize interference.

Use C0G capacitors on the analog inputs. Use ceramic capacitors (for example, X7R grade) for the power-supply decoupling capacitors. High-K capacitors (Y5V) are not recommended. Place the required capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections on the ground-side connections of the bypass capacitors.

When applying an external clock, make sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer often helps reduce overshoot. Glitches present on the clock input can lead to noise within the conversion data.

9.4.2 Layout Example

Figure 9-9 shows an example layout of the AMC130M03 requiring a minimum of two PCB layers. In general, analog and digital signals for the primary (low) side are partitioned to the right and analog and digital signals for the secondary (high) side are on the left.

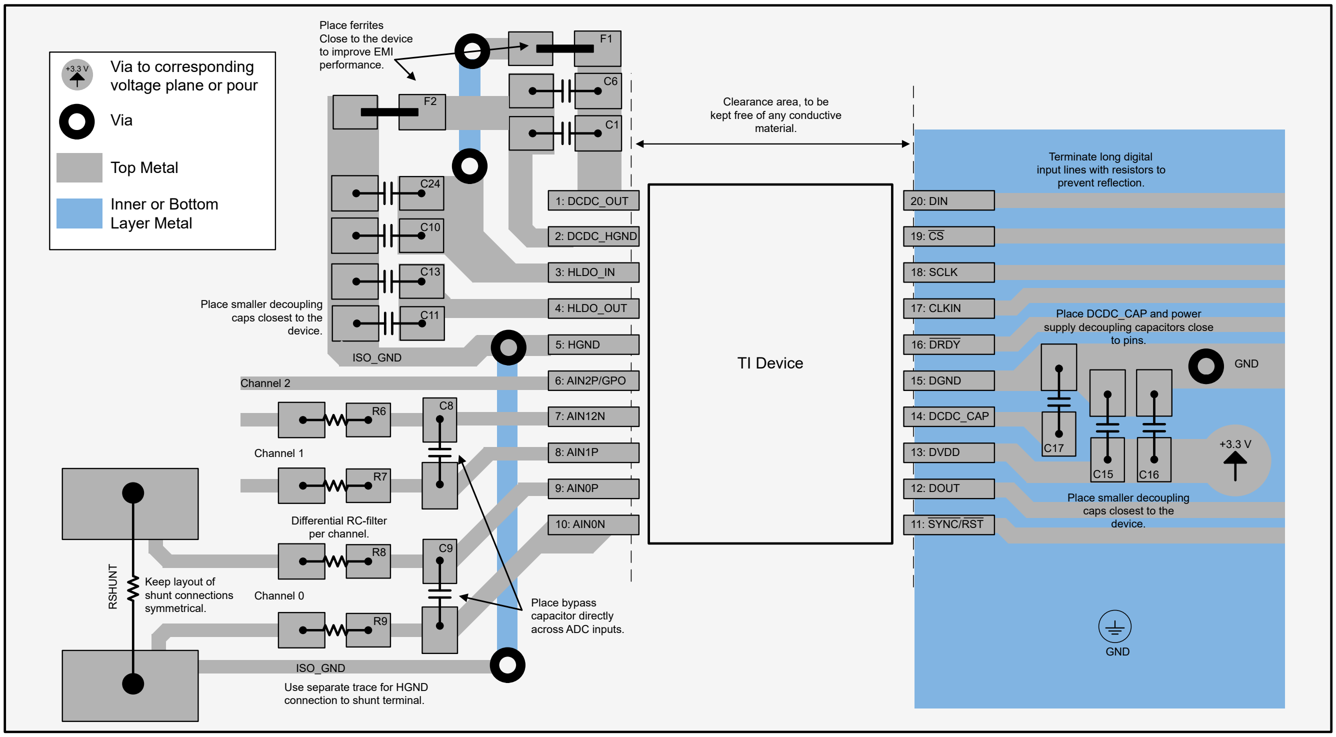


Figure 9-9. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TIDA-010243 Cost-Effective, 3-Phase CT Electricity Meter Reference Design Using Standalone ADC* design guide
- Texas Instruments, *TIDA-010036 One-phase shunt electricity meter reference design using standalone ADCs* design guide
- Texas Instruments, *TIDA-010037 High accuracy split-phase CT electricity meter reference design using standalone ADCs* design guide
- Texas Instruments, *Isolated Voltage-Measurement Circuit With ±250-mV Input and Differential Output* application note
- Texas Instruments, *TMP61 ±1% 10-kΩ Linear Thermistor* data sheet

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC130M03DFMR	ACTIVE	SOIC	DFM	20	850	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	AMC130M03	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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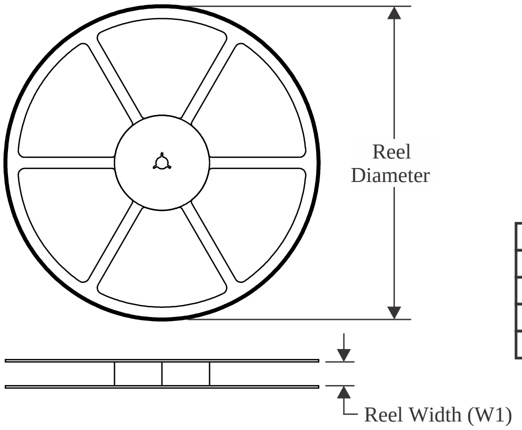
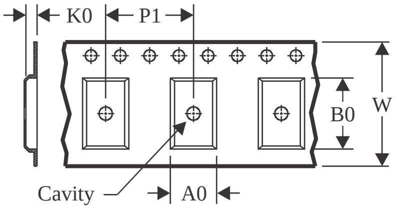
TAPE AND REEL INFORMATION

REEL DIMENSIONS

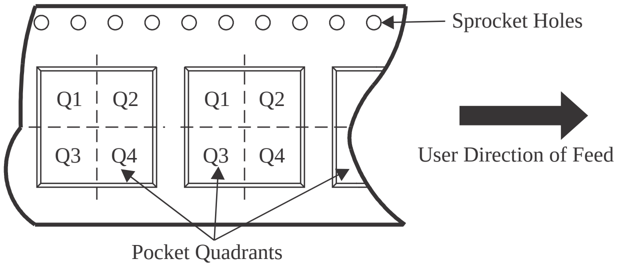


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

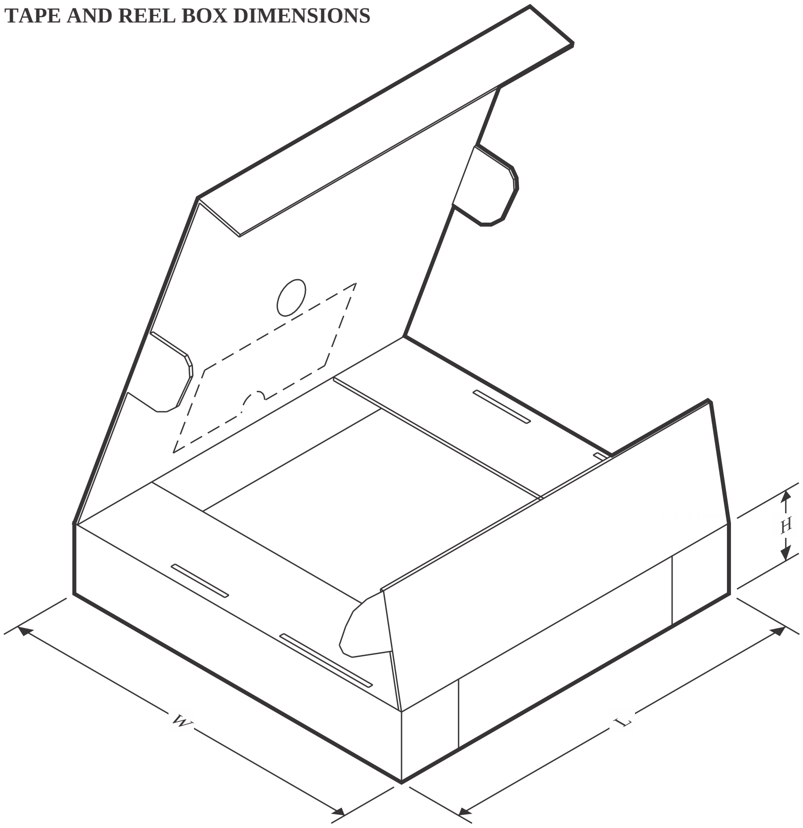
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC130M03DFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

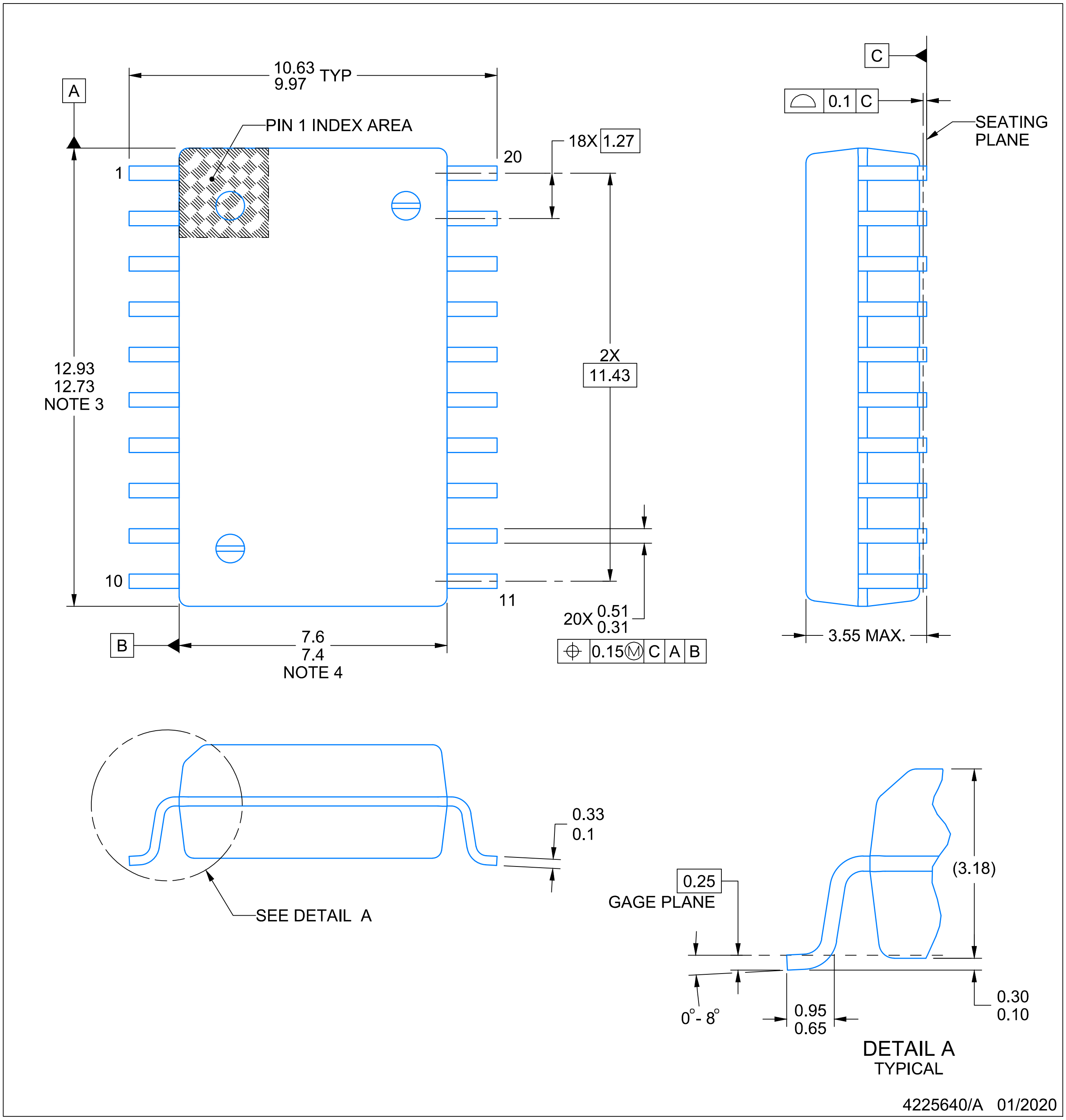
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC130M03DFMR	SOIC	DFM	20	850	350.0	350.0	43.0

PACKAGE OUTLINE

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



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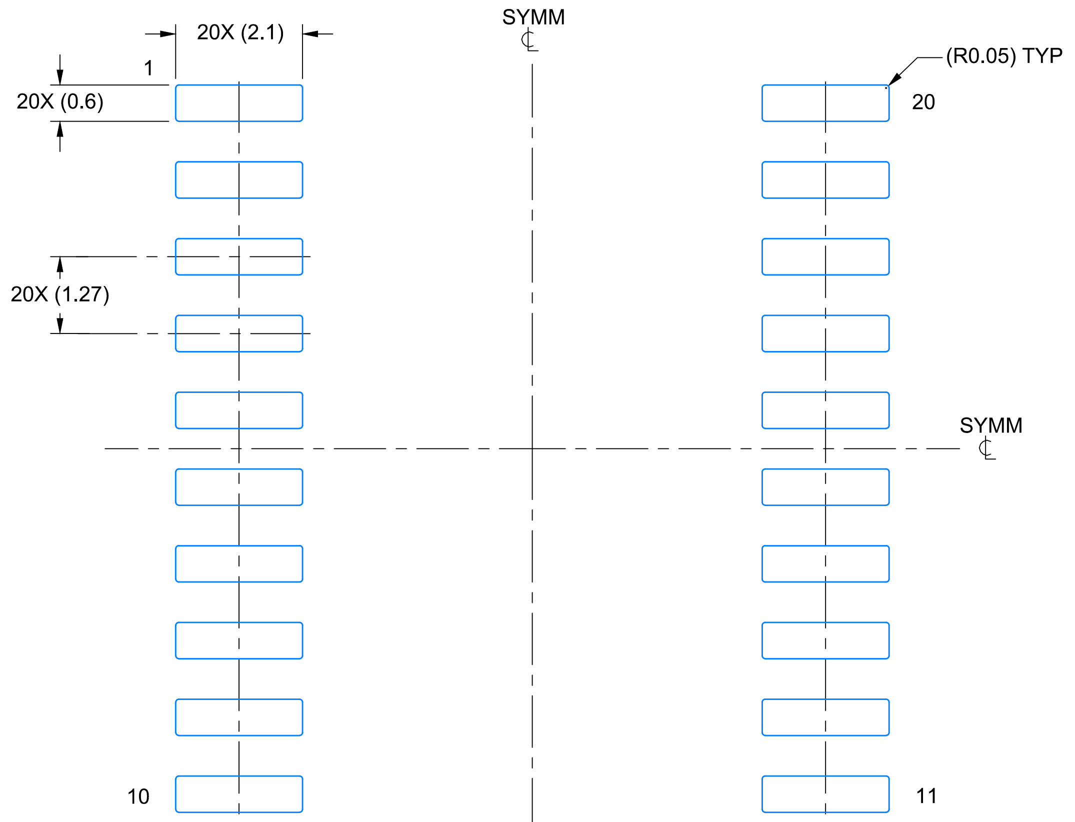
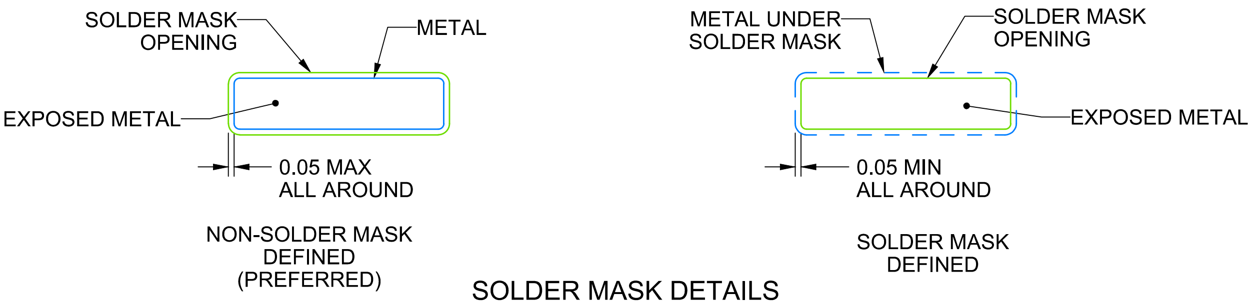
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

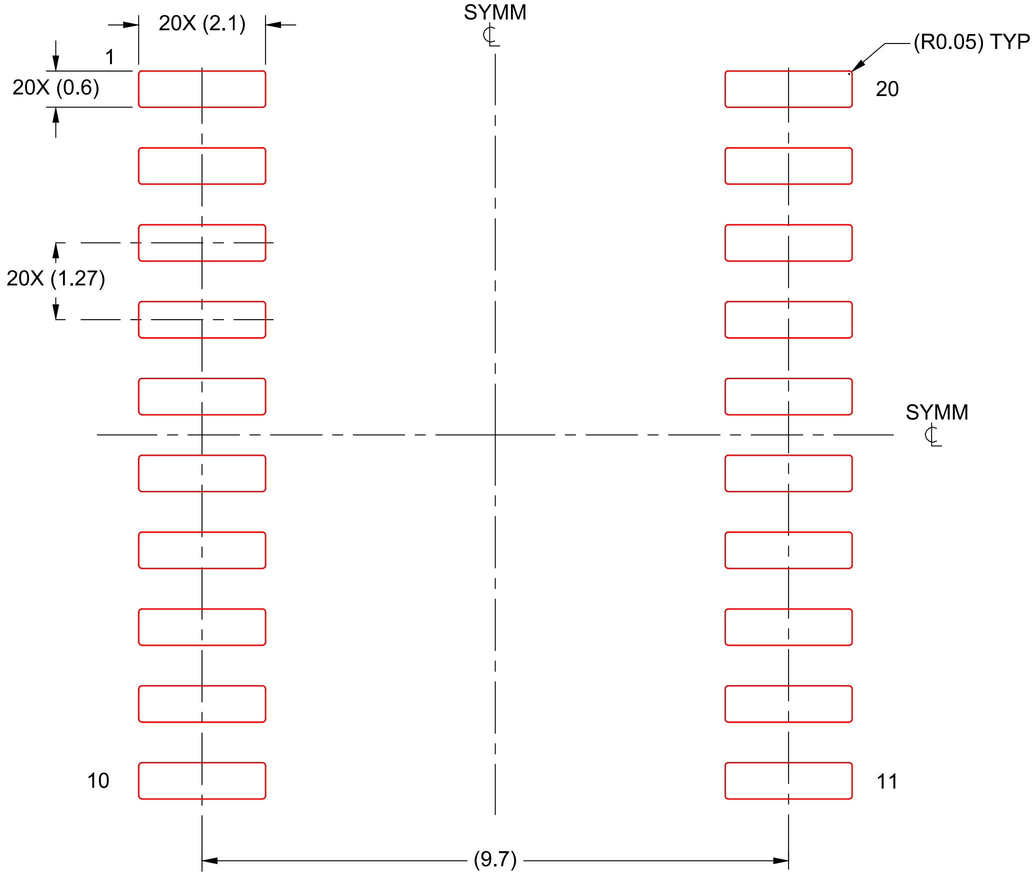


SOLDER MASK DETAILS

4225640/A 01/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225640/A 01/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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