BQ25185 1-Cell, 1A Standalone Linear Battery Charger with Power Path, Factory Mode, and Battery Tracking VINDPM

1 Features

- 1A linear battery charger
  - 3.0V to 18V input voltage operating range
  - 25V tolerant input voltage
  - External resistor programmable operation
    - ILIM/VSET pin sets battery regulation voltage to 3.6V, 3.65V, 4.02V, 4.1V, 4.2V, 4.35V, or 4.4V
    - ILIM/VSET pin sets input current limit to 100mA, 500mA, or 1100mA
    - ISET pin sets charge current from 5mA to 1A
  - Supports Li-ion, Li-poly, and $LiFePO_4$ chemistries
  - 115mΩ battery FET on-resistance
  - Supports up to 3.125A discharge current for high system loads
- Power path management for powering the system and charging the battery
  - Regulated system voltage (SYS) at 4.5V
  - Configurable input current limit
  - Supports USB suspend mode
  - Battery tracking input voltage dynamic power management (VINDPM) for high-impedance input sources
  - Dynamic power path management optimizes charging from weak adapters
- Ultra-low quiescent current
  - 4µA in battery-only mode
  - 30µA input adapter I_Q in sleep mode
  - 3.2µA battery discharge current in factory mode
- Integrated fault protection
  - Input overvoltage protection (VIN_OVP)
  - Battery undervoltage protection (BUVLO)
  - Battery short protection (BATSC)
  - Battery overcurrent protection (BATOCP)
  - Input current limit protection (ILIM)
  - Thermal regulation (TREG) and thermal shutdown (TSHUT)
  - Battery thermal fault protection (TS)
  - Safety timer fault
  - System short protection
  - System overvoltage protection
  - Short and open protection on the ISET and ILIM/VSET pins

2 Applications

- TWS headset and charging case
- Smart glasses, AR and VR
- Smart watches and other wearable devices
- Retail automation and payment
- Building automation

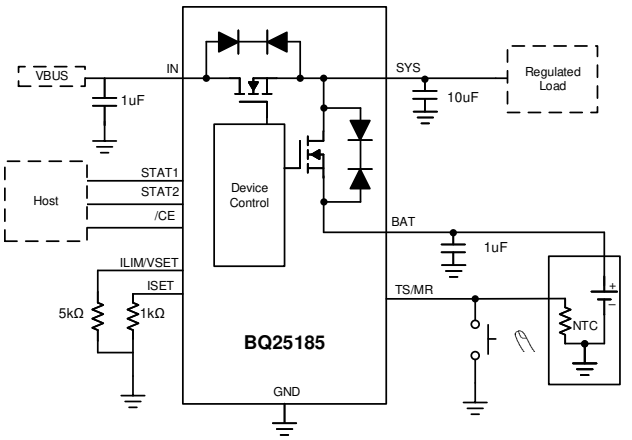
3 Description

The BQ25185 is a linear battery charger IC optimized for small solution size and low quiescent current to extend battery life. The device is available in a small leadless package with a thermal pad for heat dissipation. The device supports up to 1A charging and system loads up to 3.125A.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
BQ25185	DLH (WSON, 10)	2.2mm × 2.0mm	2.2mm x 2.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Description (continued)....3
5 Pin Configuration and Functions....4
6 Specifications....5
6.1 Absolute Maximum Ratings....5
6.2 ESD Ratings....5
6.3 Thermal Information....5
6.4 Recommended Operating Conditions....5
6.5 Electrical Characteristics....6
6.6 Timing Requirements....8
6.7 Typical Characteristics....9
7 Detailed Description....10
7.1 Overview....10
7.2 Functional Block Diagram....14
7.3 Feature Description....14
7.4 Device Functional Modes....19
8 Application and Implementation....20
8.1 Application Information....20
8.2 Typical Application....20
8.3 Power Supply Recommendations....23
8.4 Layout....23
9 Device and Documentation Support....24
9.1 Device Support....24
9.2 Receiving Notification of Documentation Updates....24
9.3 Support Resources....24
9.4 Trademarks....24
9.5 Electrostatic Discharge Caution....24
9.6 Glossary....24
10 Revision History....24
11 Mechanical, Packaging, and Orderable Information....25

4 Description (continued)

The battery is charged using a standard Li-ion or $LiFePO_4$ charging profile with three phases: precharge, constant current, and constant voltage. Thermal regulation provides the maximum charge current while managing the device temperature. The charger is optimized for battery-to-battery charging with 3V minimum input voltage operation and can withstand 25V absolute maximum line transients. The device integrates a single pushbutton input to reduce the total solution footprint.

5 Pin Configuration and Functions

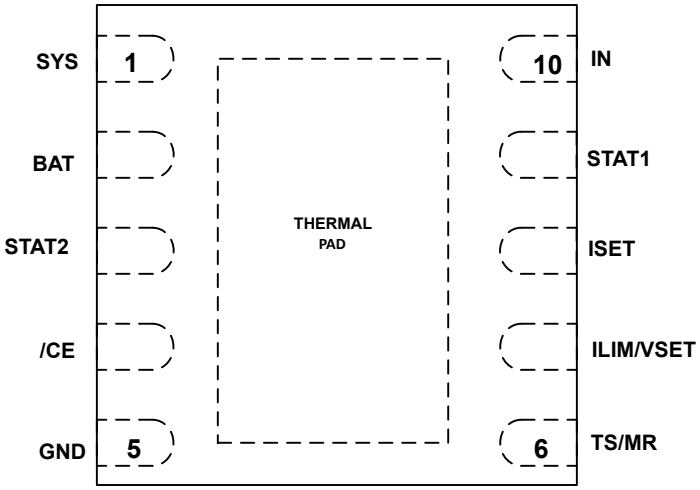


Figure 5-1. DLH Package 10-Pin (top view)

Table 5-1. Pin Functions

Pin		I/O [1]	Description
Name	NO.		
IN	10	P	DC input power supply. Connect IN to the external DC supply. Bypass IN to GND with at least 1µF of capacitance using a ceramic capacitor.
SYS	1	P	Regulated system output. Connect at least a 10µF ceramic capacitor (at least 1µF of capacitance after DC bias derating) from SYS to GND as close as possible to the SYS and GND pins.
BAT	2	P	Battery connection. Connect BAT to the positive terminal of the battery. Bypass BAT to GND with at least 1µF of capacitance using a ceramic capacitor.
GND	5	-	Ground connection. Connect to the ground plane of the circuit.
ILIM/VSET	7	I/O	Input current limit and battery regulation voltage program input. See also Section 8.3.6 ILIM/VSET Control.
ISET	8	I/O	Fast charge current program input. An RC is recommended for low charge current values. Using only one resistor on the ISET pin is preferred. See also Section 8.1.1.4 ISET Pin Detection.
STAT1	9	O	Open-drain status output. Can be pulled up with a 1kΩ to 20kΩ resistor. Typical pull-up voltage = 1.8V. Maximum pull-up voltage = 5V. See also Section 8.3.10 Status Pins. Can be left floating if unused.
TS/MR	6	I/O	Manual reset input and NTC thermistor input. TS/MR is a general-purpose input that must be held low for longer than t_{LPRESS} to enter factory mode. TS/MR may be driven by a momentary pushbutton or a MOSFET. The TS/MR pin can also have an NTC thermistor connected to it. See also Section 8.3.9 External NTC Monitoring (TS).
$\overline{CE}$	4	I	Charge enable active-low input. Connect $\overline{CE}$ to a high logic level to disable charging. Connect $\overline{CE}$ to a low logic level to enable charging.
STAT2	3	O	Open-drain status output. Can be pulled up with a 1kΩ to 20kΩ resistor. Typical pull-up voltage = 1.8V. Maximum pull-up voltage = 5V. See also Section 8.3.10 Status Pins. Can be left floating if unused.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	IN	-0.3	25	V
Voltage	All other pins	-0.3	5.5	V
Input current (DC)	IN		1.1	A
SYS discharge current (DC)	SYS		3.125	A
Output sink current	STAT1, STAT2		20	mA
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		BQ25185 DLH 10	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC(1))	68.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	34.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BAT}	Battery voltage range	2.2		4.6	V
V_{IN}	Input voltage range	2.7		5.5	V
I_{IN}	Input current range (IN to SYS)			1.1	A
I_{BAT}	Battery discharge current (BAT to SYS)			3.125	A

6.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature range	-40		125	°C

6.5 Electrical Characteristics

V_{IN} = 5 V, V_{BAT} = 3.6 V. -40°C < T_J < 125°C unless otherwise noted. Typical data at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
I_{Q_IN}	Input supply quiescent current	V_{BAT} = 3.6V, V_{IN} = 5V, Charge enabled, I_{CHG} = 0mA, SYSREG = 4.5V		0.75	1	mA
I_{SLEEP_IN}	Sleep mode input current	V_{IN} = 3.6V, V_{BAT} = 3.7V		30		µA
I_{Q_BAT}	Battery quiescent current	V_{IN} < V_{UVLO}, V_{BAT} = 3.6V, 0°C < T_J < 85°C		4	5	µA
I_{BAT_FACT}	Battery discharge current in factory mode	V_{BAT} = 3.6V, 0°C < T_J < 85°C		3.2	5	µA
POWER-PATH MANAGEMENT AND INPUT						
V_{IN_OP}	Input voltage operating range		3.6		18	V
V_{IN_UVLOZ}	Exit input undervoltage lockout	V_{IN} rising			3	V
V_{IN_UVLO}	Enter input undervoltage lockout	V_{IN} falling			2.7	V
V_{IN_LOWV}	V_{IN} threshold to start charging	V_{IN} rising		3	3.15	V
V_{IN_LOWVZ}	V_{IN} threshold to stop charging	V_{IN} falling		2.95	3.1	V
V_{IN_PORZ}	V_{IN} threshold to enter factory mode	V_{IN} falling	1.09	1.3	1.66	V
V_{SLEEPZ}	Exit sleep mode threshold	V_{IN} rising, V_{IN} - V_{BAT}, V_{BAT} = 4V, VINDPM_ACTIVE = 1	122	152	188	mV
V_{SLEEPZ}	Exit sleep mode threshold	V_{IN} rising, V_{IN} - V_{BAT}, V_{BAT} = 4V, VINDPM_ACTIVE = 0	168	208	262	mV
V_{SLEEP}	Enter sleep mode threshold	V_{IN} falling, V_{IN} - V_{BAT}, V_{BAT} = 4V, VINDPM_ACTIVE = 1		82		mV
V_{SLEEP}	Enter sleep mode threshold	V_{IN} falling, V_{IN} - V_{BAT}, V_{BAT} = 4V, VINDPM_ACTIVE = 0		82		mV
V_{SLEEP}	Enter sleep mode threshold	V_{IN} falling, V_{IN} - V_{BAT}, V_{BAT} = 4V		82		mV
V_{SLEEPZ}	Exit sleep mode threshold	V_{IN} rising, V_{IN} - V_{BAT}, V_{BAT} = 4V	110	152	188	mV
V_{IN_OVP}	V_{IN} overvoltage rising threshold	V_{IN} rising	18	18.5	19	V
$V_{IN\_OVP\_HYS}$	V_{IN} overvoltage hysteresis	V_{IN} falling		500		mV
I_{BAT_OCP}	BATOCP (reverse OCP only)	V_{BAT} = 4V		3.13		A
I_{BAT_OCPACC}	BATOCP accuracy	I_{BAT} = 3.125A, T_J = 27°C			18	%
V_{BSUP1}	Enter supplement mode threshold	V_{BAT} = 3.6V, V_{BAT} > V_{BUVLO}, V_{SYS} < V_{BAT} - V_{BSUP1}		40		mV
V_{BSUP2}	Exit supplement mode threshold	V_{BAT} > V_{BUVLO}, V_{SYS} > V_{BAT} - V_{BSUP2}		20		mV
ILIM	Input current limit	V_{IN} = 5V, ILIM = 100mA	80	90	98	mA
		V_{IN} = 5V, ILIM = 500mA	450	475	498	mA
		V_{IN} = 5V, ILIM = 1050mA	995	1050	1100	mA
V_{INDPM}	V_{IN} threshold when input current is reduced			V_{BAT} + V_{INDPM_TRACK}		V
V_{INDPM_TRACK}	V_{IN} threshold offset for when input current is reduced and when V_{BAT} > 3.5V	V_{INDPM} target = V_{BAT} + V_{INDPM_TRACK}		330		mV

6.5 Electrical Characteristics (continued)

V_{IN} = 5 V, V_{BAT} = 3.6 V. -40°C < T_J < 125°C unless otherwise noted. Typical data at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DPPM}	V_{SYS} threshold when charge current is reduced	V_{BAT} = 3.6V, V_{SYS} = V_{DPPM} + V_{BAT} before charge current is reduced		0.1		V
V_{SYS_REG}	SYS regulation voltage	V_{IN} = 5V, V_{BATREG} ≤ 4.3V		4.5		V
$V_{SYS\_REG\_ACC}$	SYS regulation accuracy	V_{IN} = 5V, V_{BAT} = 3.6V, R_{SYS} = 100Ω	-2		2	%
V_{MINSYS}	Minimum V_{SYS} when in battery tracking mode	V_{BAT} < 3.6V		3.8		V
R_{SYS_PD}	SYS pull-down resistance	V_{SYS} = 3.6V		20		Ω
V_{SYS_SHORT}	V_{SYS} threshold for detecting SYS_SHORT condition has occurred	200mV hysteresis		1.6		V
BATTERY CHARGER						
R_{ON_BAT}	Battery FET on-resistance	V_{BAT} = 4.5V, I_{BAT} = 400mA		115	140	mΩ
R_{ON_IN}	Input FET on-resistance	V_{IN} = 5V, I_{IN} = 1A		330	470	mΩ
V_{REG_RANGE}	Typical BAT charge voltage regulation range		3.6		4.4	V
V_{REG_ACC}	BAT charge voltage accuracy, summary for all settings	All V_{BATREG} settings, typical measurement at V_{BATREG} = 4.2V	–0.5		0.5	%
I_{CHG_RANGE}	Typical charge current regulation range	V_{BAT} > V_{LOWV}	5		1000	mA
V_{ISET}	ISET pin voltage when in regulation	I_{BAT} = I_{CHG}		1		V
K_{ISET}	Charge current setting factor, I_{CHG} = K_{ISET} / R_{ISET}	10mA < I_{CHG} < 1000mA	285	300	315	AΩ
I_{CHG_ACC}	Charge current accuracy	V_{IN} = 5V, fast charge current ≥ 40mA	–10		10	%
I_{CHG}	Charge current accuracy at 800 mA	R_{ISET} = 375Ω, V_{BAT} = 3.8V	720	800	880	mA
	Charge current accuracy at 500 mA	R_{ISET} = 600Ω, V_{BAT} = 3.8V	450	500	550	mA
	Charge current accuracy at 150 mA	R_{ISET} = 2.0kΩ, V_{BAT} = 3.8V	135	150	165	mA
	Charge current accuracy at 10 mA	R_{ISET} = 30kΩ, V_{BAT} = 3.8V	9	10	11	mA
I_{PRECHG}	Typical precharge current, as percentage of I_{CHG}	V_{BAT} < V_{LOWV}		20		%
I_{PRECHG_ACC}	Precharge current accuracy	Fast charge current ≥ 40mA	–10		10	%
I_{PRECHG_ACC}	Precharge current accuracy at I_{CHG} = 800 mA	R_{ISET} = 375Ω, V_{BAT} = 2.5V	144	160	176	mA
I_{PRECHG_ACC}	Precharge current accuracy at I_{CHG} = 500 mA	R_{ISET} = 600Ω, V_{BAT} = 2.5V	90	100	110	mA
I_{PRECHG_ACC}	Precharge current accuracy at I_{CHG} = 150 mA	R_{ISET} = 2.0kΩ, V_{BAT} = 2.5V	26.5	30	34.5	mA
I_{PRECHG_ACC}	Precharge current accuracy at I_{CHG} = 10 mA	R_{ISET} = 30kΩ, V_{BAT} = 2.5V	1.6	2	2.4	mA
I_{TERM}	Typical termination current, as percentage of I_{CHG}	V_{BAT} = V_{BATREG}		10		%
I_{TERM_ACC}	Termination current accuracy	I_{BAT} = 3mA (I_{CHG} = 150mA) T_J = 25°C	–15		10	%
V_{LOWV}	Precharge to fast charge transition threshold	V_{BAT} rising	2.9	3	3.1	V
V_{LOWV_HYS}	Battery LOWV hysteresis			100		mV
V_{BUVLO}	Battery UVLO	V_{BAT} falling		3		V
V_{BUVLO_HYS}	Battery UVLO hysteresis	V_{BAT} rising, V_{IN} = 5V	110	150	190	mV
V_{BUVLO_HYS}	Battery UVLO hysteresis	V_{BAT} rising, V_{IN} = 0V	90	150	210	mV
V_{RCH}	Battery recharge threshold	V_{IN} = 5V, Charge enabled, V_{BAT} falling from V_{BATREG}		100		mV

6.5 Electrical Characteristics (continued)

V_{IN} = 5 V, V_{BAT} = 3.6 V. -40°C < T_J < 125°C unless otherwise noted. Typical data at T_J = 25°C

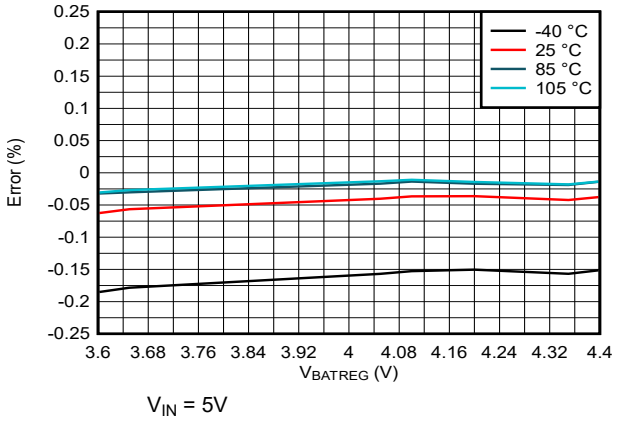
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATSC}	Short on battery threshold for trickle charge, V_{BAT} rising		1.6	1.8	2.0	V
V_{BATSC_HYS}	Battery short circuit voltage hysteresis			200		mV
I_{BATSC}	Trickle charge current	V_{BAT} < V_{BATSC}		7		mA
R_{ISET_SHORT}	Resistor value considered short	R_{ISET} below this range at startup, charger does not initiate charge, power cycle or $\overline{CE}$ toggle to reset			264	Ω
TEMPERATURE REGULATION AND TEMPERATURE SHUTDOWN						
T_{REG}	Typical junction temperature regulation			100		°C
T_{SHUT_RISING}	Thermal shutdown rising threshold	Temperature increasing		150		°C
$T_{SHUT\_FALLING}$	Thermal shutdown falling threshold	Temperature decreasing		135		°C
BATTERY NTC MONITOR						
V_{HOT_ENTRY}	High temperature trip point	Battery charging, $V_{TS/MR}$ falling	0.1050	0.1150	0.1250	V
V_{COLD_ENTRY}	Low temperature trip point	Battery charging, $V_{TS/MR}$ rising	0.9575	1.0075	1.0575	V
V_{HOT_EXIT}	Hysteresis on high trip point	Battery charging, $V_{TS/MR}$ rising from V_{HOT_ENTRY}	0.1250	0.1350	0.1450	V
V_{COLD_EXIT}	Hysteresis on low trip point	Battery charging, $V_{TS/MR}$ falling from V_{COLD_ENTRY}	0.7775	0.8200	0.8600	V
PUSHBUTTON TIMERS AND THRESHOLDS						
I_{TSMR}	Adapter present		36.5	38	39.5	µA
V_{TSMR}	TSMR voltage to detect a button press event, adapter present				90	mV
t_{LPRESS}	Long press timer. Time from button press detection to long press action.			10		s
BATTERY CHARGING TIMERS						
t_{MAXCHG}	Charge safety timer			720		min
t_{PRECHG}	Precharge safety timer			0.25 * t_{MAXCHG}		
LOGIC PINS						
V_{IL}	Input low threshold level	V_{PULLUP} = 1.8V, $\overline{CE}$ pin			0.4	V
V_{IH}	Input high threshold level	V_{PULLUP} = 1.8V, $\overline{CE}$ pin	1.3			V
V_{OL}	Output low threshold level	I_L = 5mA, sink current, V_{PULLUP} = 3.3V, STAT1, STAT2 pins			0.4	V
I_{LKG}	High-level leakage current	V_{PULLUP} = 3.3V, STAT1, STAT2 pins			1	µA

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
INPUT					
$t_{VIN\_OVPZ\_DGL}$	V_{IN_OVP} deglitch, V_{IN} falling		30		ms
BATTERY CHARGER					
t_{REC_SC}	Recovery time, BATOCP during battery discharge		250		ms
t_{RETRY_SC}	Retry window for SYS or BAT short circuit recovery (BATOCP)		2		s
t_{BUVLO}	Deglitch time to disconnect the BATFET when V_{BAT} < V_{BUVLO} setting		60		µs

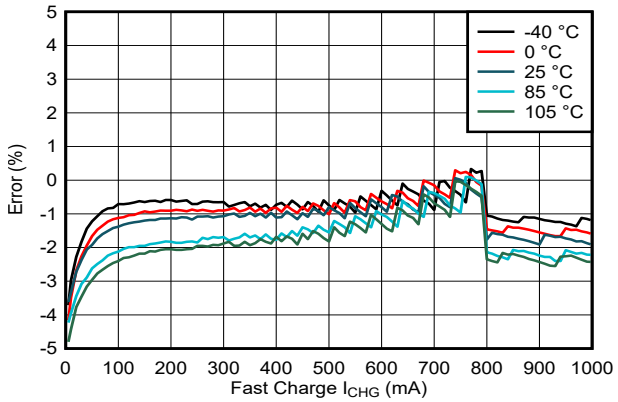
6.7 Typical Characteristics

V_{IN} = 5V, C_{IN} = 2.2µF, C_{OUT} = 10µF, C_{BAT} = 1µF (unless otherwise specified)



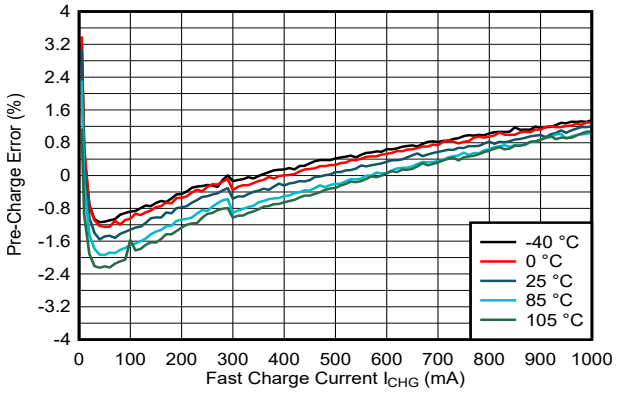
V_{IN} = 5V

Figure 6-1. Battery Regulation Voltage Accuracy vs V_{BATREG} Setting



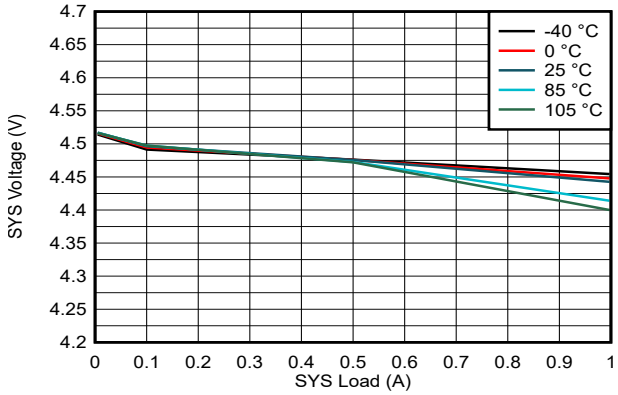
V_{IN} = 5V V_{BAT} = 3.7V

Figure 6-2. Charge Current Accuracy vs I_{CHG} Setting



V_{IN} = 5V V_{BAT} = 3.7V

Figure 6-3. Precharge Accuracy vs Battery Voltage



V_{IN} = 5V V_{BAT} = 3.7V

Figure 6-4. SYS Load Regulation

7 Detailed Description

7.1 Overview

The BQ25185 integrates a linear charger that allows the battery to be charged with a resistor-configurable charge current up to 1A. In addition to the charge current, other charging parameters can be programmed through external resistors, such as the battery regulation voltage and input current limit.

The power path allows the system to be powered from the regulated SYS output, even when the battery is empty or charging, by drawing power from the IN pin. It also prioritizes the system load on SYS, reducing the charging current, if necessary, in order to support the load when input power is limited. If the input supply is removed and the battery voltage is above V_{BUVLO}, SYS will automatically and seamlessly switch to battery power.

Charging occurs through the internal battery MOSFET. There are several loops that influence the charge current: constant current loop (CC), constant voltage loop (CV), input current limit, thermal regulation, VDPPM, and VINDPM. During the charging process, all loops are enabled, and the dominant loop takes control.

The device supports multiple battery chemistries for single-cell applications through adjustable battery regulation voltage (V_{BATREG}) and charge current (I_{CHG}) settings.

7.1.1 Battery Charging Process

When a valid input source is connected (V_{IN} > V_{INDPM} and V_{BAT} + V_{SLEEP} < V_{IN} < V_{IN_OVP}), the state of the $\overline{CE}$ pin and the TS/MR pin determines whether a charge cycle is initiated. When the $\overline{CE}$ pin is set to disable charging, V_{HOT} < $V_{TS/MR}$ < V_{COLD}, and a valid input source is connected, the battery FET is turned off, preventing any charging of the battery. Note that supplement behavior is independent of the $\overline{CE}$ pin. The device can charge a battery as long as V_{IN} is higher than the V_{INDPM} threshold. This threshold allows V_{IN} to be considered "power good" with a very low battery voltage or a 0V battery.

The following figure illustrates a typical charge cycle.

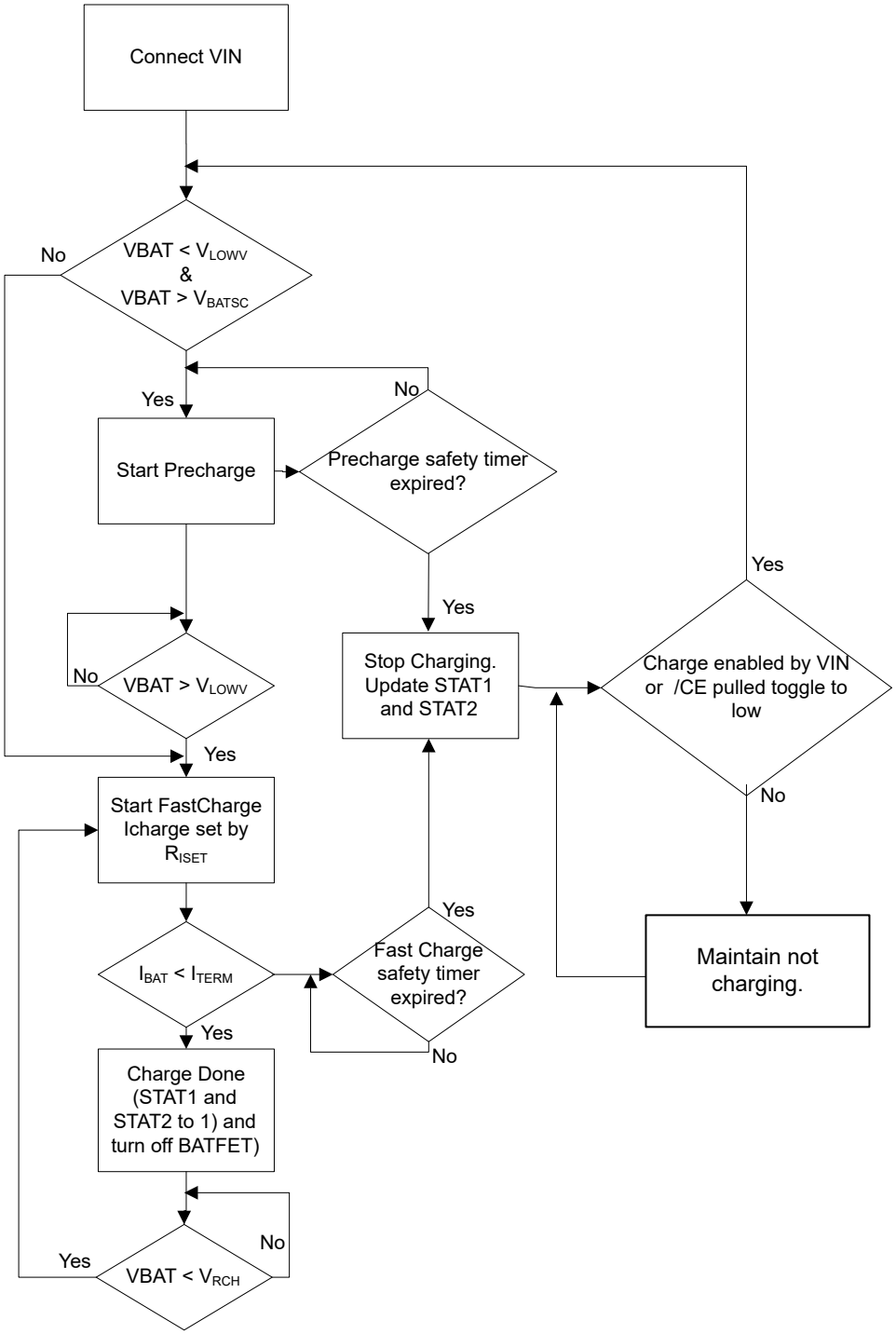


Figure 7-1. Charger Flow Diagram

7.1.1.1 Trickle Charge

To prevent damage to the battery, the device charges the battery at a much lower current level known as trickle charge (I_{BATSC}) when the battery voltage (V_{BAT}) is below the V_{BATSC} threshold. During trickle charge, the device still counts against the precharge safety timer. Rather, trickle charge and precharge are counted against the same duration of 25% of the fast charge timer.

7.1.1.2 Precharge

When the battery voltage is above the V_{BATSC} threshold but lower than the V_{LOWV} threshold, the battery is charged with the precharge current (I_{PRECHG}). The precharge current is 2x the termination current (Section 8.1.1.5 Termination). As a result, the precharge current is 20% of the fast charge current (I_{CHG}).

When the battery voltage reaches the precharge to fast charge transition threshold (V_{LOWV}), the device charges the battery at the fast charge current. If the device does not exit precharge within 25% of the fast charge safety timer, the device will stop charging. See also Section 8.3.7.7 Safety Timer.

7.1.1.3 Fast Charge

The charger has two main control loops that control charging when $V_{BAT} > V_{LOWV}$: the constant current (CC) and constant voltage (CV) loops. When the CC loop is dominant, typically when $V_{BAT} < V_{BATREG} – V_{RCH}$, the battery is charged at the maximum charge current level I_{CHG}, unless there is a TS fault condition, VINDPM, thermal regulation, or DPPM is active (see respective sections for details on these modes of operation). Once the battery voltage approaches the V_{BATREG} level, the CV loop becomes more dominant and the charging current starts tapering off as shown in Typical Charging Profile of a Battery. Once the charging current reaches the termination current (I_{TERM}), charging is done, and the STAT1 and STAT2 pins change to indicate charge complete.

7.1.1.4 ISET Pin Detection

After a valid V_{IN} is applied and the $\overline{CE}$ pin is pulled LOW, the device checks the resistor on the ISET pin for a short circuit ($R_{ISET} < R_{ISET\_SHORT}$). If a short is detected, the charger remains in the fault state until V_{IN} or the $\overline{CE}$ pin is toggled. If the ISET pin is an open circuit, the charger charges with a very low charging current on the order of 1.5mA. This pin is monitored during charging, and changes in R_{ISET} while charging immediately affect the charge current. An external pull-down resistor (±1% or better recommended to minimize charge current error) from the ISET pin to GND sets the charge current as:

$$I_{CHG} = (K_{ISET}) / (R_{ISET}) \quad (1)$$

- I_{CHG} is the desired fast charge current
- K_{ISET} is a gain factor found in the Electrical Characteristics table (typically 300AΩ)
- R_{ISET} is the pull-down resistor from the ISET pin to GND

For charge currents below 50mA, an extra RC circuit using 50pF capacitance is recommended on the ISET pin to improve signal stability. The ISET pin can also be used to monitor device current when the device is not in I_{CHG} regulation. The voltage on the ISET pin is proportional to the charging current. To measure the charge current while charging, the following formula can be used:

$$I_{CHG} = (K_{ISET}\ V_{ISET}) / (R_{ISET}) \quad (2)$$

- V_{ISET} is the measured voltage on the ISET pin in volts
- I_{CHG} is the calculated charge current

7.1.1.5 Termination

As the CV loop becomes dominant over the CC loop during fast charge, the charge current begins to taper and approaches the I_{TERM} threshold. The device terminates at 10% of I_{CHG}.

When I_{TERM} is reached during the CV phase, the charger automatically terminates charging by disabling the BATFET (disconnecting the battery from SYS) to enter high impedance mode. If a regulation loop such as VINDPM, DPPM, or thermal regulation is active during the CV taper, termination does not occur. Charge current continues to taper due to the active regulation loop and CV, but the device does not terminate charging.

Termination only occurs when the CV loop is dominant and no other regulation loop is actively reducing the charge current. After termination, the battery FET is disabled and the device monitors the BAT pin voltage. If the BAT pin voltage drops below the battery regulation voltage (V_{BATREG}) by the recharge threshold (V_{RCH}), a new charge cycle is started and the safety timers are reset.

During charging, or after charging is complete, a higher SYS load is supported through supplement mode.

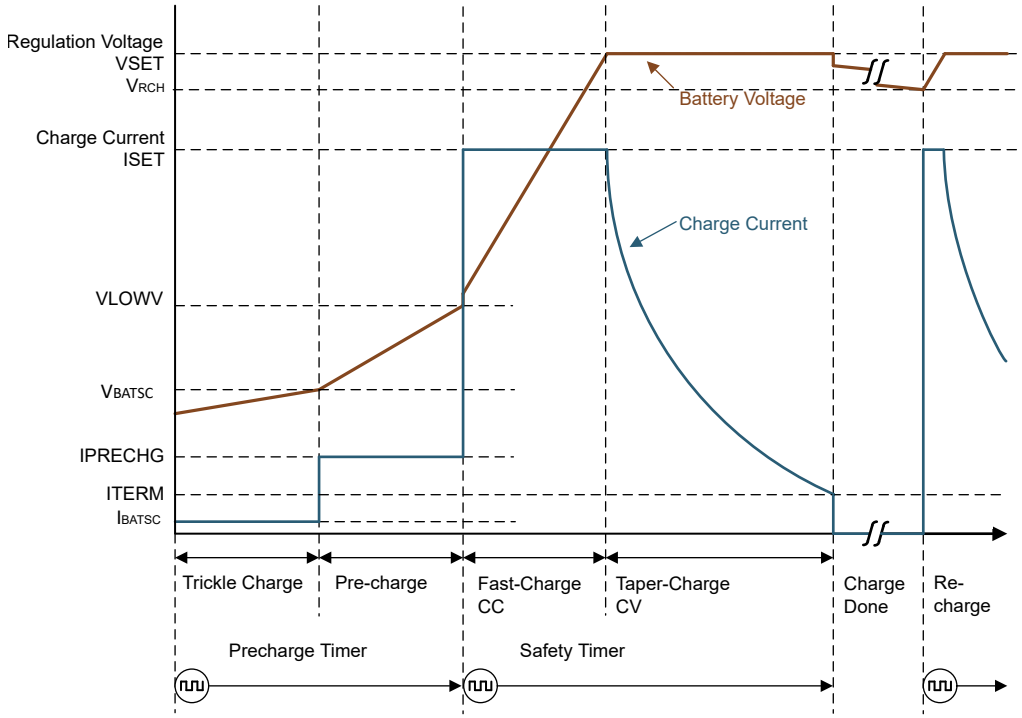
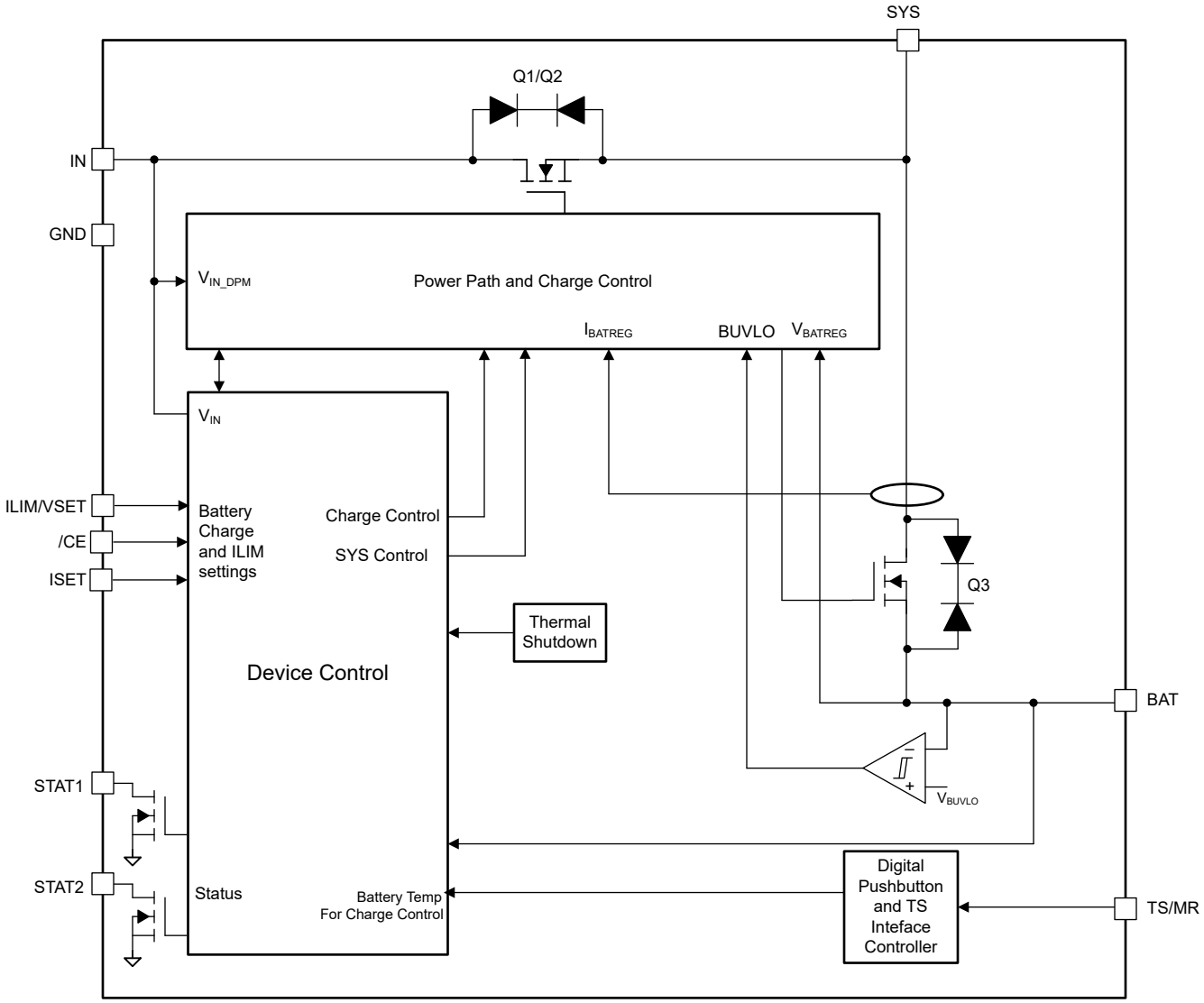


Figure 7-2. Typical Charging Profile of a Battery

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage Based Dynamic Power Management (VINDPM)

The VINDPM loop prevents the input voltage from collapsing to a level that would interrupt charging. The loop reduces the current drawn by the charger to maintain the input voltage above the VINDPM threshold (V_{INDPM}).

During normal charging, if the input power source cannot support the programmed or default charging current and system load, the supply voltage decreases. When the supply drops to the V_{INDPM} threshold, the input DPM current and voltage loops reduce the input current through the blocking FETs to prevent further drop of the supply voltage.

The VINDPM threshold is typically 300mV above V_{BAT}. If the device is not operating in battery tracking VINDPM due to battery voltage, the input is regulated to 3.6V. Termination is disabled when VINDPM is active.

7.3.2 Dynamic Power Path Management Mode (DPPM)

With a valid input source connected, the power-path management circuitry monitors the input voltage and current continuously. The current into IN is shared at SYS between charging the battery and powering the

system load at SYS. If the sum of the charging and load currents exceeds the preset maximum input current, the input DPM loop reduces the input current. If SYS drops below the DPPM voltage threshold, the charging current is reduced by the DPPM loop through the BATFET. If SYS falls below the supplement mode threshold after the charging current is reduced to zero, the device will enter supplement mode. SYS voltage is maintained above battery voltage when the DPPM loop is in control. Termination is disabled when the DPPM loop is active.

The V_{DPPM} threshold is typically 100mV above V_{BAT}.

7.3.3 Battery Supplement Mode

While in DPPM mode, if the charging current falls to zero and the system load current increases beyond the programmed input current limit, the voltage at SYS decreases. When the SYS voltage drops below the battery voltage to V_{BSUP1}, the battery supplements the input in supplying the system load. The battery stops supplementing the input in supplying the system load when the voltage on the SYS pin rises within the battery voltage to V_{BSUP2}. During supplement mode, the battery supplement current is not regulated, but the BATOCP protection circuit is active. Battery termination is disabled while in supplement mode. Battery voltage must be higher than the battery undervoltage lockout threshold (V_{BUVLO}) to supplement the input in supplying the system load.

7.3.4 Sleep Mode

The device enters the low-power sleep mode if V_{IN} falls below the sleep mode entry threshold and V_{IN} is higher than the undervoltage lockout threshold. In sleep mode, the input is isolated from the battery. This feature prevents draining the battery when V_{IN} is absent. Once $V_{IN} > V_{BAT} + V_{SLEEP}$ and V_{IN} exceeds the V_{INDPM} threshold, the device initiates a new charge cycle.

7.3.5 SYS Regulation

The BQ25185 includes a SYS voltage regulation loop. By regulating the SYS voltage, the device prevents downstream devices connected to SYS from being exposed to voltages as high as V_{IN_OVP}. SYS regulation is active only when $V_{IN} > V_{UVLO}$, $V_{IN} > V_{BAT} + V_{SLEEP}$ and $V_{IN} < V_{IN\_OVP}$.

If the ILIM/VSET pin is configured for a VBATREG setting higher than 4.3V, the device regulates the SYS voltage in battery tracking mode. As the battery voltage increases, V_{SYS} is regulated to 225mV above the battery voltage. If the battery voltage is less than 3.6V, V_{SYS} is regulated to V_{MINSYS}. This regulation ensures proper termination of the battery even if VDPPM is active.

7.3.6 ILIM/VSET Control

The input current limit can be controlled by an external programmable resistor as indicated below.

The ILIM/VSET pin is checked under the following conditions:

- A valid adapter is present on V_{IN} (V_{IN} is considered power good).
- The $\overline{CE}$ pin state is changed to enable charging.
  - Toggle the $\overline{CE}$ pin when the TS/MR pin is not LOW to avoid charging during pin detection.
- The TS/MR pushbutton is not pressed.

If an open is detected on the ILIM/VSET pin, the device disables charging but continues to regulate the SYS pin and limits the input current to 500mA.

If a short is detected on the ILIM/VSET pin, the device stays in battery-only mode.

Table 7-1. ILIM and VBATREG Resistor Map

RESISTOR (kOhm)	CURRENT LIMIT	V_{BATREG} (V)	V_{LOWV} (V)
> 180	ILIM500	Charge Disabled	
130	ILIM500	4.1	3.0
100	ILIM1100		
75	ILIM500	4.4	
56	ILIM1100		
43	ILIM500	4.35	
33	ILIM1100		
24	ILIM100	4.2	
18	ILIM500		
13	ILIM1100		
9.1	ILIM500	4.05	
6.8	ILIM1100		
5.1	ILIM1100	3.65	
3.6	ILIM500	3.6	
2.4	ILIM1100		
< 1.5	Battery-Only Mode		

7.3.7 Protection Mechanisms

7.3.7.1 Input Overvoltage Protection

The input overvoltage protection protects the device and downstream components connected to SYS and BAT against damage from overvoltage on the input supply. When $V_{IN} > V_{IN\_OVP}$, a V_{IN} overvoltage condition is detected. During the V_{IN} overvoltage condition, the device turns on the battery discharge FET and the STAT1 and STAT2 pins update to indicate a recoverable fault (STAT1 = LOW, STAT2 = HIGH). Once the V_{IN} overvoltage condition is removed, the STAT1 and STAT2 pins update to indicate normal operation after the startup routine has finished due to a V_{IN} power good detection. Thereafter, a V_{IN} power good condition is determined if $V_{IN} > V_{BAT} + V_{SLEEP}$.

7.3.7.2 Battery Undervoltage Lockout

To prevent deep discharge of the battery, the device integrates a battery undervoltage lockout feature that disconnects BAT from SYS when the battery voltage drops below the BUVLO threshold.

7.3.7.3 Battery Overcurrent Protection

To protect the device from overcurrent and prevent excessive battery discharge current, the device detects if the current from the battery through the battery FET exceeds the I_{BAT_OCP} threshold. If the BATOCP limit is reached, the battery discharge FET is turned off, and the device enters hiccup mode, re-enabling the BATFET t_{REC_SC} (250ms) after being turned off by the overcurrent condition. If the overcurrent condition is triggered upon retry 4 to 7 consecutive times within a 2s window, the BATFET remains off until a valid V_{IN} is connected (V_{IN} is power good). If the overcurrent condition and hiccup operation occur while in supplement mode, where V_{IN} is already present, V_{IN} must be toggled in order for the BATFET to be enabled and for a new detection cycle to begin.

7.3.7.4 System Overvoltage Protection

The system overvoltage protection prevents the SYS voltage from overshooting to a high voltage due to the input supply. The SYS_OVP momentarily disconnects the blocking FETs and re-engages them when the SYS voltage drops below the SYS_OVP_FALLING threshold.

The SYS_OVP_RISING threshold is 104% to 106% of the target SYS voltage, and the SYS_OVP_FALLING threshold is 101.5% to 103.5% of the target SYS voltage.

7.3.7.5 System Short Protection

System short protection is triggered when the following conditions are met: an adapter is connected, and the device turns on the input FET for 5 ms and detects that the SYS pin is shorted (V_{SYS} < V_{SYS_SHORT}). In this scenario, the device turns off the input FET for 200µs and turns it back on for 5ms to allow V_{SYS} to rise above the V_{SYS_SHORT} threshold. If, after 10 attempts, V_{SYS} does not rise above the V_{SYS_SHORT} threshold, the device disables both the input and BATFET paths and waits for adapter insertion before turning the paths on again. A 2s timer is implemented to refresh the retry counter. After 2s, the device checks again for a system short and repeats the 10 attempts if there is a system short.

7.3.7.6 Thermal Protection and Thermal Regulation

During operation, to protect the device from damage due to overheating, the junction temperature of the die, T_J, is monitored. When T_J reaches T_{SHUT_RISING}, the device stops charging and shuts down V_{SYS}. If T_J > T_{SHUT_RISING} before power is applied to the device (from either the battery or adapter), the input FET and BATFET remain off, regardless of the TS/MR pin. When T_J falls below $T_{SHUT\_FALLING}$, the device automatically powers up if V_{IN} is present or if operating in battery-only mode.

During charging, to prevent the device from overheating, the device monitors the junction temperature of the die and reduces the charge current when T_J reaches the thermal regulation threshold (T_{REG}). If the charge current is reduced to 0, the battery supplies the current needed by the SYS output.

To ensure that the system power dissipation remains within the limits of the device, the power dissipated by the device can be calculated using the following equation:

$P_{DISS} = P_{SYS} + P_{BAT}$ Where:

$P_{SYS} = (V_{IN} – V_{SYS}) * I_{IN}$

$P_{BAT} = (V_{SYS} – V_{BAT}) * I_{BAT}$

The die junction temperature, T_J, can be estimated based on the expected board performance using the following equation:

$T_J = T_A + \theta_{JA} * P_{DISS}$

The θ_{JA} is largely driven by the board layout, board layers, copper thickness and the layout. For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics Application Report*. Under typical conditions, the time spent in this state is very short.

7.3.7.7 Safety Timer

At the beginning of each charge cycle mode (precharge or fast charge), the device starts the respective safety timer. If charging does not terminate before the safety timer, t_{MAXCHG}, expires, or if the device does not exit precharge mode before t_{PRECHG} expires, charging is disabled. The precharge safety timer, t_{PRECHG}, is 25% of t_{MAXCHG}. When a safety timer fault occurs, the STAT1 and STAT2 pins change state to indicate a non-recoverable fault. To clear the safety timer, toggle the $\overline{CE}$ pin or the input power.

7.3.8 Pushbutton Long Press Function

The pushbutton function implemented through the TS/MR pin enables the device to enter factory mode after a long button press. When V_{IN} is present, holding the TS/MR pin LOW for a duration t_{LPRESS} initiates factory mode entry. After this duration, removing V_{IN} places the device into factory mode. When V_{IN} is present, toggling the $\overline{CE}$ pin restarts the long press timer. Connect a valid V_{IN} to wake the device from factory mode. The pushbutton cannot be used to wake the device from factory mode.

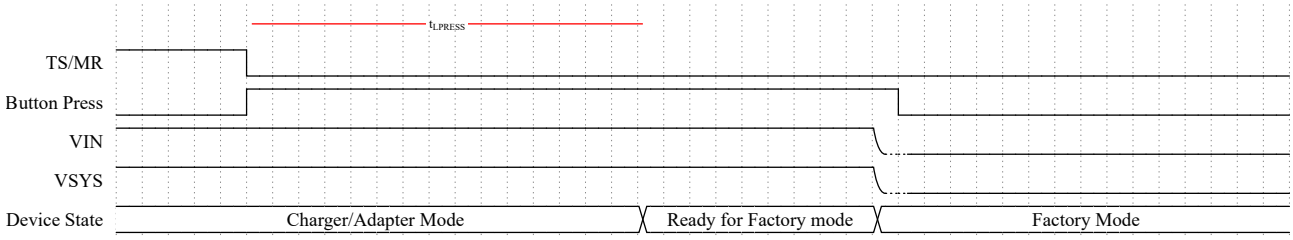


Figure 7-3. Enter Factory Mode

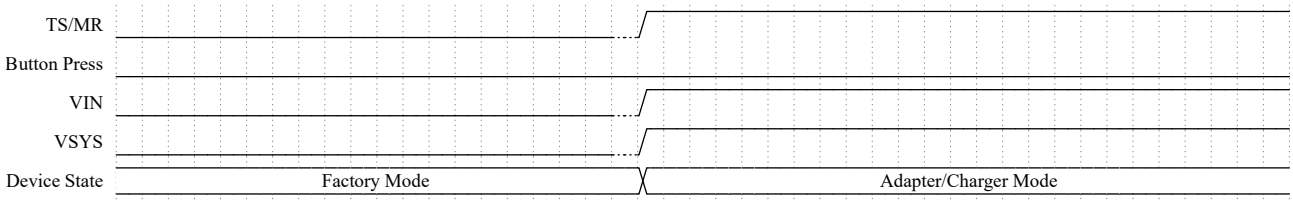


Figure 7-4. Exit Factory Mode

7.3.9 External NTC Monitoring (TS)

7.3.9.1 TS Biasing and Function

The device supports hot and cold battery temperature monitoring. Two temperature thresholds are monitored: the cold battery threshold and the hot battery threshold. These temperature thresholds correspond to the V_{COLD} and V_{HOT} thresholds in the Electrical Characteristics table. Charging and safety timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$.

The TS function is configured for use with an NTC thermistor with a resistance of 10kΩ at 25°C and a beta value of β(25/85) = 3435K. If a different NTC is used, compensating resistors may be required on the TS/MR pin.

If the TS function is not required, connect a 10kΩ resistor from the TS/MR pin to GND.

An active voltage clamp prevents the voltage on the TS/MR pin from exceeding the V_{TS_CLAMP} threshold. This clamp is active when the TS/MR pin is floating.

When a button press is detected during charging, charging is temporarily suspended until the button is released. If charging is disabled due to a TS fault, trickle charging is also disabled.

7.3.10 Status Pins

The device includes two open-drain configuration status pins (STAT1 and STAT2), which can be externally pulled up and connected to an LED or an I/O pin of an MCU to indicate the charger status to the host or user. These pins can be left floating if unused.

When no battery is present, the device charges the capacitor on the BAT pin and toggles between charging and charge completed states. During this condition, the STAT1 pin remains stable, while the STAT2 pin toggles between HIGH and LOW.

Table 7-2. Status Pins State Table

CHARGING STATE	STAT1 PIN STATE	STAT2 PIN STATE
Charge completed, charger in sleep mode or charge disabled (including $V_{BAT} > V_{RCH}$)	HIGH	HIGH
Normal charging in progress (including automatic recharge)	HIGH	LOW
Recoverable fault (VIN_OVP, TS HOT, TS COLD, TSHUT, system short protection)	LOW	HIGH
Non-recoverable or latch-off fault (ILIM/ISET pin short, BATOCP, safety timer expired)	LOW	LOW

7.4 Device Functional Modes

The BQ25185 has three main modes of operation: adapter mode (when a supply is connected to IN), battery-only mode (when only the battery is connected), and factory mode (when only the battery is connected and V_{SYS} is disabled). The following table summarizes the functions that are active in each mode of operation.

FUNCTION	ADAPTER MODE	BATTERY-ONLY MODE	FACTORY MODE
Input Overvoltage	Yes	Yes	No
Input Undervoltage	Yes	Yes	Yes
Battery Overcurrent	Yes	Yes	Yes
Input DPM	Yes	No	Yes
Dynamic Power Path Management	Yes	No	No
BATFET	Yes	Yes	No
TS Measurement	Yes	No	No
Battery Charging	Yes	No	No
Input Current Limit	Yes (Selected by $R_{ILIM/VSET}$)	No	No
Pushbutton Input	Yes	No	No
Status Pin	Yes	Yes	No

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

A typical application of the BQ25185 is a standalone, single-cell Li-ion battery charger and power path manager for battery-powered systems such as smartwatches and wireless headsets. A battery thermistor can be connected to the TS/MR pin to allow the device to monitor battery temperature and control charging accordingly. The TS/MR pin can also be connected to a pushbutton that can be used to place the device into factory mode.

8.2 Typical Application

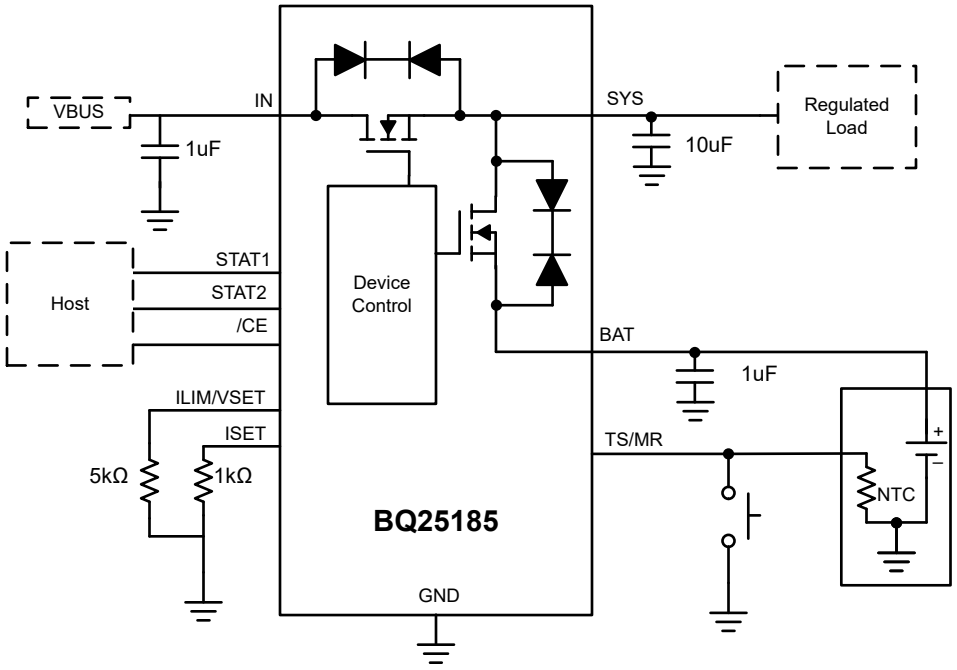


Figure 8-1. Typical Application

8.2.1 Design Requirements

The design requirements for the design example in Figure 9-1 are listed in Table 8-1.

Table 8-1. Design Parameters

PARAMETER	VALUE
IN supply voltage	5V
Battery regulation voltage	4.2V
Fast charge current	300mA
Input current limit	500mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input Current and Battery Regulation Voltage - ILIM/VSET

To configure the device for a battery regulation voltage (V_{BATREG}) of 4.2V and an input current limit of 500mA, set the $R_{ILIM/VSET}$ resistor to 18kΩ. This resistor value is listed in Table 7-1.

8.2.2.2 Fast Charge Current- ISET

To configure the device for a fast charge current of 300mA, set the R_{ISET} resistor to 1kΩ. This resistor value is calculated using the equations provided in Section 8.1.1.4 ISET Pin Detection.

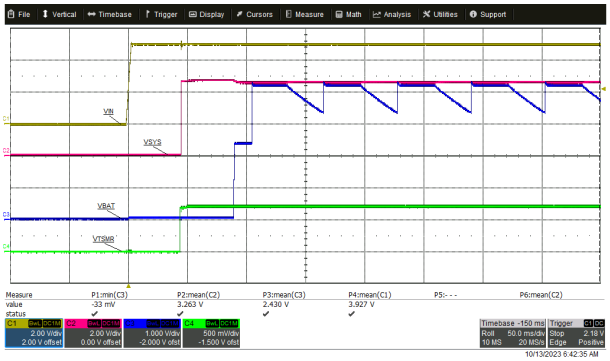
8.2.2.3 Recommended Passive Components

Low ESR ceramic capacitors, such as X7R or X5R, are preferred for input decoupling capacitors and should be placed as close as possible to the supply and ground pins of the IC. Due to voltage derating of the capacitors, it is recommended that 25V rated capacitors are used for the IN and SYS pins, which normally operate at 5V. After derating, the minimum capacitance must be greater than 1µF.

		MIN	NOM	MAX	UNIT
C_{SYS}	Capacitance on SYS pin	1	10	100	µF
C_{BAT}	Capacitance on BAT pin	1	1	-	µF
C_{IN}	Capacitance on IN pin ($t_{VIN\_PRESENT}$ > 25ms)	1			µF

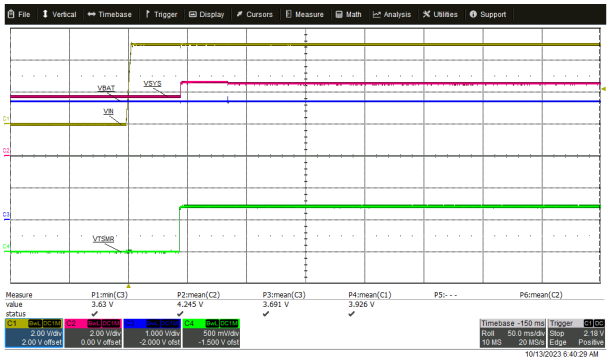
8.2.3 Application Curves

C_{IN} = 1µF, C_{OUT} = 10µF, V_{IN} = 5V, V_{BAT} = 3.7V, I_{CHG} = 100mA (unless otherwise specified)



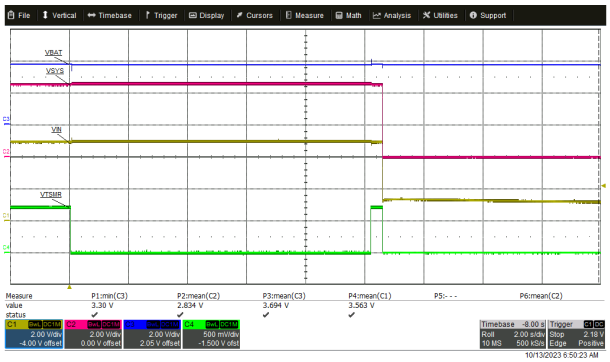
V_{IN} = 5V V_{BAT} = Floating

Figure 8-2. Power Up with IN Supply Insertion with No Battery



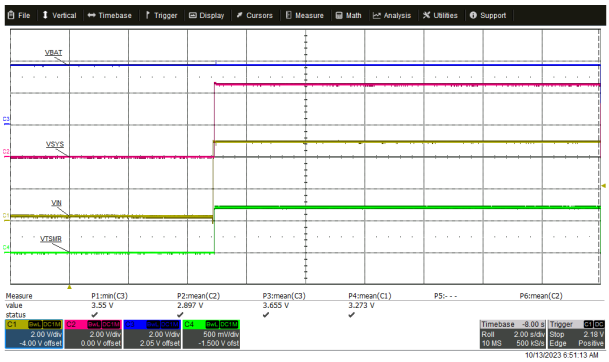
V_{IN} = 5V V_{BAT} = 3.7V

Figure 8-3. Power Up with IN Supply Insertion with Battery



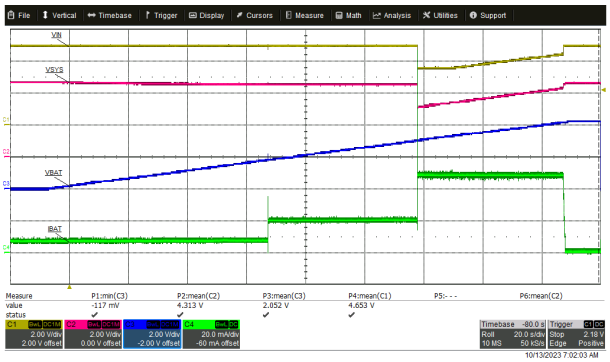
V_{IN} = 5V → 0V V_{BAT} = 3.7V

Figure 8-4. Enter Factory Mode



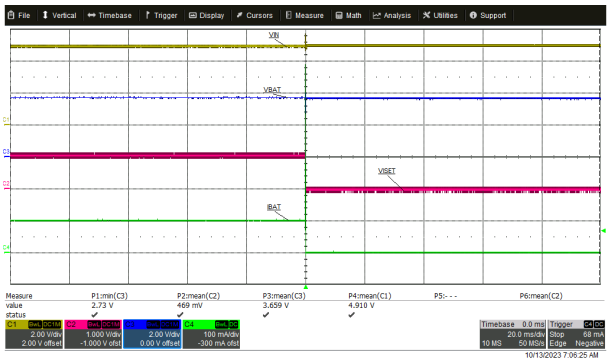
V_{IN} = 0V → 5V V_{BAT} = 3.7V

Figure 8-5. Wake Up from Factory Mode with Adapter Insertion



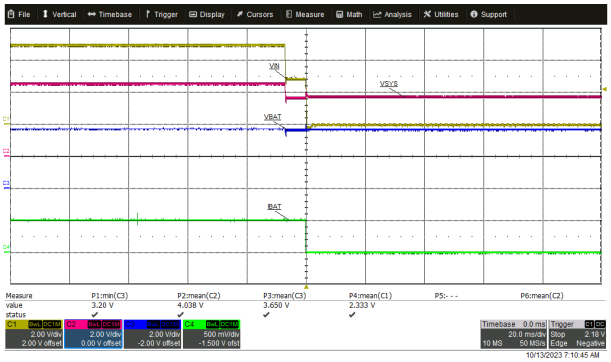
V_{IN} = 5V V_{BAT} = 3.7V I_{CHG} = 100mA
Input Source Current Limit = 50mA

Figure 8-6. Battery Tracking VINDPM



ISET Short While Charging

Figure 8-7. ISET Short Protection



V_{IN} = 5V → 0V
V_{BAT} = 3.7V

Figure 8-8. V_{IN} Power Down with V_{BAT} Present

8.3 Power Supply Recommendations

The BQ25185 requires the adapter or IN supply to be between 3.3V and 18V. The battery voltage must be greater than 3.15V or V_{BUVLO} to ensure proper operation.

8.4 Layout

8.4.1 Layout Guidelines

- To obtain optimal performance, the decoupling capacitor from IN to GND, the capacitor from SYS to GND, and the capacitor from BAT to GND should be placed as close as possible to the device.
- A solid ground plane tied to the GND pin and thermal pad should be used.
- The pushbutton GND should be connected as close to the device as possible.
- The high-current charge paths into IN, SYS, and BAT must be sized appropriately for the maximum charge current to avoid voltage drops in these traces.

8.4.2 Layout Example

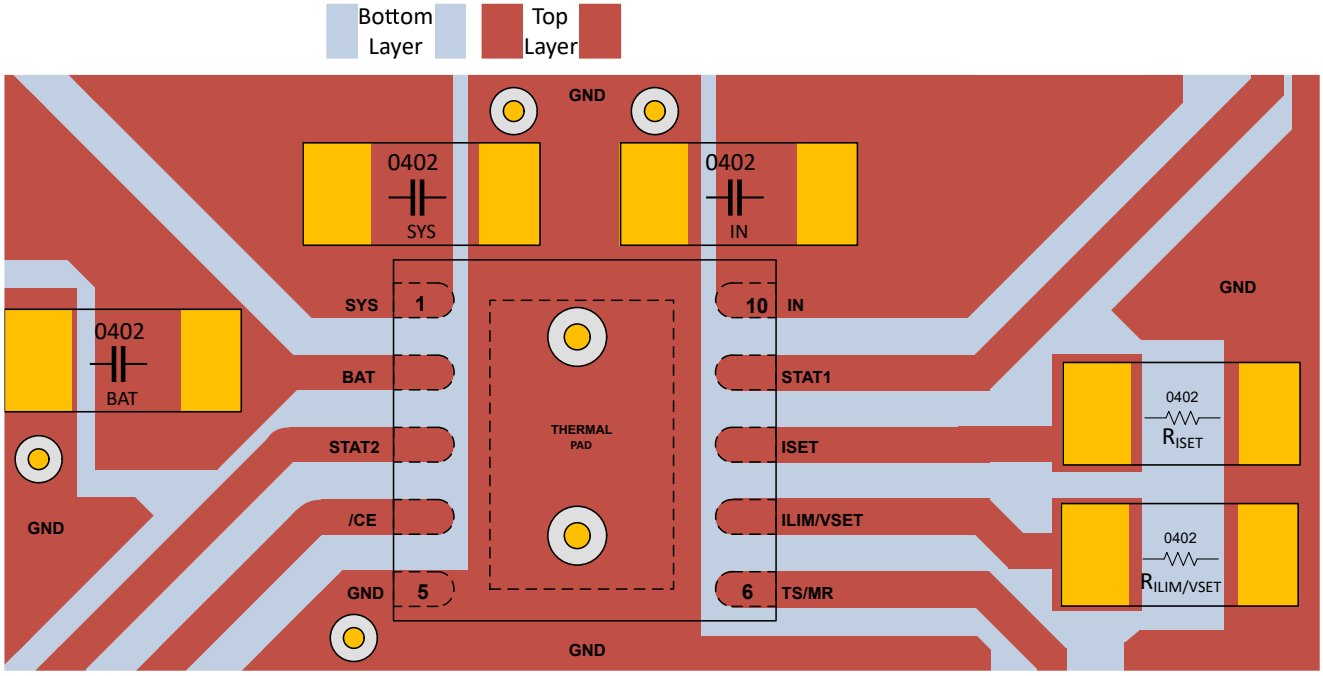


Figure 8-9. Board Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (January 2026)	Page
• Added that the STAT1 and STAT2 pins can be left floating if unused	4
• Changed V_{SLEEPZ} minimum, typical, and maximum values	6
• Changed I_{TERM_ACC} range from ±10% to -15% to 10% and its I_{CHG} test condition from 30 mA to 150 mA	6
• Updated pushbutton functionality	17
• Added details about the NTC thermistor type that the TS feature is configured for	18

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25185DLHR	Active	Production	WSON (DLH) | 10	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B185
BQ25185DLHR.A	Active	Production	null (null) |	3000 | LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	See BQ25185DLHR	B185

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

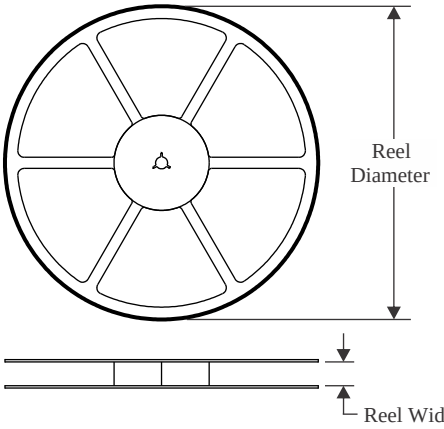
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

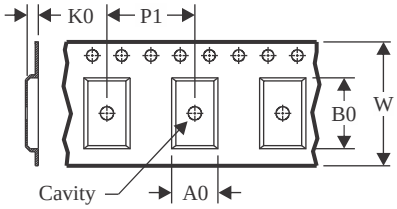
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

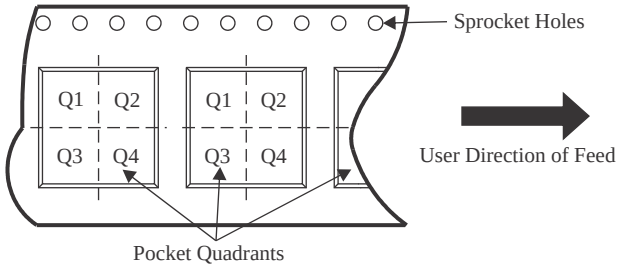


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

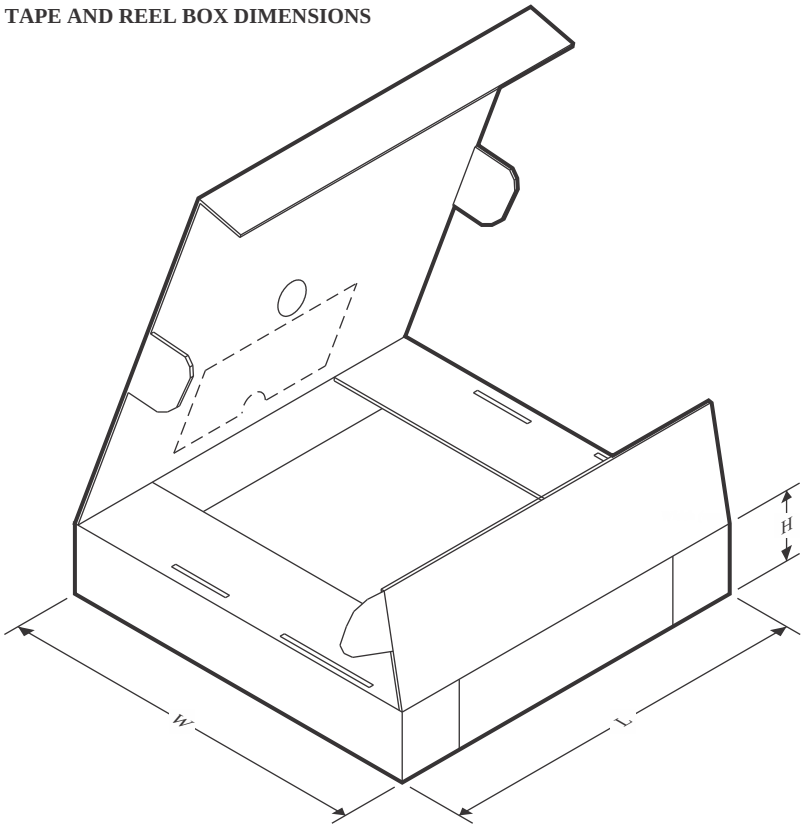
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25185DLHR	WSON	DLH	10	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

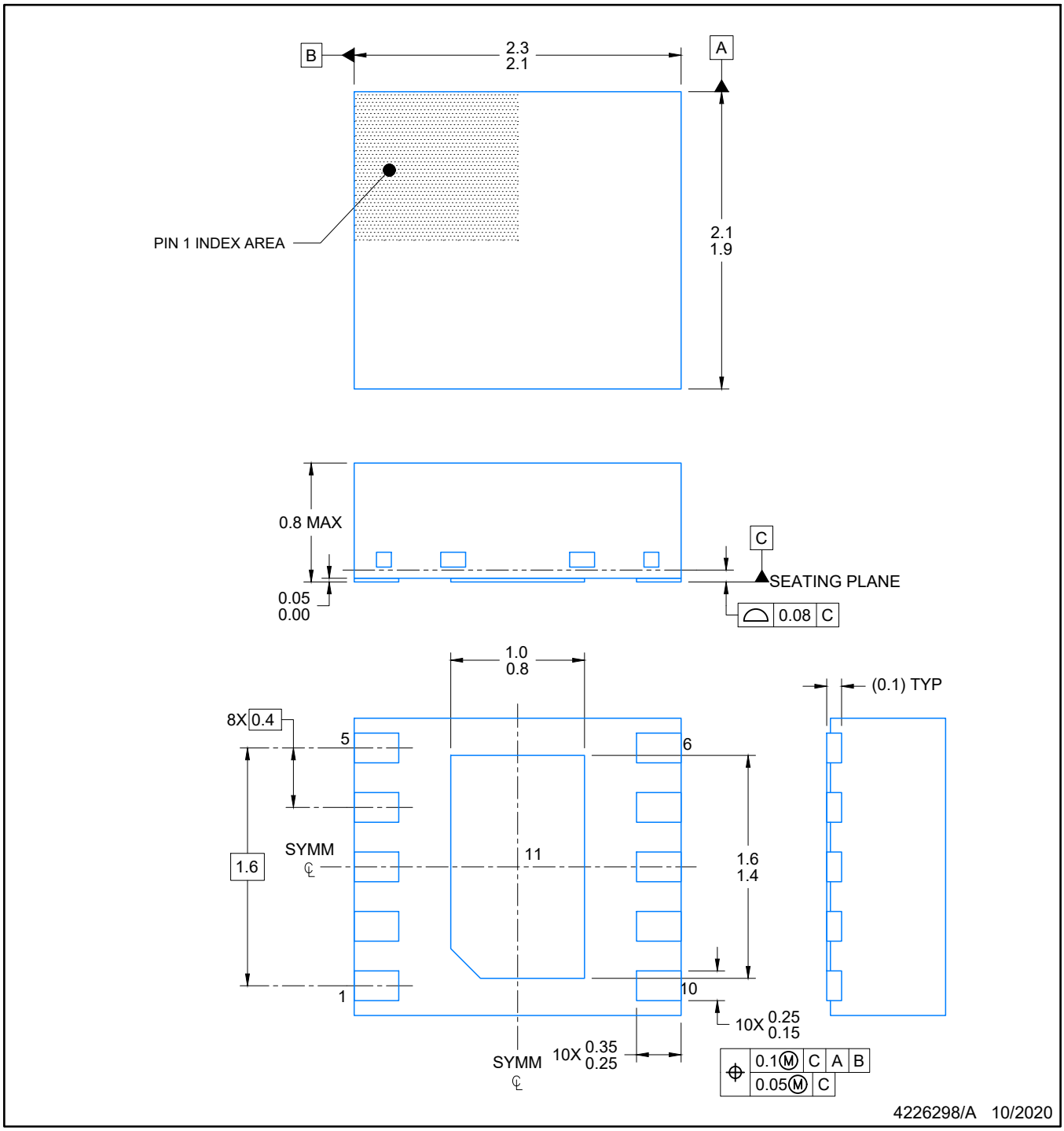
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25185DLHR	WSON	DLH	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DLH0010A

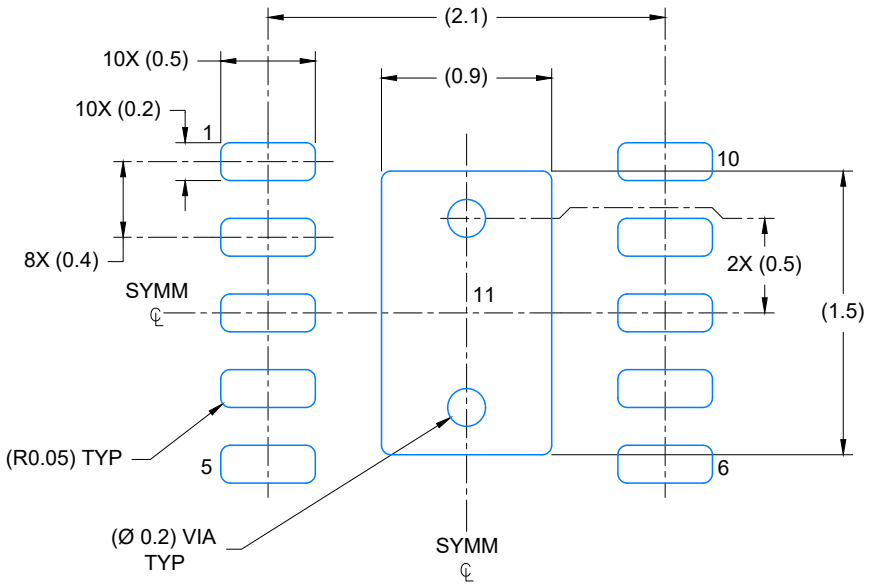
WSON - 0.8 mm max height

PLASTIC QUAD FLATPACK- NO LEAD

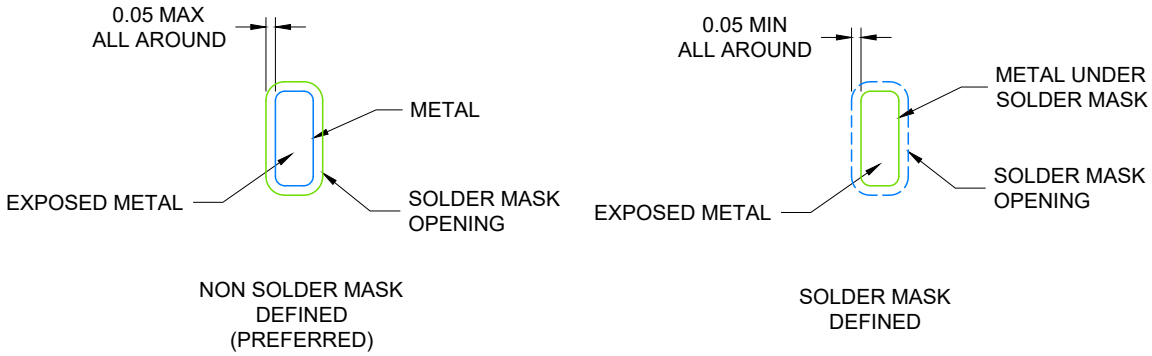


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

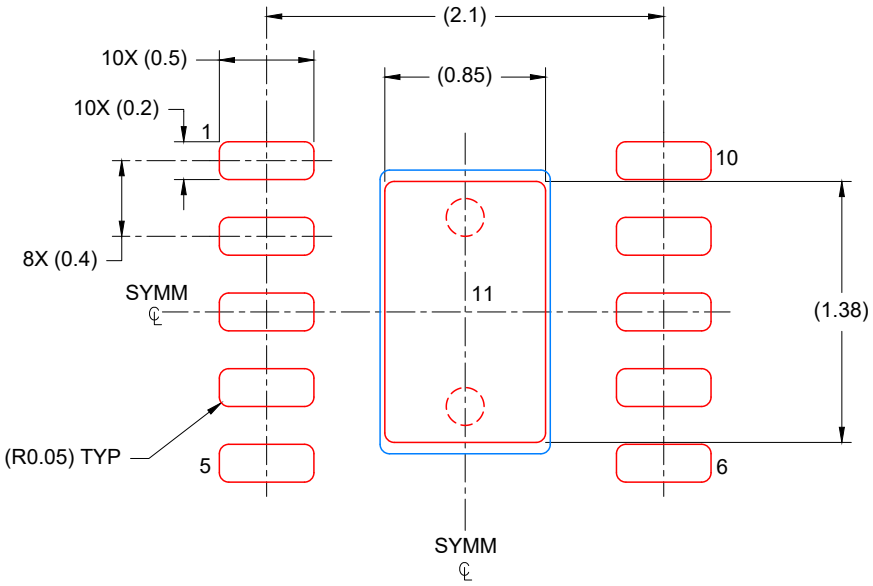


SOLDER MASK DETAILS

4226298/A 10/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 25X

4226298/A 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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