bq78350-R1 CEDV Li-Ion Gas Gauge and Battery Management Controller Companion to the bq769x0 Battery Monitoring AFE

1 Features

- Compensated End-of-Discharge Voltage (CEDV) Gauging Algorithm
- Supports SMBus Host Communication
- Flexible Configuration for 3- to 5-Series (bq76920), 6- to 10-Series (bq76930), and 9- to 15-Series (bq76940) Li-Ion and $LiFePO_4$ Batteries
- Supports Battery Configurations up to 320 Ahr
- Supports Charge and Discharge Current Reporting up to 320 A
- On-Chip Temperature Sensor Option
- External NTC Thermistor Support from Companion AFE
- Full Array of Programmable Protection Features
  - Voltage, Current, and Temperature
  - System Components
- Lifetime Data Logging
- Supports CC-CV Charging, Including Precharge, Charge Inhibit, and Charge Suspend
- Offers an Optional Resistor Programmable SMBus Slave Address for up to Eight Different Bus Addresses
- Drives up to a 5-Segment LED or LCD Display for State-Of-Charge Indication
- Provides SHA-1 Authentication

2 Applications

- Light Electric Vehicles (LEVs): eBikes, eScooters, Pedelec, and Pedal-Assist Bicycles
- Power and Gardening Tools
- Battery Backup and Uninterruptible Power Supply (UPS) Systems
- Wireless Base Station Backup Systems
- Telecom Power Systems
- Handheld Vacuum Cleaners and Robot Vacuums

3 Description

The Texas Instruments bq78350-R1 Li-Ion and $LiFePO_4$ Battery Management Controller and companion to the bq769x0 family of Analog Front End (AFE) protection devices provides a comprehensive set of Battery Management System (BMS) subsystems, helping to accelerate product development for faster time-to-market.

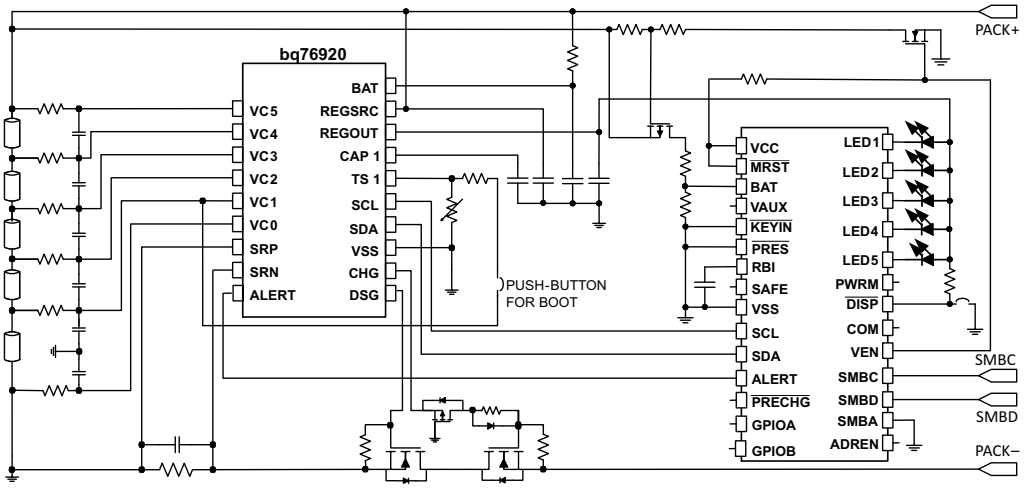
The bq78350-R1 controller and the bq769x0 AFE support 3-series to 15-series cell applications. The bq78350-R1 device provides an accurate fuel gauge and state-of-health (SoH) monitor, as well as cell balancing and a full range of voltage-, current-, and temperature-based protection features.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq78350-R1	TSSOP (30)	7.80 mm x 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2017) to Revision B — **Page**

- Changed *Gas Gauging* ... 18
- Changed *Power Supply Recommendations* ... 21

Changes from Original (August 2015) to Revision A — **Page**

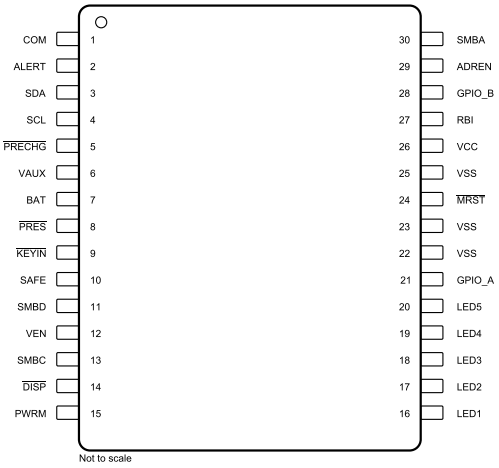
- Changed *Applications* ... 1

5 Description (continued)

The bq78350-R1 device offers optional LED or LCD display configurations for capacity reporting. It also makes data available over its SMBus 1.1 interface. Battery history and diagnostic data is also kept within the device in non-volatile memory and is available over the same interface.

6 Pin Configuration and Functions

30-Pin DBT Package



Pin Functions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	COM	O(1)	Open-drain output LCD common connection. Leave unconnected if not used.
2	ALERT	I	Input from the bq769x0 AFE
3	SDA	I/O	Data transfer to and from the bq769x0 AFE. Requires a 10-k pullup to VCC
4	SCL	I/O	Communication clock to the bq769x0 AFE. Requires a 10-k pullup to VCC
5	$\overline{\text{PRECHG}}$	O	Programmable polarity (default is active low) output to enable an optional precharge FET. This pin requires an external pullup to 2.5 V when configured as active high, and is open drain when configured as active low.
6	VAUX	AI	Auxiliary voltage input. If this pin is not used, then it should be tied to VSS.
7	BAT	AI	Translated battery voltage input
8	$\overline{\text{PRES}}$	I	Active low input to sense system insertion. This typically requires additional ESD protection. If this pin is not used, then it should be tied to VSS.
9	$\overline{\text{KEYIN}}$	I	A low level indicates application key-switch is inactive on position. A high level causes the DSG protection FET to open. If this pin is not used, then it should be tied to VSS.
10	SAFE	O	Active high output to enforce an additional level of safety protection (for example, fuse blow)
11	SMBD	I/OD	SMBus data open-drain bidirectional pin used to transfer an address and data to and from the bq78350-R1 device
12	VEN	O	Active high voltage translation enable. This open drain signal is used to switch the input voltage divider on/off to reduce the power consumption of the BAT translation divider network.
13	SMBC	I/OD	SMBus clock open-drain bidirectional pin used to clock the data transfer to and from the bq78350-R1 device
14	$\overline{\text{DISP}}$	I	Display control for the LEDs. This pin is typically connected to bq78350-R1 device REGOUT via a 100-KΩ resistor and a push-button switch connect to VSS. Not used with LCD display enabled and can be tied to VSS.
15	PWRM	O	Power mode state indicator open drain output
16	LED1	O	LED1/LCD1 display segment that drives an external LED/LCD, depending on the firmware configuration
17	LED2	O	LED2/LCD2 display segment that drives an external LED/LCD, depending on the firmware configuration
18	LED3	O	LED3/LCD3 display segment that drives an external LED/LCD, depending on the firmware configuration
19	LED4	O	LED4/LCD4 display segment that drives an external LED/LCD, depending on the firmware configuration

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

Pin Functions (continued)

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
20	LED5	O	LED5/LCD5 display segment that drives an external LED/LCD, depending on the firmware configuration
21	GPIO A	I/O	Configurable Input or Output. If not used, tie to VSS.
22	VSS	—	Negative supply voltage
23	VSS	—	Negative supply voltage
24	$\overline{\text{MRST}}$	I	Master reset input that forces the device into reset when held low. This pin must be held high for normal operation.
25	VSS	—	Negative supply voltage
26	VCC	P	Positive supply voltage
27	RBI	P	RAM backup input. Connect a capacitor to this pin and VSS to protect loss of RAM data in case of short circuit condition.
28	GPIO B	I/O	Configurable input or output. If not used, tie to VSS.
29	ADREN	O	Optional digital signal enables address detection measurement to reduce power consumption.
30	SMBA	IA	Optional SMBus address detection input. If this pin is not used, then it should be tied to VSS.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC} relative to V_{SS}	Supply voltage range	–0.3	2.75	V
$V_{(IOD)}$ relative to V_{SS}	Open-drain I/O pins	–0.3	6	V
V_I relative to V_{SS}	Input voltage range to all other pins	–0.3	VCC + 0.3	V
Operating free-air temperature range, T_A		–40	85	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Human Body Model (HBM) ESD stress voltage(1)	±2000	V
	Charged Device Model (CDM) ESD stress voltage(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.4	2.5	2.6	V
V_O	Output voltage range	SAFE			V_{CC}	
		SMBC, SMBD, VEN			5.5	V
		ADREN, GPIO A, GPIO B, SDATA, SCLK, PWRM, LED1...5 (when used as GPO)			V_{CC}	
V_{IN}	Input voltage range	BAT, VAUX, SMBA			1	V
		SMBD, SMBC, ALERT, $\overline{\text{DISP}}$, $\overline{\text{PRES}}$, KEYIN			5.5	
		SDATA, GPIO A, GPIO B, LED1...5 (when used as GPI)			V_{CC}	
T_{OPR}	Operating Temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC[1]		bq78350-R1 TSSOP (DBT) 30 PINS	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance	81.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	16.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.1	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	33.6	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics: Supply Current

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Operating mode current	No flash programming		650[1]		µA
$I_{(SLEEP)}$	Low-power storage mode current	SLEEP mode		300[2]		µA
$I_{(SHUTDOWN)}$	Low-power SHUTDOWN mode current	SHUTDOWN mode		0.1	1	µA

(1) The actual current consumption of this mode fluctuates during operation over a 1-s period. The value shown is an average using the default data flash configuration.
(2) The actual current consumption of this mode fluctuates during operation over a user-configurable period. The value shown is an average using the default data flash configuration.

7.6 Electrical Characteristics: I/O

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Output voltage low SMBC, SMBD, SDATA, SCLK, SAFE, ADREN, VEN, GPIO A, GPIO B, PWRM	I_{OL} = 0.5 mA			0.4	V
	Output voltage low LED1, LED2, LED3, LED4, LED5	I_{OL} = 3 mA			0.4	
V_{OH}	Output voltage high SMBC, SMBD, SDATA, SCLK, SAFE, ADREN, VEN, GPIO A, GPIO B, PWRM	I_{OH} = –1 mA	V_{CC} – 0.5			V
V_{IL}	Input voltage low SMBC, SMBD, SDATA, SCLK, ALERT, $\overline{DISP}$, SMBA, GPIO A, GPIO B, $\overline{PRES}$, KEYIN		–0.3		0.8	V
V_{IH}	Input voltage high SMBC, SMBD, SDATA, SCLK, ALERT, SMBA, GPIO A, GPIO B		2		6	V
	Input voltage high $\overline{DISP}$, $\overline{PRES}$, KEYIN		2		V_{CC} + 0.3	V
C_{IN}	Input capacitance			5		pF
I_{LKG}	Input leakage current				1	µA

7.7 Electrical Characteristics: ADC

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	BAT, VAUX	–0.2		1	V
Conversion time		16			ms
Resolution (no missing codes)		16			bits
Effective resolution		13		14	bits

Electrical Characteristics: ADC (continued)

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Integral nonlinearity		±0.03%			FSR(1)
Offset error(2)		140		250	µV
Offset error drift(2)	T_A = 25°C to 85°C	2.5		18	µV/°C
Full-scale error(3)		±0.1%		±0.7%	
Full-scale error drift		50			PPM/°C
Effective input resistance(4)		8			MΩ

(1) Full-scale reference
(2) Post-calibration performance and no I/O changes during conversion with VSS as the ground reference
(3) Uncalibrated performance. This gain error can be eliminated with external calibration.
(4) The A/D input is a switched-capacitor input. Since the input is switched, the effective input resistance is a measure of the average resistance.

7.8 Electrical Characteristics: Power-On Reset

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT-}	Negative-going voltage input		1.7	1.8	1.9	V
V_{HYS}	Power-on reset hysteresis		50	125	200	mV

7.9 Electrical Characteristics: Oscillator

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(OSC)}$	Operating frequency				4.194	MHz
$f_{(EIO)}$	Frequency error(1)(2)		–3%	0.25%	3%	
		T_A = 20°C to 70°C	–2	0.25	2	
$t_{(SXO)}$	Start-up time(3)			2.5	5	ms
LOW FREQUENCY OSCILLATOR						
$f_{(LOSC)}$	Operating frequency			32.768		kHz
$f_{(LEIO)}$	Frequency error(2)(4)		–2.5%	0.25%	2.5%	
		TA = 20°C to 70°C	–1.5	0.25	1.5	
$t_{(LSXO)}$	Start-up time(5)				500	ms

(1) The frequency error is measured from 4.194 MHz.
(2) The frequency drift is included and measured from the trimmed frequency at V_{CC} = 2.5 V, TA = 25°C.
(3) The start-up time is defined as the time it takes for the oscillator output frequency to be within 1% of the specified frequency.
(4) The frequency error is measured from 32.768 kHz.
(5) The start-up time is defined as the time it takes for the oscillator output frequency to be ±3%.

7.10 Electrical Characteristics: Data Flash Memory

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Data retention	See note(1)	10			Years
	Flash programming write-cycles	See note(1)	20,000			Cycles
$t_{(WORDPROG)}$	Word programming time	See note(1)			2	ms
$I_{(DDdPROG)}$	Flash-write supply current	See note(1)		5	10	mA

(1) Specified by design. Not production tested.

7.11 Electrical Characteristics: Register Backup

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(RB)}$	RB data-retention input current	$V_{(RB)} > V_{(RBMIN)}$, VCC < VIT–			1500	nA
		$V_{(RB)} > V_{(RBMIN)}$, VCC < VIT–, TA = 0°C to 50°C		40	160	
$V_{(RB)}$	RB data-retention voltage(1)		1.7			V

(1) Specified by design. Not production tested.

7.12 SMBus Timing Specifications

V_{CC} = 2.4 V to 2.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
f_{SMB}	SMBus operating frequency	SLAVE mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS}	SMBus master clock frequency	MASTER mode, no clock low slave extend		51.2		kHz
t_{BUF}	Bus free time between start and stop		4.7			µs
$t_{HD:STA}$	Hold time after (repeated) start		4			µs
$t_{SU:STA}$	Repeated start setup time		4.7			µs
$t_{SU:STO}$	Stop setup time		4			µs
$t_{HD:DAT}$	Data hold time	RECEIVE mode	0			ns
		TRANSMIT mode	300			
$t_{SU:DAT}$	Data setup time		250			
$t_{TIMEOUT}$	Error signal/detect	See note(1)	25		35	ms
t_{LOW}	Clock low period		4.7			µs
t_{HIGH}	Clock high period	See note(2)	4		50	
$t_{LOW:SEXT}$	Cumulative clock low slave extend time	See note(3)			25	ms
$t_{LOW:MEXT}$	Cumulative clock low master extend time	See note(4)			10	
t_F	Clock/data fall time	(V_{ILMAX} – 0.15 V) to (V_{IHMIN} + 0.15 V)			300	ns
t_R	Clock/data rise time	0.9 VCC to (V_{ILMAX} – 0.15 V)			1000	

(1) The bq78350-R1 device times out when any clock low exceeds $t_{TIMEOUT}$.
(2) $t_{HIGH:MAX}$ is minimum bus idle time. SMBC = 1 for t > 50 µs causes a reset of any transaction in progress involving the bq78350-R1 device.
(3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to stop.
(4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to stop.

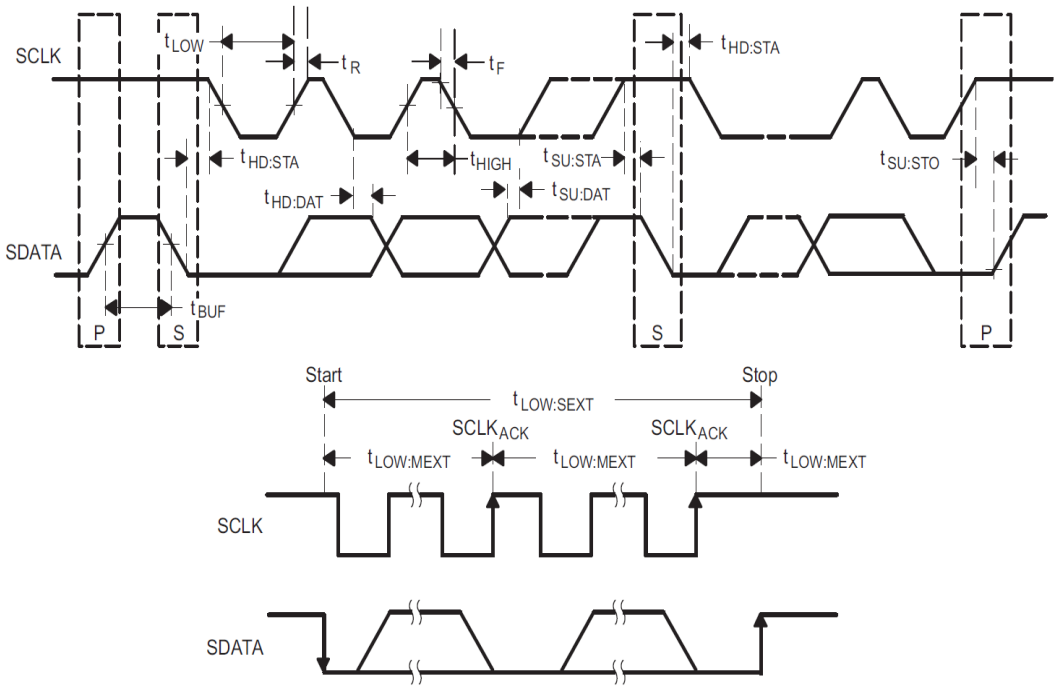


Figure 1. SMBus Timing Diagram

7.13 Typical Characteristics

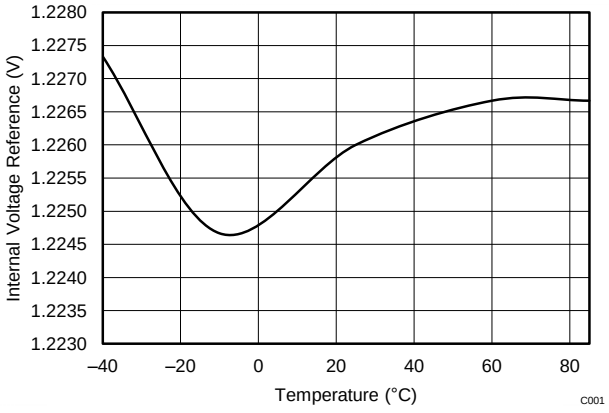


Figure 2. Internal Voltage Reference

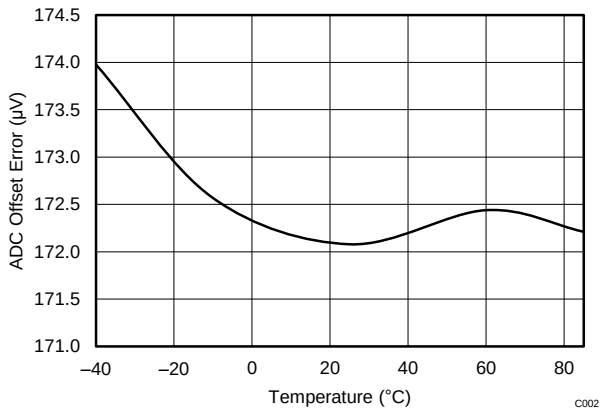


Figure 3. ADC Offset Error

Typical Characteristics (continued)

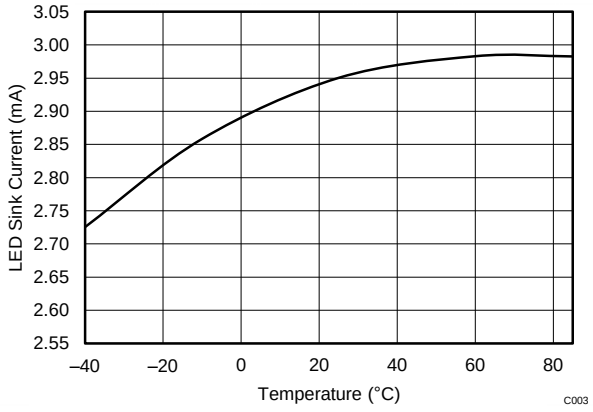


Figure 4. LED Sink Current

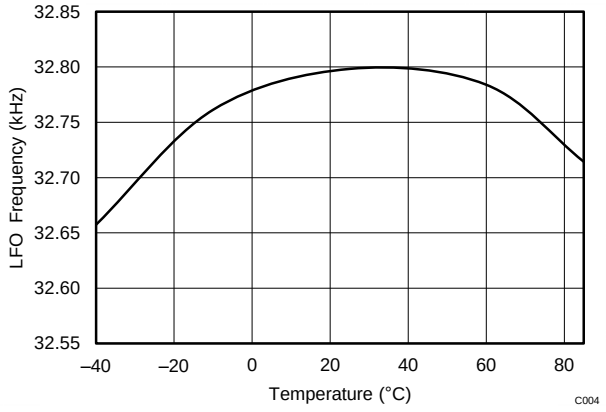


Figure 5. LFO Frequency

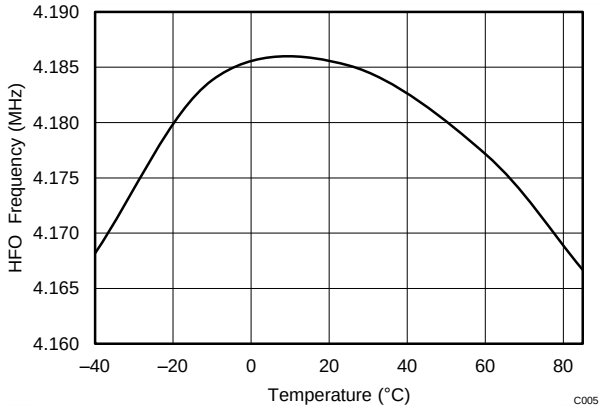


Figure 6. HFO Frequency

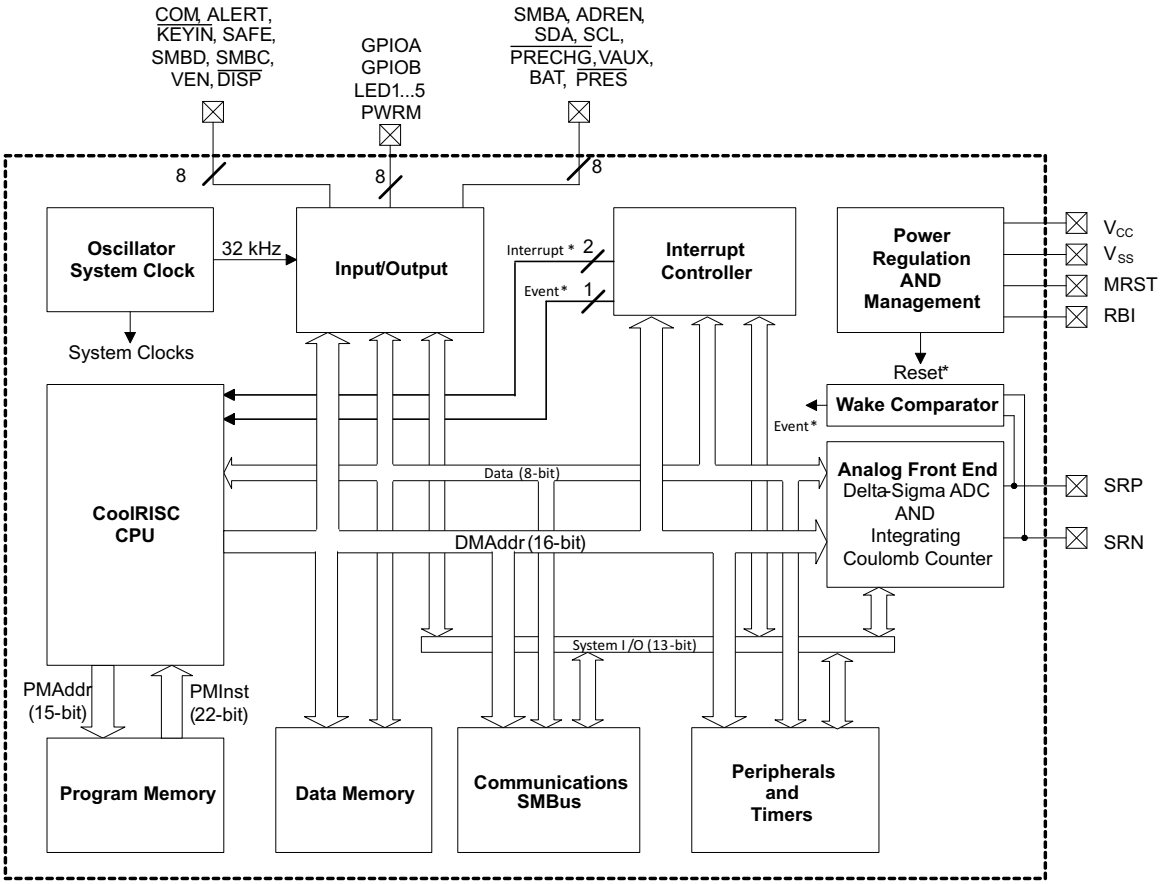
8 Detailed Description

8.1 Overview

The bq78350-R1 Li-Ion and $LiFePO_4$ Battery Management Controller is the companion to the bq769x0 family of Analog Front End (AFE) protection devices. This chipset supports 3-series to 15-series cell applications with capacities up to 320 Ah, and is suitable for a wide range of portable or stationary battery applications. The bq78350-R1 device provides an accurate fuel gauge and state-of-health (SoH) monitor, as well as the cell balancing algorithm and a full range of voltage-, current-, and temperature-based protection features.

The battery data that the bq78350-R1 device gathers can be accessed via an SMBus 1.1 interface, and state-of-charge (SoC) data can be displayed through optional LED or LCD display configurations. Battery history and diagnostic data are also kept within the device in non-volatile memory and are available over the same SMBus interface.

8.2 Functional Block Diagram



8.3 Feature Description

The following section provides an overview of the device features. For full details on the bq78350-R1 features, refer to the *bq78350-R1 Technical Reference Manual* (SLUUBD3).

8.3.1 Primary (1st Level) Safety Features

The bq78350-R1 device supports a wide range of battery and system protection features that can be configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short circuit protection
- Charge and discharge overtemperature with independent alarms and thresholds for each thermistor

8.3.2 Secondary (2nd Level) Safety Features

The secondary safety features of the bq78350-R1 device can be used to indicate more serious faults via the SAFE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety overvoltage
- Safety undervoltage
- Safety overcurrent in charge and discharge
- Safety overtemperature in charge and discharge
- Charge FET and Precharge FET fault

Feature Description (continued)

- Discharge FET fault
- Cell imbalance detection
- Open thermistor detection
- AFE communication fault

8.3.3 Charge Control Features

The bq78350-R1 charge control features include:

- Provides a range of options to configure the charging algorithm and its actions based on the application requirements
- Reports the appropriate charging current needed for constant current charging, and the appropriate charging voltage needed for constant voltage charging
- Supports pre-charging/0-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range

8.3.4 Fuel Gauging

The bq78350-R1 device uses Compensated End-of-Discharge Voltage (CEDV) technology to measure and calculate the available charge in battery cells. The bq78350-R1 device accumulates a measure of charge and discharge currents and compensates the charge current measurement for the temperature and state-of-charge of the battery. The bq78350-R1 device estimates self-discharge of the battery and also adjusts the self-discharge estimation based on temperature.

8.3.5 Lifetime Data Logging

The bq78350-R1 device offers lifetime data logging, where important measurements are stored for warranty and analysis purposes. The data monitored includes:

- Lifetime maximum temperature
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage per cell
- Lifetime minimum battery cell voltage per cell
- Cycle count
- Maximum charge current
- Maximum discharge current
- Safety events that trigger *SafetyStatus()* updates. (The 12 most common are tracked.)

8.3.6 Authentication

The bq78350-R1 device supports authentication by the host using SHA-1.

8.3.7 Battery Parameter Measurements

The bq78350-R1 device digitally reads bq769x0 registers containing recent values from the integrating analog-to-digital converter (CC) for current measurement and a second delta-sigma ADC for individual cell and temperature measurements.

8.3.7.1 Current and Coulomb Counting

The integrating delta-sigma ADC (CC) in the companion bq769x0 AFE measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN pins. The 15-bit integrating ADC measures bipolar signals from –0.20 V to 0.20 V with 15-µV resolution. The AFE reports charge activity when VSR = $V_{(SRP)} – V_{(SRN)}$ is positive, and discharge activity when VSR = $V_{(SRP)} – V_{(SRN)}$ is negative. The bq78350-R1 device continuously monitors the measured current and integrates the digital signal from the AFE over time, using an internal counter.

To support large battery configurations, the current data can be scaled to ensure accurate reporting through the SMBus. The data reported is scaled based on the setting of the *SpecificationInfo()* command.

Feature Description (continued)

8.3.7.2 Voltage

The bq78350-R1 device updates the individual series cell voltages through the bq769x0 at 1-s intervals. The bq78350-R1 device configures the bq769x0 to connect to the selected cells in sequence and uses this information for cell balancing and individual cell fault functions. The internal 14-bit ADC of the bq769x0 measures each cell voltage value, which is then communicated digitally to the bq78350-R1 device where they are scaled and translated into unit mV. The maximum supported input range of the ADC is 6.075 V.

The bq78350-R1 device also separately measures the average cell voltage through an external translation circuit at the BAT pin. This value is specifically used for the fuel gauge algorithm. The external translation circuit is controlled via the VEN pin so that the translation circuit is only enabled when required to reduce overall power consumption. For correct operation, VEN requires an external pull-up to VCC, typically 100 k.

In addition to the voltage measurements used by the bq78350-R1 algorithms, there is an optional auxiliary voltage measurement capability via the VAUX pin. This feature measures the input on a 1-s update rate and provides the programmable scaled value through an SMBus command.

To support large battery configurations, the voltage data can be scaled to ensure accurate reporting through the SMBus. The data reported is scaled based on the setting of the *SpecificationInfo()* command.

8.3.7.3 Temperature

The bq78350-R1 device receives temperature information from external or internal temperature sensors in the bq769x0 AFE. Depending on the number of series cells supported, the AFE will provide one, two, or three external thermistor measurements.

8.4 Device Functional Modes

The bq78350-R1 device supports three power modes to optimize the power consumption:

- In NORMAL mode, the bq78350-R1 device performs measurements, calculations, protection decisions, and data updates in 1-s intervals. Between these intervals, the bq78350-R1 device is in a reduced power mode.
- In SLEEP mode, the bq78350-R1 device performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq78350-R1 device is in a reduced power mode.
- In SHUTDOWN mode, the bq78350-R1 device is completely powered down.

The bq78350-R1 device indicates through the PWRM pin which power mode it is in. This enables other circuits to change based on the power mode detection criteria of the bq78350-R1 device.

8.5 Programming

8.5.1 Physical Interface

The bq78350-R1 device uses SMBus 1.1 with packet error checking (PEC) as an option and is used as a slave only.

8.5.2 SMBus Address

The bq78350-R1 device determines its SMBus 1.1 slave address through a voltage on SMBA, Pin 30. The voltage is set with a pair of high-value resistors if an alternate address is required and is measured either upon exit of POR or when system present is detected. ADREN, Pin 29, may be used to disable the voltage divider after use to reduce power consumption.

8.5.3 SMBus On and Off State

The bq78350-R1 device detects an SMBus off state when SMBC and SMBD are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

9 Application and Implementation

9.1 Application Information

The bq78350-R1 Battery Management Controller companion to the bq769x0 family of battery monitoring AFEs enables many standard and enhanced battery management features in a 3-series to 15-series Li-Ion/Li Polymer battery pack.

To design and implement a complete solution, users need the Battery Management Studio (bqStudio) tool to configure a "golden image" set of parameters for a specific battery pack and application. The bqStudio tool is a graphical user-interface tool installed on a PC during development. The firmware installed in the product has default values, which are summarized in the *bq78350-R1 Technical Reference Manual* (SLUUBD3). With the bqStudio tool, users can change these default values to cater to specific application requirements. Once the system parameters are known (for example, fault trigger thresholds for protection, enable/disable of certain features for operation, configuration of cells, among others), the data can be saved. This data is referred to as the "golden image."

9.2 Typical Applications

The bq78350-R1 device can be used with the bq76920, bq76930, or bq76940 device, but it is set up, by default, for a 5-series cell, 4400-mA battery application using the bq76920 AFE.

Typical Applications (continued)

9.2.1 Schematic

The schematic is split into two sections: the gas gauge section (Figure 7) and the AFE section (Figure 8).

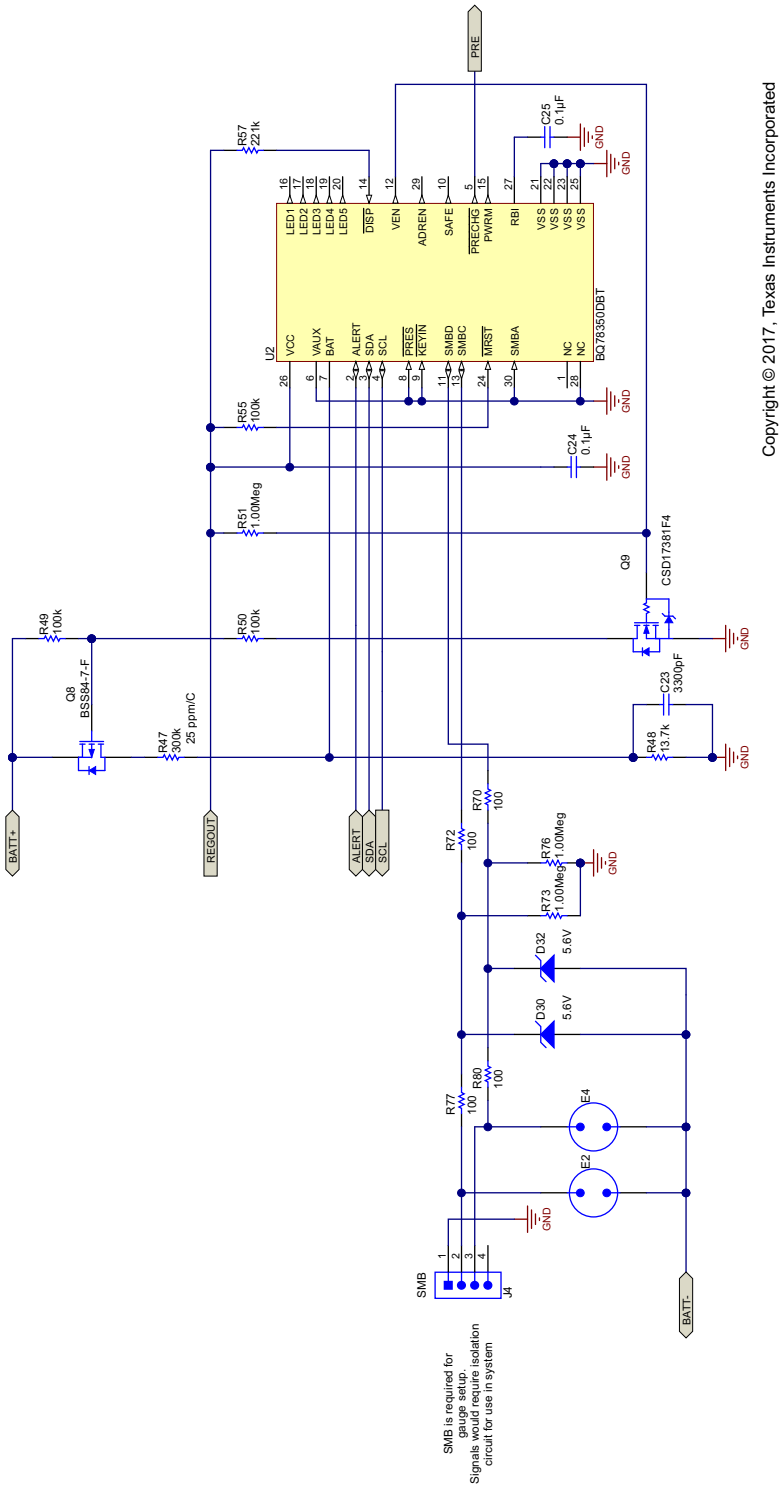


Figure 7. 5-Series Cell Typical Schematic, Gas Gauge (bq78350-R1)

Typical Applications (continued)

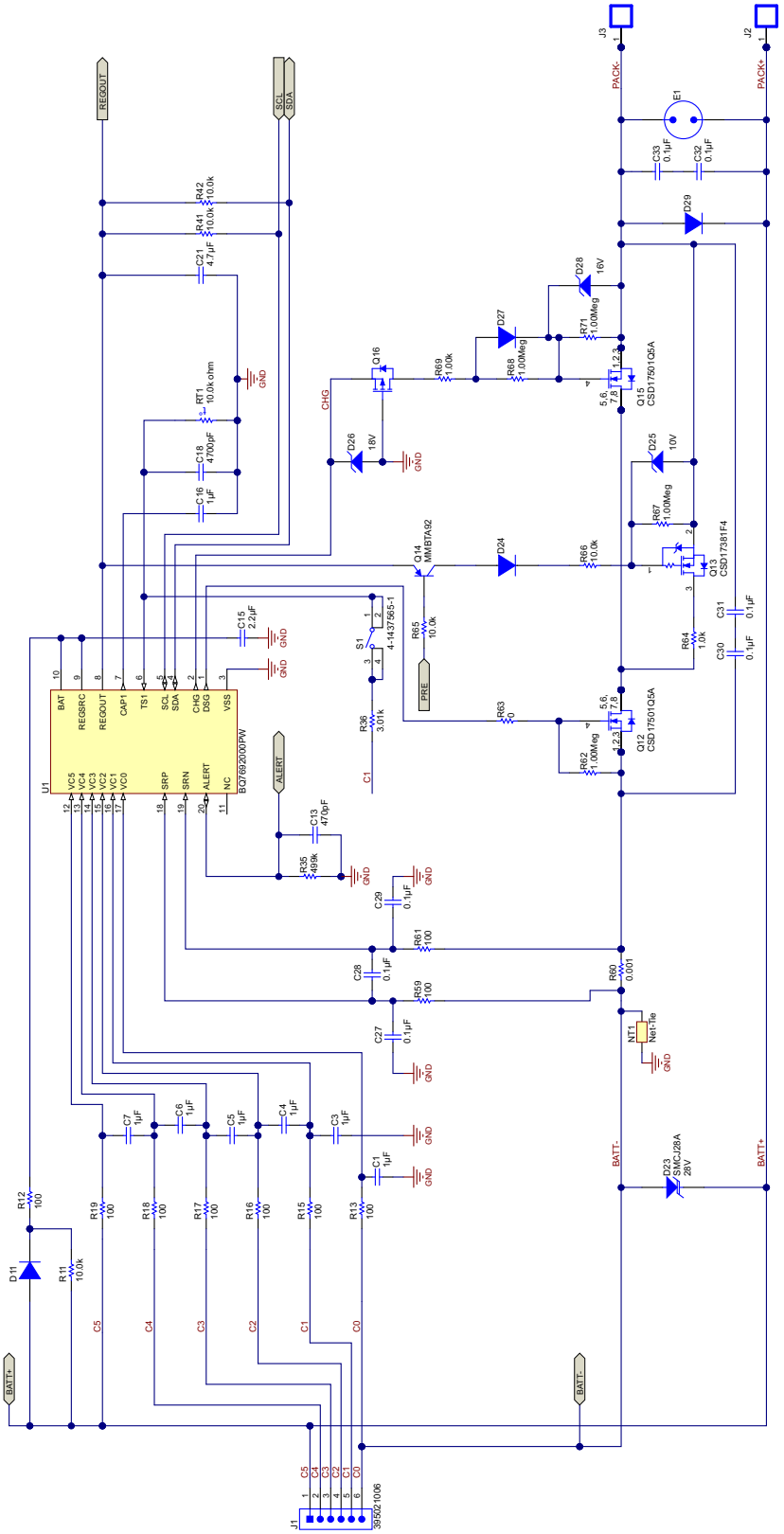


Figure 8. 5-Series Cell Typical Schematic, AFE (bq76920)

Typical Applications (continued)

9.2.2 Design Requirements

Table 1 lists the device's default settings and feature configurations when shipped from Texas Instruments.

Table 1. TI Default Settings

Design Parameter	Value or State
Cell Configuration	5s2p (5-series with 1 Parallel)
Design Capacity	4400 mAh
Device Chemistry	Chem ID 1210 ($LiCoO_2$/graphitized carbon)
Cell Over Voltage (per cell)	4250 mV
Cell Under Voltage (per cell)	2500 mV
Overcurrent in CHARGE Mode	6000 mA
Overcurrent in DISCHARGE Mode	–6000 mA
Over Load Current	0.017 V/Rsense across SRP, SRN
Short Circuit in DISCHARGE Mode	0.44 V/Rsense across SRP, SRN
Over Temperature in CHARGE Mode	55°C
Over Temperature in DISCHARGE Mode	55°C
SAFE Pin Activation Enabled	No
Safety Overvoltage (per cell)	4400 mV
Safety Undervoltage (per cell)	2500 mV
Shutdown Voltage	2300 mV
Cell Balancing Enabled	Yes
Internal or External Temperature Sensor	External Enabled
SMB BROADCAST Mode	Disabled
Display Mode (# of bars and LED or LCD)	5-bar LED
Dynamic SMB Address Enabled	No (SMB Address = 0x16)
KEYIN Feature Enabled	No
$\overline{\text{PRES}}$ Feature Enabled	No

9.2.3 Detailed Design Procedure

By default, the bq78350-R1 device is initially set up to keep the CHG, DSG, and PCHG FETs OFF and many other features disabled until the appropriate *ManufacturingStatus()* bit that enables *ManufacturerAccess()* commands are received, or when the default Manufacturing Status is changed.

In the first steps to evaluating the bq78350-R1 device and bq769x0 AFE, use the *ManufacturerAccess()* commands to ensure correct operation of features, and if they are needed in the application. Then enable features' reading for more in-depth application evaluation.

Prior to using the bq78350-R1 device, the default settings should be evaluated as the device has many configuration settings and options. These can be separated into five main areas:

- Measurement System
- Gas Gauging
- Charging
- Protection
- Peripheral Features

The key areas of focus are covered in the following sections.

9.2.3.1 Measurement System

9.2.3.1.1 Cell Voltages

The bq78350-R1 device is required to be configured in the AFE Cell Map register to determine which cells to measure based on the physical connections to the bq76920 AFE. The cell voltage data is available through *CellVoltage1()*…*CellVoltage5()*. The cell voltages are reported as they are physically stacked. For example, if the device is configured for 3-series cells connected to VC1, VC2, and VC5 per the AFE Cell Map, then the cell voltages are still reported via *CellVoltage1()*, *CellVoltage2()*, and *CellVoltage3()*, respectively.

For improved accuracy, offset calibration is available for each of these values and can be managed through the bqStudio tool. The procedure for calibration is described in the *bq78350-R1 Technical Reference Manual* (SLUUBD3) in the ***Calibration*** chapter.

9.2.3.1.2 External Average Cell Voltage

This is enabled by default (***DA Configuration [ExtAveEN]*** = 1) and uses the external resistor divider connected to the VEN and BAT pins to determine the average cell voltage of the battery pack. The average cell voltage is available through *ExtAveCellVoltage()*.

CAUTION

Care should be taken in the selection of the resistor and FETs used in this divider circuit as the tolerance and temperature drift of these components can cause increased measurement error and a gas gauging error if ***CEDV Gauging Config [ExtAveCell]*** = 1 (default = 1).

For improved accuracy, offset and gain calibration is available for this value and can be managed through the bqStudio tool. The procedure for calibration is described in the *bq78350-R1 Technical Reference Manual* (SLUUBD3) in the ***Calibration*** chapter.

9.2.3.1.3 Current

Current data is taken from the bq76920 and made available through *Current()*. The selection of the current sense resistor connected to SRP and SRN of the bq76920 is very important and there are several factors involved.

The aim of the sense resistor selection is to use the widest ADC input voltage range possible.

To maximize accuracy, the sense resistor value should be calculated based on the following formula:

$$RSNS_{(min)} = V_{(SRP)} – V_{(SRN)} / I_{(max)} \quad (1)$$

Where: $|V_{(SRP)} – V_{(SRN)}| = 200$ mV

$I_{(max)}$ = Maximum magnitude of charge of discharge current (transient or DC)

NOTE

$RSNS_{(min)}$ should include tolerance, temperature drift over the application temperature, and PCB layout tolerances when selecting the actual nominal resistor value.

When selecting the RSNS value, be aware that when selecting a small value, for example, 1 mΩ, then the resolution of the current measurement will be > 1 mA. In the example of RSNS = 1 mΩ, the current LSB will be 8.44 mA.

For improved accuracy, offset and gain calibration are available for this value and can be managed through the bqStudio tool. The procedure for calibration is described in the *bq78350-R1 Technical Reference Manual* (SLUUBD3) in the ***Calibration*** chapter.

9.2.3.1.4 Temperature

By default, the 78350 uses an external negative temperature coefficient (NTC) thermistor connected to the bq76920 as the source for the *Temperature()* data. The measurement uses a polynomial expression to transform the bq76920 ADC measurement into 0.1°C resolution temperature measurement. The default polynomial coefficients are calculated using the Semitec 103AT, although other resistances and manufacturers can be used.

To calculate the ***External Temp Model*** coefficients, use the bq78350-R1 Family Thermistor Coefficient Calculator shown in the application report, *Using the bq78350-R1* (SLUA924).

For improved accuracy, offset calibration is available for this value and can be managed through the bqStudio tool. The procedure for calibration is described in the *bq78350-R1 Technical Reference Manual* (SLUUBD3) in the ***Calibration*** chapter.

9.2.3.2 Gas Gauging

The default battery chemistry (Chem ID) is 1210, which is a Li-CoO_2 type chemistry. The Chem ID should be updated using bqStudio to select the specific battery used in the application. See the application report, *Using the bq78350-R1* (SLUA924) for details on selecting the Chem ID.

The default maximum capacity of the battery is 4400 mAh and this should be changed based on the cell and battery configuration chosen.

The CEDV gas gauging algorithm requires seven coefficients to enable accurate gas gauging. The default values are generic for Li-CoO_2 chemistry, but for accurate gas gauging these coefficients should be re-calculated. The procedure to gather the required data and generate the coefficients can be found at http://www.ti.com/tool/GPCCEDV.

More details on the required steps to set up the bq78350-R1 device for gas gauging can be found in the application report, *Using the bq78350-R1* (SLUA924).

9.2.3.3 Charging

The charging algorithm in the bq78350-R1 device is configured to support Constant Voltage/Constant Current (CC/CV) charging of a nominal 18-V, 4400-mAh battery.

9.2.3.3.1 Fast Charging Voltage

The charging voltage is configured (Fast Charging: Voltage) based on an individual cell basis (for example, 4200 mV), but the *ChargingVoltage()* is reported as the required battery voltage (for example, 4200 mV × 5 = 21000 mV).

9.2.3.3.2 Fast Charging Current

The fast charging current is configured to 2000 mA (Fast Charging: Current) by default, which is conservative for the majority of 4400-mAh battery applications. This should be configured based on the battery configuration, cell manufacturer's data sheet, and system power design requirements.

9.2.3.3.3 Other Charging Modes

The bq78350-R1 device is configured to limit, through external components, and report either low or 0 *ChargingVoltage()* and *ChargingCurrent()*, based on temperature, voltage, and fault status information.

The ***Charge Algorithm*** section of the *bq78350-R1 Technical Reference Manual* (SLUUBD3) details these features and settings.

9.2.3.4 Protection

The safety features and settings of the bq78350-R1 device are configured conservatively and are suitable for bench evaluation. However, in many cases, users will need to change these values to meet system requirements. These values should not be changed to exceed the safe operating limits provided by the cell manufacturer and any industry standard.

For details on the safety features and settings, see the ***Protections*** and ***Permanent Fail*** sections of the *bq78350-R1 Technical Reference Manual* (SLUUBD3).

9.2.3.5 Peripheral Features

9.2.3.5.1 LED Display

The bq78350-R1 device is configured by default to display up to five LEDs in a bar graph configuration based on the value of *RemainingStateOfCharge()* (RSOC). Each LED represents 20% of RSOC and is illuminated when the bq78350-R1 $\overline{\text{DISP}}$ pin transitions low, and remains on for a programmable period of time.

In addition to many other options, the number of LEDs used and the percentage at which they can be illuminated are configurable.

9.2.3.5.2 SMBus Address

Although the SMBus slave address is a configurable value in the bq78350-R1 device, this feature is disabled by default and the slave address is 0x16. The SMBus Address feature can allow up to nine different addresses based on external resistor value variation per address.

The default setup of the bq78350-R1 device is generic, but there are many additional features that can be enabled and configured to support a variety of system requirements. These are detailed in the *bq78350-R1 Technical Reference Manual* (SLUUBD3).

9.2.4 Application Performance Plots

When the bq78350-R1 device is powered up, there are several signals that are enabled at the same time. Figure 9 shows the rise time of each of the applicable signals.

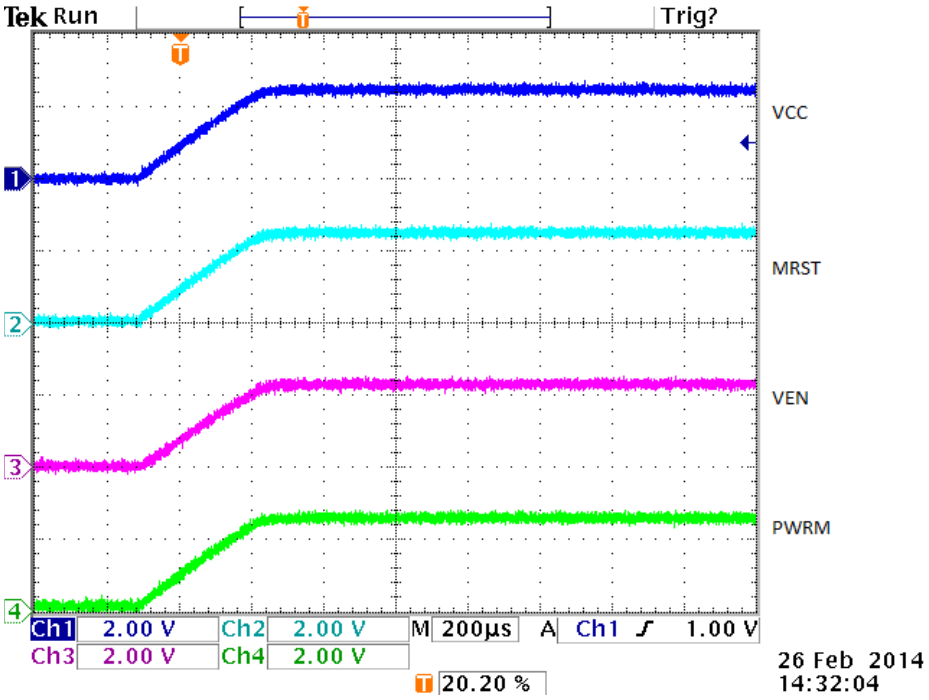


Figure 9. VCC, $\overline{\text{MRST}}$, VEN, and PWRM upon Power Up

The bq78350-R1 device takes a short period of time to boot up before the device can begin updating battery parameter data that can be then reported via the SMBus or the optional display. Normal operation after boot-up is indicated by the VEN pin pulsing to enable voltage data measurements for the *ExtAveCell()* function. Figure 10 shows the timing of these signals.

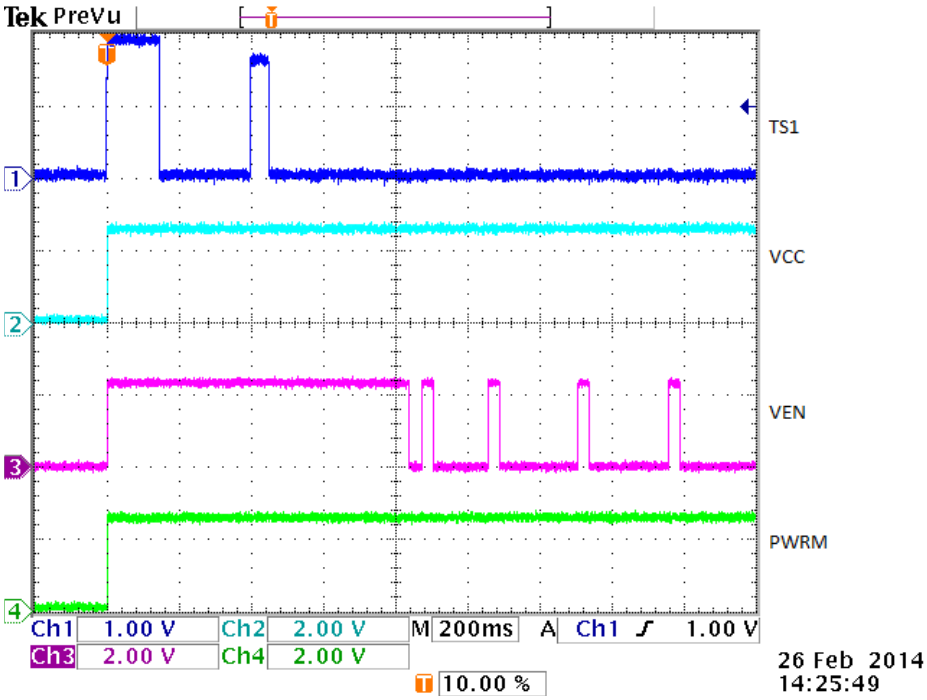


Figure 10. Valid VCC to Full FW Operation

Figure 11, Figure 12, Figure 13, and Figure 14 show Measurement System Performance Data of the bq78350-R1 device + the bq76920 EVM. This data was taken using a standard bq76920 EVM with power supplies providing the voltage and current reference inputs.

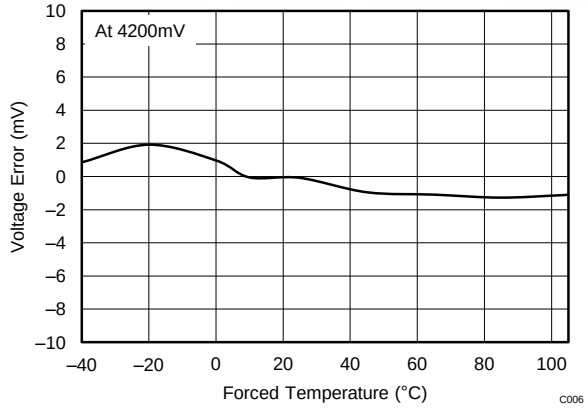


Figure 11. Cell Voltage Error Reported Through *CellVoltage1…5()*

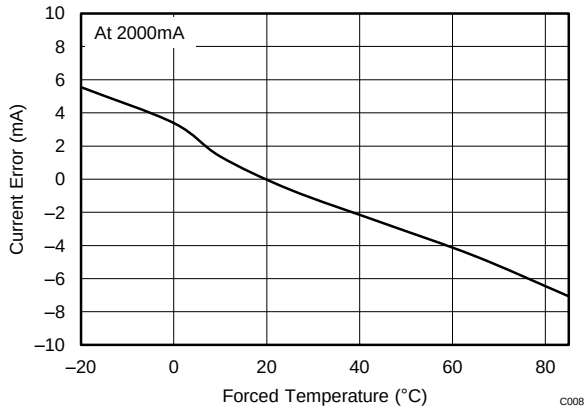


Figure 12. Battery Charge Current Error Reported Through *Current()*

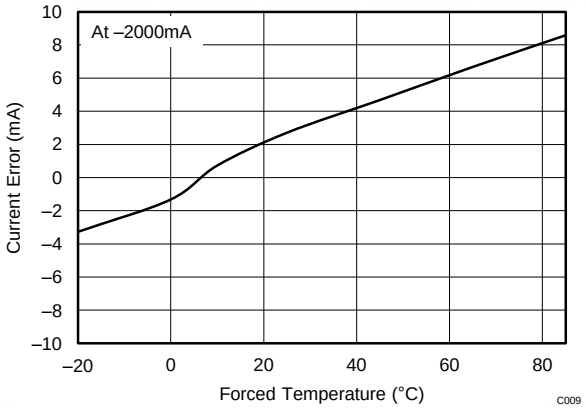


Figure 13. Battery Discharge Current Error Reported Through *Current()*

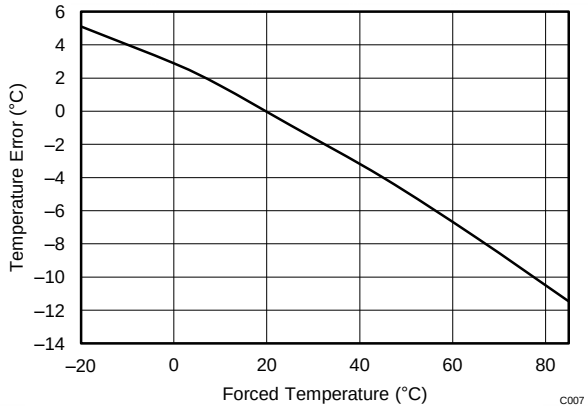


Figure 14. Battery Temperature (External) Error Reported Through *Temperature()*

10 Power Supply Recommendations

The bq78350-R1 device is powered directly from the 2.5-V REGOUT pin of the bq769x0 companion AFE. An input capacitor of 0.1 µF is required between VCC and VSS and should be placed as close to the bq78350-R1 device as possible.

To ensure a fast ramp-down voltage on the VCC pin during a MAC *Shutdown()* command, connect a 1-k pullup resistor between the PWRM pin and VCC, and connect a 1-µF capacitor between PWRM and VSS.

To ensure correct power up of the bq78350-R1 device, a 100-k resistor between $\overline{\text{MRST}}$ and VCC is also required. See the *Schematic* for further details.

11 Layout

11.1 Layout Guidelines

11.1.1 Power Supply Decoupling Capacitor

Power supply decoupling from VCC to ground is important for optimal operation of the bq78350-R1 device. To keep the loop area small, place this capacitor next to the IC and use the shortest possible traces. A large-loop area renders the capacitor useless and forms a small-loop antenna for noise pickup.

Ideally, the traces on each side of the capacitor must be the same length and run in the same direction to avoid differential noise during ESD. If possible, place a via near the VSS pin to a ground plane layer.

Placement of the RBI capacitor is not as critical. It can be placed further away from the IC.

11.1.2 $\overline{\text{MRST}}$ Connection

The $\overline{\text{MRST}}$ pin controls the gas gauge reset state. The connections to this pin must be as short as possible to avoid any incoming noise. Direct connection to VCC is possible if the reset functionality is not desired or necessary.

If unwanted resets are found, one or more of the following solutions may be effective:

- Add a 0.1-µF capacitor between $\overline{\text{MRST}}$ and ground.
- Provide a 1-kΩ pullup resistor to VCC at $\overline{\text{MRST}}$.
- Surround the entire circuit with a ground pattern.

If a test point is added at $\overline{\text{MRST}}$, it must be provided with a 10-kΩ series resistor.

Layout Guidelines (continued)

11.1.3 Communication Line Protection Components

The 5.6-V Zener diodes, which protect the bq78350-R1 communication pins from ESD, must be located as close as possible to the pack connector. The grounded end of these Zener diodes must be returned to the PACK(–) node, rather than to the low-current digital ground system. This way, ESD is diverted away from the sensitive electronics as much as possible.

11.1.4 ESD Spark Gap

Protect the SMBus clock, data, and other communication lines from ESD with a spark gap at the connector. The following pattern is recommended, with 0.2-mm spacing between the points.

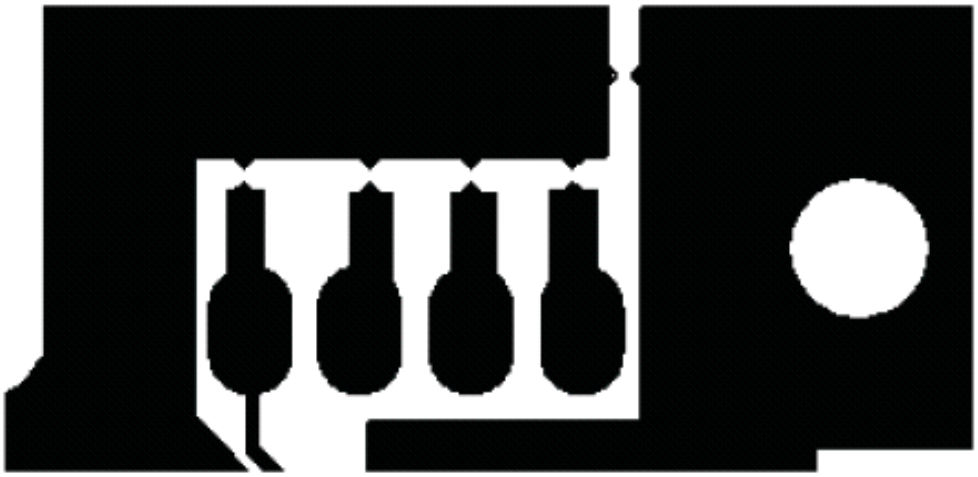


Figure 15. Recommended Spark-Gap Pattern Helps Protect Communication Lines From ESD

11.2 Layout Example

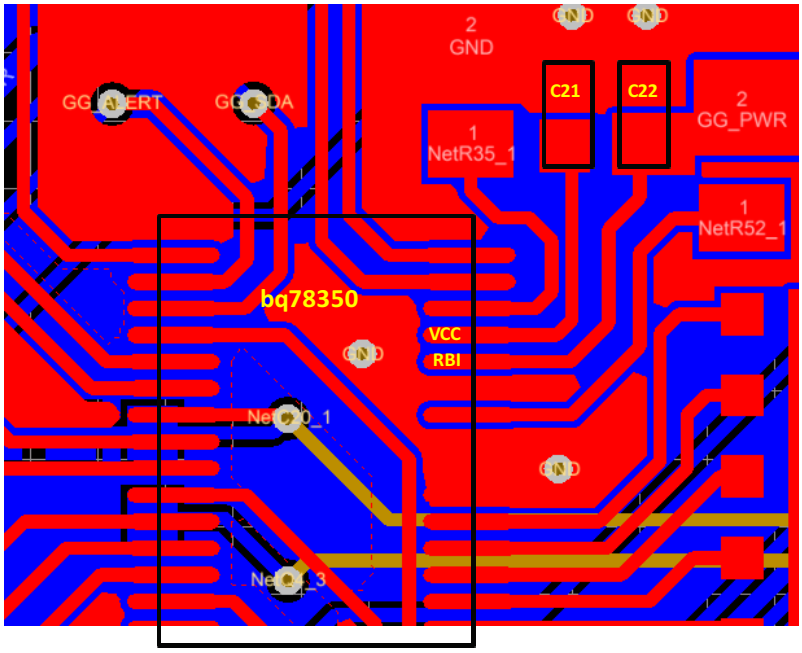


Figure 16. bq78350-R1 Layout

12 Device and Documentation Support

12.1 Related Documentation

For related documentation, see the following:

- *bq78350-R1 Technical Reference Manual* (SLUUBD3)
- *Using the bq78350-R1 Application Report* (SLUA924)
- *bq769x0 3-Series to 15-Series Cell Battery Monitor Family for Li-Ion and Phosphate Applications Data Manual* (SLUSBK2)

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ78350DBT-R1	NRND	TSSOP	DBT	30	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ78350	
BQ78350DBTR-R1	NRND	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ78350	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

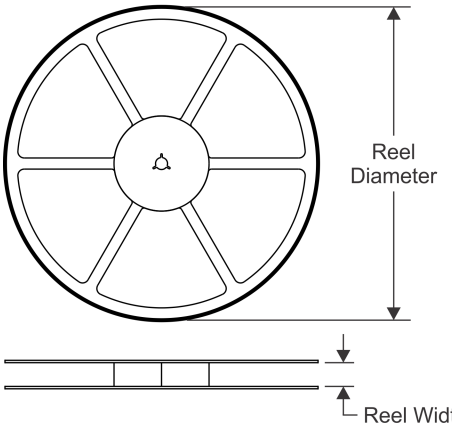
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

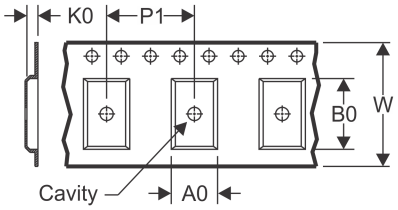
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

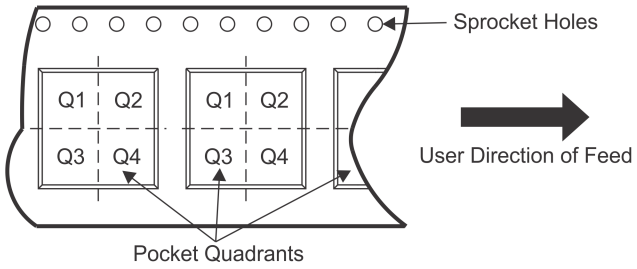


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

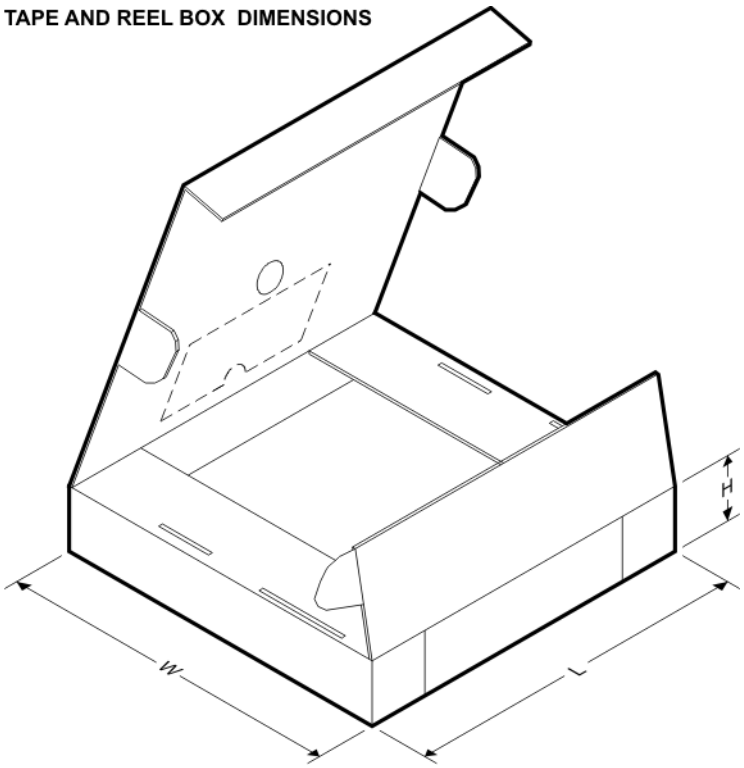
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ78350DBTR-R1	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

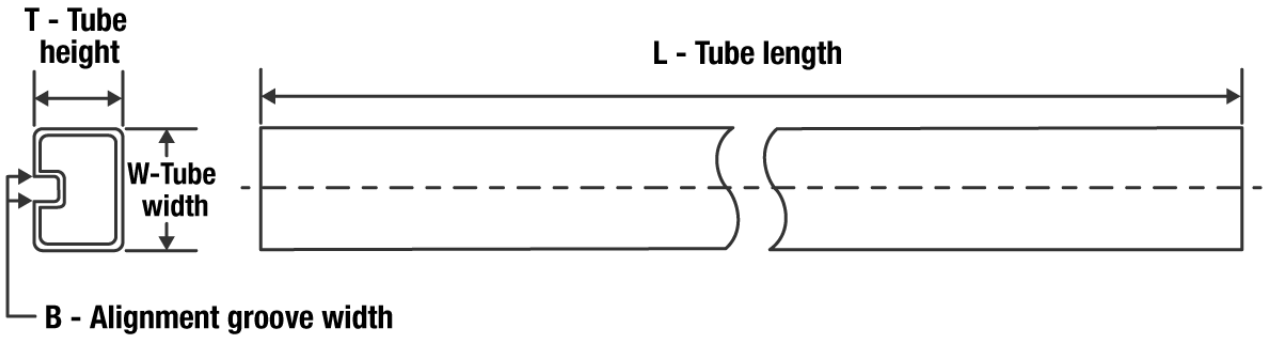
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ78350DBTR-R1	TSSOP	DBT	30	2000	367.0	367.0	38.0

TUBE



*All dimensions are nominal

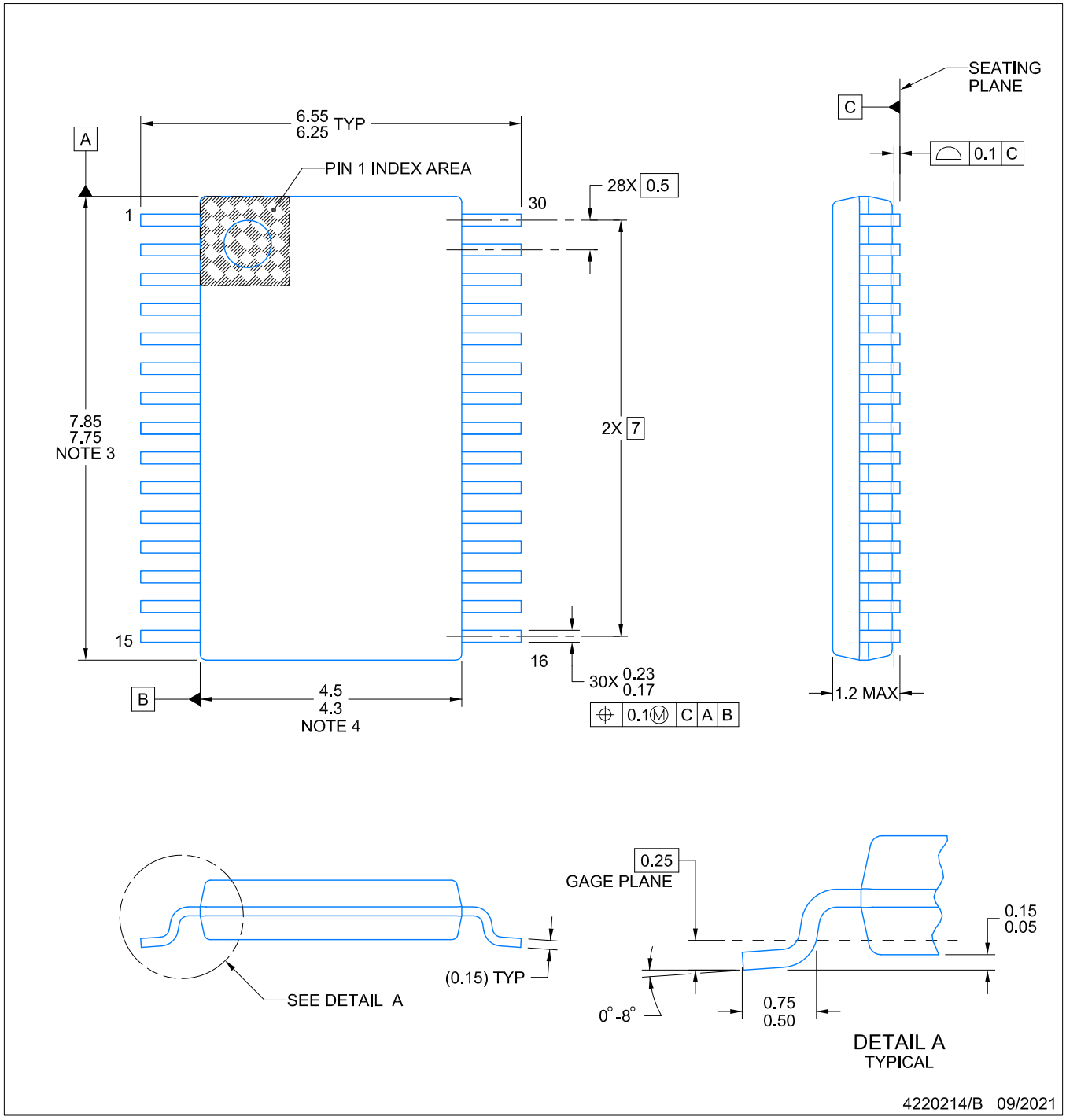
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ78350DBT-R1	DBT	TSSOP	30	60	530	10.2	3600	3.5

PACKAGE OUTLINE

DBT0030A

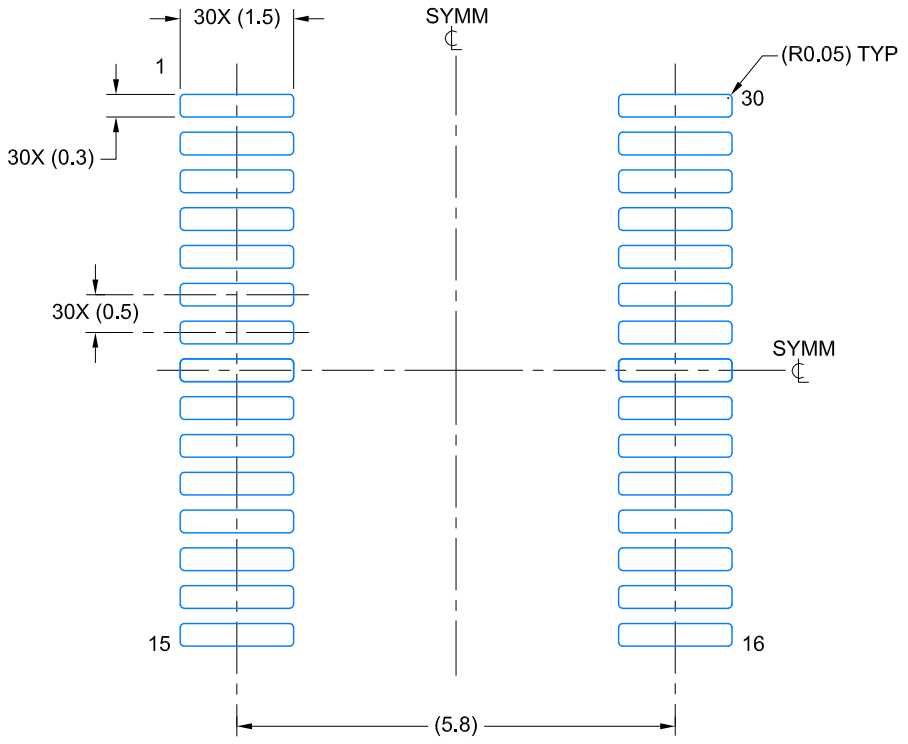
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

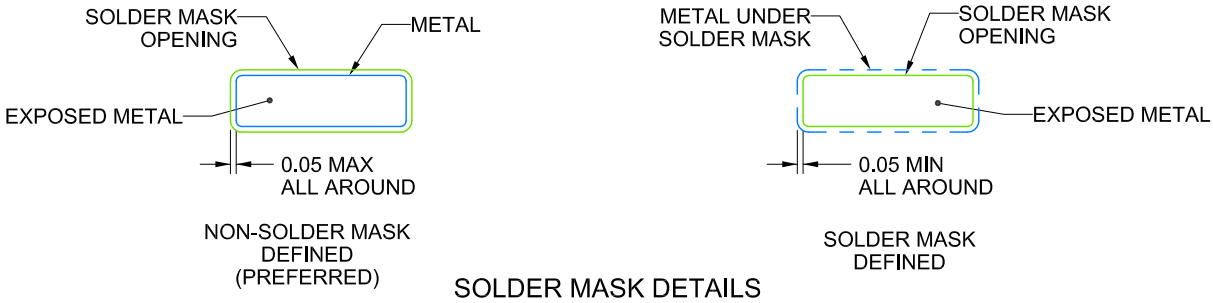


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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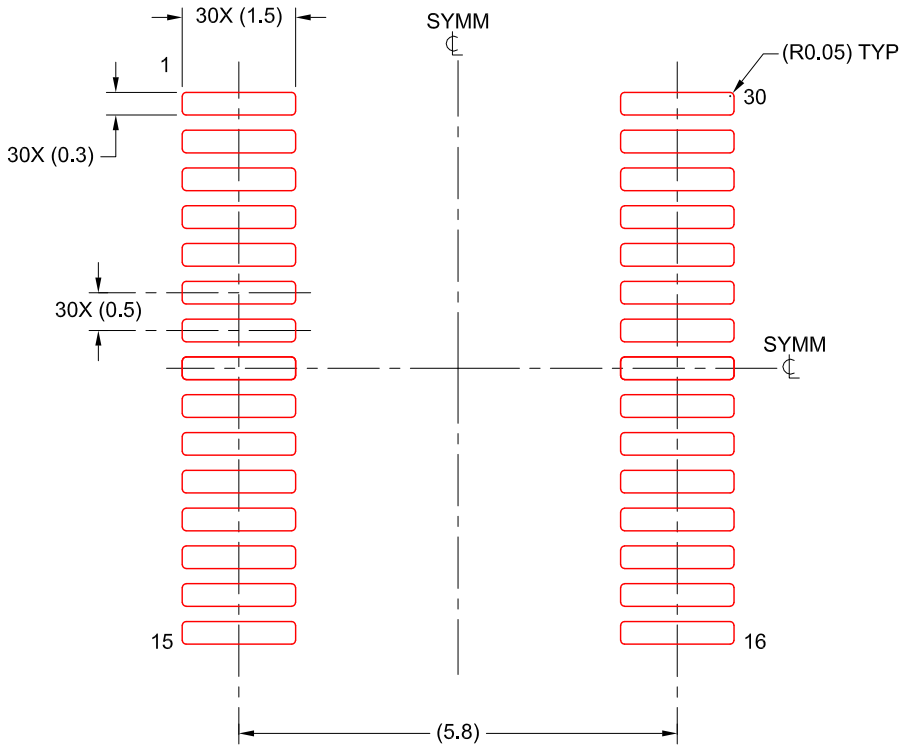
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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