

BZX84Cx-Q1 Automotive Zener Voltage Regulator Diode in SOT-23

1 Features

- Total power dissipation: 250mW (max)
- Low I/O capacitance: 80pF (max)
- Low leakage current: 0.6μA (max)
- Tolerance: ±5%
- Temperature range: -55°C to +150°C
- AEC-Q101 qualified
- Leaded package used for automatic optical inspection (AOI)

2 Applications

- Voltage regulation
- Over-voltage protection

3 Description

The BZX84Cx-Q1 is a family of voltage regulating diodes in a SOT-23 package. The diodes are available in Zener voltages ranging from 8.2V to 27V.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
BZX84Cx-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm

- (1) For more information, see [Section 8](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.

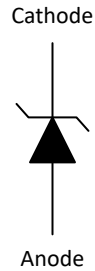


Figure 3-1. Functional Block Diagram



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4 Pin Configuration and Functions

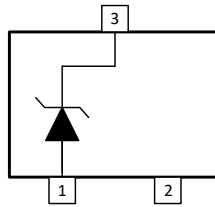


Figure 4-1. DBZ Package, 3-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	A	Anode
2	NC	No Connect
3	K	Cathode

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
P_D ^{(2) (3)}	Total Power Dissipation		250	mW
T_A	Ambient Operating Temperature	-55	150	°C
T_{stg}	Storage Temperature	-65	155	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) FR-4 printed circuit board, single sided copper, standard footprint
- (3) Measured at 25°C

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_F	Forward Voltage	$I_F = 10\text{mA}$			0.9	V
T_A	Operating free-air temperature		-55		150	°C

5.3 Thermal Information

THERMAL METRIC ⁽¹⁾		BZX84Cx-Q1	UNIT
		DBZ (SOT-23)	
		3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	285.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	197.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	118.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	90.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	117.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Electrical Characteristics

At $T_A = 25^\circ\text{C}$ (unless otherwise noted)

Part Number	Zener Voltage V_Z (V) at I_Z				Zener Impedance Z_{ZT} (Ω) at I_Z		Reverse Leakage Current I_R (μA)		Temperature Coefficient S_Z (mV/C) at I_Z		Capacitance C_D (pF) ⁽¹⁾
	MIN	TYP	MAX	I_Z (mA)	MAX	I_Z (mA)	MAX	V_R (V)	MAX	I_Z (mA)	MAX
BZX84C8V2-Q1	7.79	8.2	8.61	5	15	5	0.6	5.75	6.2	5	80
BZX84C15V-Q1	14.25	15	15.75	5	30	5	0.03	10.5	13	5	50
BZX84C27V-Q1	25.65	27	28.35	2	80	2	0.03	18.9	25.3	2	35

(1) $f = 1\text{MHz}$, $V_R = 0$

5.5 Typical Characteristics

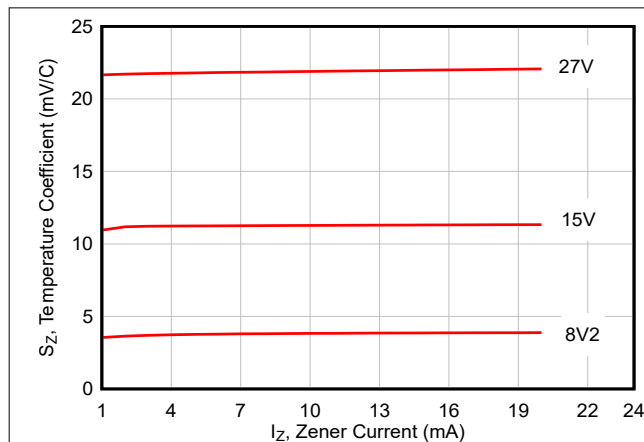


Figure 5-1. Temperature Coefficient

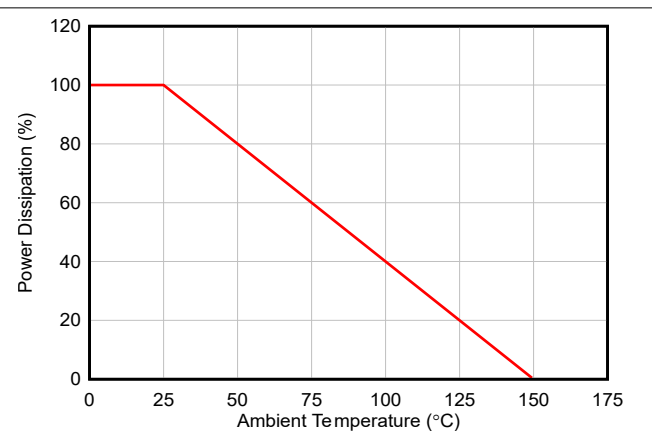


Figure 5-2. Power Derating Curve

6 Device and Documentation Support

6.1 Documentation Support

6.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Diodes Packaging and Layout Guide](#)
- Texas Instruments, [Diodes Layout Guide user's guide](#)
- Texas Instruments, [Generic Evaluation Module user's guide](#)

6.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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6.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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6.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

6.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BZX84C15VDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	3LMG	Samples
BZX84C27VDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	3LNG	Samples
BZX84C8V2DBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	3IWG	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF BZX84C15V-Q1, BZX84C27V-Q1, BZX84C8V2-Q1 :

- Catalog : [BZX84C15V](#), [BZX84C27V](#), [BZX84C8V2](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

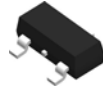
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BZX84C8V2DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BZX84C8V2DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

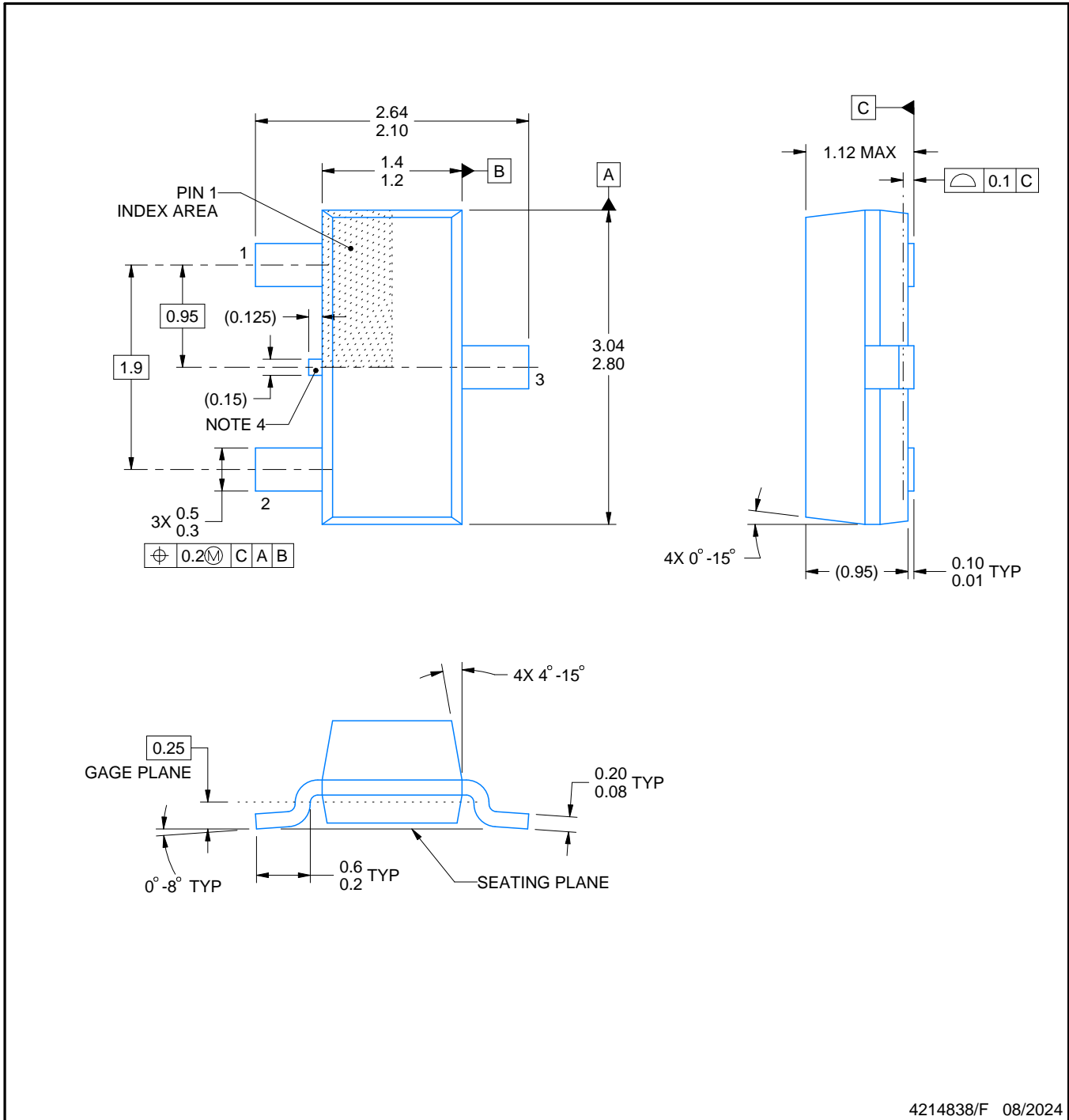
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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NOTES:

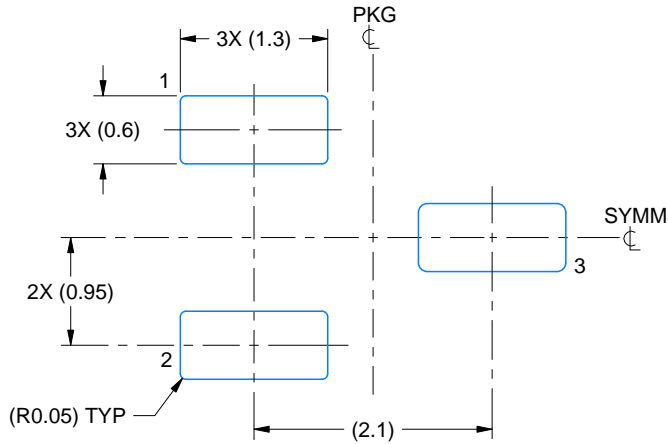
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

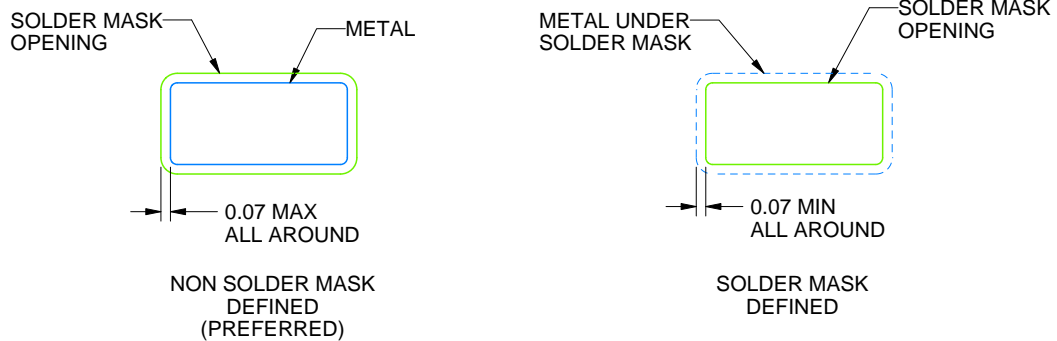
DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

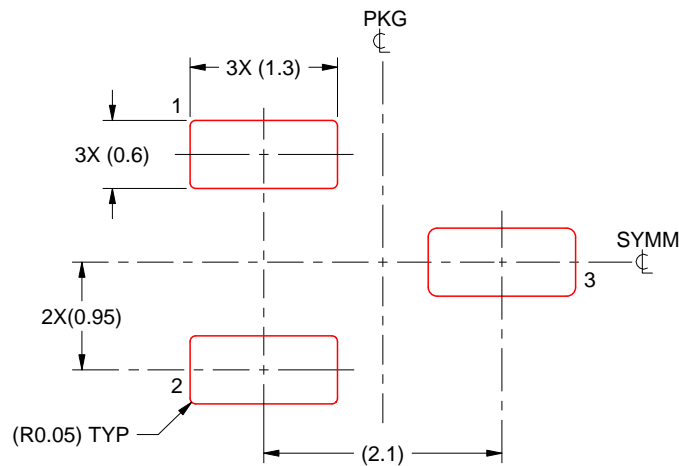
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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