

CDx4AC161 4-Bit Synchronous Binary Counters

1 Features

- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Synchronously programmable
- SCR-latchup-resistant CMOS process and circuit design
- Exceeds 2kV ESD protection per MIL-STD-883, method 3015

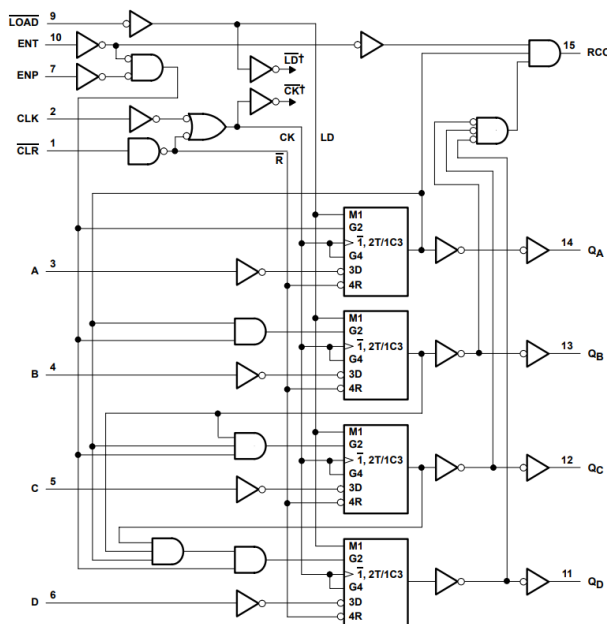
2 Description

The 'AC161 devices are 4-bit binary counters. These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
CDx4AC161	E (PDIP, 16)	19.3mm x 9.4mm	19.3mm x 6.35mm
	M (SOIC, 16)	9.9mm x 6mm	9.9mm x 3.9mm

- (1) For all available packages, see the package option addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.
- (3) The body size (length × width) is a nominal value and does not include pins.



Logic Diagram (Positive Logic)



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3 Pin Configuration and Functions

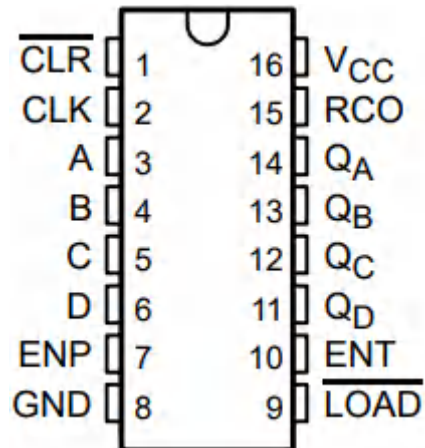


Figure 3-1. CD54AC161 F Package, CD74AC161 E or M Package (Top View)

Pin Functions

NAME	PIN	TYPE	DESCRIPTION
CLR	1	I	Clear, active low
CLK	2	I	Clock, rising edge triggered
A	3	I	Load data A
B	4	I	Load data B
C	5	I	Load data C
D	6	I	Load data D
ENP	7	I	Count enable, does not affect RCO
GND	8	—	Ground
LOAD	9	I	Parallel load, active low
ENT	10	I	Count enable, affects RCO
Q _D	11	O	Q _D output
Q _C	12	O	Q _C output
Q _B	13	O	Q _B output
Q _A	14	O	Q _A output
RCO	15	O	Ripple-carry output
V _{CC}	16	—	Supply

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	6	V
I _{IK} ⁽²⁾	Input clamp current	(V _I < 0 or V _I > V _{CC})		±20 mA
I _{OK} ⁽²⁾	Output clamp current	(V _O < 0 or V _O > V _{CC})		±50 mA
I _O	Continuous output current	(V _O > 0 V or V _O < V _{CC})		±50 mA
	Continuous current through V _{CC} or GND			±100 mA
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		TA = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.5	1.2	1.2		1.2		V
		V _{CC} = 3	2.1	2.1		2.1		
		V _{CC} = 5.5	3.85	3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 1.5 V		0.3		0.3		V
		V _{CC} = 3 V		0.9		0.9		
		V _{CC} = 5.5 V		1.65		1.65		
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 4.5 V to 5.5 V		-24	-24		-24	mA
I _{OL}	Low-level output current	V _{CC} = 4.5 V to 5.5 V		24	24		24	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.5 V to 3 V		50	50		50	ns/V
		V _{CC} = 3.6 V to 5.5 V		20	20		20	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, [Implications of Slow or Floating CMOS Inputs](#) (SCBA004).

4.4 Thermal Information

THERMAL METRIC ⁽¹⁾		CDx4AC161		UNIT
		E	M	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67	73	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	TA = 25°C		–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu A$	1.5 V	1.4	1.4	1.4			V	
			3 V	2.9	2.9	2.9				
			4.5 V	4.4	4.4	4.4				
		$I_{OH} = -4 \text{ mA}$	3 V	2.58	2.4	2.48				
			4.5 V	3.94	3.7	3.8				
			5.5 V	–	3.85	–				
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$	1.5 V		0.1	0.1	0.1	V		
			3 V		0.1	0.1	0.1			
			4.5 V		0.1	0.1	0.1			
		$I_{OL} = 12 \text{ mA}$	3 V		0.36	0.5	0.44			
			4.5 V		0.36	0.5	0.44			
			5.5 V			1.65				
I_I	$V_I = V_{CC}$ or GND		5.5 V	± 0.1		± 1	± 1	μA		
			I_{CC}	$V_I = V_{CC}$ or GND	$I_O = 0$	5.5 V	8	160	80	μA
C_i				10		10	10	pF		

4.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	1.5 V		7		8	MHz
		3.3 V \pm 0.3 V		64		73	
		5 V \pm 0.5 V		90		103	
t_w	CLK high or low	1.5 V		69		61	ns
		3.3 V \pm 0.3 V		7.7		6.8	
		5 V \pm 0.5 V		5.5		4.8	
	\overline{CLR} low	1.5 V		63		55	ns
		3.3 V \pm 0.3 V		7		6.1	
		5 V \pm 0.5 V		5		4.4	

4.6 Timing Requirements (continued)

over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	–55°C to 125°C		–40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_{su}	Setup time, before CLK \uparrow	1.5 V	63		55		ns
		3.3 V \pm 0.3 V	7		6.1		
		5 V \pm 0.5 V	5		4.4		
	\overline{LOAD}	1.5 V	75		66		ns
		3.3 V \pm 0.3 V	8.4		7.4		
		5 V \pm 0.5 V	6		5.3		
t_h	Hold time	1.5 V	0		0		ns
		3.3 V \pm 0.3 V	0		0		
		5 V \pm 0.5 V	0		0		
	ENP or ENT	1.5 V	0		0		ns
		3.3 V \pm 0.3 V	0		0		
		5 V \pm 0.5 V	0		0		
t_{rec}	Recovery time, \overline{CLR} \uparrow before CLK \uparrow	1.5 V	75		66		ns
		3.3 V \pm 0.3 V	8.4		7.4		
		5 V \pm 0.5 V	6		5.3		

4.7 Switching Characteristics

over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (see [Parameter Measurement Information](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	–55°C to 125°C		–40°C to 85°C		UNIT
				MIN	MAX	MIN	MAX	
f_{max}			1.5 V	7		8		MHz
			3.3 V \pm 0.3 V	64		73		
			5 V \pm 0.5 V	90		103		
t_{pd}	CLK	RCO	1.5 V	–	209	–	190	ns
			3.3 V \pm 0.3 V	6	23.4	6	21	
			5 V \pm 0.5 V	4.3	16.7	4.3	15.2	
		Any Q	1.5 V	–	207	–	188	
			3.3 V \pm 0.3 V	5.9	23.1	5.9	21	
			5 V \pm 0.5 V	4.2	16.5	4.2	15	
	ENT	RCO	1.5 V	–	129	–	117	
			3.3 V \pm 0.3 V	3.6	14.4	3.7	13.1	
			5 V \pm 0.5 V	2.6	10.3	2.7	9.4	
	CLR	Any Q	1.5 V	–	207	–	188	
			3.3 V \pm 0.3 V	5.9	23.1	5.9	21	
			5 V \pm 0.5 V	4.2	16.5	4.2	15	
RCO		1.5 V	–	207	–	188		
		3.3 V \pm 0.3 V	5.9	23.1	5.9	21		
		5 V \pm 0.5 V	4.2	16.5	4.2	15		

4.8 Timing Diagrams

The following sequence is illustrated below:

1. Clear outputs to zero (asynchronous)
2. Preset to binary 12
3. Count to 13, 14, 15, 0, 1, and 2
4. Inhibit

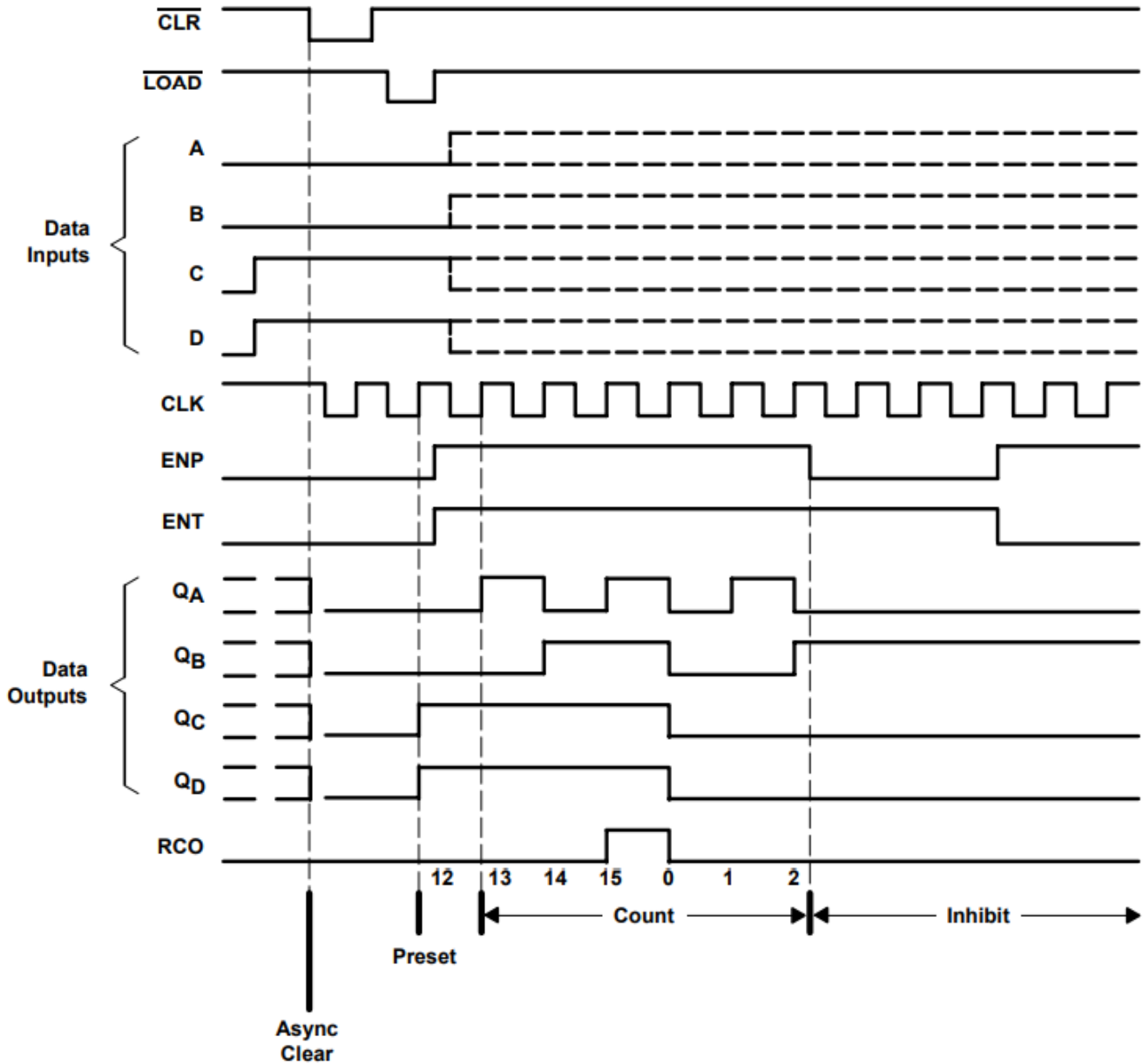


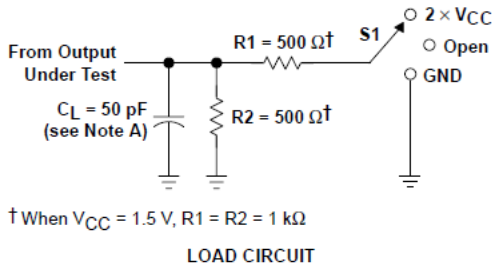
Figure 4-1. Typical clear, preset, count, and inhibit sequence

4.9 Operating Characteristics

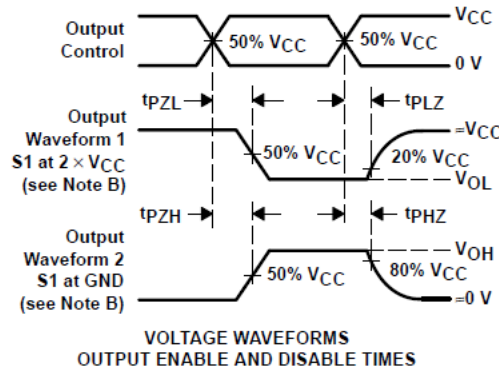
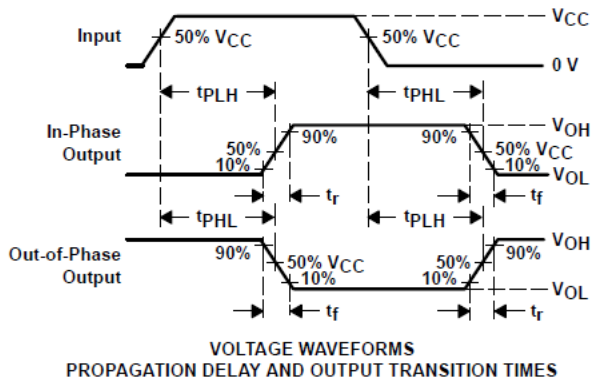
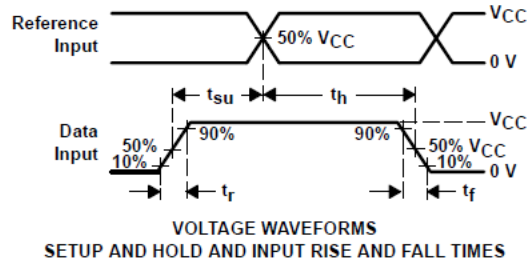
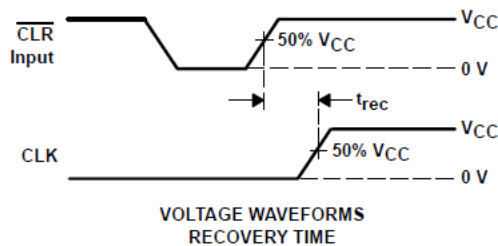
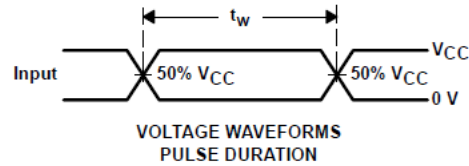
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load	66	pF

5 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



A. CL includes probe and test-fixture capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 3 \text{ ns}$, $t_f = 3 \text{ ns}$. Phase relationships between waveforms are arbitrary.

D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.

E. The outputs are measured one at a time with one input transition per measurement.

F. t_{PLH} and t_{PHL} are the same as t_{pd} .

G. t_{PZL} and t_{PZH} are the same as t_{en} .

H. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

6 Detailed Description

6.1 Overview

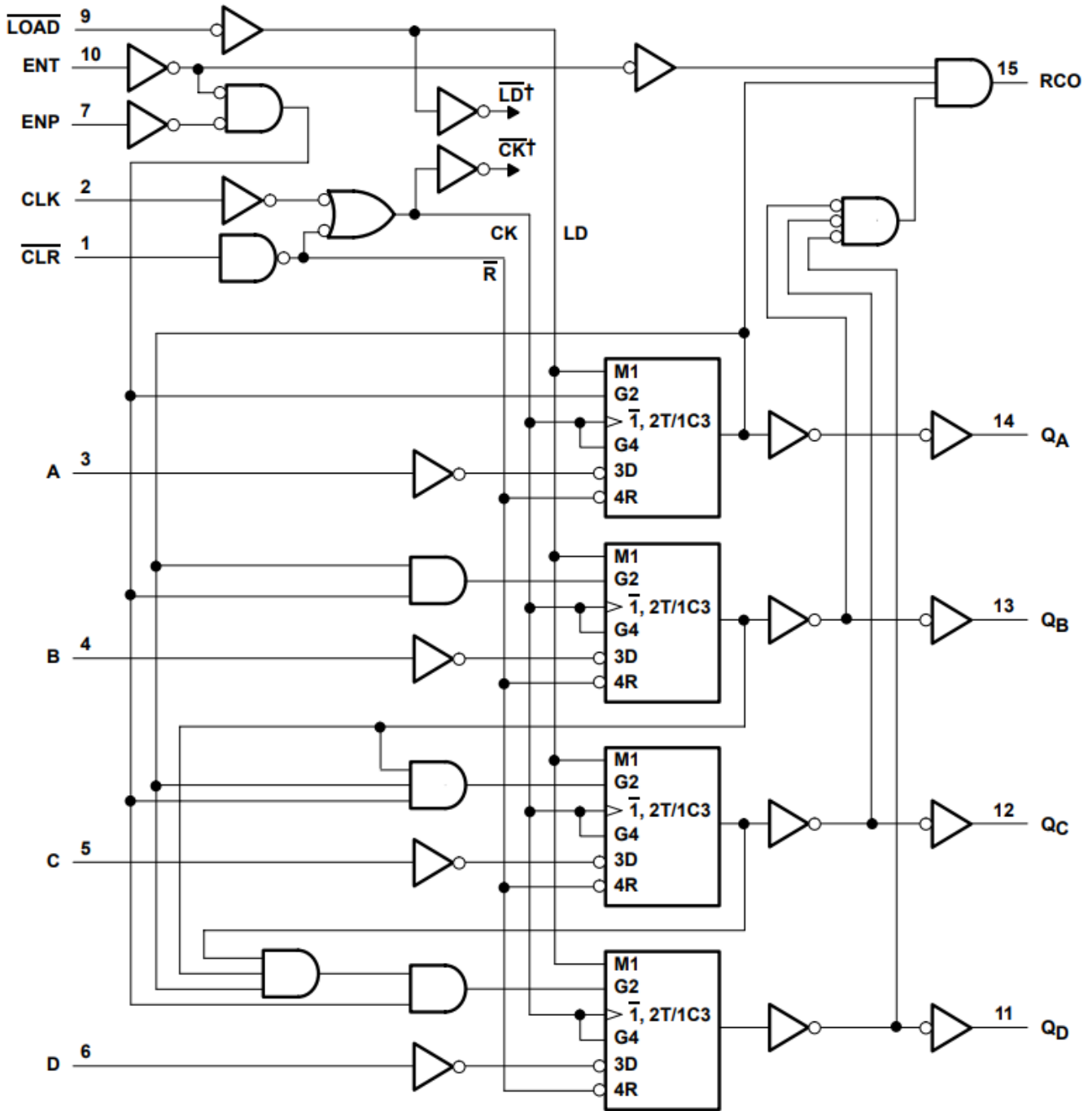
The 'AC161 devices are 4-bit binary counters. These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting. These devices are fully programmable; that is, they can be preset to any number between 0 and 9 or 15. Presetting is synchronous; therefore, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable inputs.

The clear function is asynchronous. A low level at the clear ($\overline{\text{CLR}}$) input sets all four of the flip-flop outputs low, regardless of the levels of the CLK, load ($\overline{\text{LOAD}}$), or enable inputs.

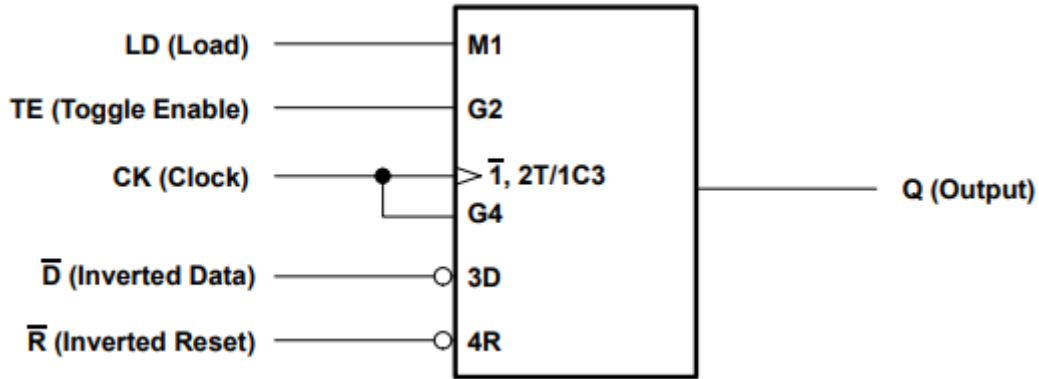
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are ENP, ENT, and a ripple-carry output (RCO). Both ENP and ENT must be high to count, and ENT is fed forward to enable RCO. Enabling RCO produces a high-level pulse while the count is maximum (9 or 15, with QA high). This high-level overflow ripple-carry pulse can be used to enable successive cascaded stages. Transitions at ENP or ENT are allowed, regardless of the level of CLK.

The counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

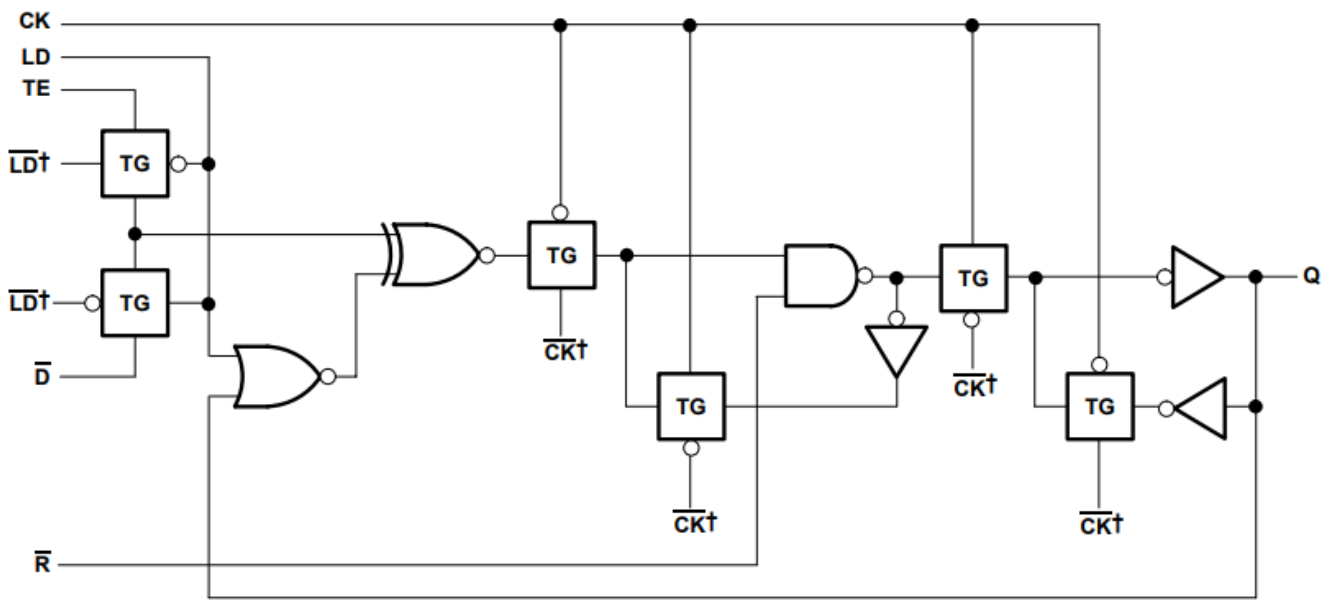
6.2 Functional Block Diagram



Logic Diagram (positive logic)



Logic Symbol, each D/T flip-flop



logic diagram, each D/T flip-flop (positive logic)

6.3 Device Functional Modes

Table 6-1. Function Table

INPUTS						OUTPUTS		FUNCTION
CLR	CLK	ENP	ENT	LOAD	A,B,C,D	Q _n	R _{CO}	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	Note 1	
H	↑	h	h	h	X	Count	Note 1	Count
H	X	l	X	h	X	q _n	Note 1	Inhibit
H	X	X	l	h	X	q _n	L	

H = high level, L = low level, X = don't care, h = high level one setup time prior to the CLK low-to-high transition, l = low level one setup time prior to the CLK low-to-high transition, q = the state of the referenced output prior to the CLK low-to-high transition, and ↑ = CLK low-to-high transition.

NOTE 1: The RCO output is high when ENT is high and the counter is at terminal count

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply may be any voltage between the minimum and maximum supply voltage rating located in [Section 4.3](#).

Each V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for devices with a single supply. If there are multiple V_{CC} terminals, then 0.01- μ F or 0.022- μ F capacitors are recommended for each power terminal. It is permissible to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor must be installed as close to the power terminal as possible for the best results.

7.2 Layout

7.2.1 Layout Guidelines

Inputs must not float when using multiple bit logic devices. In many cases, functions or parts of functions of digital logic devices are unused. Some examples include situations when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, they are tied to GND or V_{CC} , whichever makes more sense or is more convenient.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD54AC161	Click here	Click here	Click here	Click here	Click here
CD74AC161	Click here	Click here	Click here	Click here	Click here

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 1998) to Revision D (May 2024)	Page
• Added <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54AC161F3A	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54AC161F3A	Samples
CD74AC161E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74AC161E	Samples
CD74AC161M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC161M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54AC161, CD74AC161 :

- Catalog : [CD74AC161](#)
- Military : [CD54AC161](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC161M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC161M96	SOIC	D	16	2500	340.5	336.1	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74AC161E	N	PDIP	16	25	506	13.97	11230	4.32
CD74AC161E	N	PDIP	16	25	506	13.97	11230	4.32

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



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- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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