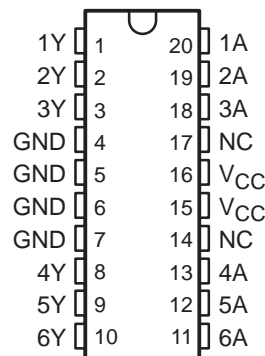


# CDC204 HEX INVERTER/CLOCK DRIVER

SCAS098E – OCTOBER 1989 – REVISED OCTOBER 1998

- CDC204 Replaces 74AC11204
- Low-Skew Propagation Delay Specifications for Clock-Driver Applications
- CMOS-Compatible Inputs and Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin  $V_{CC}$  and GND Pin Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- $\mu$ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Package (DW))

DW PACKAGE  
(TOP VIEW)



NC – No internal connection

## description

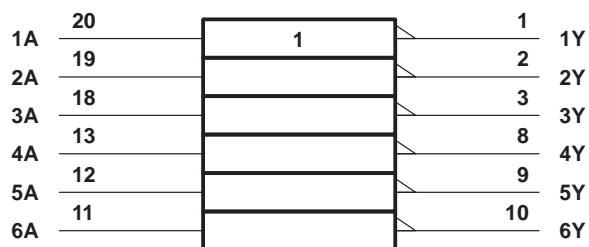
The CDC204 contains six independent inverters. The device performs the Boolean function  $Y = \bar{A}$ . It is designed specifically for applications requiring low skew between switching outputs.

The CDC204 is characterized for operation from  $T_A = 25^\circ\text{C}$  to  $70^\circ\text{C}$ .

FUNCTION TABLE

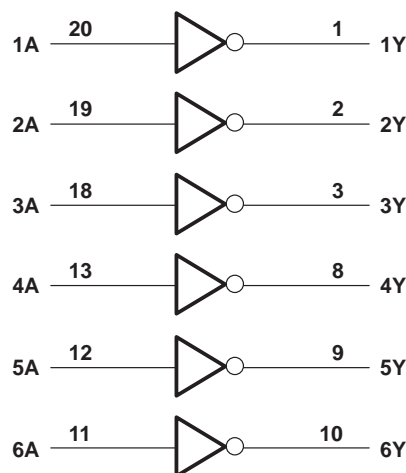
INPUT A	OUTPUT Y
H	L
L	H

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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# CDC204

## HEX INVERTER/CLOCK DRIVER

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 150$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2)	1.6 W
Storage temperature range, $T_{stg}$	$-65^\circ\text{C}$ to $150^\circ\text{C}$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage	$V_{CC} = 4.75$ V	3.3		V
		$V_{CC} = 5.25$ V	3.7		
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.75$ V		1.4	V
		$V_{CC} = 5.25$ V		1.6	
$V_I$	Input voltage	0		$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 4.75$ V		-24	mA
		$V_{CC} = 5.25$ V		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 4.75$ V		24	mA
		$V_{CC} = 5.25$ V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	ns/V
$f_{clock}$	Input clock frequency			80	MHz
$T_A$	Operating free-air temperature	25		70	$^\circ\text{C}$



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		T <sub>A</sub> †	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level voltage output	I <sub>OH</sub> = -50 μA	V <sub>CC</sub> = 4.75 V	25°C	4.65			V
				Full range	4.65			
			V <sub>CC</sub> = 5.25 V	25°C	5.15			
				Full range	5.15			
		I <sub>OH</sub> = -24 mA	V <sub>CC</sub> = 4.75 V	25°C	4.19			
				Full range	4.05			
			V <sub>CC</sub> = 5.25 V	25°C	4.68			
				Full range	4.55			
		I <sub>OH</sub> = -75 mA‡, V <sub>CC</sub> = 5.25 V	Full range	3.6				
		V <sub>OL</sub>	Low-level voltage output	I <sub>OL</sub> = 50 μA	V <sub>CC</sub> = 4.75 V	25°C	0.1	
Full range	0.1							
V <sub>CC</sub> = 5.25 V	25°C				0.1			
	Full range				0.1			
I <sub>OL</sub> = 24 mA	V <sub>CC</sub> = 4.75 V			25°C	0.36			
				Full range	0.44			
	V <sub>CC</sub> = 5.25 V			25°C	0.36			
				Full range	0.44			
I <sub>OL</sub> = 75 mA‡, V <sub>CC</sub> = 5.25 V	Full range			1.65				
I <sub>I</sub>	Input current			V <sub>I</sub> = V <sub>CC</sub> or GND	V <sub>CC</sub> = 5.25 V	25°C	±0.1	
		Full range	±1					
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	V <sub>CC</sub> = 5.25 V,	25°C	4			μA
				Full range	40			
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND,	V <sub>CC</sub> = 5 V	25°C	4			pF

† Full range is T<sub>A</sub> = 25°C to 70°C.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.25 V (see Note 3 and Figures 1 and 2)**

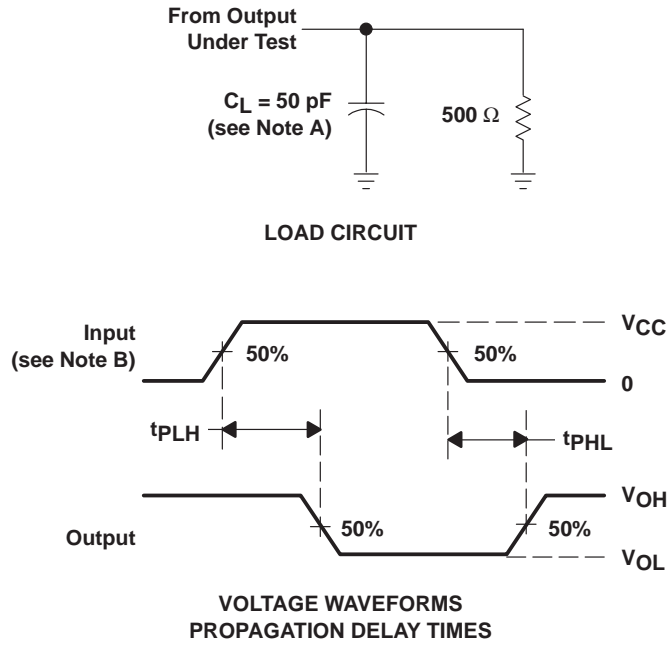
PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high level (see Figure 1)	A	Y	3.7	5.7	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low level (see Figure 1)			2.9	5.7	
t <sub>sk(o)</sub>	Output skew time (see Figure 2)	A	Y	1		ns

NOTE 3: All specifications are valid only for all outputs switching simultaneously and in phase.

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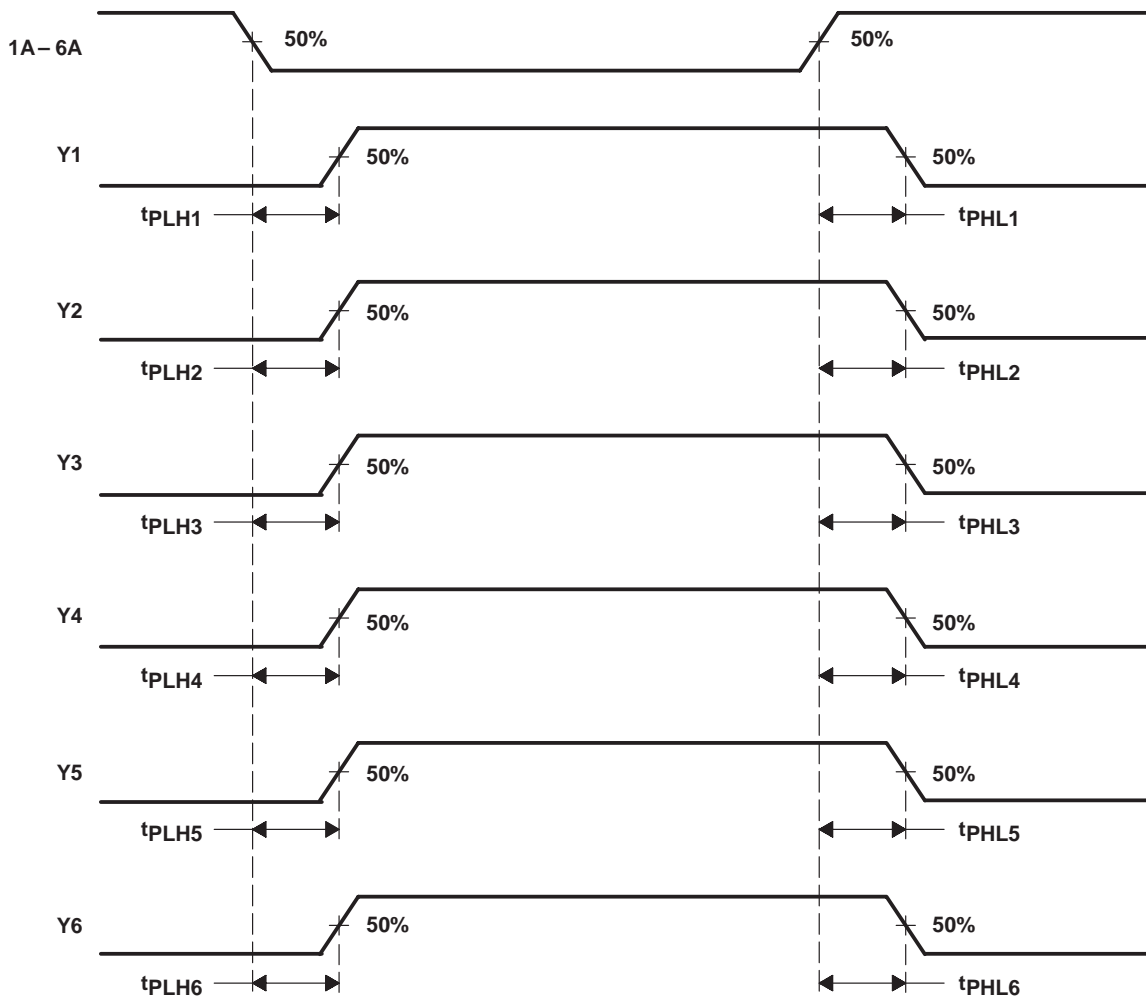
## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ .  
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew,  $t_{sk(o)}$ , is calculated as the greater of:  
 – The difference between the fastest and slowest of  $t_{PHLn}$  ( $n = 1, 2, \dots, 6$ )  
 – The difference between the fastest and slowest of  $t_{PLHn}$  ( $n = 1, 2, \dots, 6$ )

Figure 2. Waveforms for Calculation of  $t_{sk(o)}$

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDC204DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	25 to 70	CDC204	<a href="#">Samples</a>
CDC204DWG4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	25 to 70	CDC204	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CDC204DW	DW	SOIC	20	25	507	12.83	5080	6.6
CDC204DWG4	DW	SOIC	20	25	507	12.83	5080	6.6



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