CSD19538Q2 100V N-Channel NexFET™ Power MOSFET

1 Features

- Ultra-low Q_g and Q_{gd}
- Low-thermal resistance
- Avalanche rated
- Lead free
- RoHS compliant
- Halogen free
- SON 2mm × 2mm plastic package

2 Applications

- Power over ethernet (PoE)
- Power sourcing equipment (PSE)
- Motor control

Description

This 100V, 49mΩ, SON 2mm × 2mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

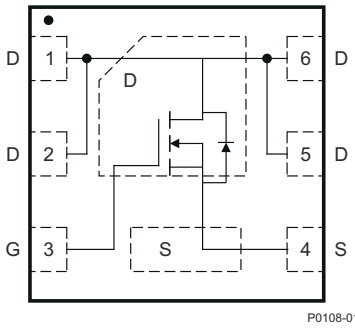


Figure 3-1. Top View

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	100		V
Q_g	Gate Charge Total (10V)	4.3		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.8		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 6V	58	mΩ
		V_{GS} = 10V	49	
$V_{GS(th)}$	Threshold Voltage	3.2		V

Device Information(1)

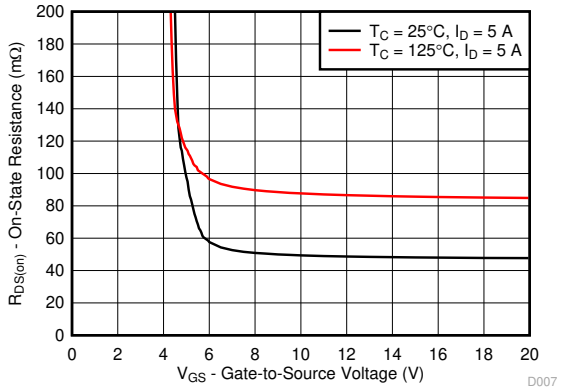
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD19538Q2	3000	7 Inch Reel	SON 2.00mm x 2.00mm Plastic Package	Tape and Reel
CSD19538Q2T	250			
CSD19538Q2R	10,000	13 Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

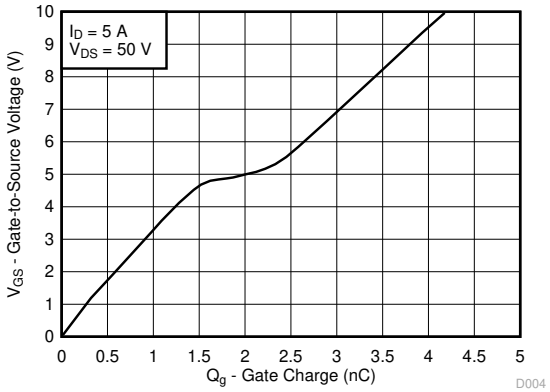
Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limited)	14.4	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	13.1	
	Continuous Drain Current(1)	4.6	
I_{DM}	Pulsed Drain Current(2)	34.4	A
P_D	Power Dissipation(1)	2.5	W
	Power Dissipation, T_C = 25°C	20.2	
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse I_D = 12.6A, L = 0.1mH, R_G = 25Ω	8	mJ

(1) Typical $R_{\theta JA}$ = 50°C/W on a 1 inch², 2oz Cu pad on a 0.06 inch thick FR4 PCB.
(2) Max $R_{\theta JC}$ = 6.2°C/W, pulse duration ≤ 100µs, duty cycle ≤ 1%.



$R_{DS(on)}$ vs V_{GS}



Gate Charge

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

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3 Specifications

3.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250µA	100			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0V, V_{DS} = 80V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	2.8	3.2	3.8	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 6V, I_D = 5A		58	72	mΩ
		V_{GS} = 10V, I_D = 5A		49	59	
g_{fs}	Transconductance	V_{DS} = 10V, I_D = 5A		19		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		349	454	pF
C_{oss}	Output capacitance			69	90	pF
C_{rss}	Reverse transfer capacitance			12.6	16.4	pF
R_G	Series gate resistance			4.6	9.2	Ω
Q_g	Gate charge total (10V)	V_{DS} = 50V, I_D = 5A		4.3	5.6	nC
Q_{gd}	Gate charge gate-to-drain			0.8		nC
Q_{gs}	Gate charge gate-to-source			1.6		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.0		nC
Q_{oss}	Output charge	V_{DS} = 50V, V_{GS} = 0V		12.3		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 50V, V_{GS} = 10V, I_{DS} = 5A, R_G = 0Ω		5		ns
t_r	Rise time			3		ns
$t_{d(off)}$	Turnoff delay time			7		ns
t_f	Fall time			2		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 5A, V_{GS} = 0V		0.85	1.0	V
Q_{rr}	Reverse recovery charge	V_{DS}= 50V, I_F = 5A, di/dt = 300A/µs		94		nC
t_{rr}	Reverse recovery time			32		ns

3.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance(1)			6.2	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1) (2)			65	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu pad on a 1.5in × 1.5in (3.81cm × 3.81cm), 0.06in (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu.

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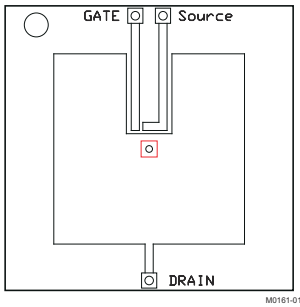
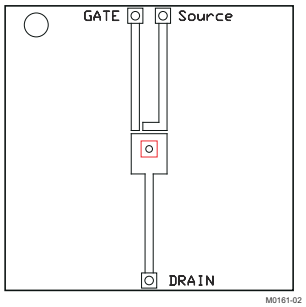


Max $R_{\theta JA}$ = 65°C/W when mounted on 1in^2 (6.45cm^2) of 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 250°C/W when mounted on a minimum pad area of 2oz (0.071mm) thick Cu.

3.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

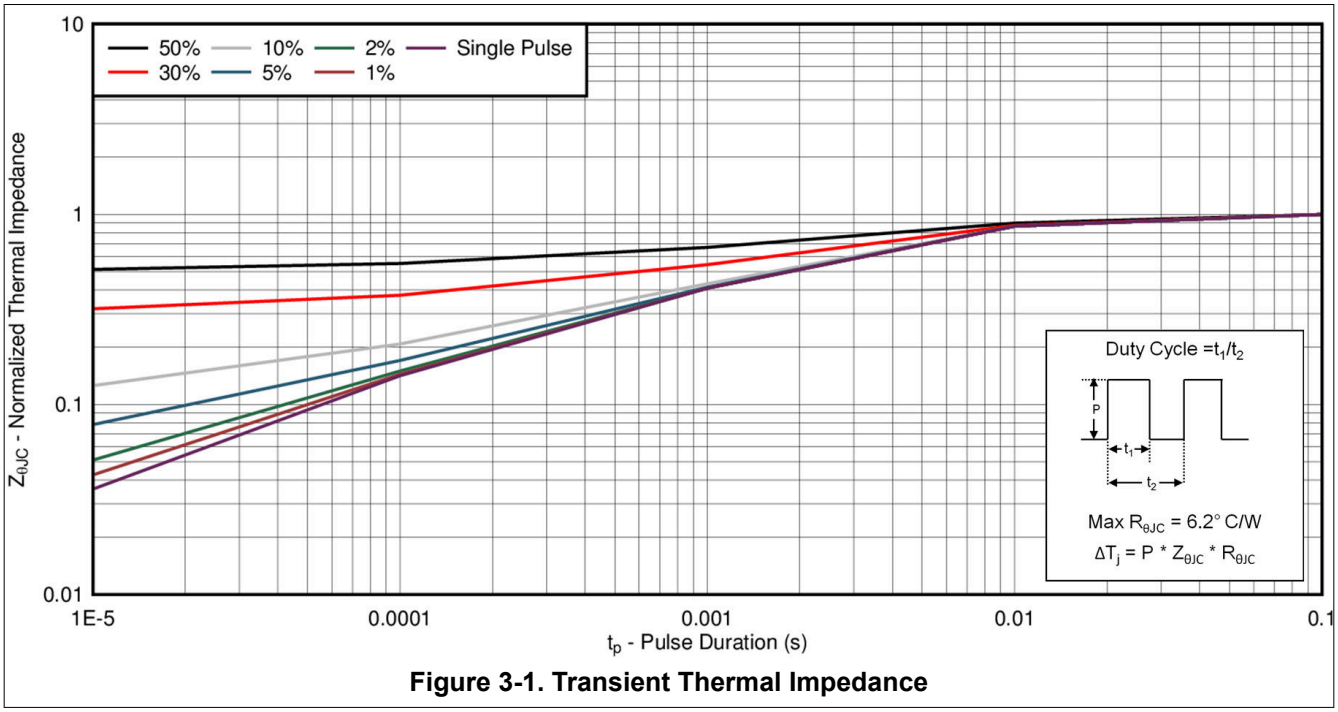


Figure 3-1. Transient Thermal Impedance

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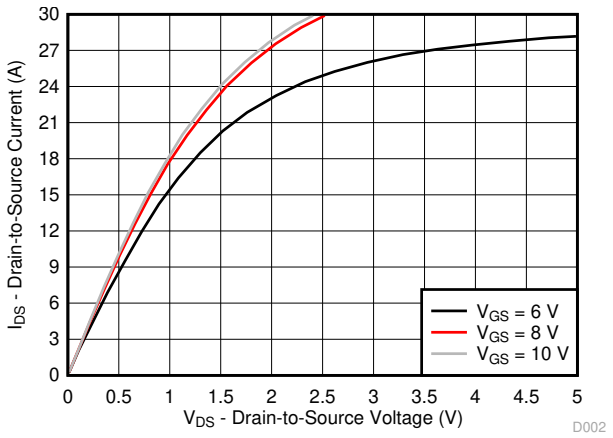
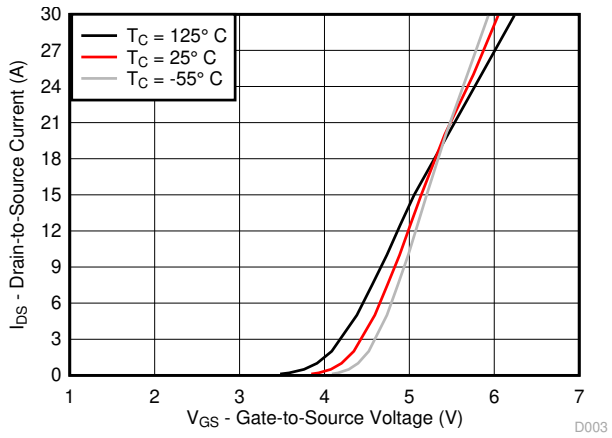
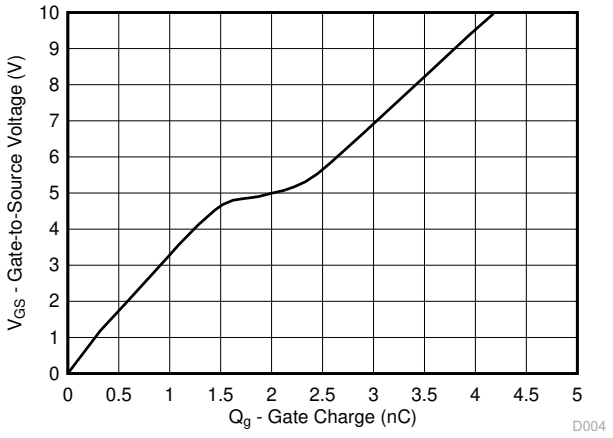


Figure 3-2. Saturation Characteristics



V_{DS} = 5V

Figure 3-3. Transfer Characteristics



I_D = 5A V_{DS} = 50V

Figure 3-4. Gate Charge

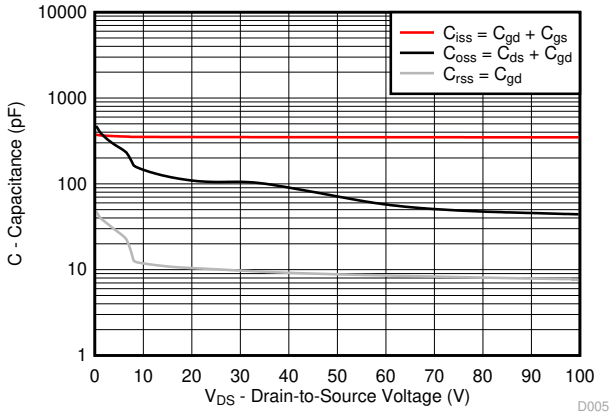
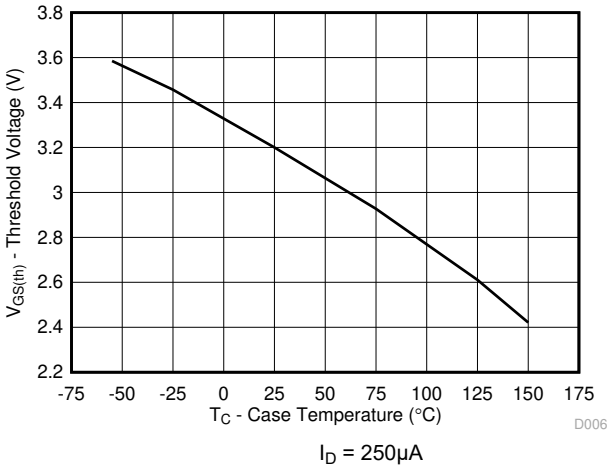


Figure 3-5. Capacitance



I_D = 250µA

Figure 3-6. Threshold Voltage vs Temperature

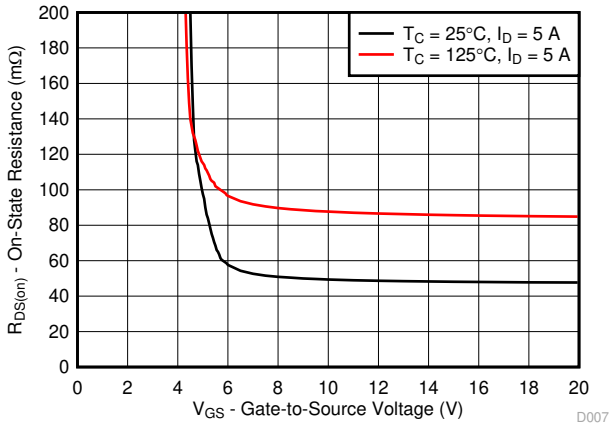
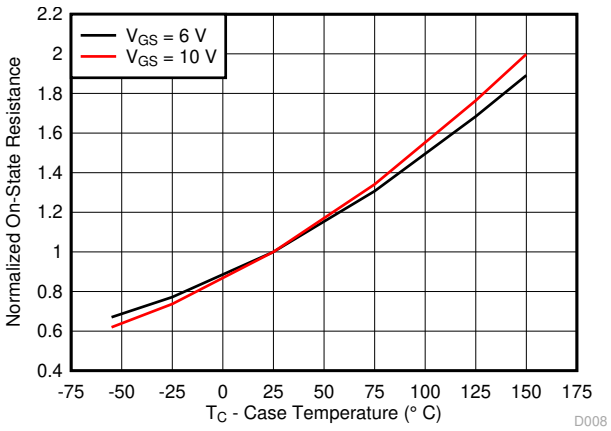


Figure 3-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 5A

Figure 3-8. Normalized On-State Resistance vs Temperature

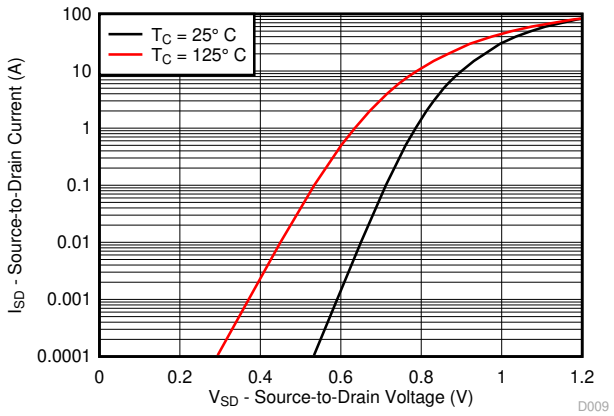
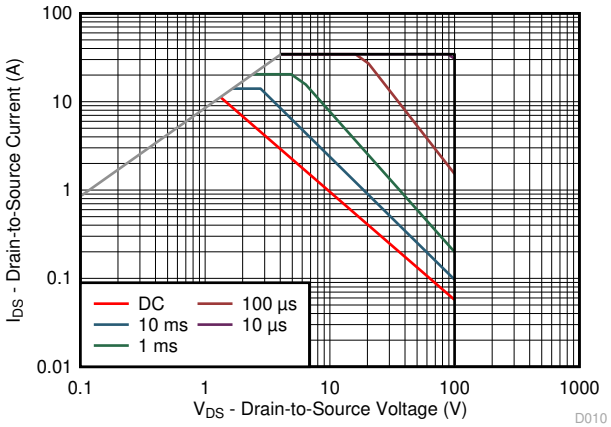


Figure 3-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 6.2°C/W

Figure 3-10. Maximum Safe Operating Area

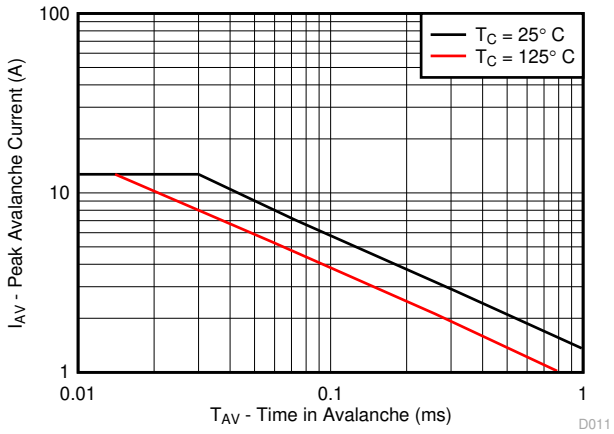


Figure 3-11. Single Pulse Unclamped Inductive Switching

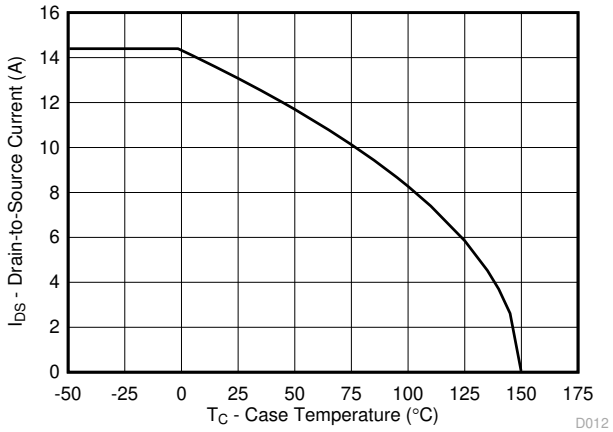


Figure 3-12. Maximum Drain Current vs Temperature

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4 Device and Documentation Support

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

Changes from Revision A (January 2017) to Revision B (March 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision * (July 2016) to Revision A (January 2017)	Page
• Changed test voltage V_{DS} from 100V : to 50V in Figure 3-2 curve	1
• Changed test voltage V_{DS} from 100V : to 50V in Figure 3-4	4

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6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19538Q2	ACTIVE	WSON	DQK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958	Samples
CSD19538Q2R	ACTIVE	WSON	DQK	6	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958	Samples
CSD19538Q2T	ACTIVE	WSON	DQK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1958	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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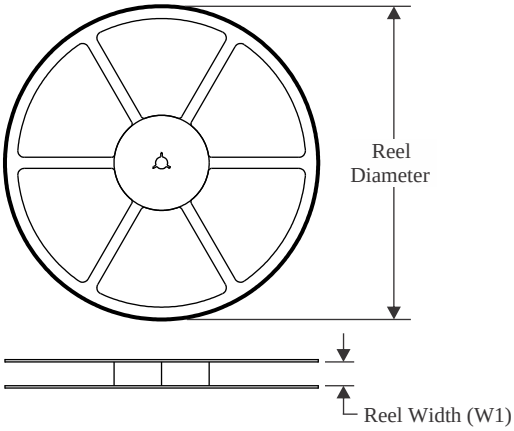
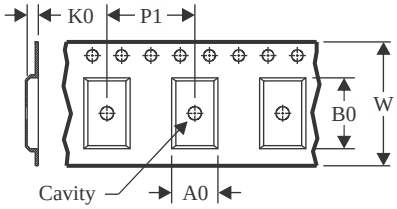
TAPE AND REEL INFORMATION

REEL DIMENSIONS

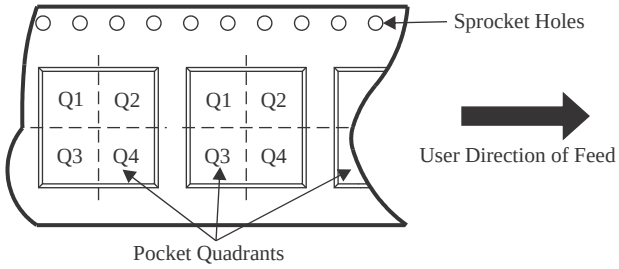


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

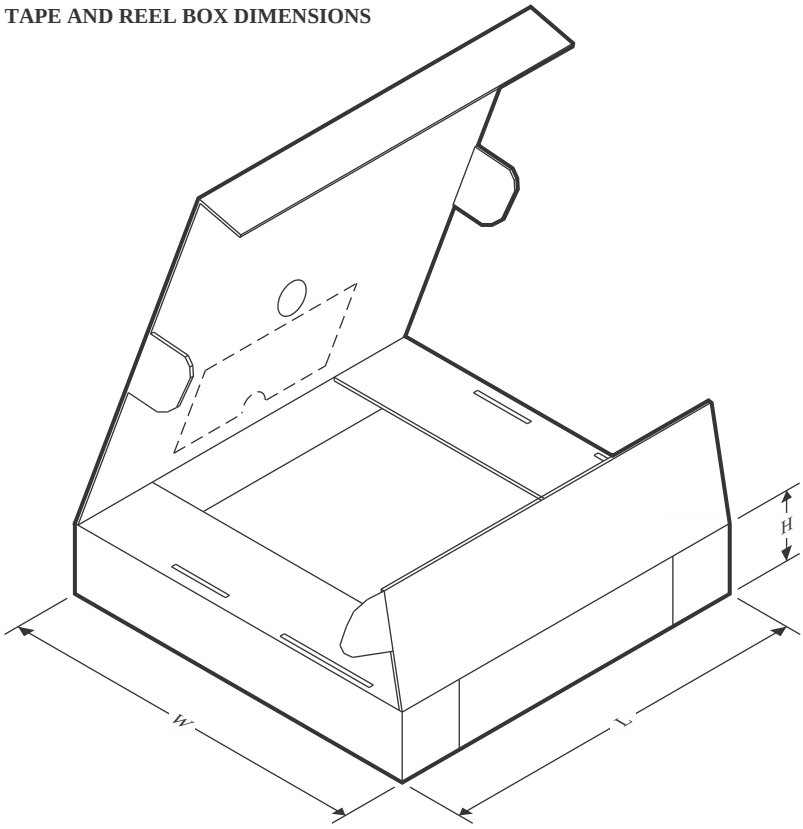
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD19538Q2	WSON	DQK	6	3000	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1
CSD19538Q2T	WSON	DQK	6	250	180.0	9.5	2.3	2.3	1.0	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD19538Q2	WSON	DQK	6	3000	189.0	185.0	36.0
CSD19538Q2T	WSON	DQK	6	250	189.0	185.0	36.0

GENERIC PACKAGE VIEW

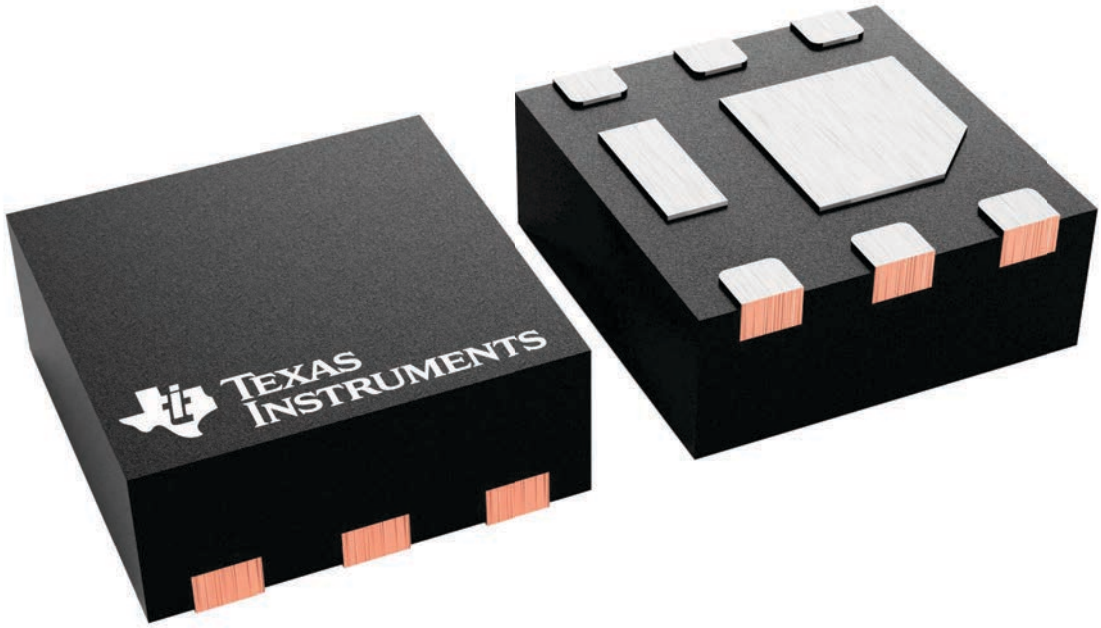
DQK 6

WSON - 0.8 mm max height

2 x 2, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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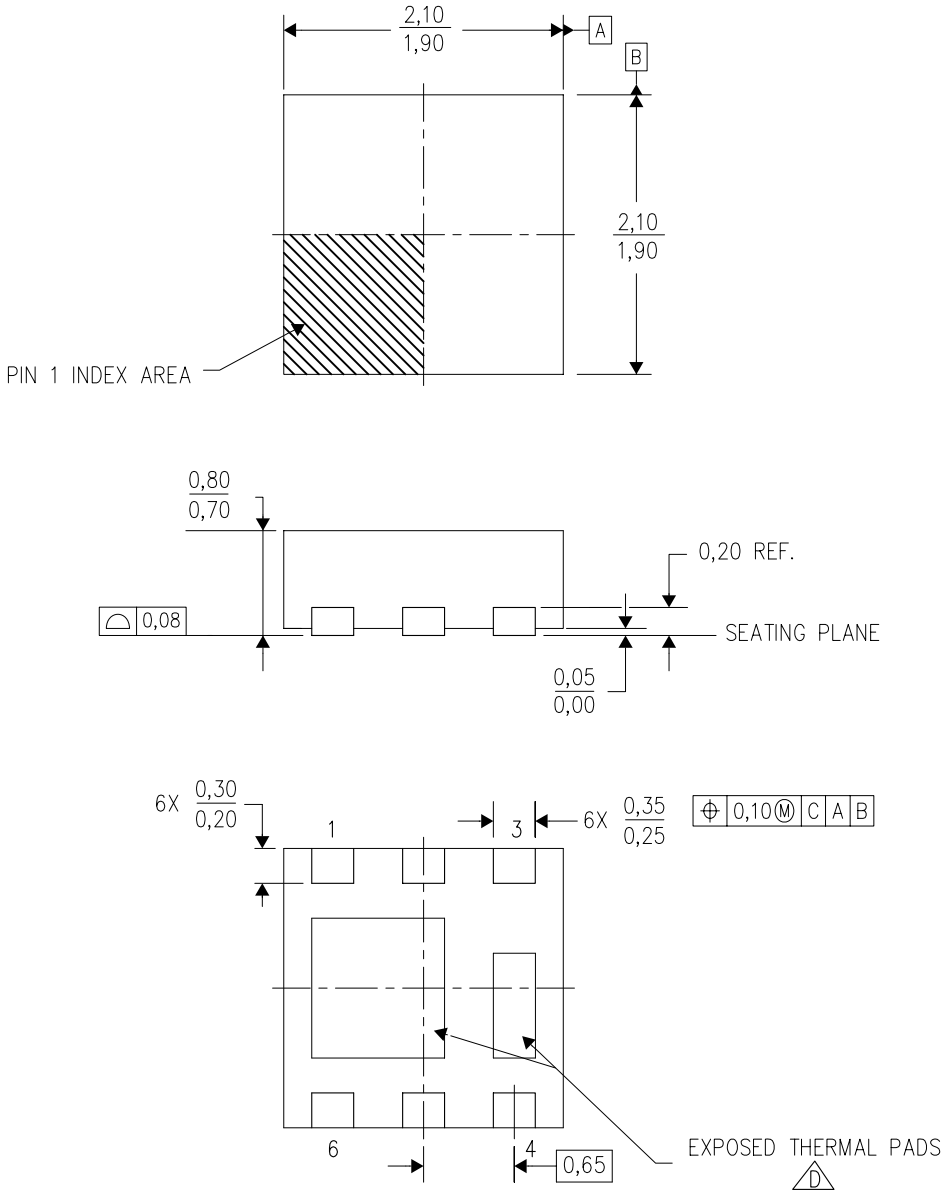
DQK (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4210192/B 01/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

THERMAL PAD MECHANICAL DATA

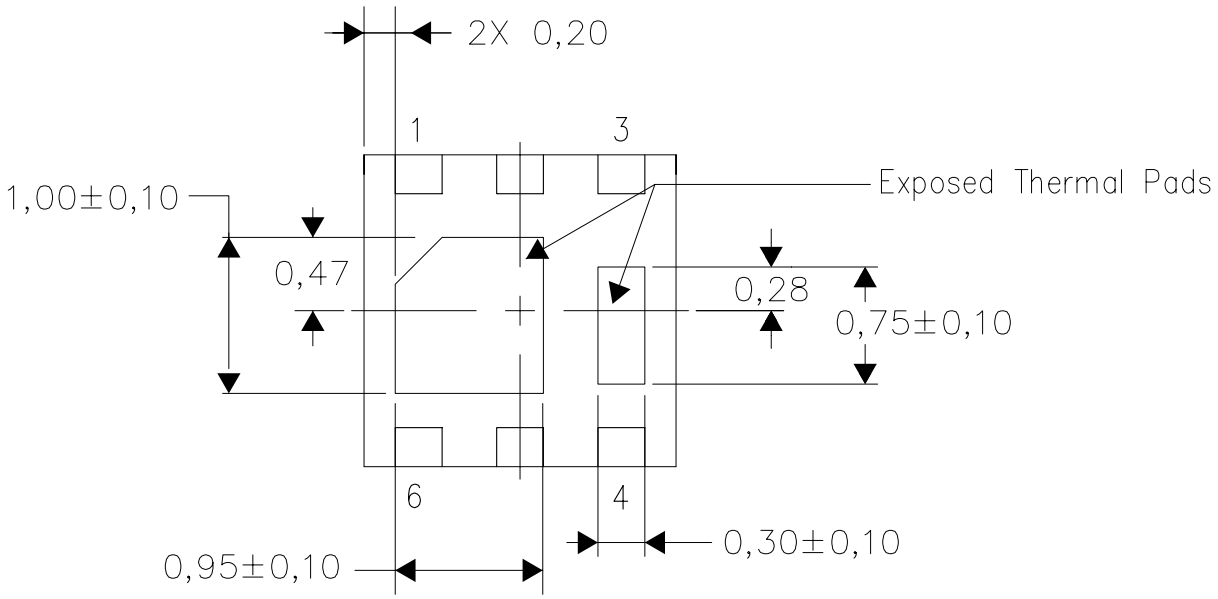
DQK (S–PWSON–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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