# DP83TC818S-Q1 Precise and Secure 100BASE-T1 Automotive Ethernet with TC10, IEEE802.1AS, IEEE802.1AE MACsec and AVB Clock Generation

## 1 Features

- IEEE 802.1AE MACsec
  - MACsec frame expansion: Inbuilt buffering and flow control support to handle 12 byte IPG ethernet frames
  - Authentication, encryption at line rate
  - Cipher suites: GCM-AES-XPN-128/256, GCM-AES-128/256
  - Secure Channel: Total 16 SAK enabling 8 Tx/Rx SC
  - Auto rollover support for SAK
  - Ingress/Egress classification for Ethertype, VLAN, DMAC: up to 8 parallel rules
  - Window replay protection
- IEEE 802.1AS time synchronization & fractional clock generation
  - Highly accurate 1pps signal < +/-5 ns
  - Precise time stamping for MACsec encoded PTP packets
  - I2S & TDM8 SCLK/FSYNC clock generation
  - Mulitple IOs for event capture and trigger
- IEEE 802.3bw & OA 100BASE-T1 compliant
- TC-10 compliant
  - < 20µA sleep current
  - Fast wake from sleep by retaining PHY configuration during sleep (optional)
- MAC Interfaces: MII, RMII, RGMII, SGMII
- Pin compatible with TI's 1000BASE-T1 PHY
  - Single board design for 100BASE-T1 and 1000BASE-T1 with required BOM change
- Diagnostic tool kit
  - Signal Quality Indication (SQI) & Time Domain Reflectometry (TDR)
  - Voltage, Temperature & ESD sensors
- AEC-Q10 qualified for Automotive Applications:
  - Temperature grade 1: –40°C to +125 °C

## 2 Applications

- ADAS
  - Radar
- Infotainment & Cluster
  - AVB Audio/Video
- Body Electronics & Lighting
  - Body Control Module
  - Zone Control Module
- Telematics

## 3 Description

The DP83TC818S-Q1 device is an IEEE 802.3bw automotive Ethernet physical layer transceiver. The device provides all physical layer functions needed to transmit and receive data, and xMII interface flexibility. DP83TC818S-Q1 is compliant to Open Alliance EMC and interoperable specifications over unshielded single twisted-pair cable. DP83TC818S-Q1 supports OA TC-10 low power sleep feature with wake forwarding for reduced system power consumption when communication is not required.

The DP83TC818S-Q1 integrates IEEE 802.1AE line rate security with authentication and optional encryption support, to secure communication over the network. The DP83TC818S-Q1 supports up to 16 secure association (SA) channels with automatic SAK rollover and extended packet numbering support. DP83TC818S-Q1 offers ingress classification to filter the unwanted packets & supports WAN MACsec for end-to-end security.

DP83TC818S-Q1 integrates IEEE 1588v2/802.1AS hardware time stamping & fractional PLL, enabling highly accurate time synchronization. The fractional PLL enables frequency and phase synchronization of the wall clock (eliminating the need for external VCXO) and generation of a wide range of time synchronized frequencies needed for audio and other ADAS applications. The PHY also integrates IEEE 1722 CRF decode to generate Media clock and Bit Clock for AVB & other audio applications.

**Device Information**

| PART NUMBER | PACKAGE(1) | BODY SIZE (NOM) (2) |
|---|---|---|
| DP83TC818S-Q1 | VQFN (36) | 6.00mm × 6.00mm |

(1) For all available packages, see Mechanical, Packaging and Orderable Information.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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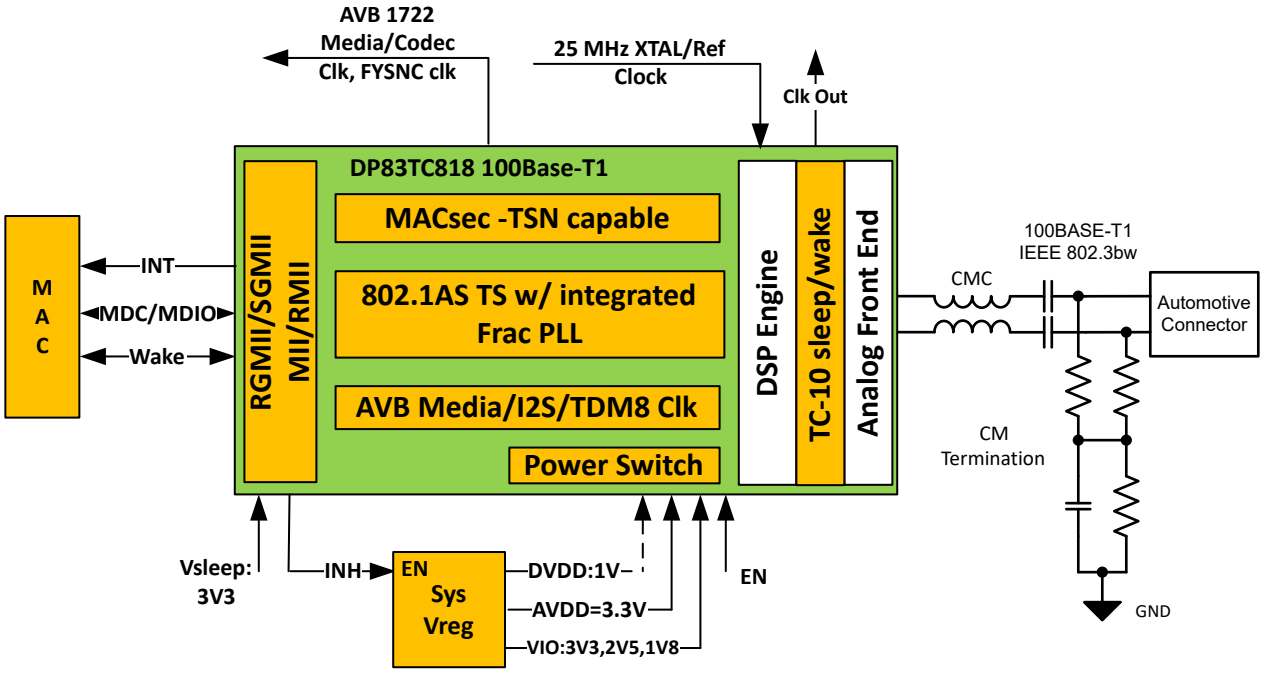


**Simplified Schematics**

## 4 Device Comparison Table

| PART NUMBER | TC10 SUPPORT | MACsec SUPPORT | 802.1AS SUPPORT | AVB CLOCK GENERATION SUPPORT | FOOTPRINT COMPATIBLE |
|---|---|---|---|---|---|
| DP83TC812x-Q1 | Yes | No | No | No | Yes |
| DP83TC814x-Q1 | No | No | No | No | Yes |
| DP83TC817S-Q1 | Yes | Yes | Yes | No | Yes |
| DP83TC818S-Q1 | Yes | Yes | Yes | Yes | Yes |

# 5 Application Information

## 5.1 MAC Security

DP83TC818S-Q1 integrates MAC Security, or MACsec (IEEE 802.1AE) hardware engine to perform line-rate security (encryption and authentication) on both egress and ingress data paths. IEEE802.1AE is a Layer 2 network security protocol that prevents a range of attacks including: denial of service, intrusion, man-in-the-middle, and eavesdropping. The block diagram below shows the major MACsec blocks within the PHY.

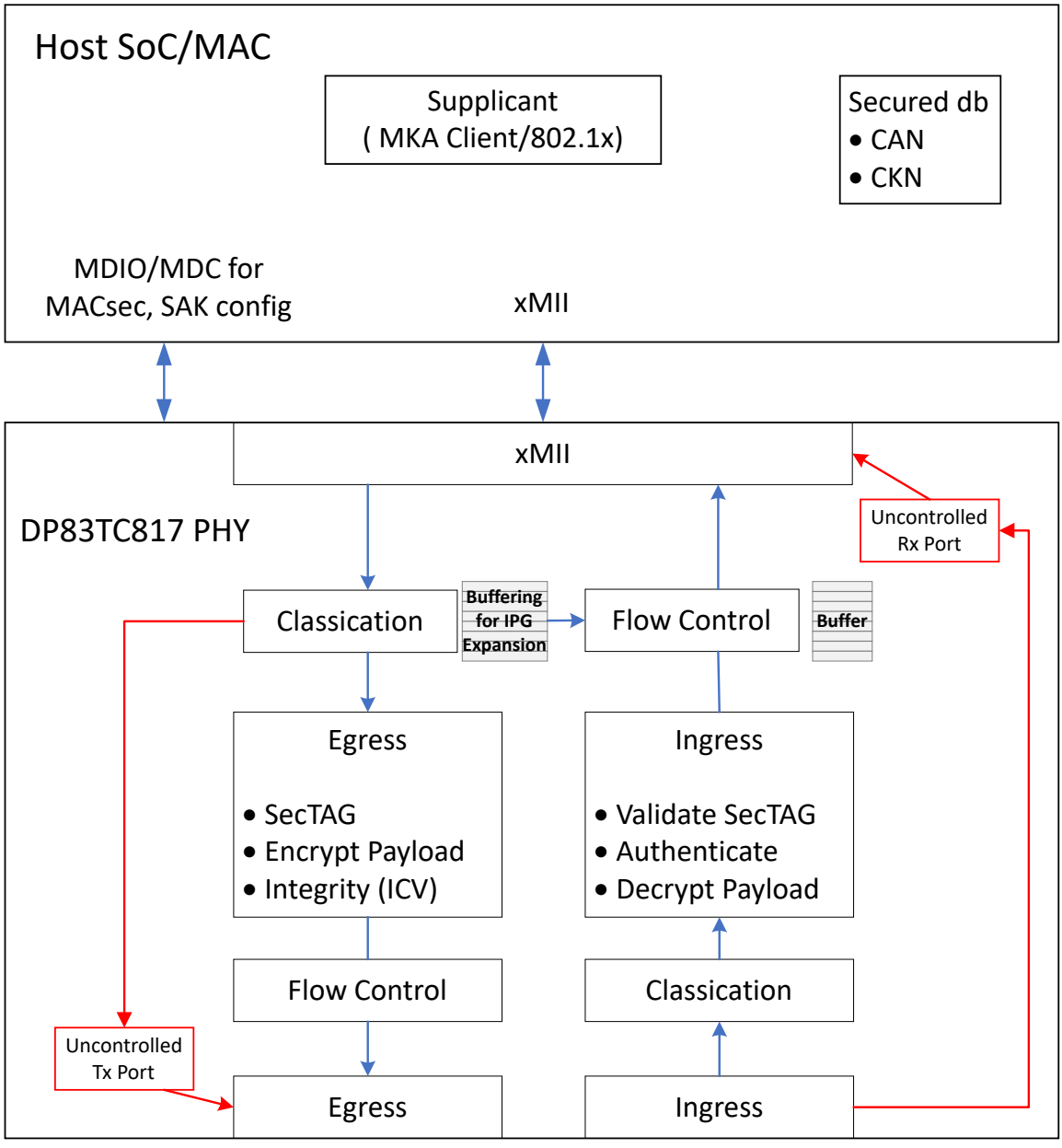


**Figure 5-1. MACsec Block Diagram**

## 5.2 TC10 Sleep Wake-up

DP83TC818S-Q1 is a 100BASE-T1 Ethernet PHY with TC-10 power saving feature with the following features.

- Open Alliance TC10 compliant
- Sleep request feature to shut down Ethernet network to save power
- 8µA (Typical, 27 °C), 20µA (Maximum, 125 °C) sleep current
- Wake forwarding feature for Ethernet network wake-up
- Fast Wake-up

This block diagram shows an example of how TC10 can be implemented in an automotive system. First, the wake up request originates over active link and then the wake up pulse is forwarded over passive link. The wake up request and pulses are exchanged over the Ethernet cable without needing dedicated wake up wire.

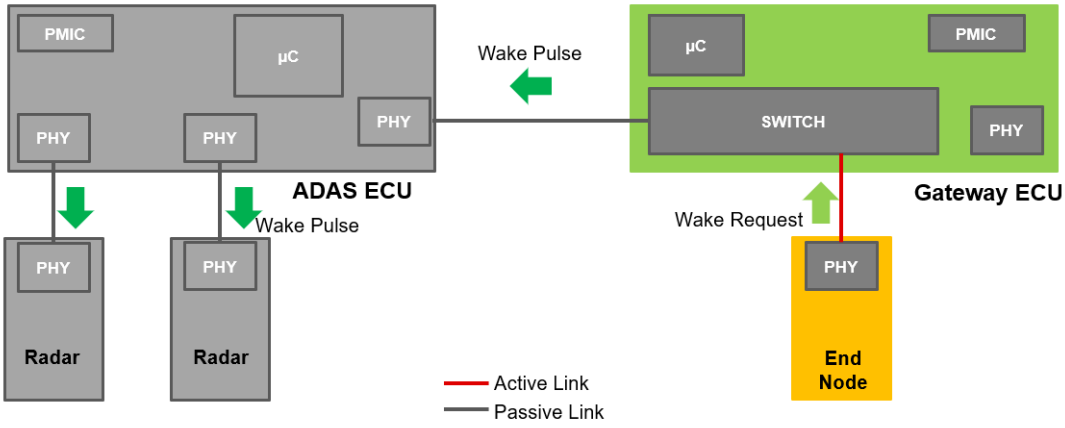


**Figure 5-2. TC10 ADAS System Use Case Example**

This block diagram shows the system level integration of DP83TC818S-Q1 to support the TC10 sleep/wake-up feature.

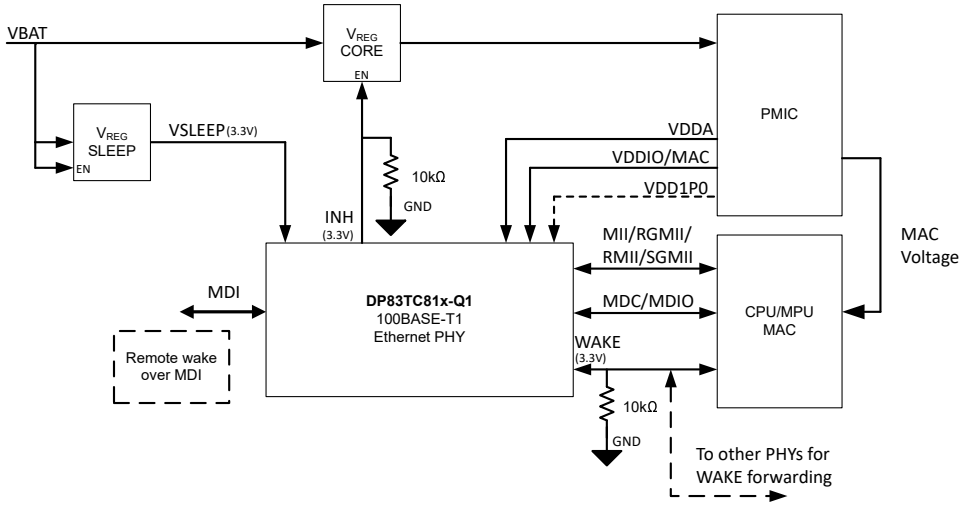


**Figure 5-3. System Block Diagram**

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## 5.3 Time Syncronization

The DP83TC818S-Q1 integrates IEEE 1588v2/802.1AS timestamping and other additional hardware engines to offer +/-5ns synchronization accuracy.

The DP83TC818S-Q1 is also capable of providing a high quality time synchronized clock signal to achieve system level synchronization for ADAS sensor data synchronisation, Corner RADAR Chirp synchronisation, 1 pps signal for LiDAR, V2X, etc.

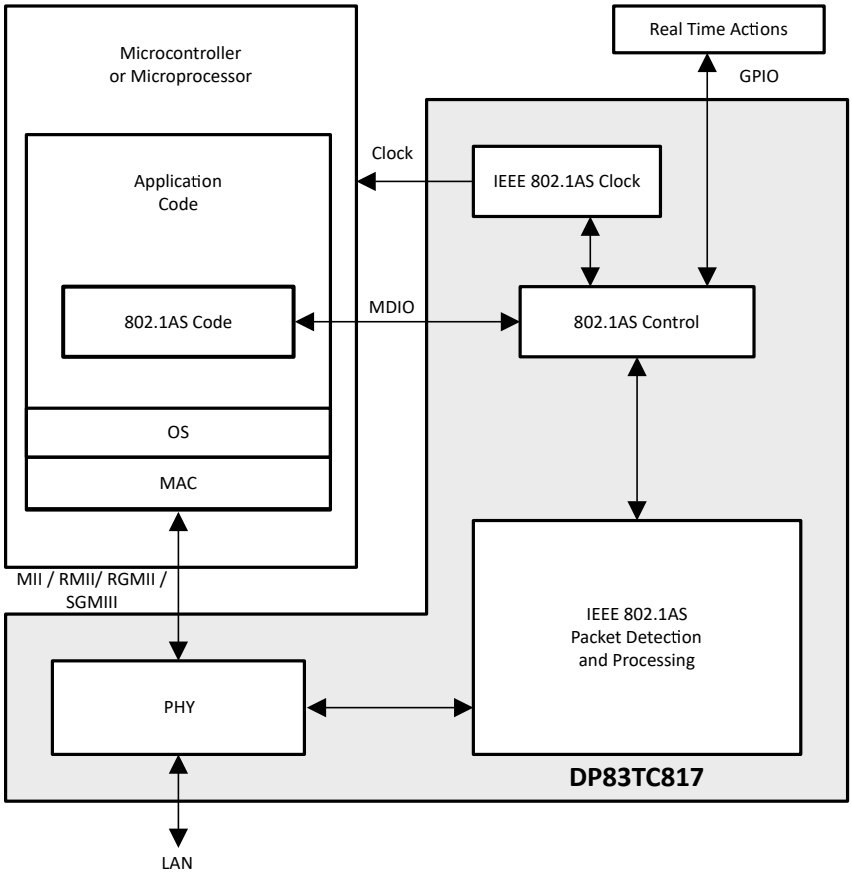


**Figure 5-4. DP83TC818S-Q1 Example PTP System Application**

## 5.4 Integrated Audio Over Ethernet

DP83TC818S-Q1 offers audio clocking solutions for AVB (Audio Video Bridging) and other Audio transports protocols (IES676, IEEE 1733 RTP, Dante) by:

- Generating IEEE 1722 Media Clock with embedded CRF packet decode
- Synchronised clocks (FSYNC, BCLK, MCLK) for Audio interface I2S and TDMx.

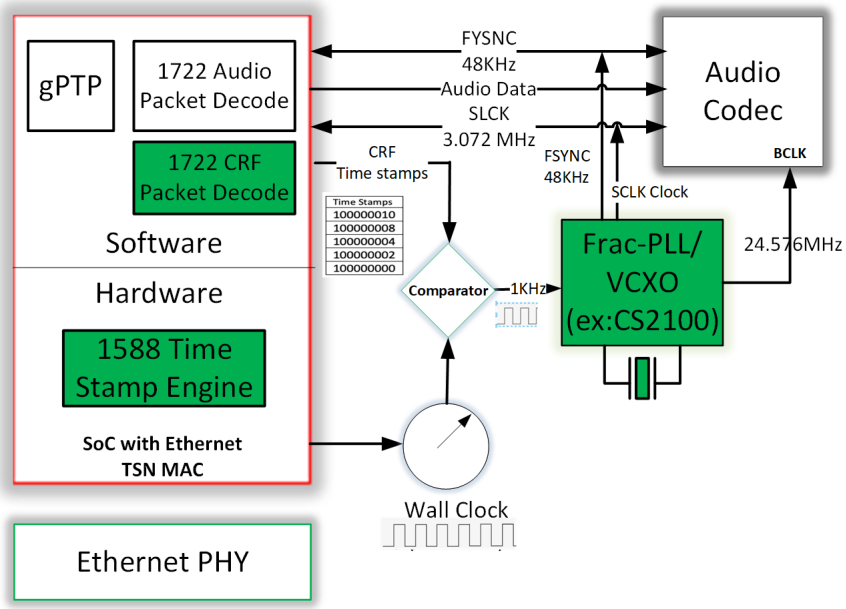


**Figure 5-5. Typical Audio Over Ethernet Architecture**

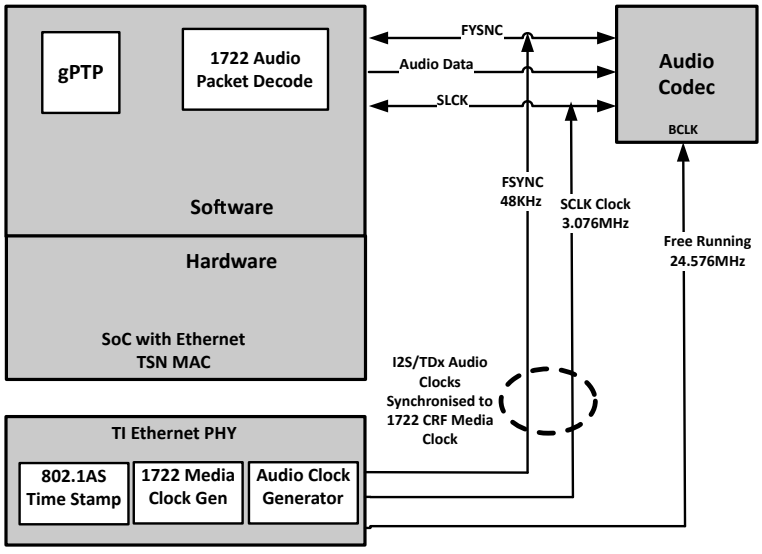


**Figure 5-6. Audio Over Ethernet Architecture with DP83TC818S-Q1**

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## 5.5 DP83TC818EVM-MC and Software Support

### DP83TC818EVM-MC

The DP83TC818EVM-MCsupports 100-Mbps speed and is IEEE 802.3bw compliant. This evaluation board is a media converter from 100Base-TX to 100Base-T1. There is an onboard MSP430F5529 for MDIO/MDC register access with the USB2MDIO and DIEP graphical user interface tools. DP83867 is provided for copper (100BASE-TX) support using RGMII MAC interface.

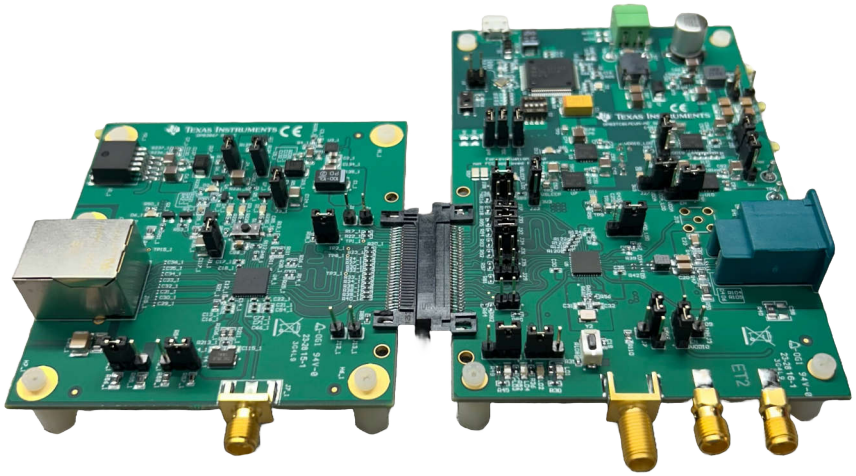

**Figure 5-7. DP83TC818EVM-MC**

**Features:**

- TC10 Support
- Jumpers to customize PHY strap settings
- Option to supply external reference clock
- Additional test points for debug
- Status LEDs
  - Link
  - Link + Activity
  - Power-On
- EVM User's Guide for reference

**New DIEP Debug Interface Experience**

DIEP offers all your Ethernet PHY debug needs in one place including MDIO bus serial management, device control registers, access to both extended registers and standard registers, and the ability to save data read and run script text files.

- ***NEW*** restructured navigation and register display
- ***NEW*** improved text script execution

Debug Interface for Ethernet PHY's (DIEP)

# 6 Device and Documentation Support

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

## 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 6.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 6.3 Community Resources

## 6.4 Trademarks

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## 6.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 6.6 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

ADVANCE INFORMATION

# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 7.1 Package Option Addendum

### 7.1.1 Packaging Information

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish[4] | MSL Peak Temp [3] | Op Temp (°C) | Device Marking[5] [6] |
|---|---|---|---|---|---|---|---|---|---|---|
| DP83TC818SRHATQ1 | EARLY SAMPLE | VQFN | RHA | 36 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | 40 to 125 | TBD |
| DP83TC818SRHARQ1 | EARLY SAMPLE | VQFN | RHA | 36 | 2500 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | 40 to 125 | TBD |

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PDP83TC818SRHATQ1 | ACTIVE | VQFN | RHA | 36 | 250 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# GENERIC PACKAGE VIEW

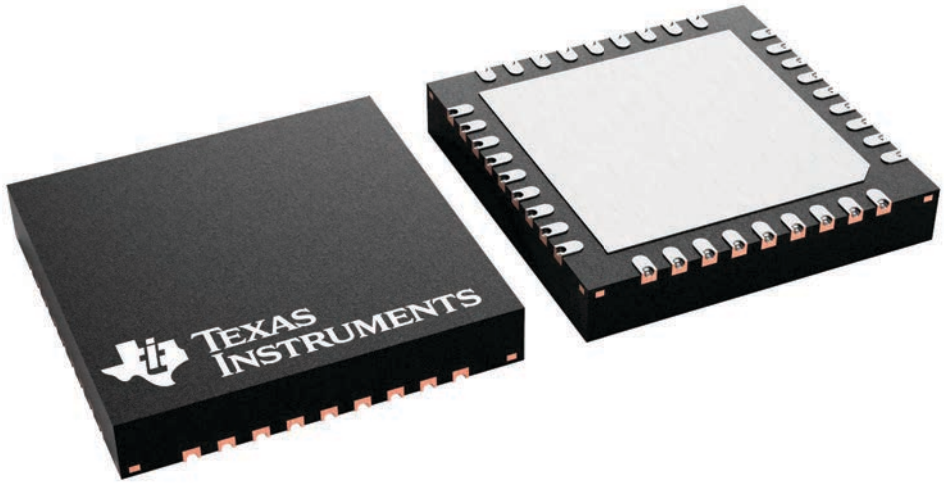
## RHA 36

## VQFN - 1 mm max height

**6 x 6, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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