DS26C31MQML CMOS Quad TRI-STATE Differential Line Driver

Check for Samples: DS26C31MQML

FEATURES

- **TTL Input Compatible**
- **Outputs Will Not Load Line When V_{CC} = 0V**
- **Meets the Requirements of EIA Standard RS-422**
- **Operation from Single 5V Supply**
- **TRI-STATE Outputs for Connection to System Buses**
- **Low Quiescent Current**

DESCRIPTION

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31 meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31 is compatible with EIA standard RS-422; however, one exception in test methodology is taken. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Connection Diagram

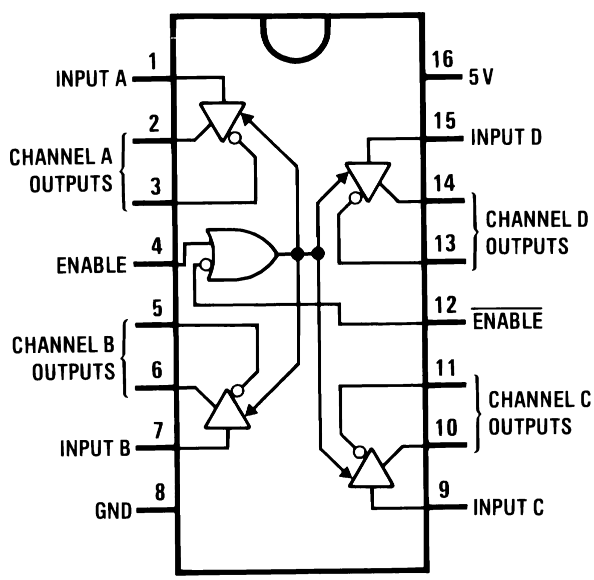


Figure 1. CDIP, CLGA Packages- Top View
See Package Numbers NFE0016A, NAD0016A

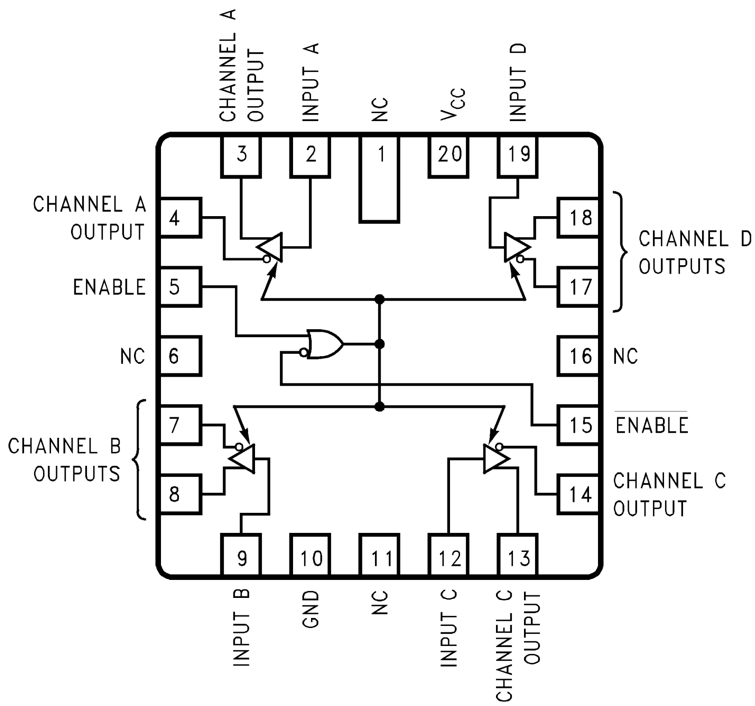
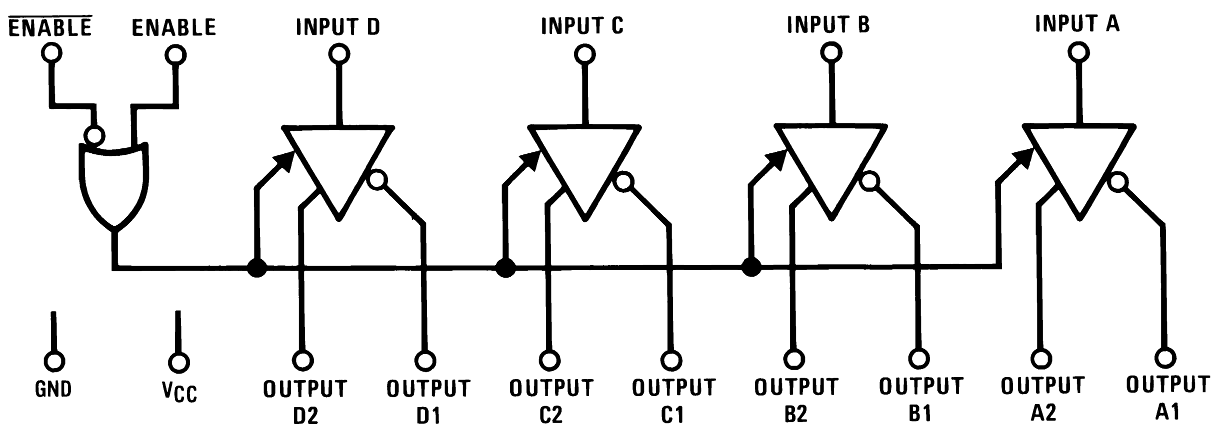


Figure 2. 20-Lead LCCC Package- Top View
See Package Number NAJ0020A

Logic Diagram



Truth Table (1)

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting	Inverting
			Output	Output
L	H	X	Z	Z
All other		L	L	H
combinations of		H	H	L
enable inputs				

(1) L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE (high impedance)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})	−0.5V to 7.0V
DC Input Voltage (V_I)	−1.5V to V_{CC} +0.5V
DC Output Voltage (V_O)	−0.5V to 7V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_O)	±150 mA
DC V_{CC} or Gnd Current, per pin (I_{CC})	±150 mA
Storage Temperature Range (T_{Stg})	−65°C ≤ T_A ≤ +150°C
Lead Temperature (T_L) Soldering, 4 sec.	260°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not verify specific performance limits. For verified specifications and test conditions, see the Electrical Characteristics. The verified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.50	5.50	V
DC Input or Output Voltage (V_I, V_O)	0	V_{CC}	V
Operating Temperature Range (T_A)	−55	+125	°C

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

DS26C31M Electrical Characteristics DC Parameters

Parameter		Test Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IH}	Logical "1" Input Voltage			2.0		V	1, 2, 3
V_{IL}	Logical "0" Input Voltage				0.8	V	1, 2, 3
V_{OH}	Logical "1" Output Voltage	$V_I = V_{IH}$ or V_{IL}, $V_{CC} = 4.5V$, $I_O = -20mA$		2.5		V	1, 2, 3
V_{OL}	Logical "0" Output Voltage	$V_I = V_{IH}$ or V_{IL}, $I_O = 20mA$, $V_{CC} = 4.5V$			0.5	V	1, 2, 3
V_T	Differential Output Voltage	$R_L = 100\Omega$, $V_{CC} = 4.5V$	(1)	2.0		V	1, 2, 3
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Difference in Differential Output	$R_L = 100\Omega$, $V_{CC} = 4.5V$	(1)		0.4	V	1, 2, 3
V_{OS}	Common Mode Output Voltage	$R_L = 100\Omega$, $V_{CC} = 5.5V$	(1)		3.0	V	1, 2, 3
$\lvert V_{OS} - \overline{V_{OS}}\rvert$	Diff in Common Mode Output	$R_L = 100\Omega$, $V_{CC} = 5.5V$	(1)		0.4	V	1, 2, 3
I_I	Input Current	$V_I = V_{CC}$, Gnd, V_{IH}, or V_{IL}, $V_{CC} = 5.5V$			±1.0	µA	1, 2, 3
I_{CC}	Quiescent Power Supply Current	$I_O = 0\mu A$, $V_I = V_{CC}$ or Gnd, $V_{CC} = 5.5V$	(2)		500	µA	1, 2, 3
		$I_O = 0\mu A$, $V_I = 2.4V$ or $0.5V$, $V_{CC} = 5.5V$	(2)		2.1	mA	1, 2, 3
I_{OZ}	TRI-STATE Output Leakage Current	$V_O = V_{CC}$ or Gnd, Enable = V_{IL}, $V_{CC} = 5.5V$, $\overline{Enable} = V_{IH}$			±5.0	µA	1, 2, 3
I_{SC}	Output Short Circuit Current	$V_I = V_{CC}$ or Gnd, $V_{CC} = 5.5V$	(1), (3)	-30	-150	mA	1, 2, 3
I_{Off}	Output Leakage Current "Power Off"	$V_{CC} = 0V$, $V_O = 6V$			100	µA	1, 2, 3
		$V_{CC} = 0V$, $V_O = 0V$			-100	µA	1, 2, 3

(1) See EIA Specification RS-422 for exact test conditions.
(2) Measured per input. All other inputs at V_{CC} or GND.
(3) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

DS26C31M Electrical Characteristics AC Parameters - Propagation Delay Time (see Figure 26)

The following conditions apply, unless otherwise specified. $V_{CC} = 5V$, $t_R \leq 6ns$, $t_F \leq 6ns$

Parameter		Test Conditions	Notes	Min	Max	Unit	Sub-groups
t_{PLH}	Input to Output Prop Delay	Figure 27			14	ns	9, 10, 11
t_{PHL}	Input to Output Prop Dalay	Figure 27			14	ns	9, 10, 11
	Skew		(1)		3.0	ns	9, 10, 11
t_{TLH}	Output Rise Time	Figure 29			14	ns	9, 10, 11
t_{THL}	Output Fall Time	Figure 29			14	ns	9, 10, 11
t_{PZH}	Output Enable Time	Figure 28			22	ns	9, 10, 11
t_{PZL}	Output Enable Time	Figure 28			28	ns	9, 10, 11
t_{PHZ}	Output Disable Time	Figure 28	(2)		12	ns	9, 10, 11
t_{PLZ}	Output Disable Time	Figure 28	(2)		14	ns	9, 10, 11

(1) Skew is defined as the difference in propagation delays between complimentary outputs at the 50% point.
(2) Output disable time is the delay from ENABLE or $\overline{ENABLE}$ being switched to the output transistors turning off.

Typical Performance Characteristics

Differential Propagation Delay vs Temperature

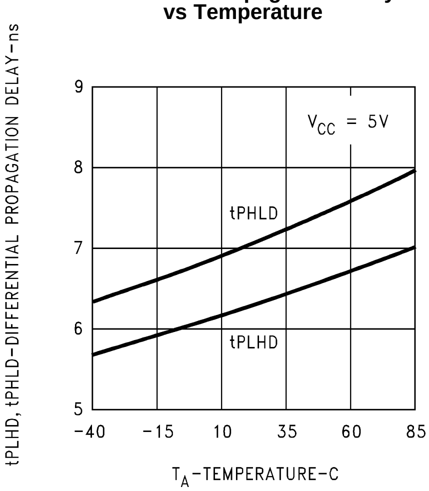


Figure 3.

Differential Propagation Delay vs Power Supply Voltage

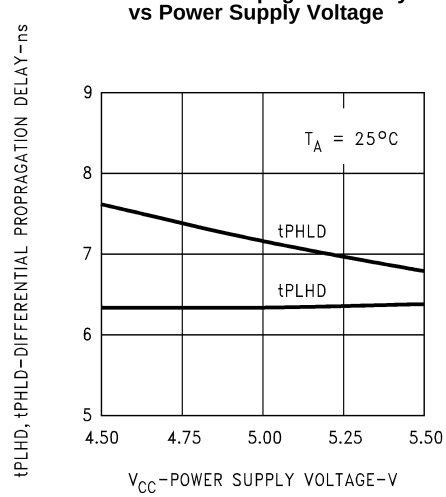


Figure 4.

Differential Skew vs Temperature

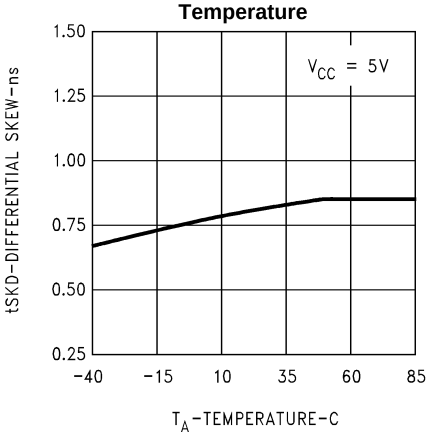


Figure 5.

Differential Skew vs Power Supply Voltage

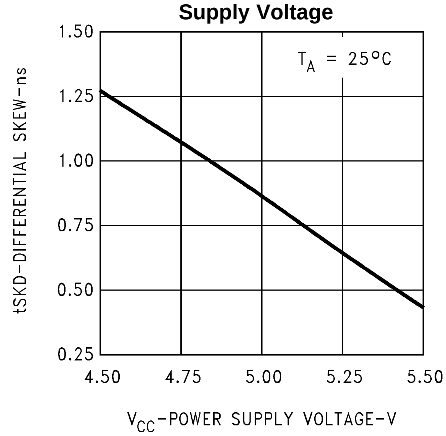


Figure 6.

Differential Transition Time vs Temperature

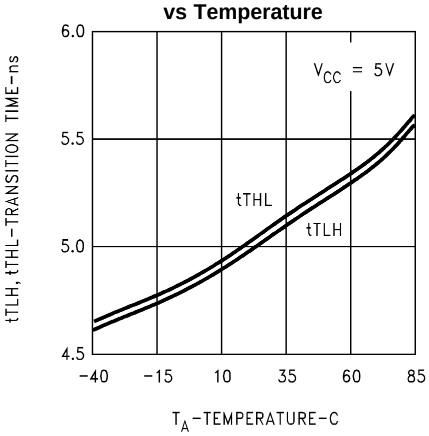


Figure 7.

Differential Transition Time vs Power Supply Voltage

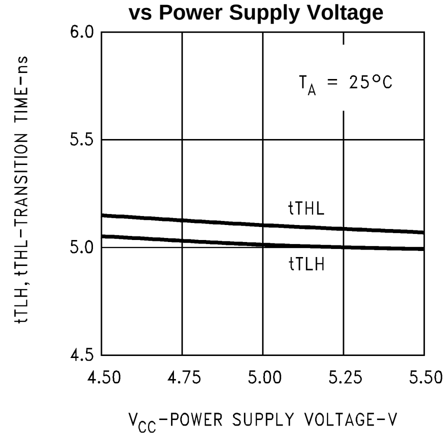


Figure 8.

Typical Performance Characteristics (continued)

Complementary Skew vs Temperature

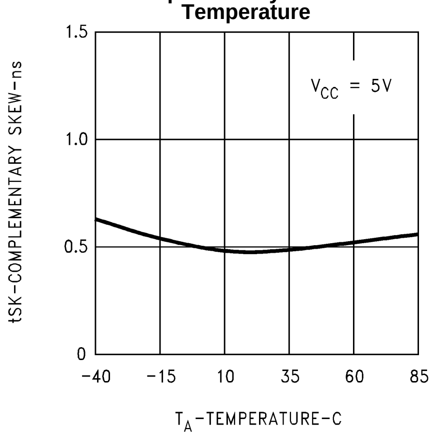


Figure 9.

Complementary Skew vs Power Supply Voltage

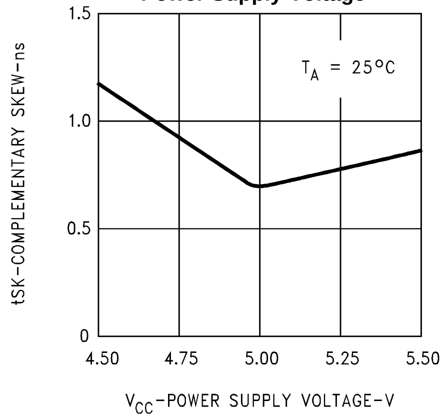


Figure 10.

Differential Output Voltage vs Output Current

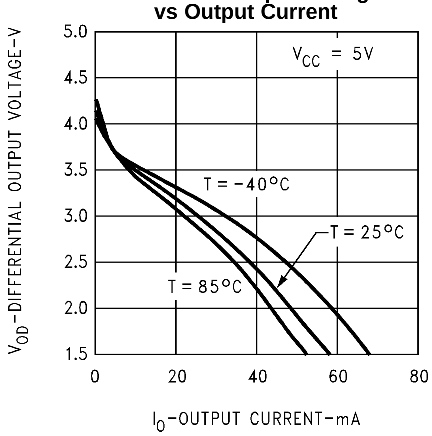


Figure 11.

Differential Output Voltage vs Output Current

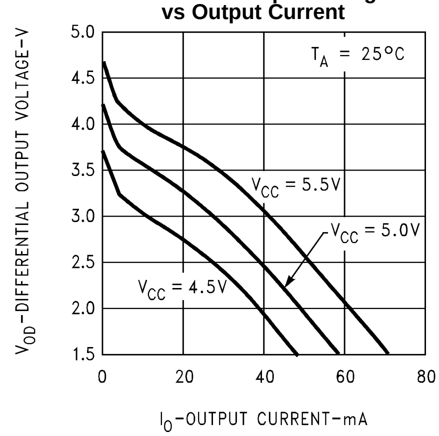


Figure 12.

Output High Voltage vs Output High Current

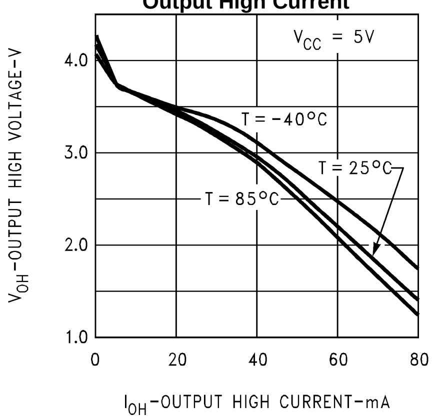


Figure 13.

Output High Voltage vs Output High Current

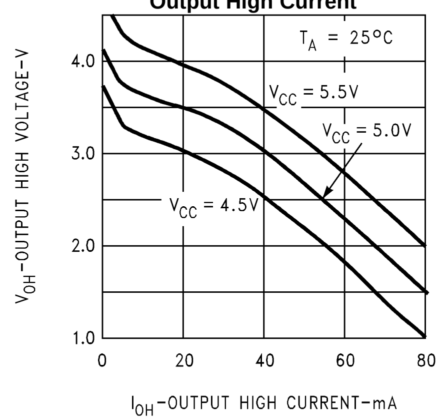


Figure 14.

Typical Performance Characteristics (continued)

Output Low Voltage vs Output Low Current

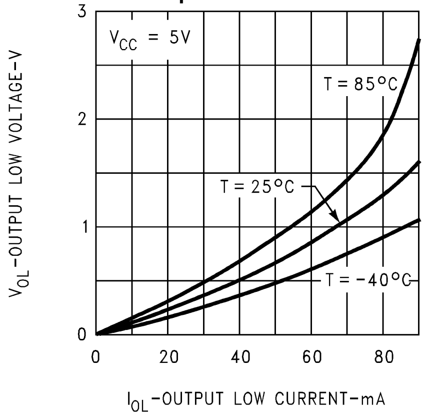


Figure 15.

Output Low Voltage vs Output Low Current

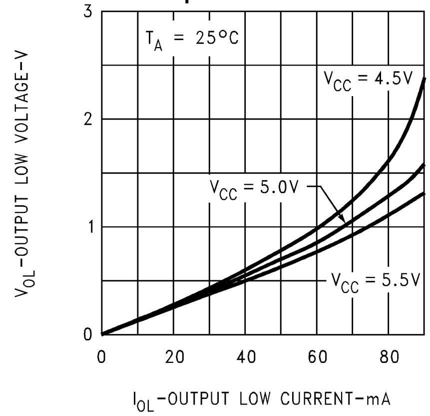


Figure 16.

Supply Current vs Temperature

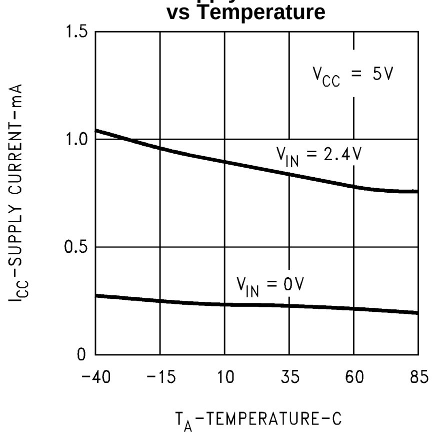


Figure 17.

Output Low Voltage vs Output Low Current

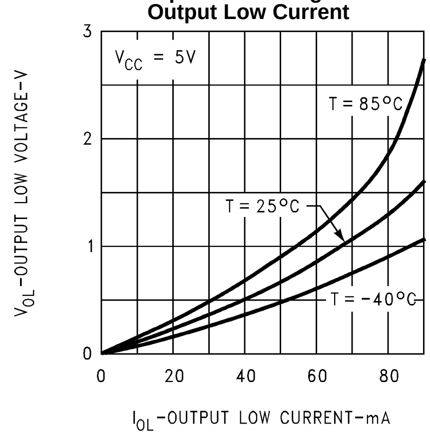


Figure 18.

Output Low Voltage vs Output Low Current

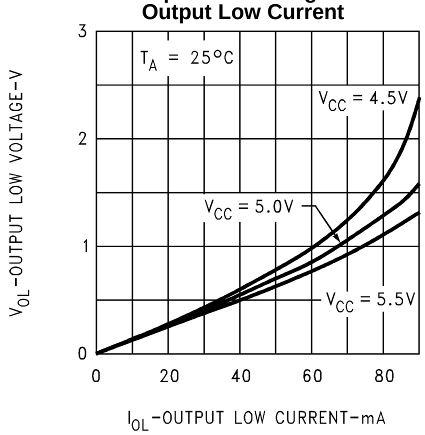


Figure 19.

Supply Current vs Temperature

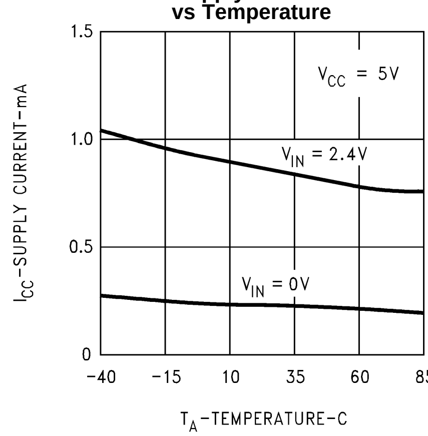


Figure 20.

Typical Performance Characteristics (continued)

Supply Current vs Power Supply Voltage

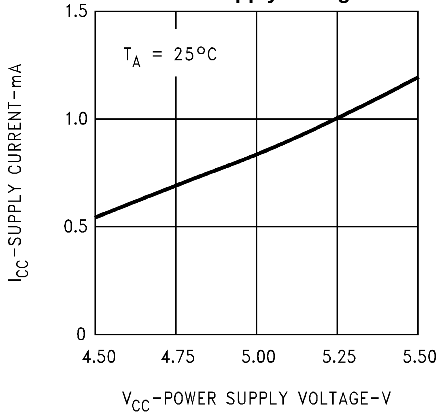


Figure 21.

No Load Supply Current vs Data Rate

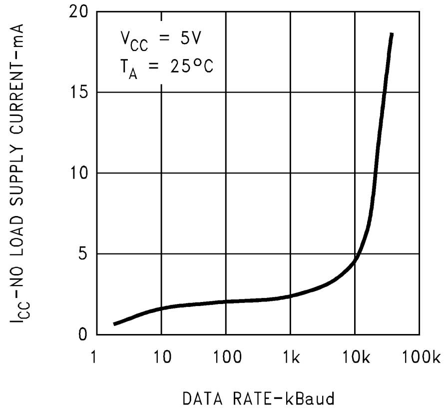


Figure 22.

Loaded Supply Current vs Data Rate

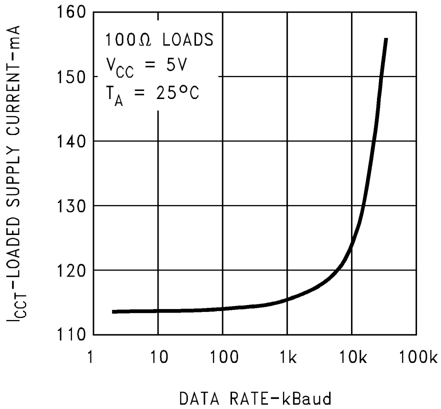


Figure 23.

Output Short Circuit Current vs Temperature

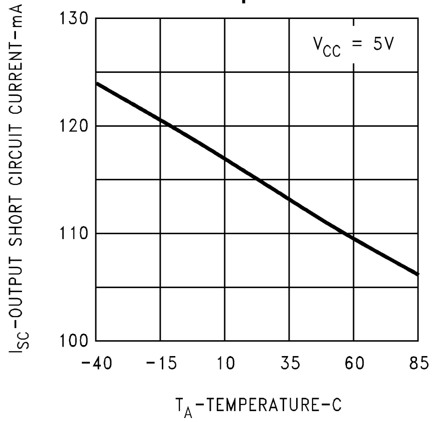


Figure 24.

Output Short Circuit Current vs Power Supply Voltage

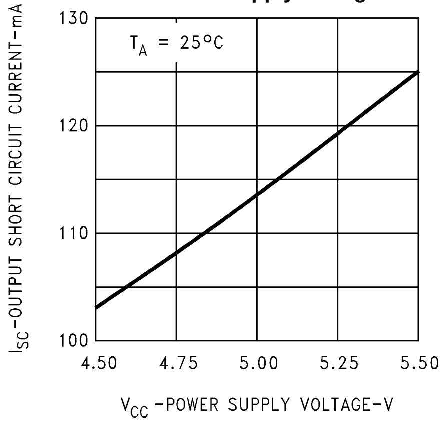
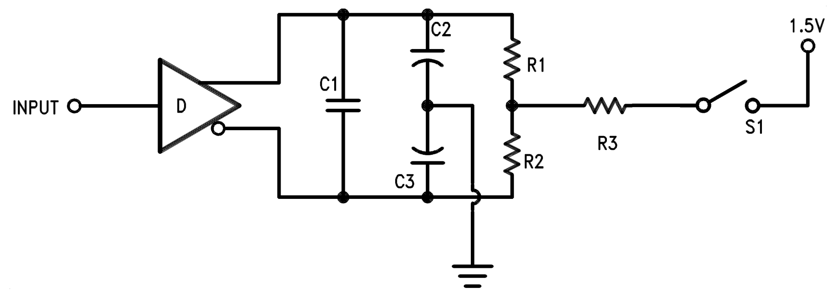


Figure 25.

AC TEST CIRCUIT AND SWITCHING TIME WAVEFORMS



Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

Figure 26. AC Test Circuit

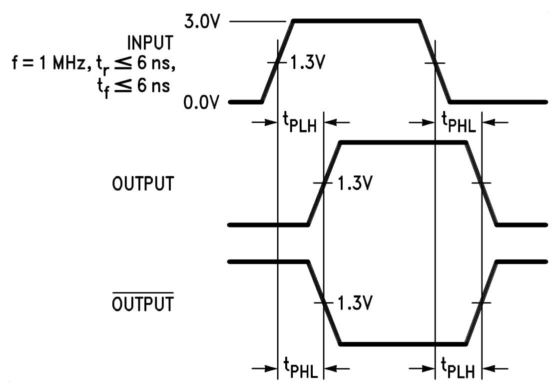


Figure 27. Propagation Delays

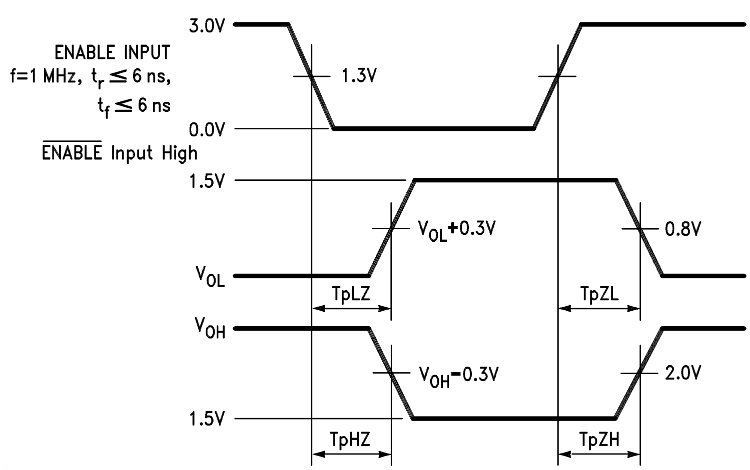
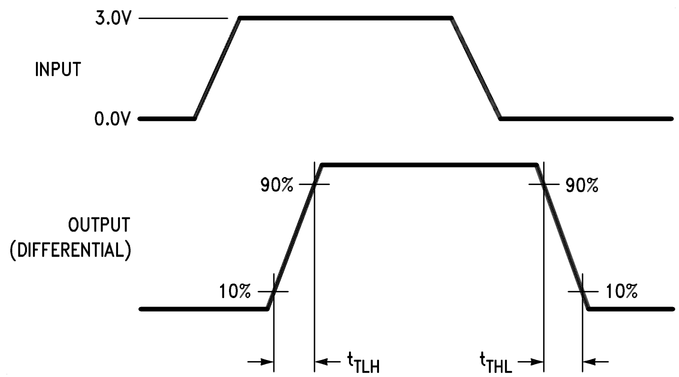


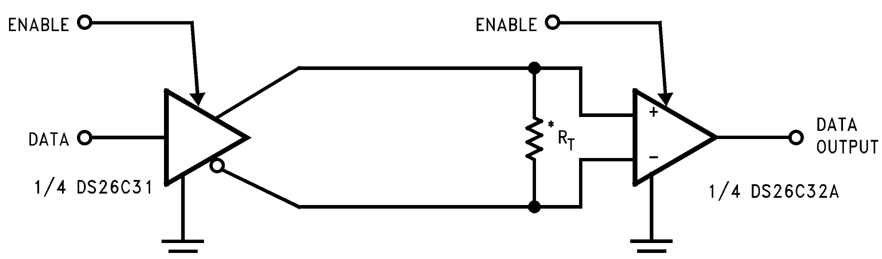
Figure 28. Enable and Disable Times



Input pulse; f = 1 MHz, 50%; $t_r \leq 6$ ns, $t_f \leq 6$ ns

Figure 29. Differential Rise and Fall Times

TYPICAL APPLICATIONS



*R_T is optional although highly recommended to reduce reflection.

Figure 30. Two-Wire Balanced System, RS-422

REVISION HISTORY

Table 2. Revision History

Released	Revision	Section	Changes
10/26/2010	A	New Release, Corporate format	1 MDS data sheets converted into one Corp. data sheet format. MNDS26C31M-X Rev 0B0 will be archived.

Changes from Original (April 2013) to Revision A **Page**

- Changed layout of National Data Sheet to TI format 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26C31ME/883	ACTIVE	LCCC	NAJ	20	50	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C31ME/ 883 Q 5962-91639 01M2A ACO 01M2A >T	Samples
DS26C31MJ/883	ACTIVE	CDIP	NFE	16	25	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C31MJ/883 5962-9163901MEA Q	Samples
DS26C31MW/883	ACTIVE	CFP	NAD	16	19	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	DS26C31MW /883 Q 5962-91639 01MFA ACO 01MFA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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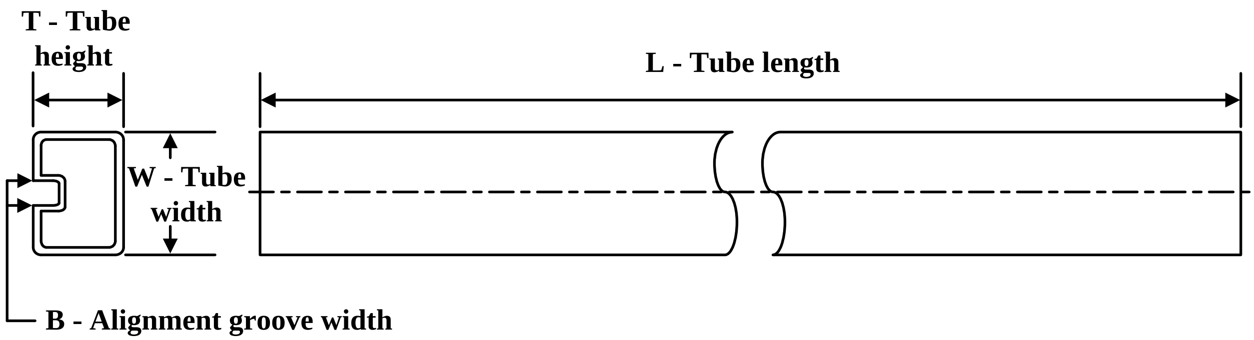
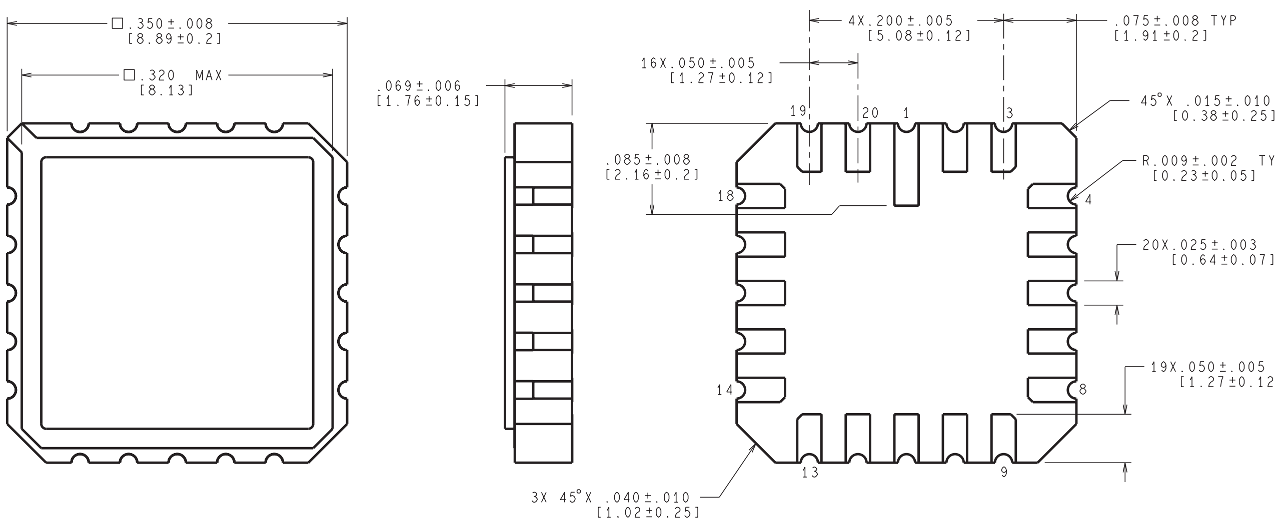
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS26C31ME/883	NAJ	LCCC	20	50	470	11	3810	0
DS26C31MJ/883	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26C31MJ/883	NFE	CDIP	16	25	506.98	15.24	13440	NA
DS26C31MW/883	NAD	CFP	16	19	502	23	9398	9.78

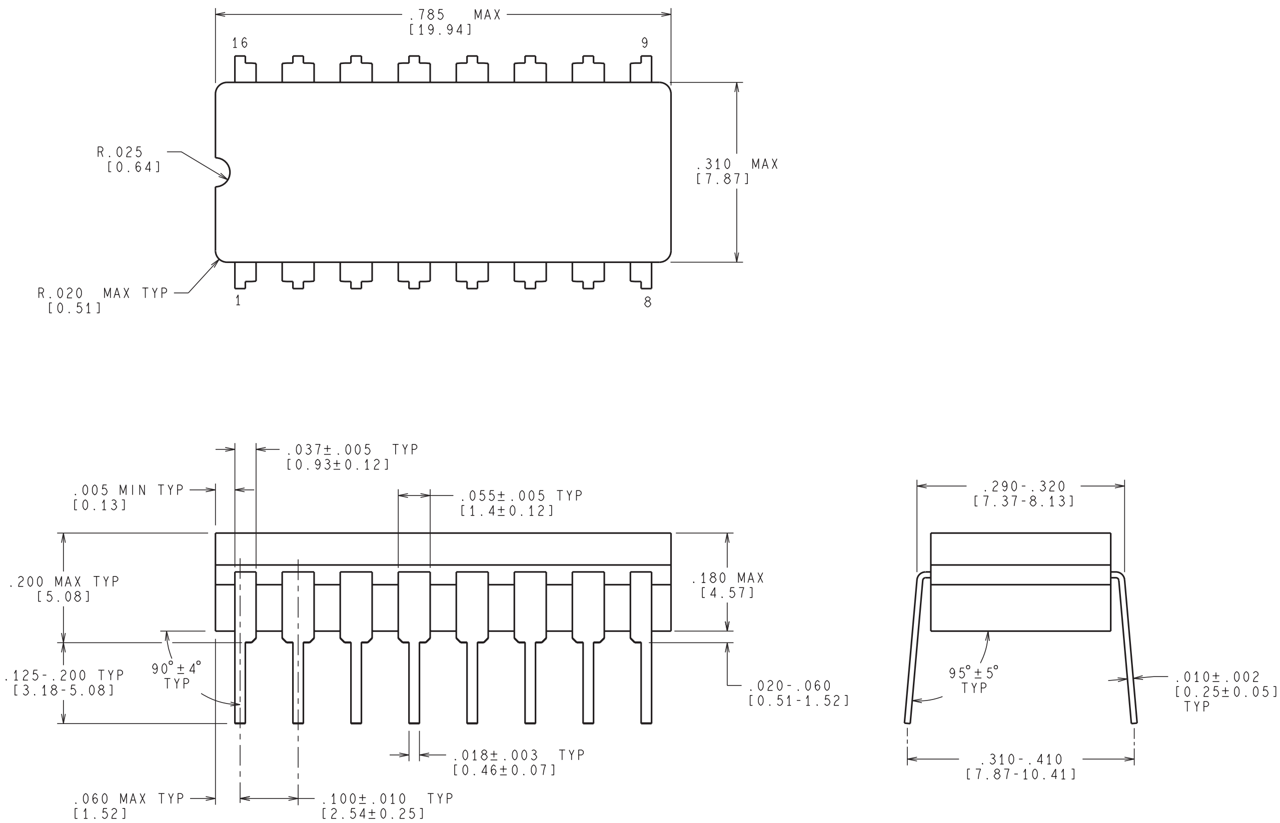
NAJ0020A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

E20A (Rev F)

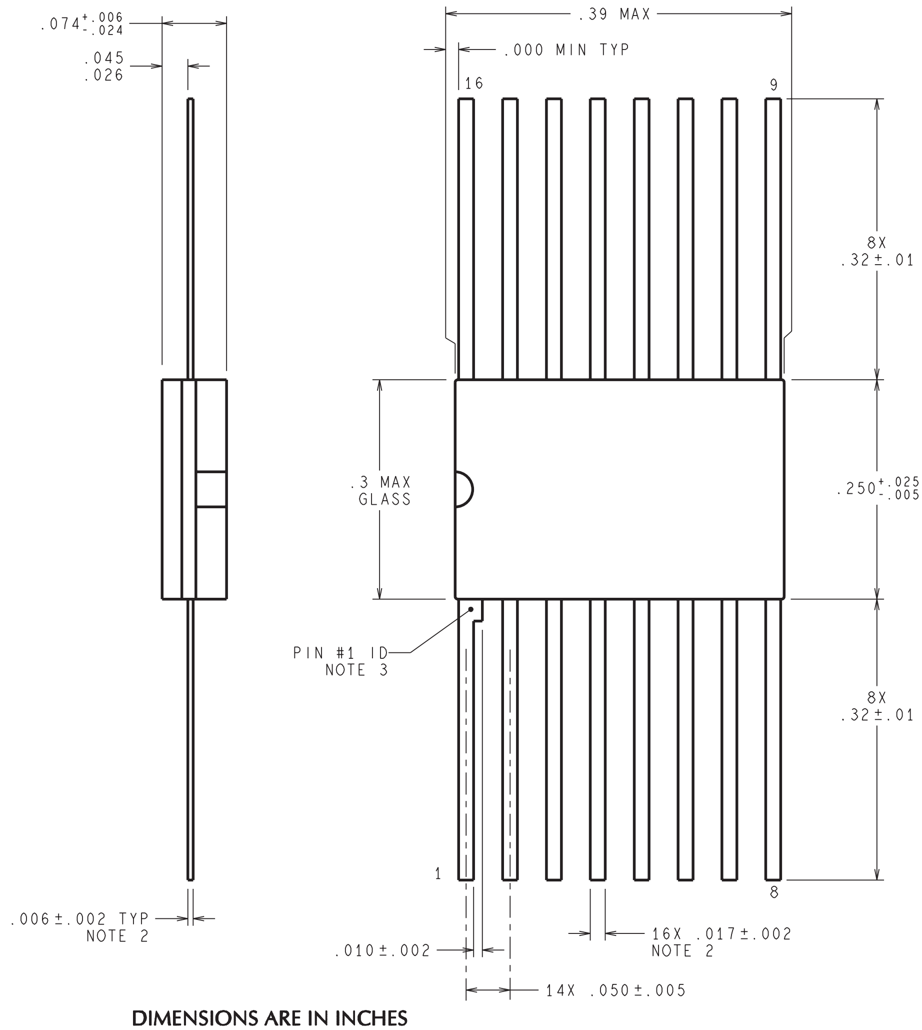
NFE0016A



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

J16A (REV L)

NAD0016A



W16A (Rev T)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265