DS90CR215/DS90CR216 +3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link - 66 MHz

Check for Samples: DS90CR215, DS90CR216

FEATURES

- Single +3.3V Supply
- Chipset (Tx + Rx) Power Consumption <250 mW (typ)
- Power-down Mode (<0.5 mW total)
- Up to 173 Megabytes/sec Bandwidth
- Up to 1.386 Gbps Data Throughput
- Narrow Bus Reduces Cable Size
- 290 mV Swing LVDS Devices for Low EMI
- +1V Common Mode Range (Around +1.2V)
- PLL Requires No External Components
- Low Profile 48-Lead TSSOP Package
- Rising Edge Data Strobe
- Compatible with TIA/EIA-644 LVDS Standard
- ESD Rating > 7 kV
- Operating Temperature: −40°C to +85°C

DESCRIPTION

The DS90CR215 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR216 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 66 MHz, 21 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.386 Gbit/s (173 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 21-bit wide data and one clock, up to 44 conductors are required. With the Channel Link chipset as few as 9 conductors (3 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 21 CMOS/TTL inputs can support a variety of signal combinations. For example, five 4-bit nibbles plus 1 control, or two 9-bit (byte + parity) and 3 control.

Block Diagram

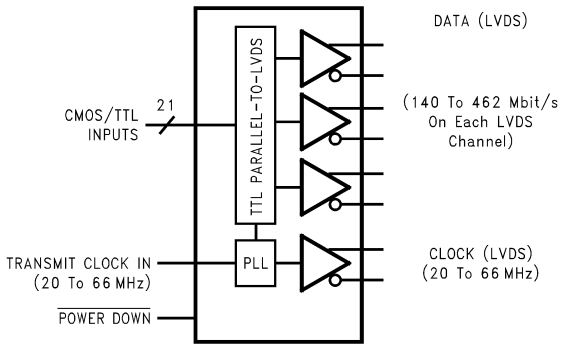


Figure 1. DS90CR215
48-Lead TSSOP
See Package Number DGG0048A

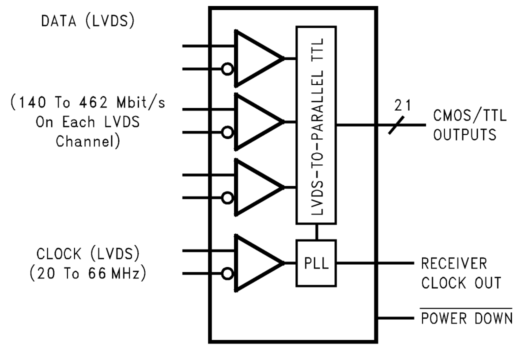


Figure 2. DS90CR216 - Improved AC Specifications
See Package Number DGG0048A
Recommended Alternative Device

Connection Diagrams

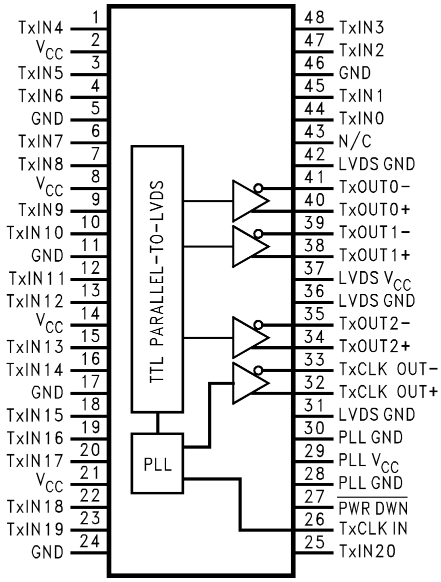


Figure 3. DS90CR215

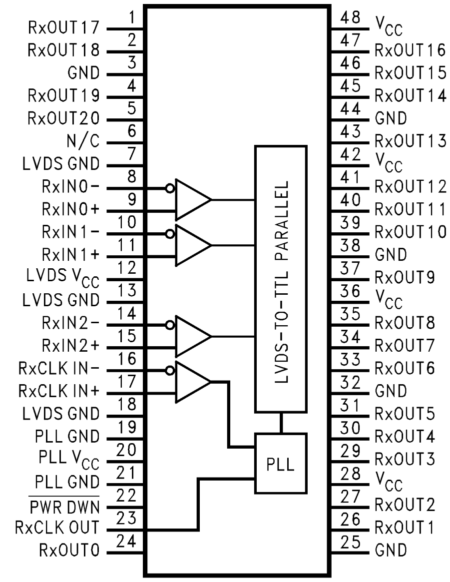
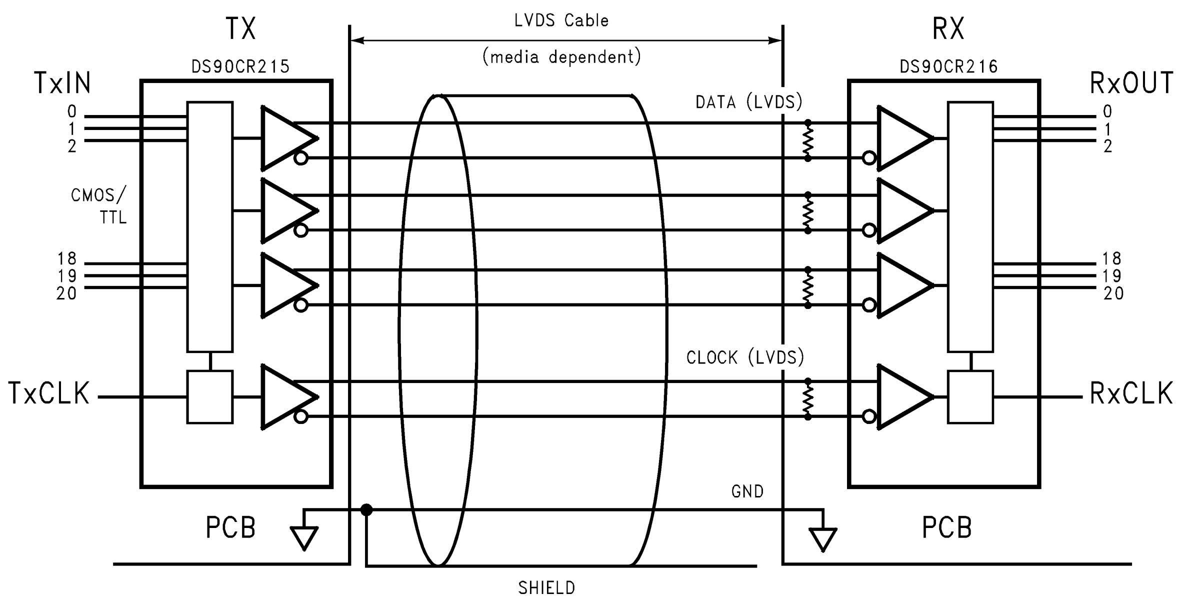


Figure 4. DS90CR216

Typical Application



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})			−0.3V to +4V
CMOS/TTL Input Voltage			−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Driver Output Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Output Short Circuit Duration			Continuous
Junction Temperature			+150°C
Storage Temperature Range			−65°C to +150°C
Lead Temperature (Soldering, 4 sec.)			+260°C
Maximum Package Power Dissipation @ +25°C	DGG0048A (TSSOP) Package:	DS90CR215	1.98 W
		DS90CR216	1.89 W
	Package Derating	DS90CR215	16 mW/°C above +25°C
		DS90CR216	15 mW/°C above +25°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)			> 7 kV

(1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(2) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. “Electrical Characteristics” specify conditions for device operation.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})				100 mV_{PP}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.06	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = V_{CC}, GND, 2.5V or 0.4V		±5.1	±10	μA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		-60	−120	mA
LVDS DRIVER DC SPECIFICATIONS						
V_{OD}	Differential Output Voltage	R_L = 100Ω	250	290	450	mV
ΔV_{OD}	Change in V_{OD} between Complimentary Output States				35	mV
V_{OS}	Offset Voltage[1]		1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between Complimentary Output States				35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V, R_L = 100Ω		−3.5	−5	mA
I_{OZ}	Output TRI-STATE Current	$\overline{PWR\ DWN}$ = 0V, V_{OUT} = 0V or V_{CC}		±1	±10	μA
LVDS RECEIVER DC SPECIFICATIONS						

(1) V_{OS} previously referred as V_{CM}.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	μA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	μA
TRANSMITTER SUPPLY CURRENT							
I_{CCTW}	Transmitter Supply Current Worst Case (with Loads)	R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (Figure 5 Figure 6), T_A = −10°C to +70°C	f = 32.5 MHz		31	45	mA
			f = 37.5 MHz		32	50	mA
			f = 66 MHz		37	55	mA
		R_L = 100Ω, C_L = 5 pF, Worst Case Pattern (Figure 5 Figure 6), T_A = −40°C to +85°C	f = 40 MHz		38	51	mA
			f = 66 MHz		42	55	mA
I_{CCTZ}	Transmitter Supply Current Power Down	$\overline{PWR\ DWN}$ = Low Driver Outputs in TRI-STATE under Powerdown Mode			10	55	μA
RECEIVER SUPPLY CURRENT							
I_{CCRW}	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern (Figure 5 Figure 7), T_A = −10°C to +70°C	f = 32.5 MHz		49	65	mA
			f = 37.5 MHz		53	70	mA
			f = 66 MHz		78	105	mA
		C_L = 8 pF, Worst Case Pattern (Figure 5 Figure 7), T_A = −40°C to +85°C	f = 40 MHz		55	82	mA
			f = 66 MHz		78	105	mA
I_{CCRZ}	Receiver Supply Current Power Down	$\overline{PWR\ DWN}$ = Low Receiver Outputs Stay Low during Powerdown Mode			10	55	μA

Transmitter Switching Characteristics

Over recommended operating supply and −40°C to +85°C ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
LLHT	LVDS Low-to-High Transition Time (Figure 6)			0.5	1.5	ns
LHLT	LVDS High-to-Low Transition Time (Figure 6)			0.5	1.5	ns
TCIT	TxCLK IN Transition Time (Figure 8)				5	ns
TCCS	TxOUT Channel-to-Channel Skew (Figure 9)			250		ps
TPPos0	Transmitter Output Pulse Position for Bit0 (1) (Figure 20)	f = 40 MHz	−0.4	0	0.4	ns
TPPos1	Transmitter Output Pulse Position for Bit1		3.1	3.3	4.0	ns
TPPos2	Transmitter Output Pulse Position for Bit2		6.5	6.8	7.6	ns
TPPos3	Transmitter Output Pulse Position for Bit3		10.2	10.4	11.0	ns
TPPos4	Transmitter Output Pulse Position for Bit4		13.7	13.9	14.6	ns
TPPos5	Transmitter Output Pulse Position for Bit5		17.3	17.6	18.2	ns
TPPos6	Transmitter Output Pulse Position for Bit6		21.0	21.2	21.8	ns

(1) The min. and max. are based on the actual bit position of each of the 7 bits within the LVDS data stream across PVT.

Transmitter Switching Characteristics (continued)

Over recommended operating supply and −40°C to +85°C ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
TPPos0	Transmitter Output Pulse Position for Bit0 [(2)] (Figure 20)	f = 66 MHz	−0.4	0	0.3	ns
TPPos1	Transmitter Output Pulse Position for Bit1		1.8	2.2	2.5	ns
TPPos2	Transmitter Output Pulse Position for Bit2		4.0	4.4	4.7	ns
TPPos3	Transmitter Output Pulse Position for Bit3		6.2	6.6	6.9	ns
TPPos4	Transmitter Output Pulse Position for Bit4		8.4	8.8	9.1	ns
TPPos5	Transmitter Output Pulse Position for Bit5		10.6	11.0	11.3	ns
TPPos6	Transmitter Output Pulse Position for Bit6		12.8	13.2	13.5	ns
TCIP	TxCLK IN Period (Figure 10)		15	T	50	ns
TCIH	TxCLK IN High Time (Figure 10)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK IN Low Time (Figure 10)		0.35T	0.5T	0.65T	ns
TSTC	TxIN Setup to TxCLK IN (Figure 10)		2.5			ns
THTC	TxIN Hold to TxCLK IN (Figure 10)		0			ns
TCCD	TxCLK IN to TxCLK OUT Delay @ 25°C,V_{CC}=3.3V (Figure 12)		3	3.7	5.5	ns
TPLLS	Transmitter Phase Lock Loop Set (Figure 14)				10	ms
TPDD	Transmitter Powerdown Delay (Figure 18)				100	ns

(2) The min. and max. limits are based on the worst bit by applying a −400ps/+300ps shift from ideal position.

Receiver Switching Characteristics

Over recommended operating supply and −40°C to +85°C ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 7)			2.2	5.0	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 7)			2.2	5.0	ns
RSPos0	Receiver Input Strobe Position for Bit 0 [(1)](Figure 21)	f = 40 MHz	1.0	1.4	2.15	ns
RSPos1	Receiver Input Strobe Position for Bit 1		4.5	5.0	5.8	ns
RSPos2	Receiver Input Strobe Position for Bit 2		8.1	8.5	9.15	ns
RSPos3	Receiver Input Strobe Position for Bit 3		11.6	11.9	12.6	ns
RSPos4	Receiver Input Strobe Position for Bit 4		15.1	15.6	16.3	ns
RSPos5	Receiver Input Strobe Position for Bit 5		18.8	19.2	19.9	ns
RSPos6	Receiver Input Strobe Position for Bit 6		22.5	22.9	23.6	ns
RSPos0	Receiver Input Strobe Position for Bit 0 [(2)](Figure 21)	f = 66 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin [(3)](Figure 22)	f = 40 MHz	490			ps
		f = 66 MHz	400			ps
RCOP	RxCLK OUT Period (Figure 11)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 11)	f = 40 MHz	6.0	10.0		ns
		f = 66 MHz	4.0	6.1		ns

(1) The min. and max. are based on the actual bit position of each of the 7 bits within the LVDS data stream across PVT.
(2) The min. and max. limits are based on the worst bit by applying a −400ps/+300ps shift from ideal position.
(3) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account for transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window). This margin allows LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter less than 250 ps.

Receiver Switching Characteristics (continued)

Over recommended operating supply and −40°C to +85°C ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
RCOL	RxCLK OUT Low Time (Figure 11)	f = 40 MHz	10.0	13.0		ns
		f = 66 MHz	6.0	7.8		ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 11)	f = 40 MHz	6.5	14.0		ns
		f = 66 MHz	2.5	8.0		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 11)	f = 40 MHz	6.0	8.0		ns
		f = 66 MHz	2.5	4.0		ns
RCCD	RxCLK IN to RxCLK OUT Delay (Figure 13)	f = 40 MHz	4.0	6.7	8.0	ns
		f = 66 MHz	5.0	6.6	9.0	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 15)				10	ms
RPDD	Receiver Powerdown Delay (Figure 19)				1	µs

AC Timing Diagrams

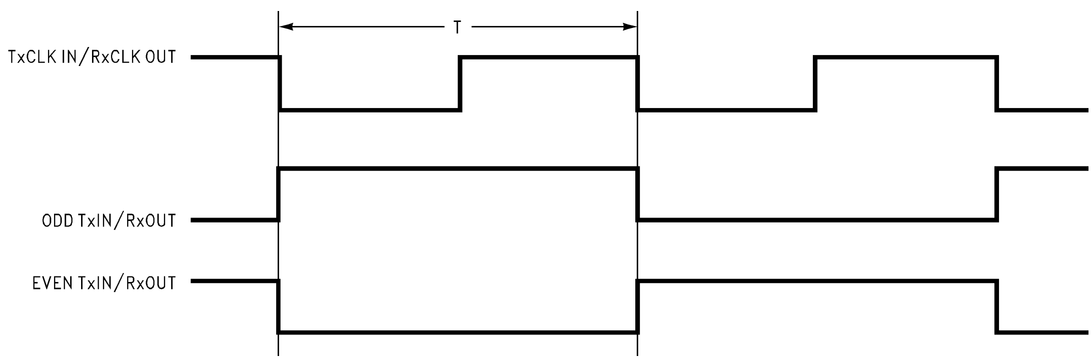


Figure 5. "Worst Case" Test Pattern

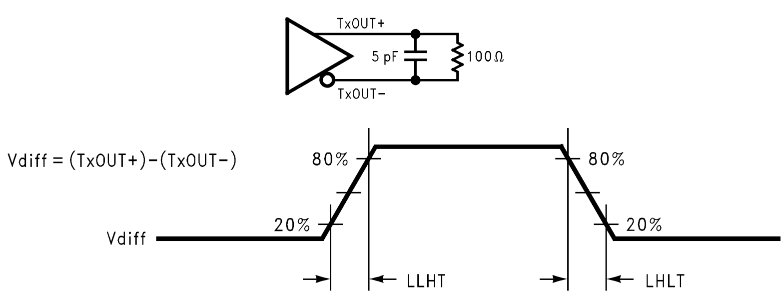
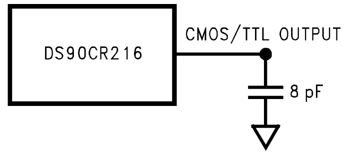


Figure 6. DS90CR215 (Transmitter) LVDS Output Load and Transition Times



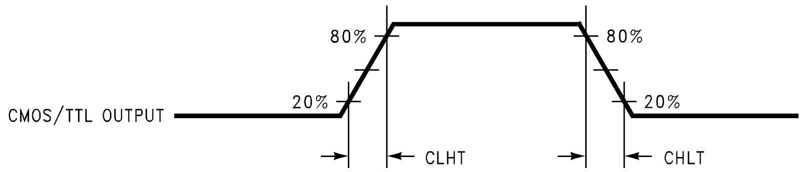


Figure 7. DS90CR216 (Receiver) CMOS/TTL Output Load and Transition Times

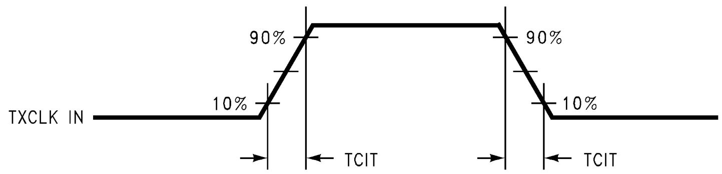
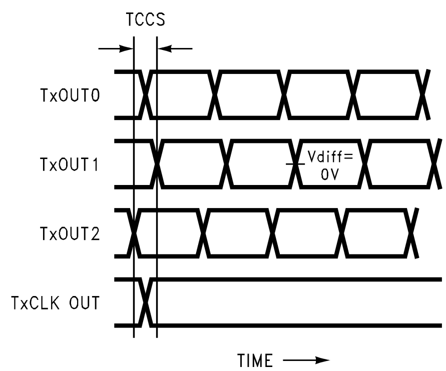


Figure 8. D590CR215 (Transmitter) Input Clock Transition Time



A. Measurements at V_{DIFF} = 0V

B. TCCS measured between earliest and latest LVDS edges

C. TxCLK Differential Low→High Edge

Figure 9. D590CR215 (Transmitter) Channel-to-Channel Skew

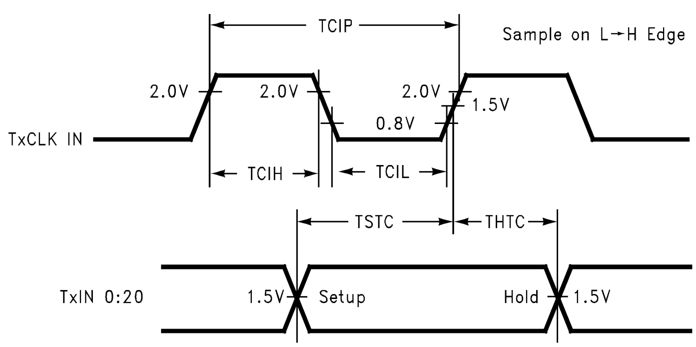


Figure 10. D590CR215 (Transmitter) Setup/Hold and High/Low Times

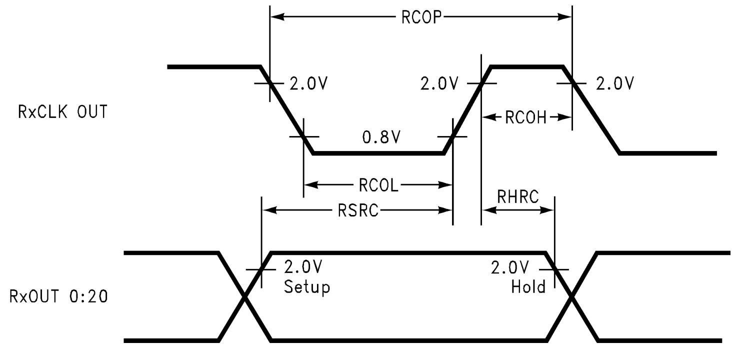


Figure 11. D590CR216 (Receiver) Setup/Hold and High/Low Times

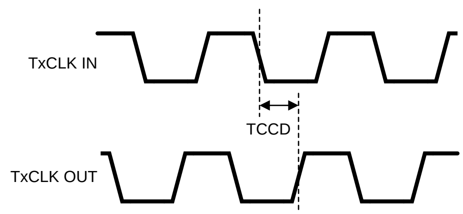


Figure 12. DS90CR215 (Transmitter) Clock In to Clock Out Delay

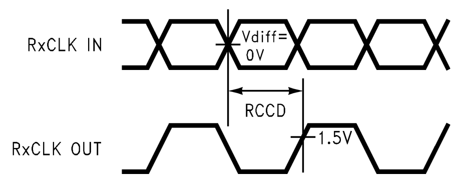


Figure 13. D590CR216 (Receiver) Clock In to Clock Out Delay

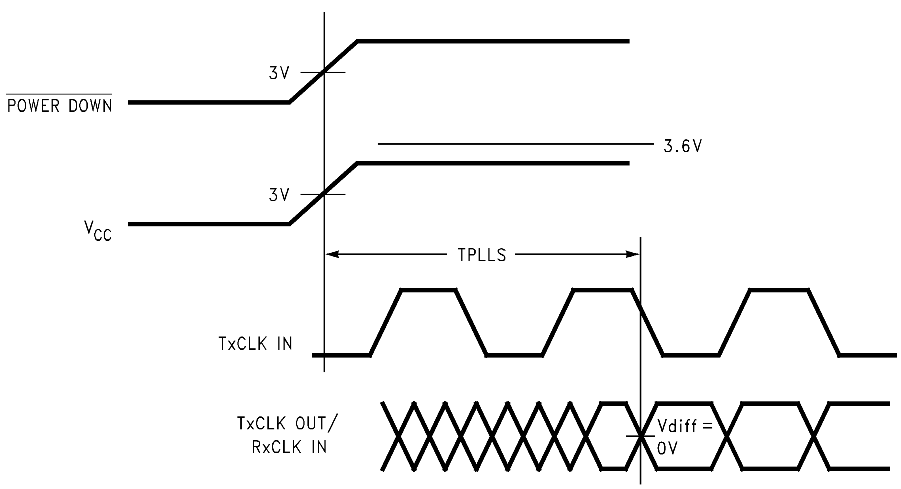


Figure 14. DS90CR215 (Transmitter) Phase Lock Loop Set Time

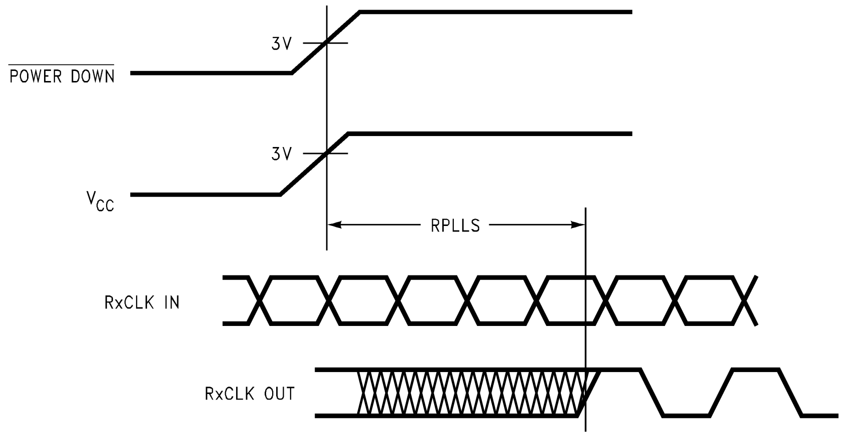


Figure 15. DS9OCR216 (Receiver) Phase Lock Loop Set Time

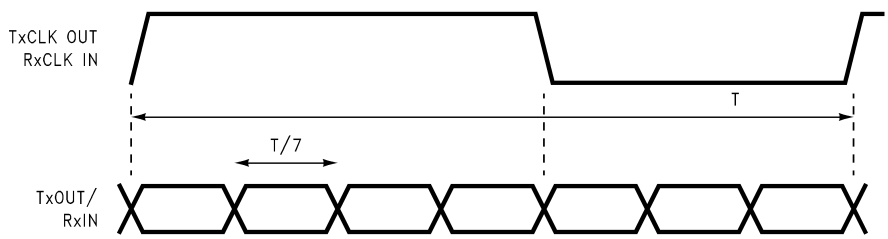


Figure 16. Seven Bits of LVDS in Once Clock Cycle

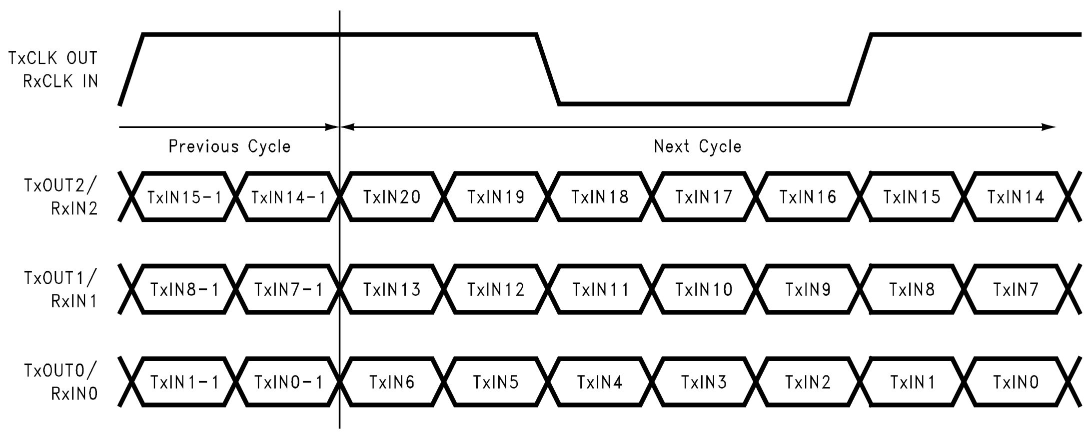


Figure 17. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR215)

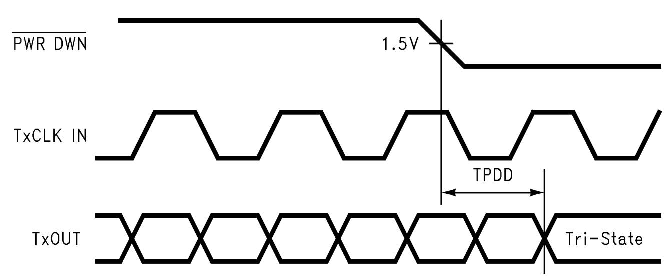


Figure 18. Transmitter Powerdown Delay

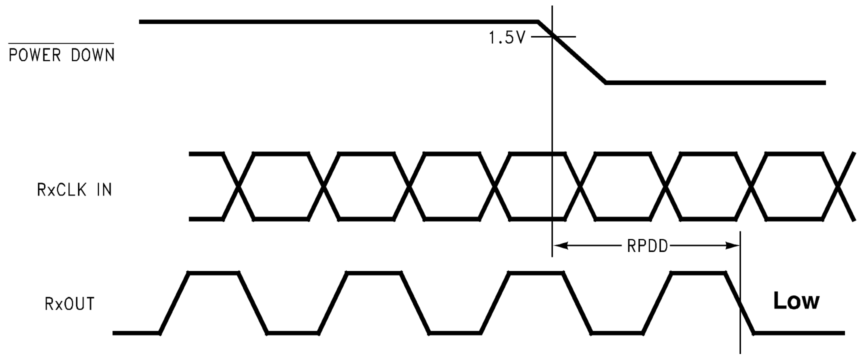


Figure 19. Receiver Powerdown Delay

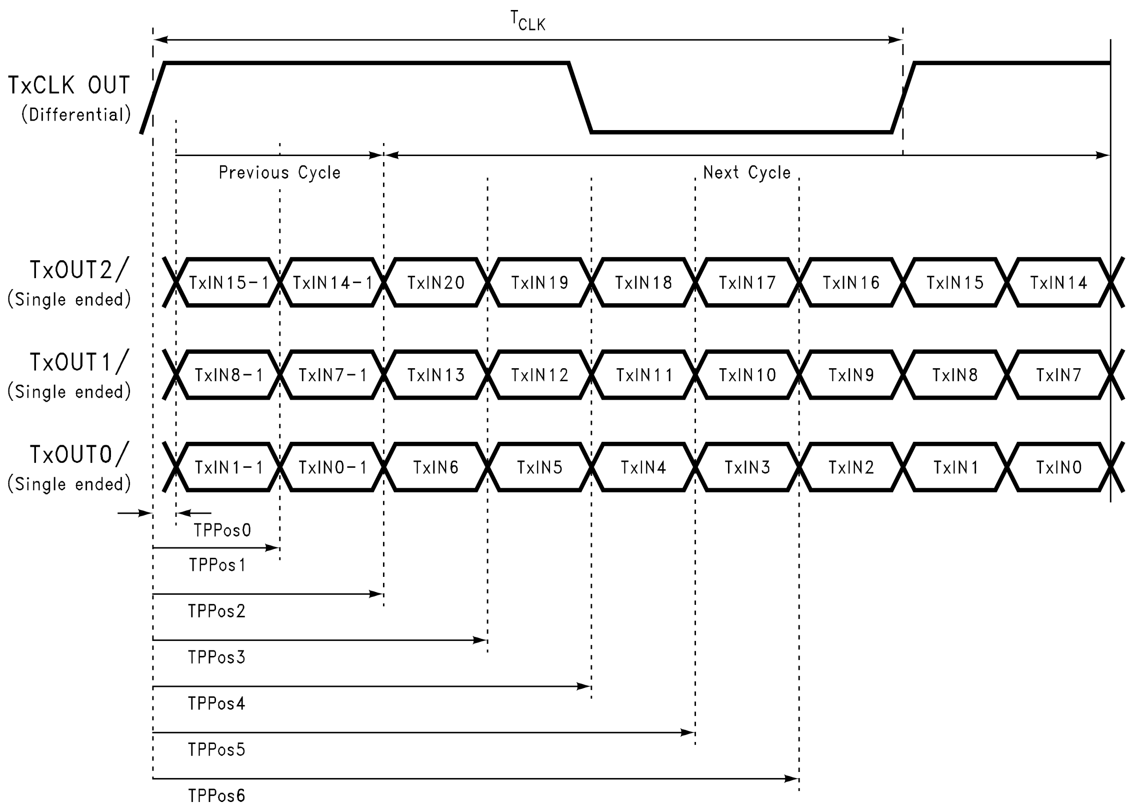


Figure 20. Transmitter LVDS Output Pulse Position Measurement

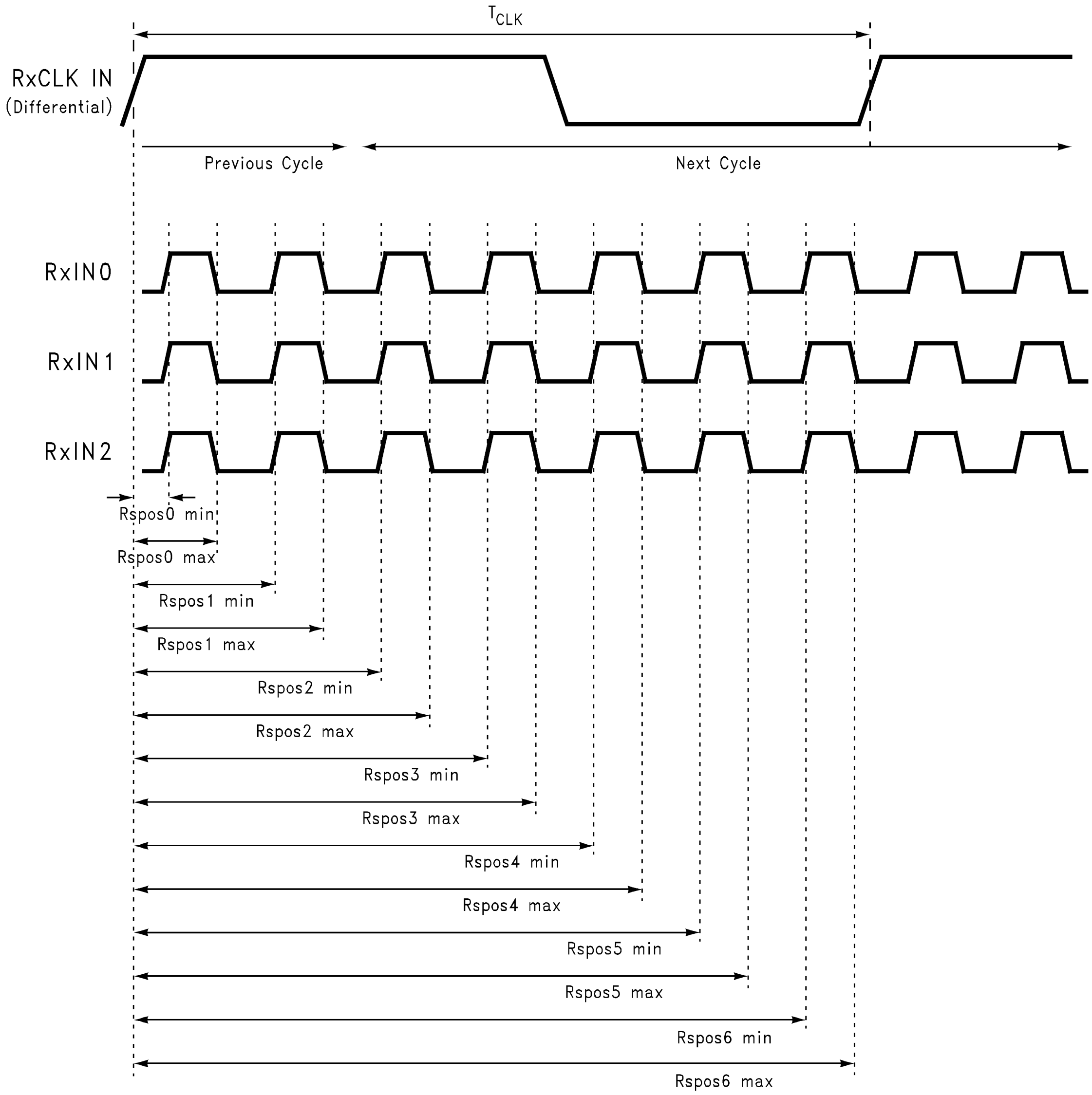
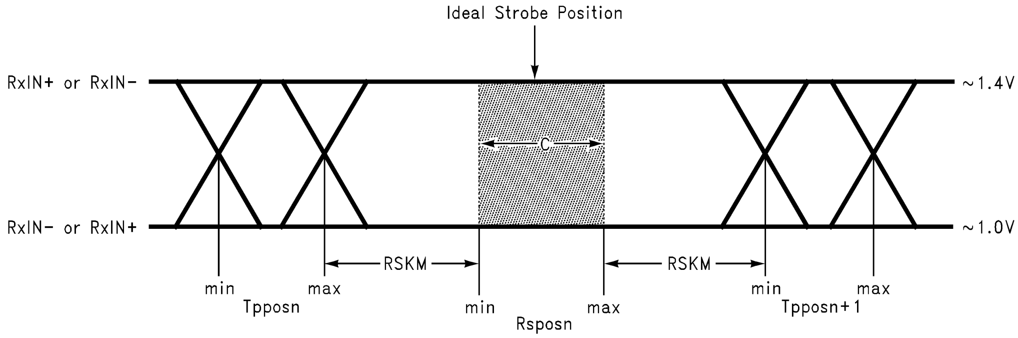


Figure 21. Receiver LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
Tppos—Transmitter output pulse position (min and max)
RSKM ≥ Cable Skew (type, length) + Source Clock Jitter (cycle to cycle) + ISI (Inter-symbol interference)
Cable Skew—typically 10 ps–40 ps per foot, media dependent

Cycle-to-cycle jitter is less than 250 ps

ISI is dependent on interconnect length; may be zero

Figure 22. Receiver LVDS Input Skew Margin

APPLICATIONS INFORMATION

The DS90CR215 and DS90CR216 are backward compatible with the existing 5V Channel Link transmitter/receiver pair (DS90CR213, DS90CR214). To upgrade from a 5V to a 3.3V system the following must be addressed:

1. Change 5V power supply to 3.3V. Provide this supply to the V_{CC}, LVDS V_{CC} and PLL V_{CC}.
2. Transmitter input and control inputs except 3.3V TTL/CMOS levels. They are not 5V tolerant.
3. The receiver powerdown feature when enabled will lock receiver output to a logic low. However, the 5V/66 MHz receiver maintain the outputs in the previous state when powerdown occurred.

DS90CR215 Pin Descriptions — Channel Link Transmitter

Pin Name	I/O	No.	Description
TxIN	I	21	TTL level input.
TxOUT+	O	3	Positive LVDS differential data output.
TxOUT−	O	3	Negative LVDS differential data output.
TxCLK IN	I	1	TTL level clock input. The rising edge acts as data strobe. Pin name TxCLK IN.
TxCLK OUT+	O	1	Positive LVDS differential clock output.
TxCLK OUT−	O	1	Negative LVDS differential clock output.
$\overline{\text{PWR DWN}}$	I	1	TTL level input. Assertion (low input) TRI-STATEs the outputs, ensuring low current at power down.
V_{CC}	I	4	Power supply pins for TTL inputs.
GND	I	5	Ground pins for TTL inputs.
PLL V_{CC}	I	1	Power supply pins for PLL.
PLL GND	I	2	Ground pins for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS outputs.
LVDS GND	I	3	Ground pins for LVDS outputs.

DS90CR216 Pin Descriptions — Channel Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs.
RxIN−	I	3	Negative LVDS differential data inputs.
RxOUT	O	21	TTL level data outputs.
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The rising edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	1	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

The Channel Link devices are intended to be used in a wide variety of data transmission applications. Depending upon the application the interconnecting media may vary. For example, for lower data rate (clock rate) and shorter cable lengths (< 2m), the media electrical performance is less critical. For higher speed/long distance applications the media's performance becomes more critical. Certain cable constructions provide tighter skew (matched electrical length between the conductors and pairs). Twin-coax for example, has been demonstrated at distances as great as 5 meters and with the maximum data transfer of 1.38 Gbit/s. Additional applications information can be found in the following Interface Application Notes:

AN = ####	Topic
AN-1041 (SNLA218)	Introduction to Channel Link
AN-1035 (SNOA355)	PCB Design Guidelines for LVDS and Link Devices
AN-806 (SNLA026)	Transmission Line Theory
AN-905 (SNLA035)	Transmission Line Calculations and Differential Impedance
AN-916 (SNLA219)	Cable Information

CABLES

A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The 21-bit CHANNEL LINK chipset (DS90CR215/216) requires four pairs of signal wires and the 28-bit CHANNEL LINK chipset (DS90CR285/286) requires five pairs of signal wires. The ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is also recommended that cable skew remain below 150 ps (@ 66 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common mode return path for the two devices. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI.

The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental application notes provide the subsystem communications designer with many useful guidelines. It is recommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.

BOARD LAYOUT

To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.

UNUSED INPUTS

All unused inputs at the TxIN inputs of the transmitter must be tied to ground. All unused outputs at the RxOUT outputs of the receiver must then be left floating.

TERMINATION

Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single 100Ω resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance (90Ω to 120Ω typical) of the cable. Figure 23 shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

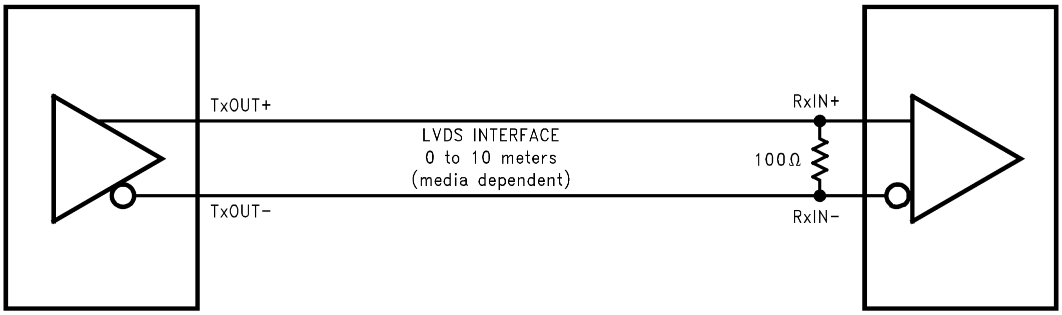


Figure 23. LVDS Serialized Link Termination

DECOUPLING CAPACITORS

Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. The three capacitor values are 0.1 μF, 0.01μF and 0.001 μF. An example is shown in Figure 24. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering/bypassing. Next would be the LVDS V_{CC} pins and finally the logic V_{CC} pins.

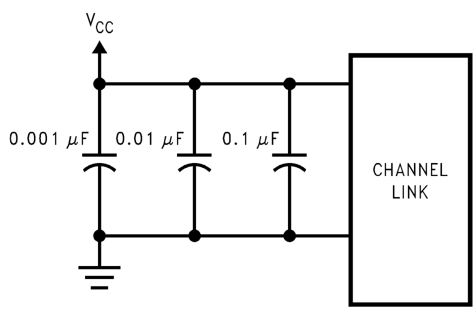


Figure 24. CHANNEL LINK Decoupling Configuration

CLOCK JITTER

The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 66 MHz clock has a period of 15 ns which results in a data bit width of 2.16 ns. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

COMMON MODE vs. DIFFERENTIAL MODE NOISE MARGIN

The typical signal swing for LVDS is 300 mV centered at +1.2V. The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4V. This allows for a ±1.0V shifting of the center point due to ground potential differences and common mode noise.

POWER SEQUENCING AND POWERDOWN MODE

Outputs of the CNANNEL LINK transmitter remain in TRI-STATE until the power supply reaches 2V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 3V and the Powerdown pin is above 1.5V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5 μW (typical).

The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through an internal diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.

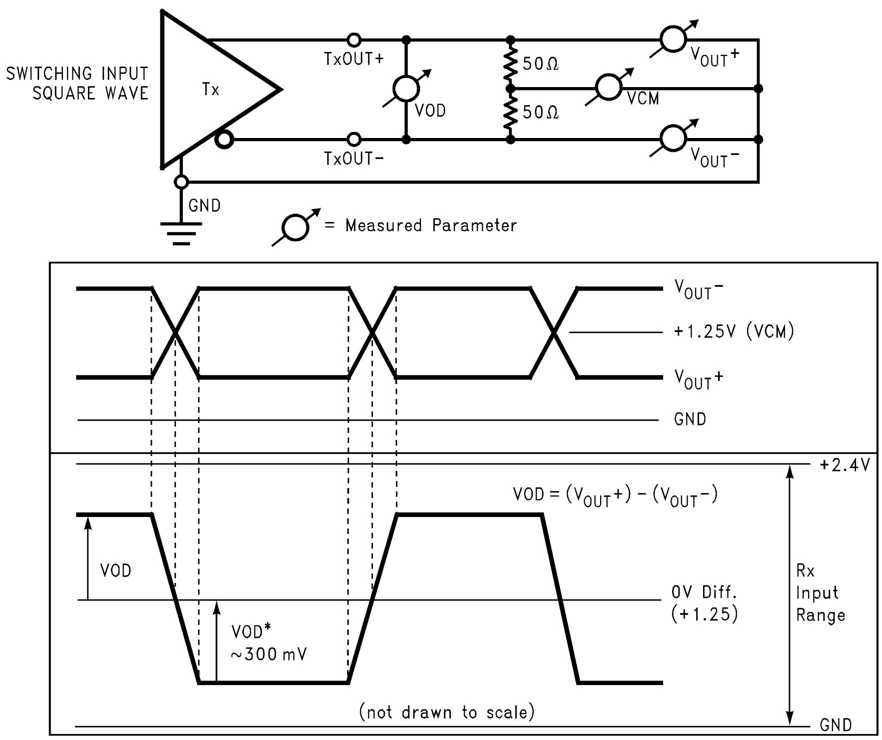


Figure 25. Single-Ended and Differential Waveforms

REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CR215MTD	LIFEBUY	TSSOP	DGG	48	38	Non-RoHS & Non-Green	Call TI	Call TI	-40 to 85	DS90CR215MTD >B	
DS90CR215MTD/NOPB	ACTIVE	TSSOP	DGG	48	38	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR215MTD >B	Samples
DS90CR215MTDX/NOPB	ACTIVE	TSSOP	DGG	48	1000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	DS90CR215MTD >B	Samples
DS90CR216MTD	LIFEBUY	TSSOP	DGG	48	38	Non-RoHS & Green	Call TI	Level-2-235C-1 YEAR		DS90CR216MTD >B	
DS90CR216MTD/NOPB	NRND	TSSOP	DGG	48	38	RoHS & Green	SN	Level-2-260C-1 YEAR		DS90CR216MTD >B	
DS90CR216MTDX	LIFEBUY	TSSOP	DGG	48	1000	Non-RoHS & Green	Call TI	Level-2-235C-1 YEAR		DS90CR216MTD >B	
DS90CR216MTDX/NOPB	NRND	TSSOP	DGG	48	1000	RoHS & Green	SN	Level-2-260C-1 YEAR		DS90CR216MTD >B	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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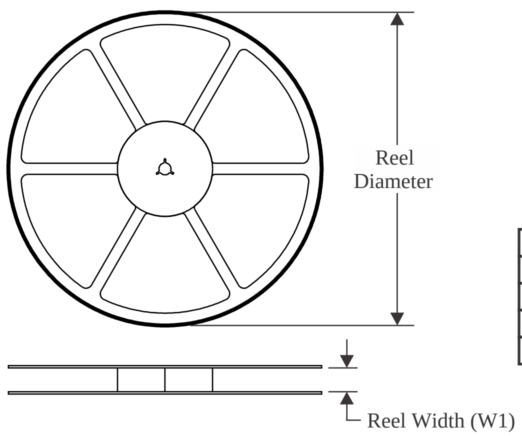
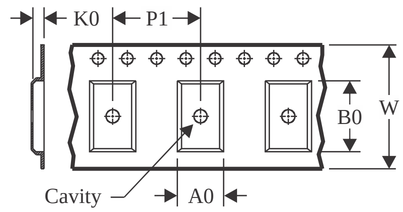
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

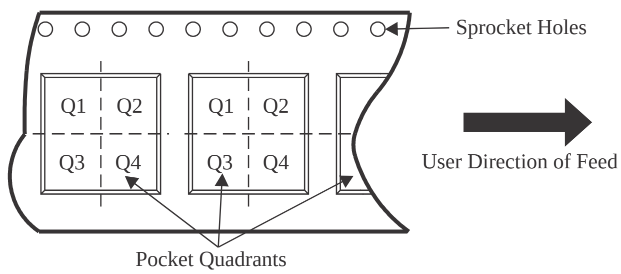


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

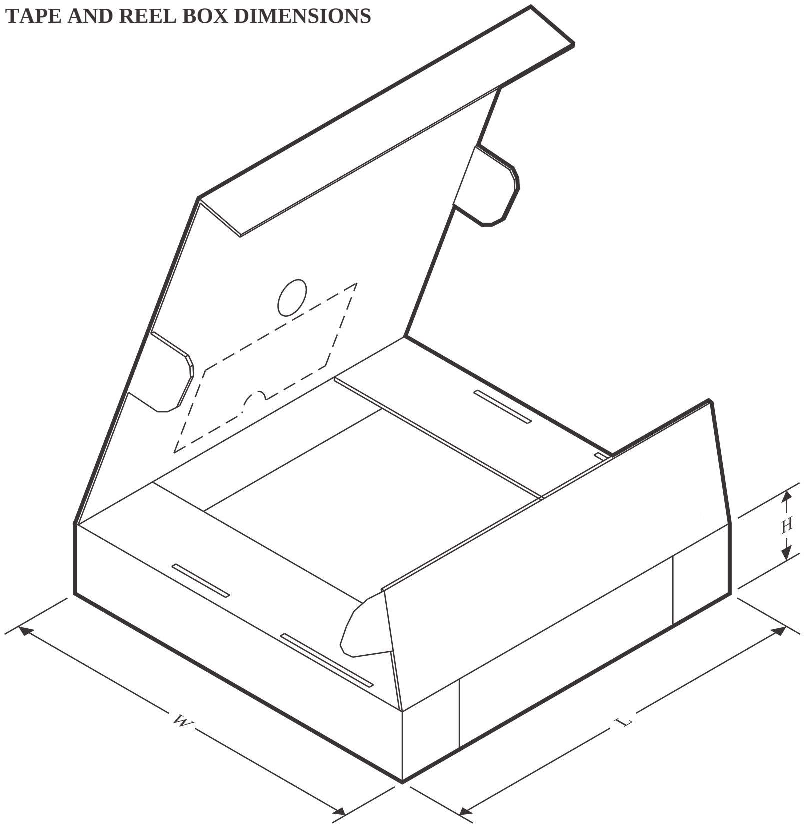
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CR215MTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
DS90CR216MTDX	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
DS90CR216MTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1

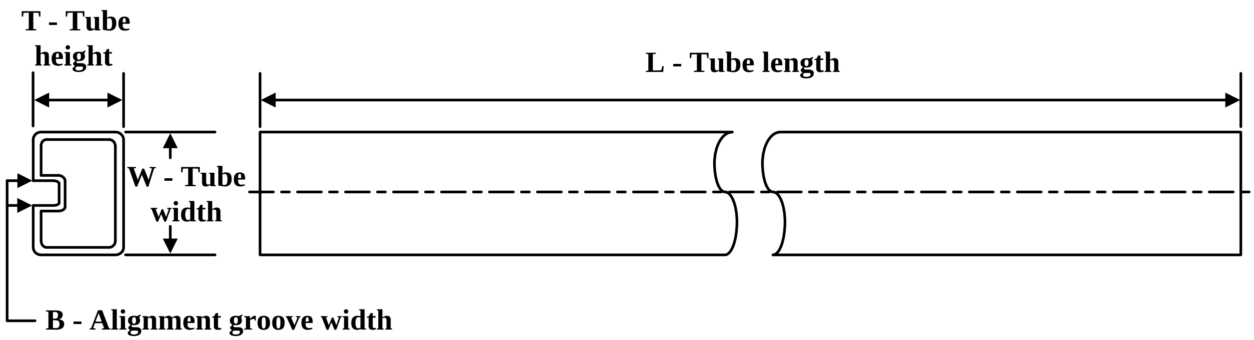
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

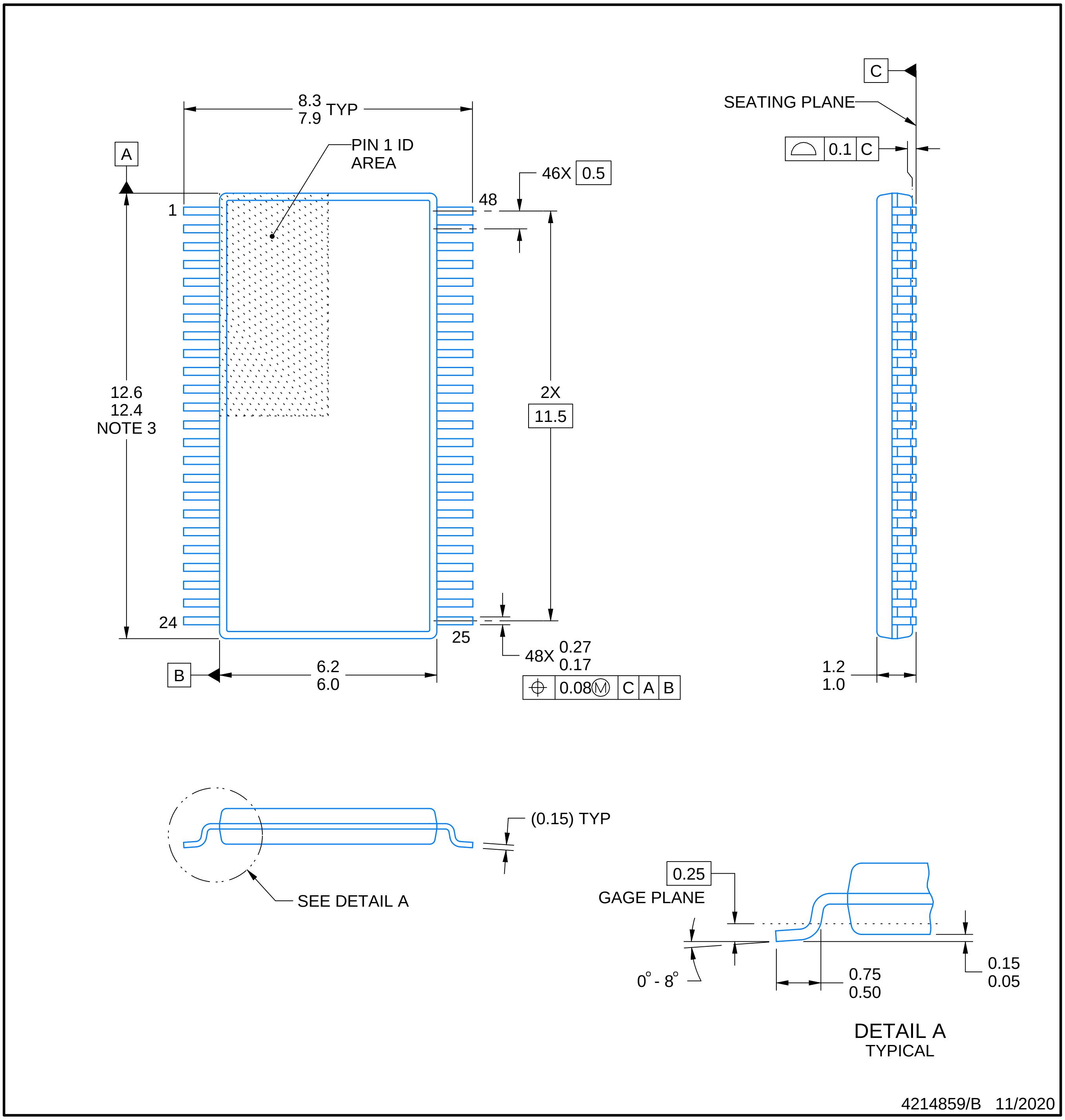
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CR215MTDX/NOPB	TSSOP	DGG	48	1000	356.0	356.0	45.0
DS90CR216MTDX	TSSOP	DGG	48	1000	356.0	356.0	45.0
DS90CR216MTDX/NOPB	TSSOP	DGG	48	1000	356.0	356.0	45.0

TUBE



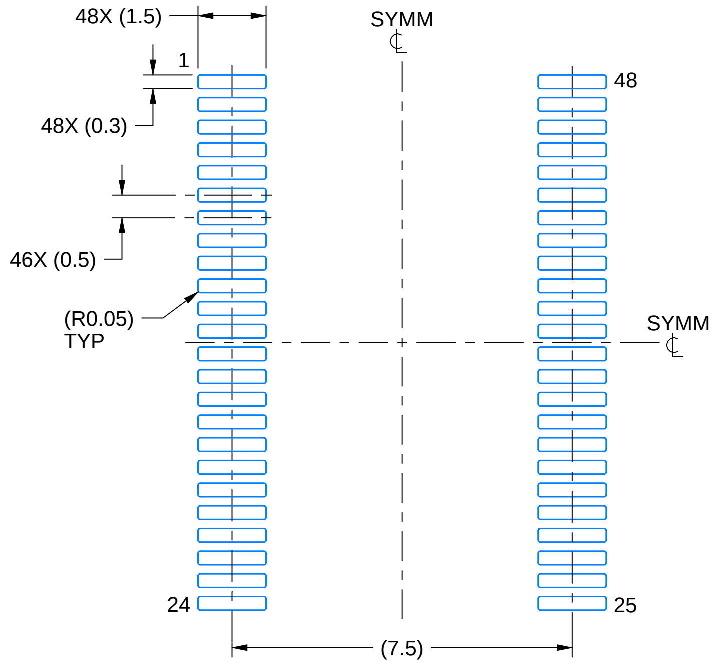
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90CR215MTD	DGG	TSSOP	48	38	495	10	2540	5.79
DS90CR215MTD/NOPB	DGG	TSSOP	48	38	495	10	2540	5.79
DS90CR216MTD	DGG	TSSOP	48	38	495	10	2540	5.79
DS90CR216MTD	DGG	TSSOP	48	38	495	10	2540	5.79
DS90CR216MTD/NOPB	DGG	TSSOP	48	38	495	10	2540	5.79

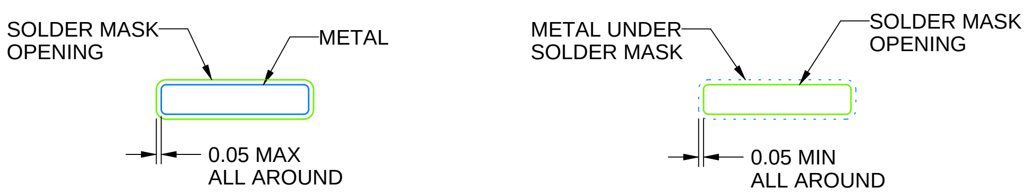


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED

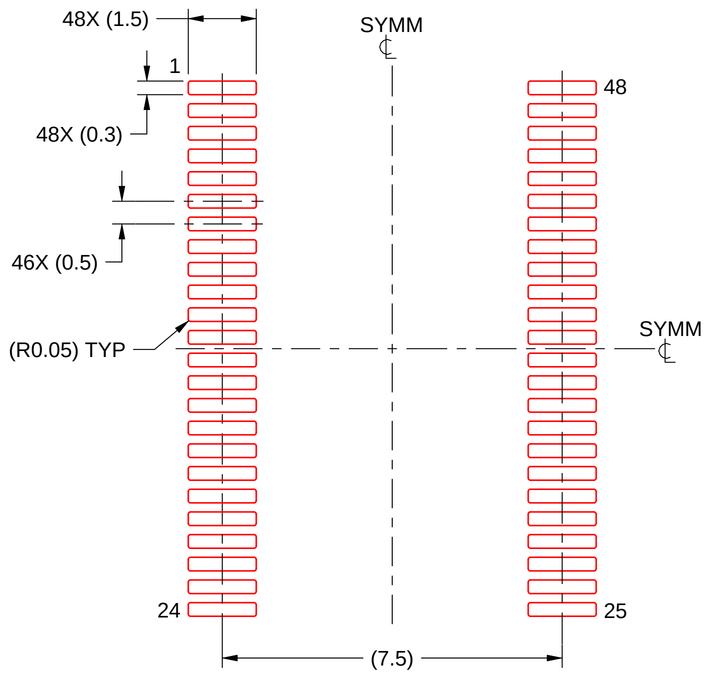
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

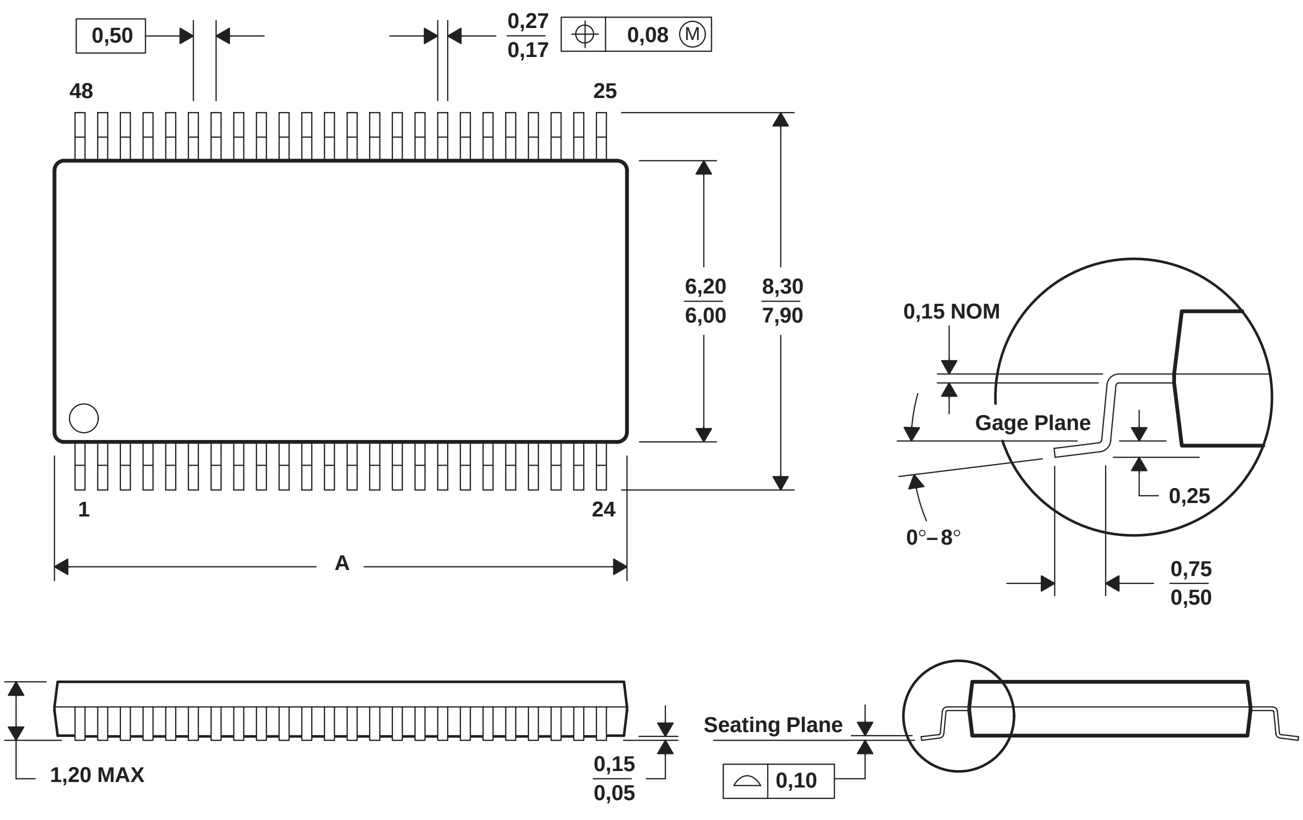
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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