Burr-Brown Products from Texas Instruments

INA166

www.ti.com

Low-Noise, Low-Distortion, G = 2000 INSTRUMENTATION AMPLIFIER

FEATURES

- LOW NOISE: 1.3nV/√Hz at 1kHz
- LOW THD+N: 0.09% at 1kHz
- WIDE BANDWIDTH: 450kHz
- WIDE SUPPLY RANGE: ±4.5V to ±18V
- HIGH CMR: > 100dB
- GAIN SET WITH EXTERNAL RESISTOR
- SO-14 SURFACE-MOUNT PACKAGE

APPLICATIONS

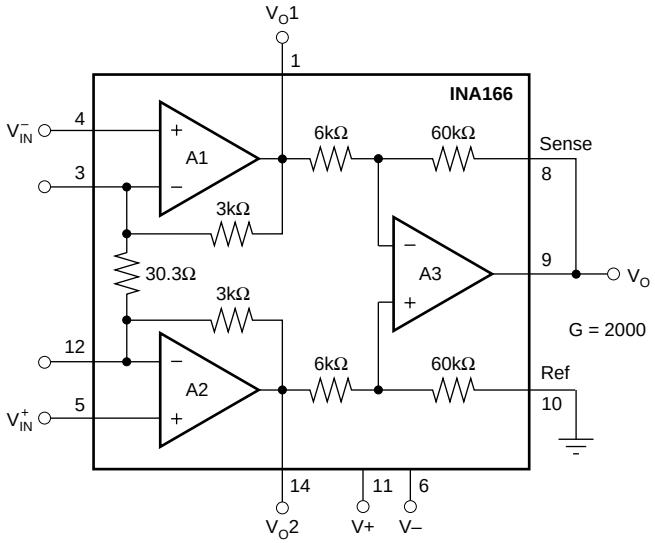
- MOVING-COIL TRANSDUCER AMPLIFIERS
- DIFFERENTIAL RECEIVERS
- BRIDGE TRANSDUCER AMPLIFIERS
- MICROPHONE AND HYDROPHONE PREAMPS

DESCRIPTION

The INA166 is a very low-noise, low-distortion, monolithic instrumentation amplifier. Its current-feedback circuitry achieves very wide bandwidth and excellent dynamic response over a wide range of gain. It is ideal for low-level signals such as microphones or hydrophones. Many industrial, instrumentation, and medical applications also benefit from its low noise and wide bandwidth.

Unique distortion cancellation circuitry reduces distortion to extremely low levels, even in high gain. The INA166 provides near-theoretical noise performance for 200Ω source impedance. Its differential input, low noise, and low distortion provide superior performance as a low-level signal amplifier.

The INA166 is available in a space-saving SO-14 surface-mount package, specified for operation over the –40°C to +85°C temperature range.



TEXAS INSTRUMENTS

Printed in U.S.A. December, 2000

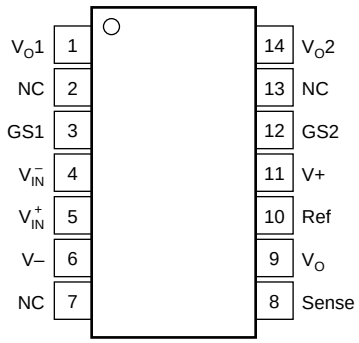
SPECIFICATIONS: $V_S = \pm 5V$

T_A = +25°C and at rated supplies, V_S = ±5V, R_L = 2kΩ connected to ground, G = 2000, unless otherwise noted.

PARAMETER	CONDITIONS	INA166UA MIN	INA166UA TYP	INA166UA MAX	UNITS
GAIN					
Gain Error			±0.3	±1	%
Gain Temp Drift Coefficient			±10		ppm/°C
Nonlinearity			±0.005		% of FS
INPUT REFERRED NOISE					
Voltage Noise	R_{SOURCE} = 0Ω				
f_O = 1kHz			1.3		nV/√Hz
f_O = 100Hz			1.6		nV/√Hz
f_O = 10Hz			2		nV/√Hz
Current Noise					
f_O = 1kHz			0.8		pA/√Hz
INPUT OFFSET VOLTAGE					
Input Offset Voltage	$V_{CM} = V_{OUT}$ = 0V		±50	±250	µV
vs Temperature	$T_A = T_{MIN}$ to T_{MAX}		±2.5		µV/°C
vs Power Supply	V_S = ±4.5V to ±18V		±1	±3	µV/V
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range	$V_{IN}^+ - V_{IN}^-$ = 0V	(V+) – 4	(V+) – 3		V
	$V_{IN}^+ - V_{IN}^-$ = 0V	(V–) + 4	(V–) + 3		V
Common-Mode Rejection	V_{CM} = ±1V, R_{SRC} = 0Ω	100	120		dB
INPUT BIAS CURRENT					
Initial Bias Current			2.5	12	µA
vs Temperature			15		nA/°C
Initial Offset Current			0.1	1	µA
vs Temperature			0.5		nA/°C
INPUT IMPEDANCE					
	Differential		60 || 2		MΩ || pF
	Common-Mode		60 || 2		MΩ || pF
DYNAMIC RESPONSE					
Bandwidth, Small Signal, –3dB			450		kHz
Slew Rate			15		V/µs
THD+Noise, f = 1kHz			0.09		%
Settling Time, 0.1%	5V Step		2.5		µs
0.01%	5V Step		3.5		µs
Overload Recovery	50% Overdrive		1		µs
OUTPUT					
Voltage	R_L = 2kΩ to Ground	(V+) – 2	(V+) – 1.8		V
		(V–) + 2	(V–) + 1.8		V
Load Capacitance Stability			1000		pF
Short-Circuit Current	Continuous-to-Common		±60		mA
POWER SUPPLY					
Rated Voltage			±5		V
Voltage Range		±4.5		±18	V
Current, Quiescent	I_O = 0mA		±10	±12	mA
TEMPERATURE RANGE					
Specification		–40		+85	°C
Operating		–40		+125	°C
Thermal Resistance, θ_{JA}			100		°C/W

PIN CONFIGURATION

Top View



SO-14

NC = No Internal Connection

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage	±18V
Signal Input Terminals, Voltage[2]	(V–) – 0.5V to (V+) + 0.5V
Current[2]	10mA
Output Short-Circuit to Ground	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

PACKAGE/ORDERING INFORMATION

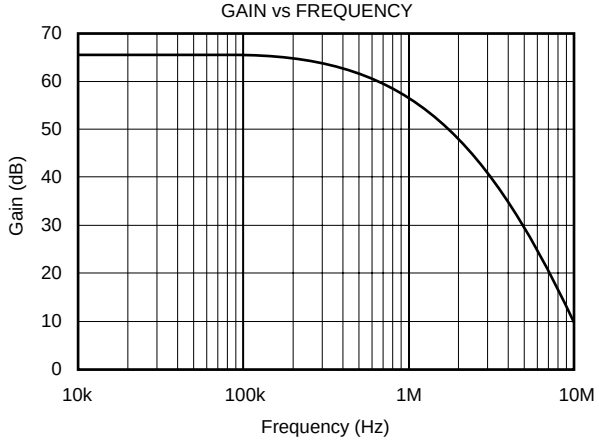
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
INA166UA	SO-14 Surface Mount	235	INA166UA	INA166UA	Rails
"	"	"	"	INA166UA/2K5	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of “INA166UA/2K5” will get a single 2500-piece Tape and Reel.

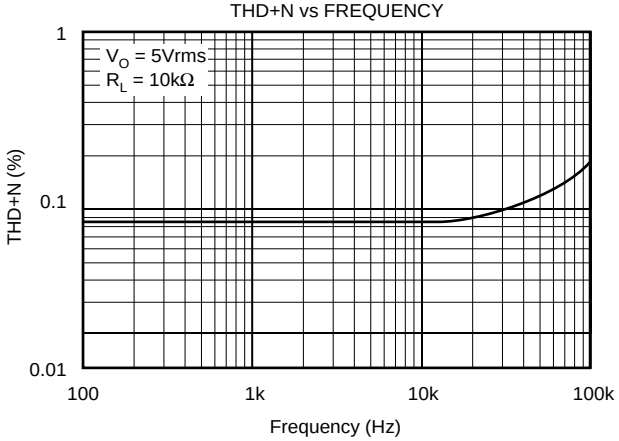
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = ±5V, R_L = 2kΩ, C_L = 50pF, G = 2000, unless otherwise noted.

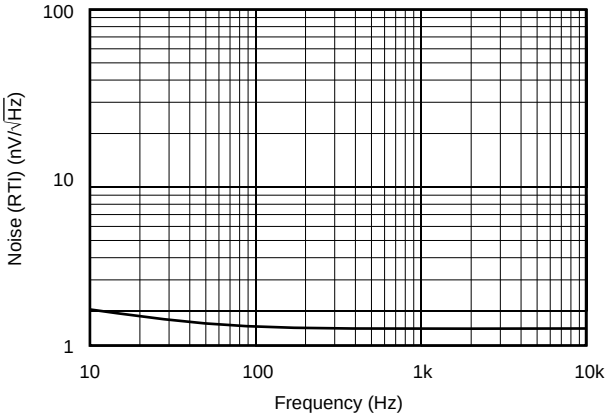
GAIN vs FREQUENCY



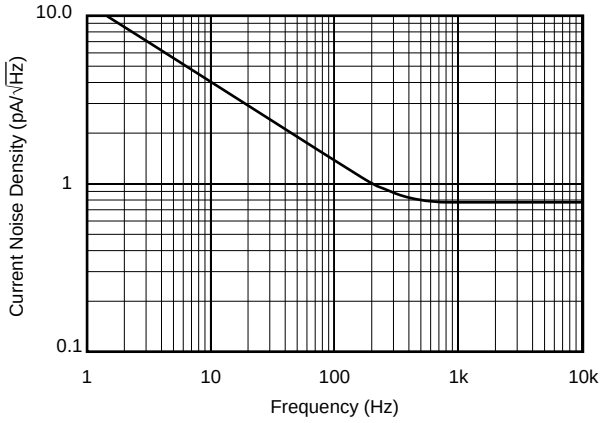
THD+N vs FREQUENCY



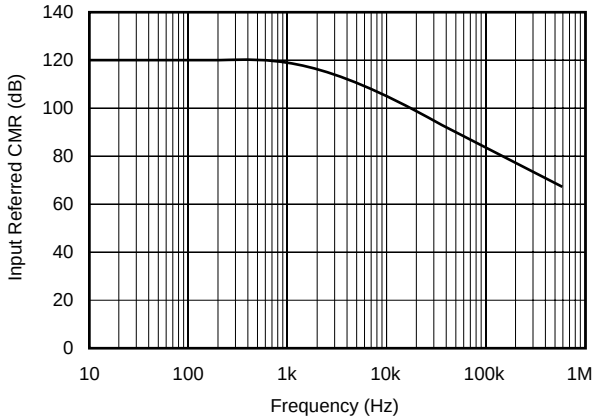
NOISE VOLTAGE (RTI) vs FREQUENCY



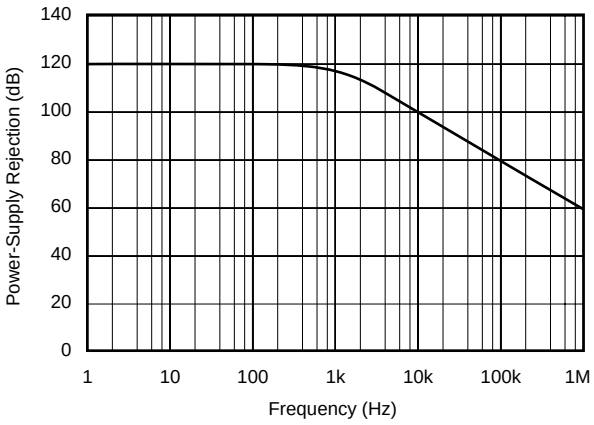
CURRENT NOISE SPECTRAL DENSITY



CMR vs FREQUENCY



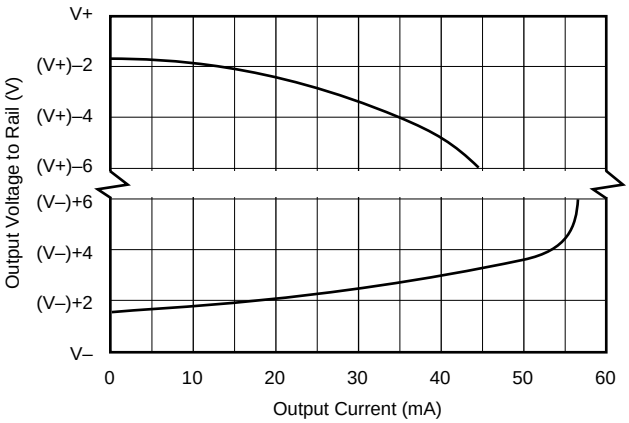
POWER-SUPPLY REJECTION vs FREQUENCY



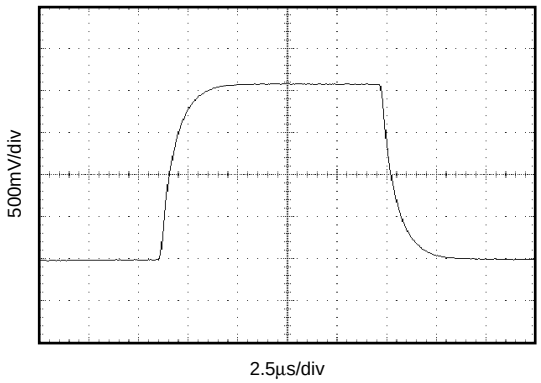
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = ±5V, R_L = 2kΩ, C_L = 50pF, G = 2000, unless otherwise noted.

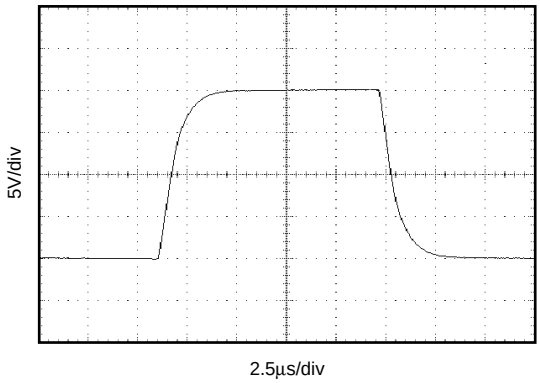
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



SMALL-SIGNAL RESPONSE



LARGE-SIGNAL RESPONSE



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation. Power supplies should be bypassed with 0.1µF tantalum capacitors near the device pins. The output Sense (pin 8) and output Reference (pin 10) should be low-impedance connections. Resistance of greater than 5Ω in series with these connections will degrade the common-mode rejection of the INA166.

GAIN

Gain of the INA166 is internally set for G = 2000. Input stage (A1, A2) gain is 200 and the output stage gain (A3) is 10. Internal resistor values are laser trimmed for accurate ratios to achieve excellent gain accuracy and common-mode rejection, but absolute resistor values are approximately ±20%. Nominal resistor values are shown.

Although the INA166 is primarily intended for fixed-gain applications, the gain can be increased by connecting a gain-set resistor, R_G, between pin 3 and pin 12 The nominal gain will be:

$$G = 2000 + \frac{60000}{R_G}$$

Accuracy of the 60000 term in this equation is approximately ±20%. The stability and temperature drift of R_G contributes to the overall gain accuracy and these effects can be inferred from this gain equation.

NOISE PERFORMANCE

The INA166 provides very low-noise with low-source impedance. Its 1.3nV/√Hz voltage noise delivers near-theoretical noise performance with a source impedance of 200Ω. The input stage design used to achieve this low noise, results in relatively high input bias current and input bias current noise. As a result, the INA166 may not provide the best noise performance with a source impedance greater than 10kΩ. For source impedance greater than 10kΩ, other instrumentation amplifiers may provide improved noise performance.

INPUT CONSIDERATIONS

Very low source impedance (less than 10Ω) can cause the INA166 to oscillate. This depends on circuit layout, signal source, and input cable characteristics. An input network consisting of a small inductor and resistor, as shown in Figure 2, can greatly reduce any tendency to oscillate. This is especially useful if a variety of input sources are to be connected to the INA166. Although not shown in other figures, this network can be used as needed with all applications shown.

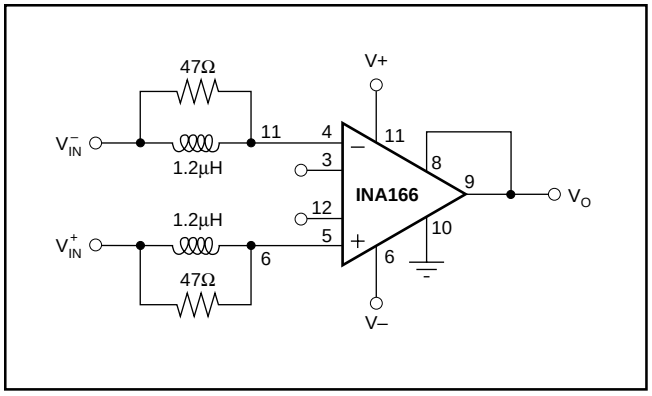


FIGURE 2. Input Stabilization Network.

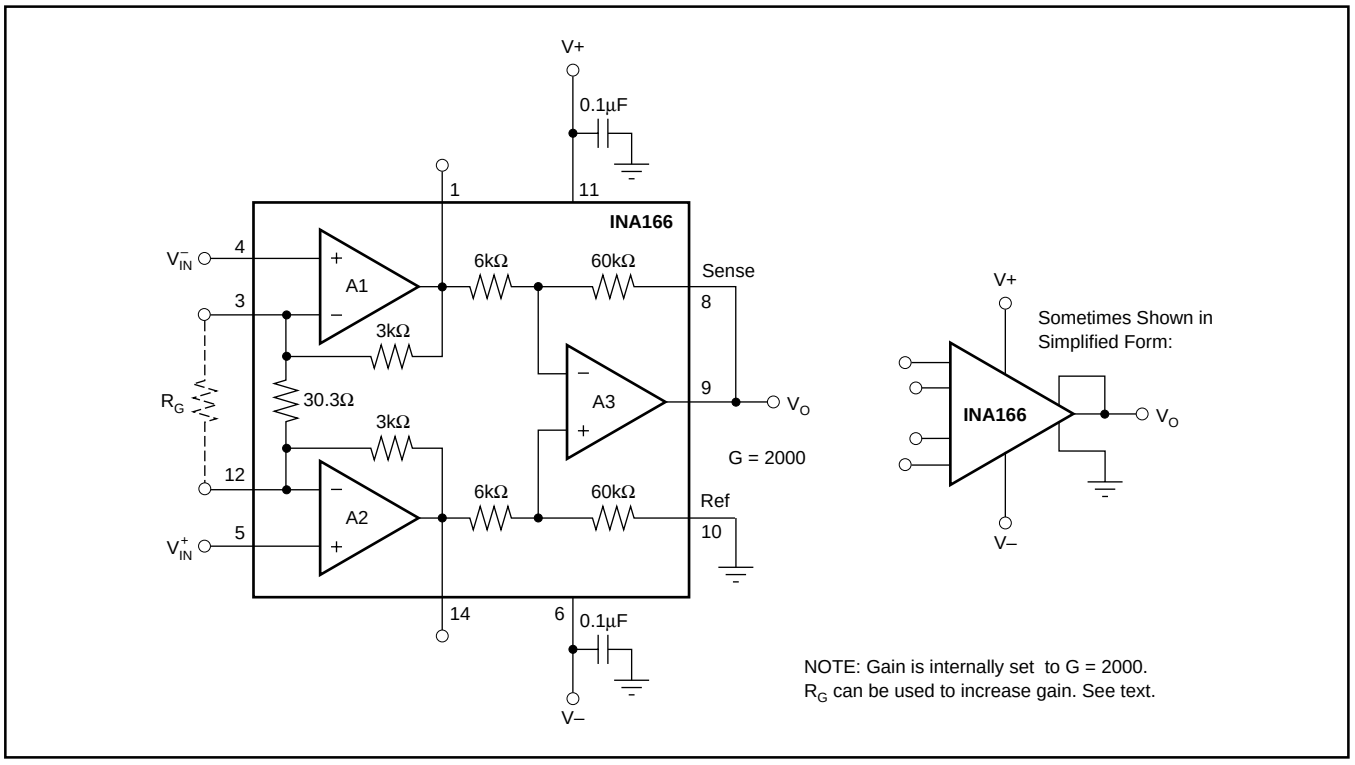


FIGURE 1. Basic Circuit Connections.

OFFSET VOLTAGE TRIM

A variable voltage applied to pin 10, as shown in Figure 3, can be used to adjust the output offset voltage. A voltage applied to pin 10 is summed with the output signal. An op amp connected as a buffer is used to provide a low impedance at pin 10 to assure good common-mode rejection.

OUTPUT SENSE

An output sense terminal allows greater gain accuracy in driving the load. By connecting the sense connection at the load, I • R voltage loss to the load is included inside the feedback loop. Current drive can be increased by connecting a buffer amp inside the feedback loop, as shown in Figure 4.

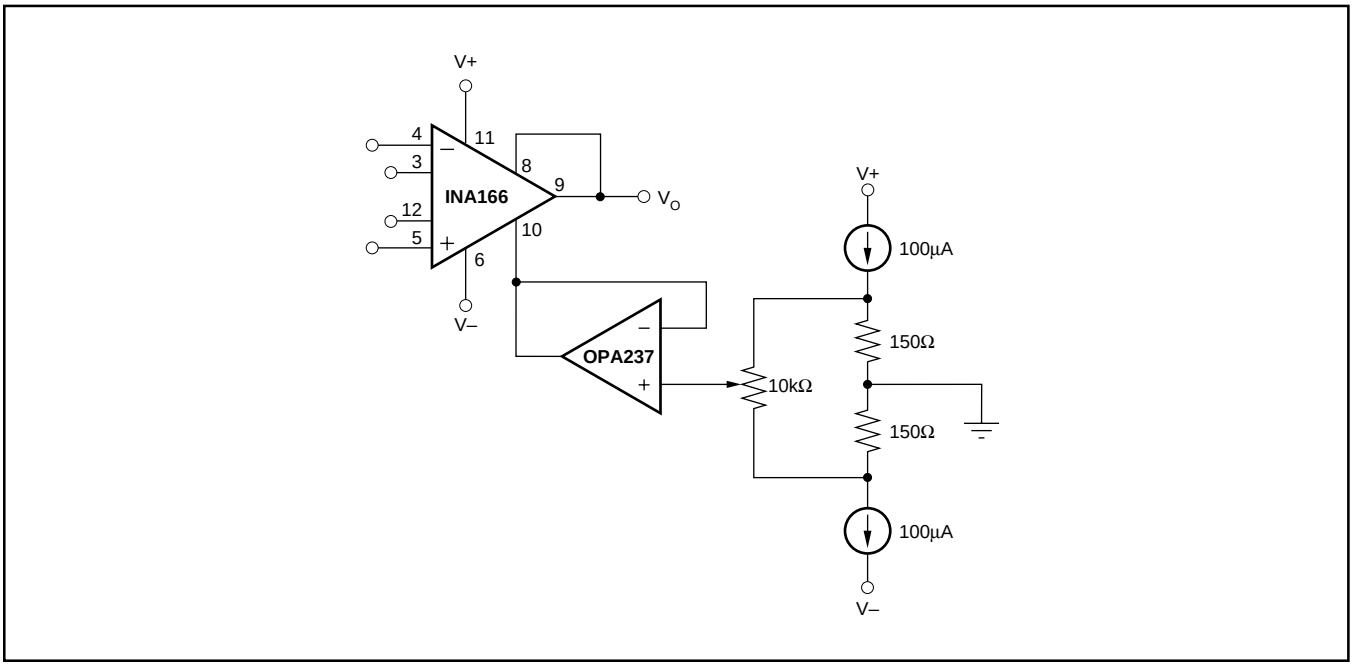


FIGURE 3. Offset Voltage Adjustment Circuit.

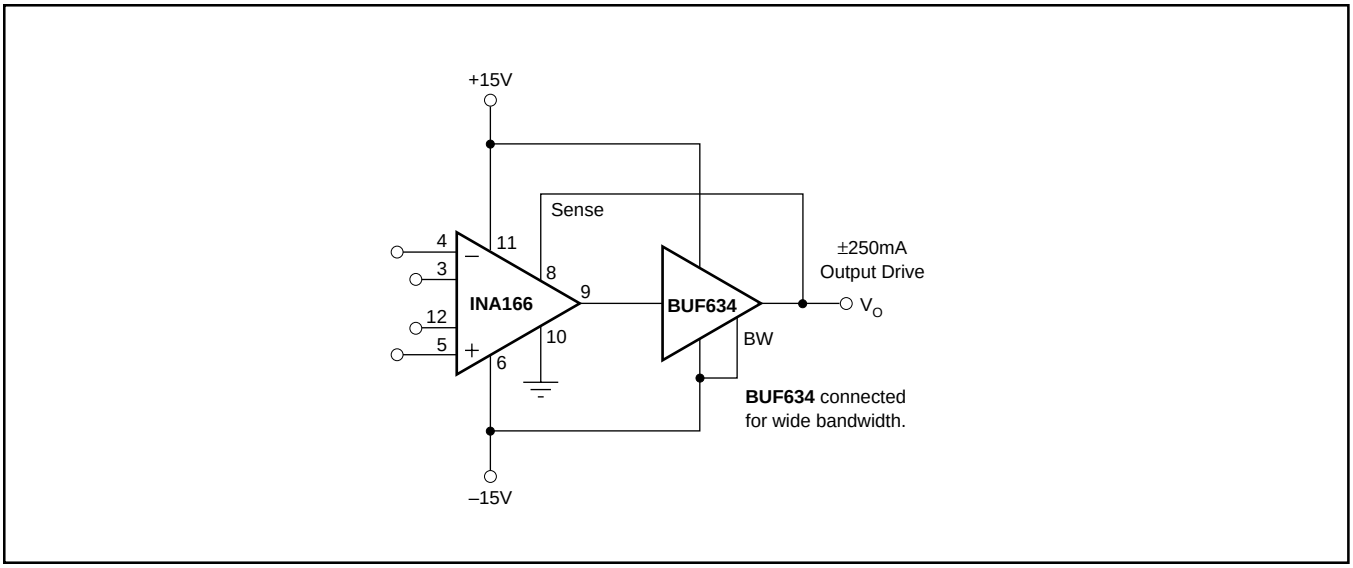


FIGURE 4. Buffer for Increase Output Current.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA166UA	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	INA166UA	
INA166UA/2K5	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	INA166UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

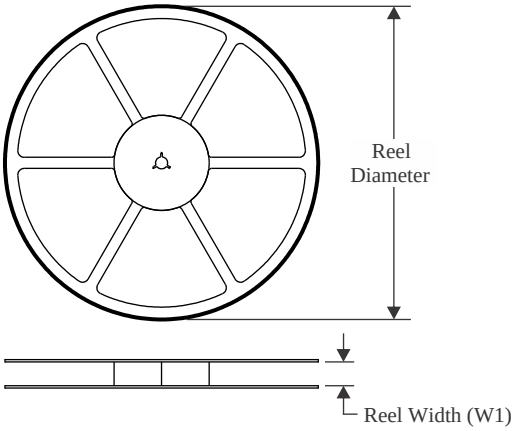
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

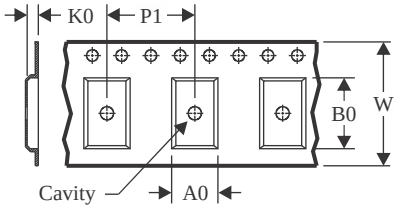
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

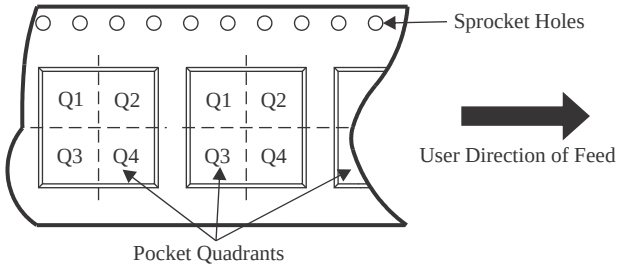


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

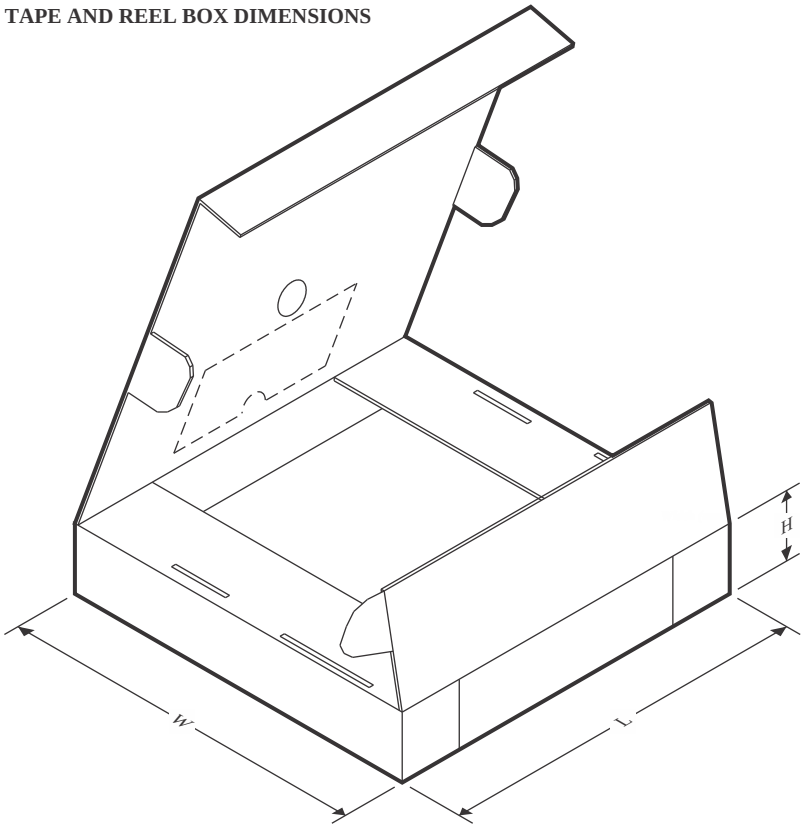
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA166UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA166UA/2K5	SOIC	D	14	2500	356.0	356.0	35.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265