Micro-Power, Zerø-Drift, Rail-to-Rail Out Instrumentation Amplifier

Check for Samples: INA333-HT

FEATURES

- **Low Offset Voltage: 25 µV (max at 25°C), G ≥ 100**
- **Low Drift: 0.2 µV/°C, G ≥ 1000**
- **Low Noise: 55 nV/√Hz, G ≥ 100**
- **High CMRR: 100 dB (min at 25°C), G ≥ 10**
- **Supply Range: +1.8 V to +5.5 V**
- **Input Voltage: (V–) +0.1 V to (V+) –0.1 V**
- **Output Range: (V–) +0.05 V to (V+) –0.05V**
- **Low Quiescent Current: 198 µA**
- **RFI Filtered Inputs**

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range** (1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

(1) Custom temperature ranges available

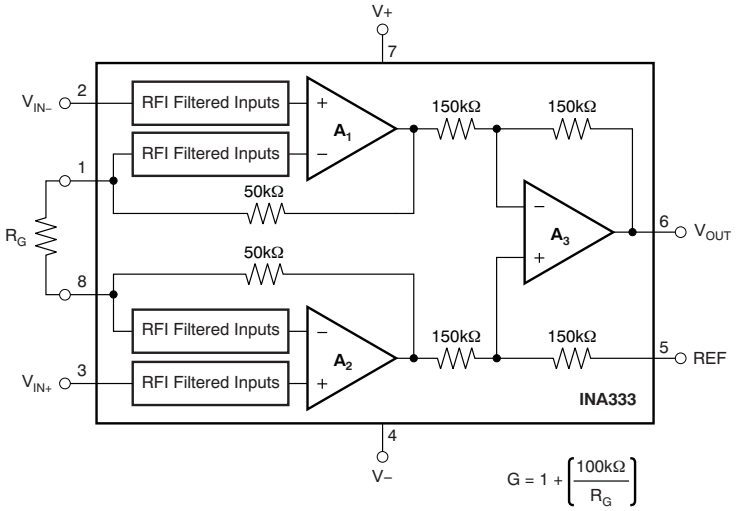
DESCRIPTION

The INA333 is a low-power, precision instrumentation amplifier offering excellent accuracy. The versatile 3-op amp design, small size, and low power make it ideal for a wide range of portable applications.

A single external resistor sets any gain from 1 to 1000. The INA333 is designed to use an industry-standard gain equation: $G = 1 + (100k\Omega/R_G)$.

The INA333 provides very low offset voltage (25 µV at 25°C, G ≥ 100), excellent offset voltage drift (0.2 µV/°C, G ≥ 100), and high common-mode rejection (100 dB at 25°C, G ≥ 10). It operates with power supplies as low as 1.8 V (±0.9V), and quiescent current is only 50 µA—ideal for battery-operated systems. Using autocalibration techniques to ensure excellent precision over the extended industrial temperature range, the INA333 also offers exceptionally low noise density (55 nV/√Hz) that extends down to dc.

The INA333 is is specified over the T_A = –55°C to +210°C temperature range.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	PACKAGE QTY | CARRIER
–55°C to 210°C	KGD	INA333SKGD1	NA	240 | TRAY
		INA333SKGD2	NA	10 | TRAY
	JD	INA333SJD	INA333SJD	1 | TUBE
	HKJ	INA333SHKJ	INA333SHKJ	1 | TUBE
	HKQ	INA333SHKQ	INA333SHKQ	1 | TUBE

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packaging quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

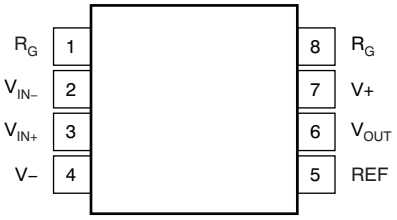
ABSOLUTE MAXIMUM RATINGS(1)

		INA333	UNIT
Supply voltage		+7	V
Analog input voltage range(2)		(V–) – 0.3 to (V+) + 0.3	V
Output short-circuit(3)		Continuous	
Operating temperature range, T_A		–55 to +210	°C
Storage temperature range, T_{STG}		–65 to +210	°C
Junction temperature, T_J		+210	°C
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
(3) Short-circuit to ground.

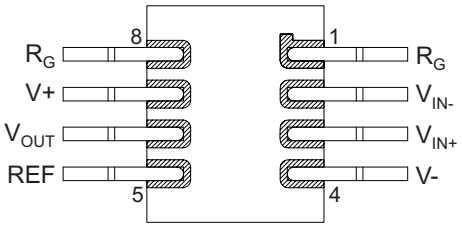
PIN CONFIGURATIONS

JD OR HKJ PACKAGE
MSOP-8
(TOP VIEW)



INA333

HKQ PACKAGE
(TOP VIEW)



HKQ as formed or HKJ mounted dead bug

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	V-	Al-Si-Cu (0.5%)

Origin

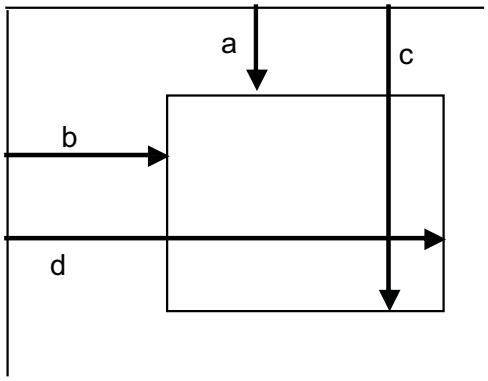
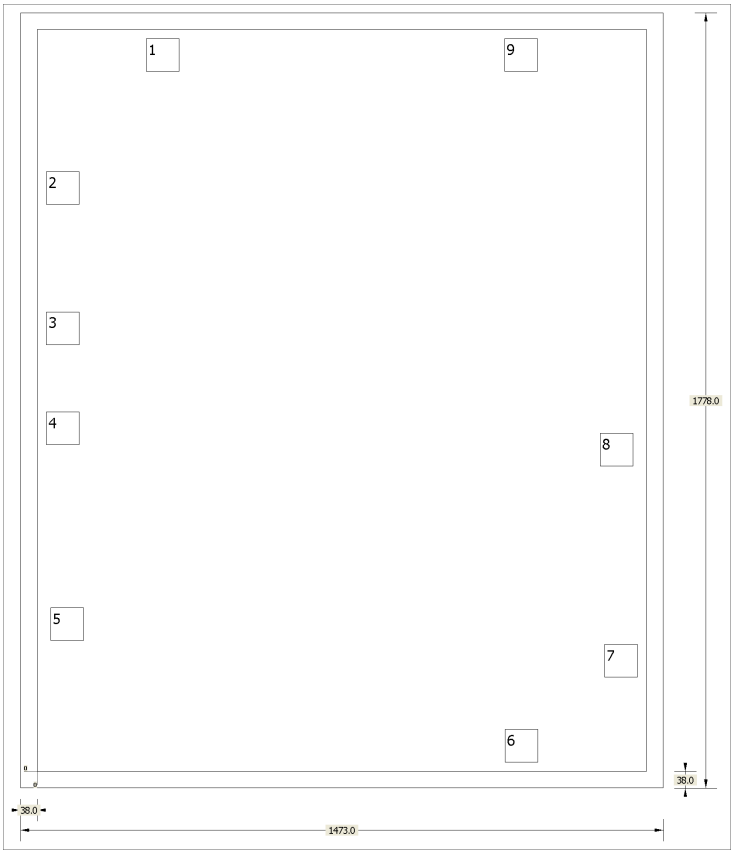


Table 1. Bond Pad Coordinates in Microns(1)

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
R_G	1	250	1604.8	326	1680.8
V_{IN-}	2	21.2	1300	97.2	1376
V_{IN+}	3	21.2	978.5	97.2	1054.5
NC	4	21.2	748.65	97.2	824.65
V-	5	31.3	300	107.3	376
REF	6	1072.15	21.2	1148.15	97.2
V_{OUT}	7	1299.8	216.2	1375.8	292.2
V+	8	1289.7	700	1365.7	776
R_G	9	1071	1604.8	1147	1680.8

(1) Substrate is N/C



THERMAL CHARACTERISTICS FOR JD PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(1)	High-K board(2), no airflow		64.9		°C/W
		No airflow		83.4		
θ_{JB}	Junction-to-board thermal resistance	High-K board without underfill		27.9		°C/W
θ_{JC}	Junction-to-case thermal resistance			6.49		°C/W

(1) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodolgy is not meant to and will not predict the performance of a package in an application-specific environment.
(2) JED51-7, high effective thermal conductivity test board for leaded surface mount packages.

THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance	to ceramic side of case			5.7	°C/W
		to top of case lid (metal side of case)			13.7	

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V

At T_A = +25°C, R_L = 10kΩ, V_{REF} = V_S/2, and G = 1, unless otherwise noted.

PARAMETER		TEST CONDITIONS	T_A = –55°C to +125°C			T_A = +210°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT(1)									
Offset voltage, RTI(2)	V_{OSI}			±10 ±25/G	±25 ±75/G		±15		µV
vs Temperature					**±0.1 ±0.5/G(3)**		0.2(4)(5)		µV/°C
vs Power supply	PSR	1.8 V ≤ V_S ≤ 5.5 V		±1 ±5/G	±5 ±15/G		2.5(4)		µV/V
Long-term stability				See note (6)					
Turn-on time to specified V_{OSI}			See Typical characteristics			See Typical characteristics			
Impedance									
Differential	Z_{IN}			100 || 3			100 || 3		GΩ || pF
Common-mode	Z_{IN}			100 || 3			100 || 3		GΩ || pF
Common-mode voltage range	V_{CM}	V_O = 0 V	(V–) + 0.1		(V+) – 0.1	(V–) + 0.1		(V+) – 0.1 V	V
Common-mode rejection	CMR	DC to 60 Hz							
G = 1		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	80	90					dB
G = 10		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	100	110					dB
G = 100		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	100	115			110		dB
G = 1000		V_{CM} = (V–) + 0.1 V to (V+) – 0.1 V	100	115			113		dB
INPUT BIAS CURRENT									
Input bias current	I_B			±70	±200		±1260	±2044	pA
vs Temperature			**See Typical Characteristic curve**			See Typical Characteristic curve			pA/°C
Input offset current	I_{OS}			±50	±200				pA
vs Temperature			**See Typical Characteristic curve**			See Typical Characteristic curve			pA/°C

(1) Total V_{OS}, Referred-to-input = (V_{OSI}) + (V_{OSO}/G).
(2) RTI = Referred-to-input.
(3) Temperature drift is measured from –55°C to +125°C.
(4) G = 1000
(5) Temperature drift is measured from 125°C to +210°C.
(6) 300-hour life test at +150°C demonstrated randomly distributed variation of approximately 1 µV.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V (continued)

At T_A = +25°C, R_L = 10kΩ, V_{REF} = V_S/2, and G = 1, unless otherwise noted.

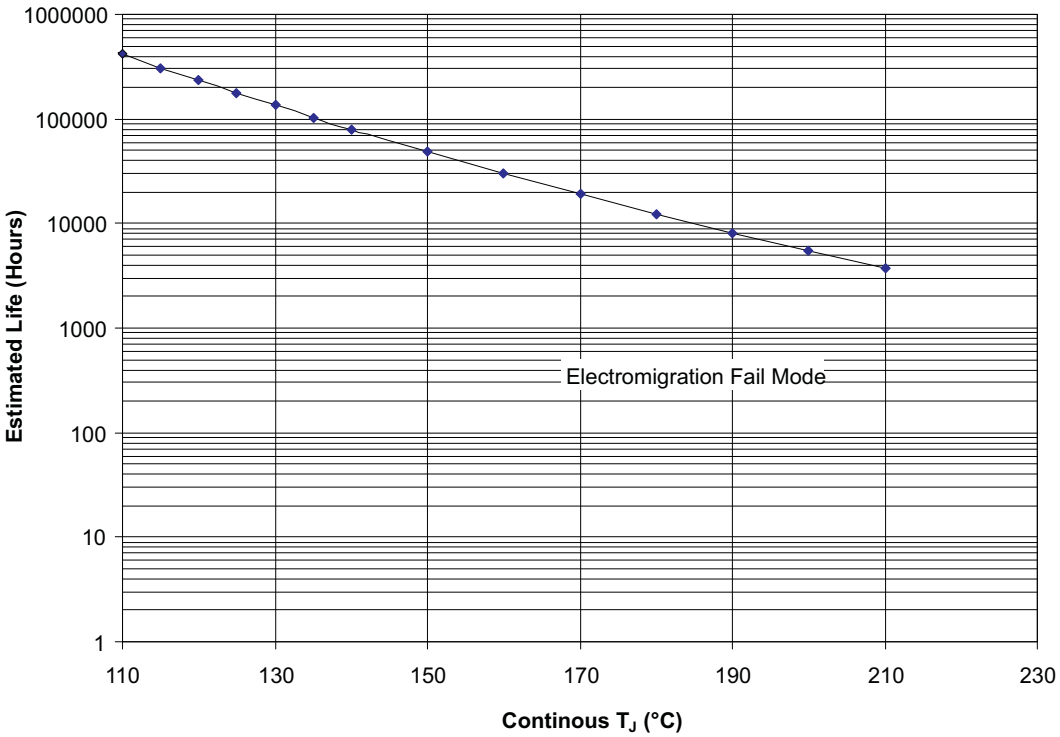
PARAMETER	TEST CONDITIONS	T_A = –55°C to +125°C			T_A = +210°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT VOLTAGE NOISE								
Input voltage noise e_{NI}	G = 100, R_S = 0 Ω							
f = 10 Hz			42			63		nV/√Hz
f = 100 Hz			40			70		nV/√Hz
f = 1 kHz			50			55		nV/√Hz
f = 0.1Hz to 10 Hz			2			6		μV_{PP}
Input current noise i_N								
f = 10Hz			100					fA/√Hz
f = 0.1Hz to 10Hz			2					pA_{PP}
GAIN								
Gain equation G			1 + (100kΩ/R_G)			1 + (100kΩ/R_G)		V/V
Range of gain[7]		1		1000	100		1000	V/V
Gain error	V_S = 5.5 V, (V–) + 100mV ≤ V_O ≤ (V+) – 100mV							
G = 1			±0.02	±0.1				%
G = 10			±0.05	±0.5				%
G = 100			±0.01	±0.5		±1.3		%
G = 1000			±0.43	±1.15		±1.7		%
GAIN (continued)								
Gain vs Temperature								
G = 1			**±1**	**±5**				ppm/°C
G > 1[8]			**±15**	**±50**				ppm/°C
Gain nonlinearity	V_S = 5.5 V, (V–) + 100mV ≤ V_O ≤ (V+) – 100mV							
G = 1 to 1000	R_L = 10 kΩ		10			10		ppm
OUTPUT								
Output voltage swing from rail[9]	V_S = 5.5 V, R_L = 10 kΩ		See note [9]	50			185	mV
Capacitive load drive			500			500		pF
Short-circuit current I_{SC}	Continuous to common		–55, +5			–36, +1		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB								
Range of gain[7]								
G = 1			150					kHz
G = 10			35					kHz
G = 100			3.5			3.1		kHz
G = 1000			350			300		Hz
Slew rate SR	V_S = 5 V, V_O = 4 V Step							
G = 1			0.16			0.25		V/µs
G = 100			0.06			0.04		V/µs
Settling time to 0.01% t_S								
G = 1	V_{STEP} = 4 V		35			32		µs
G = 100	V_{STEP} = 4 V		240			326		µs
Settling time to 0.001% t_S								

(7) Not recommend gain < 100 for 210°C application.
(8) Does not include effects of external resistor R_G.
(9) See Typical Characteristics curve, *Output Voltage Swing vs Output Current* (Figure 31).

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V (continued)

At T_A = +25°C, R_L = 10kΩ, V_{REF} = V_S/2, and G = 1, unless otherwise noted.

PARAMETER	TEST CONDITIONS	T_A = –55°C to +125°C			T_A = +210°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
G = 1	V_{STEP} = 4 V		60			55		µs
G = 100	V_{STEP} = 4 V		500			530		µs
Overload recovery	50% overdrive		52			28		µs
REFERENCE INPUT								
R_{IN}			300			300		kΩ
Voltage range		V–		V+	V–		V+	V
POWER SUPPLY								
Voltage range								
Single		+1.8		+5.5	+1.8		+5.5	V
Dual		±0.9		±2.75	±0.9		±2.75	V
Quiescent current I_Q	V_{IN} = V_S/2		50	75				µA
vs Temperature				**80**		**198**	**345**	**µA**
TEMPERATURE RANGE								
Specified temperature range		–55		+125	–55		+210	°C
Operating temperature range		–55		+125	–55		+210	°C



Notes
1. See datasheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

Figure 1. INA333SKGD1 Operating Life Derating Chart

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = 5V, R_L = 10kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

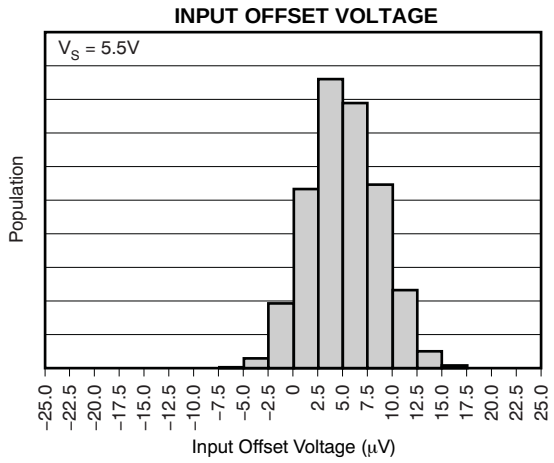


Figure 2.

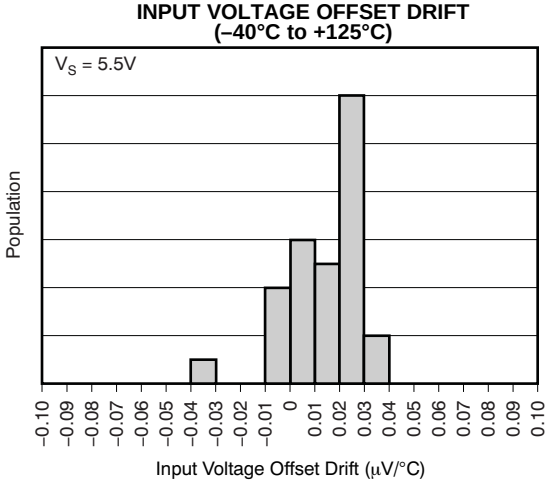


Figure 3.

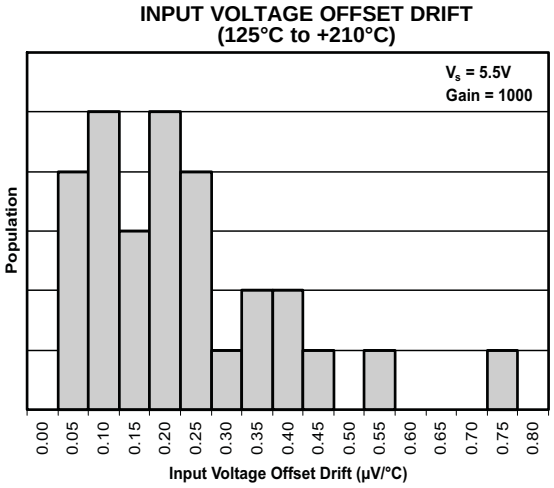


Figure 4.

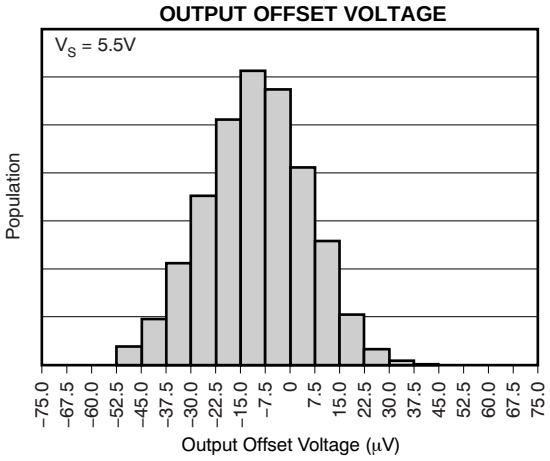


Figure 5.

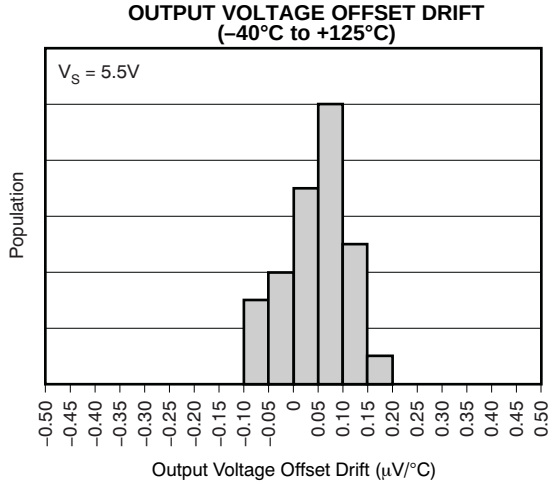


Figure 6.

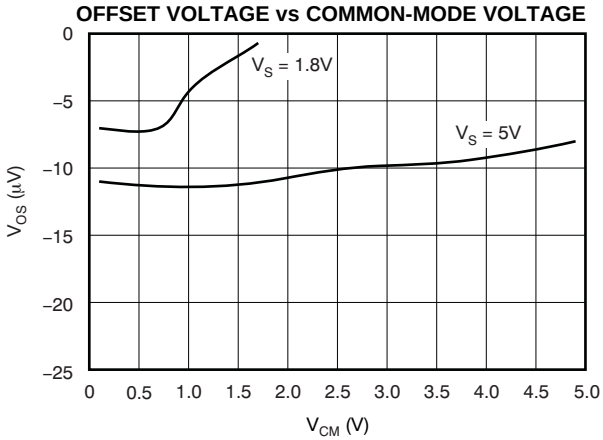


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, R_L = 10kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

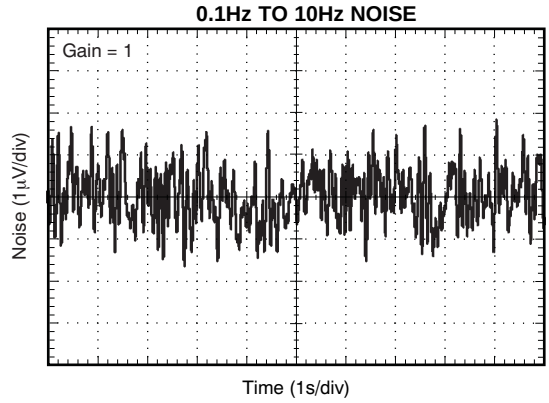


Figure 8.

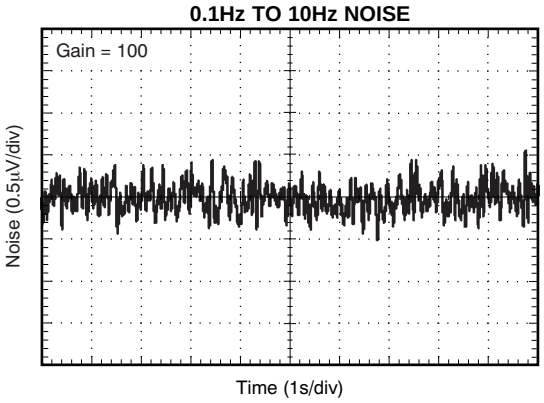


Figure 9.

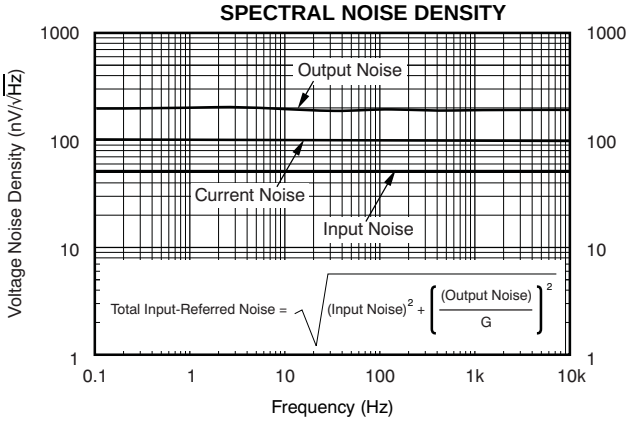


Figure 10.

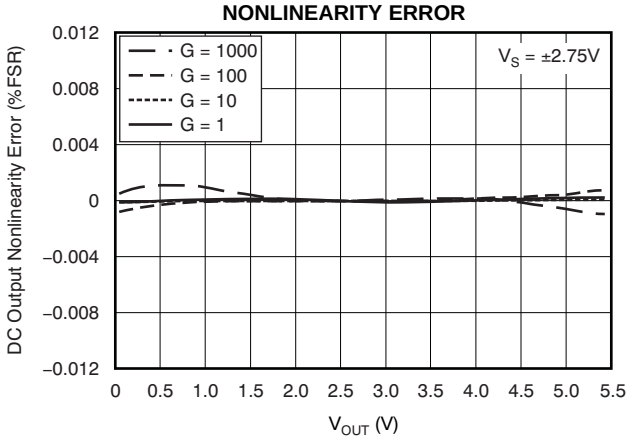


Figure 11.

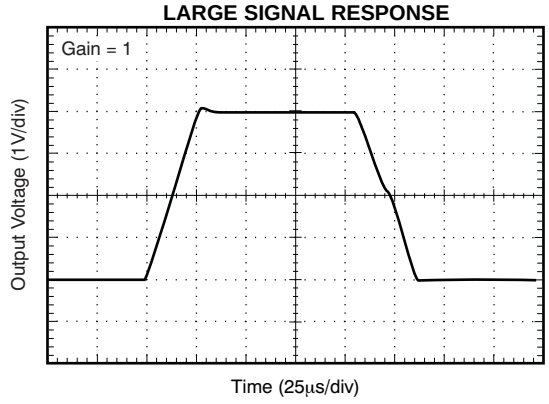


Figure 12.

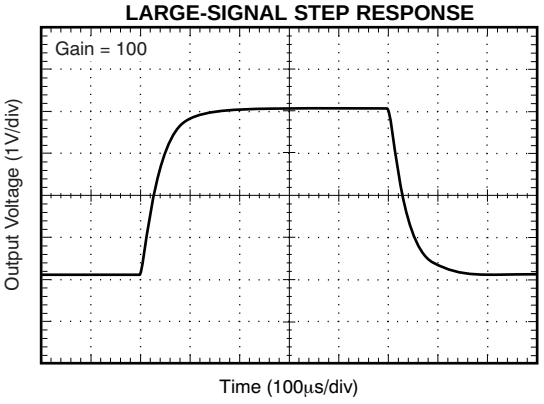


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, R_L = 10kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

SMALL-SIGNAL STEP RESPONSE

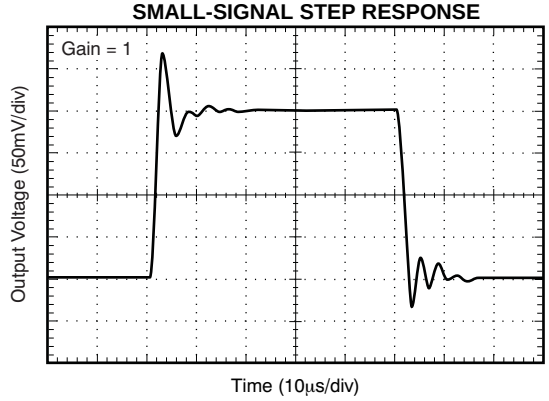


Figure 14.

SMALL-SIGNAL STEP RESPONSE

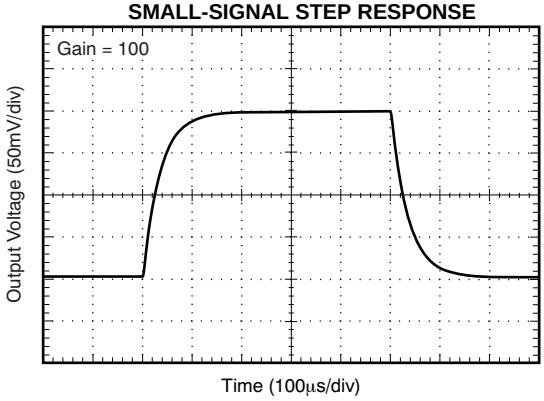


Figure 15.

SETTLING TIME vs GAIN

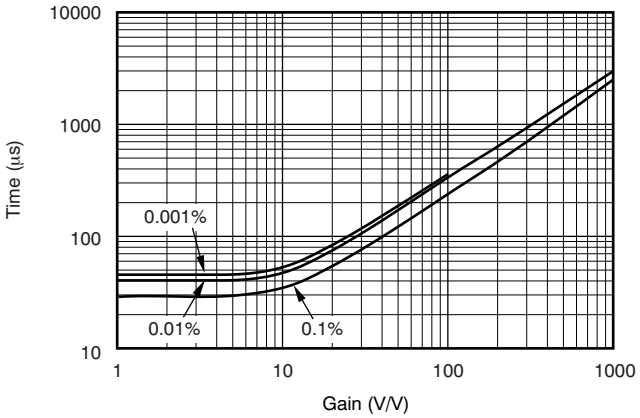


Figure 16.

STARTUP SETTLING TIME

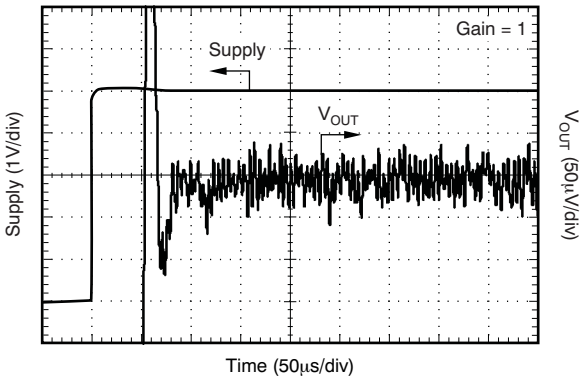


Figure 17.

GAIN vs FREQUENCY

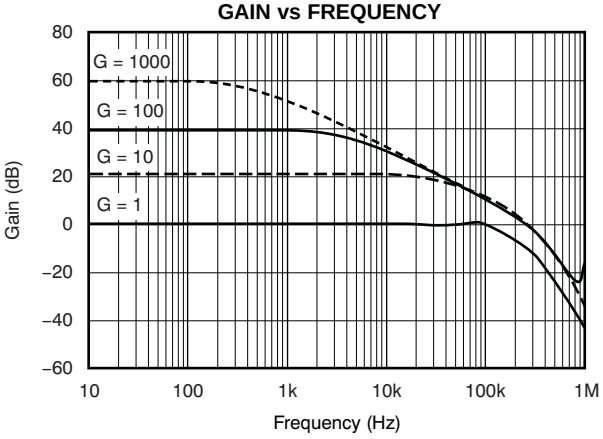


Figure 18.

COMMON-MODE REJECTION RATIO

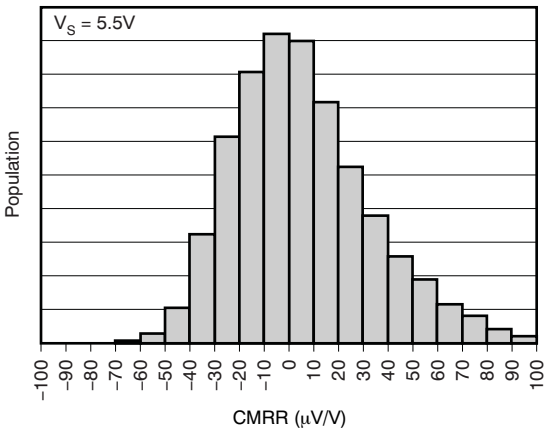


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, R_L = 10kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

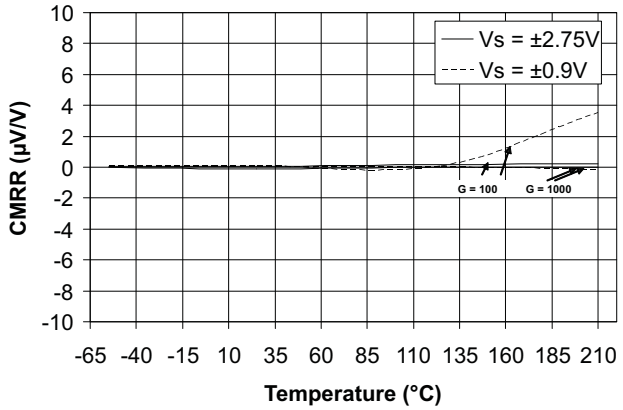


Figure 20.

COMMON-MODE REJECTION RATIO vs FREQUENCY

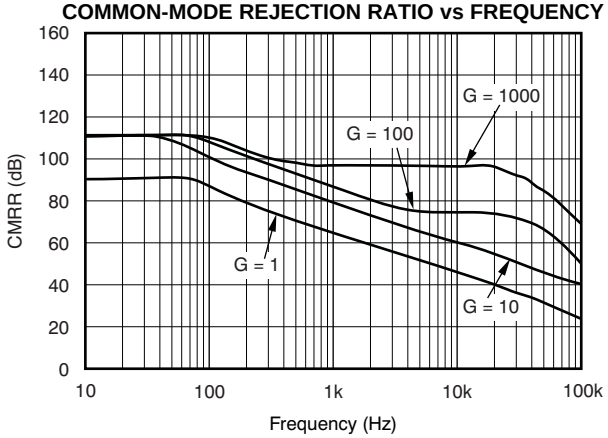


Figure 21.

TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE

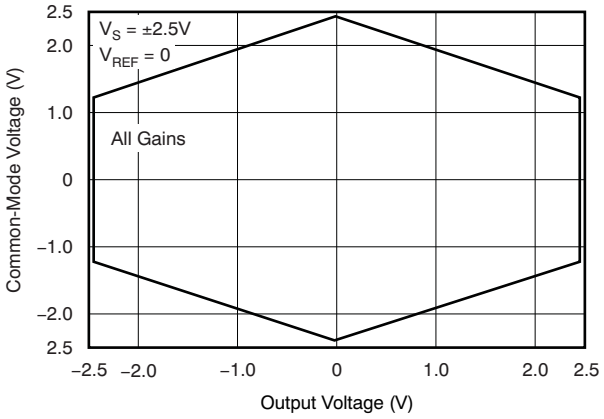


Figure 22.

TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE

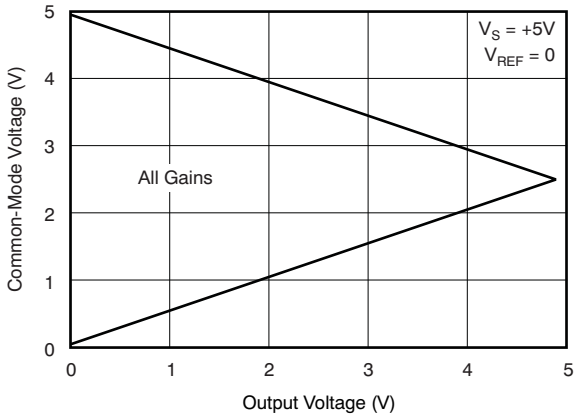


Figure 23.

TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE

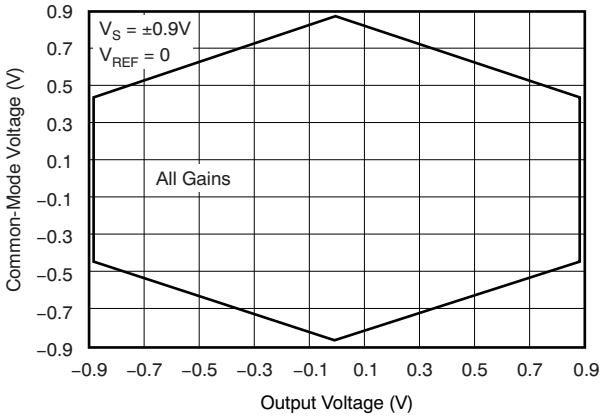


Figure 24.

TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE

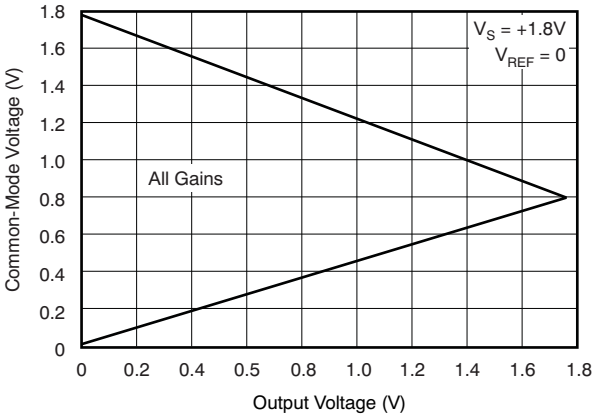


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, R_L = 10kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

POSITIVE POWER-SUPPLY REJECTION RATIO

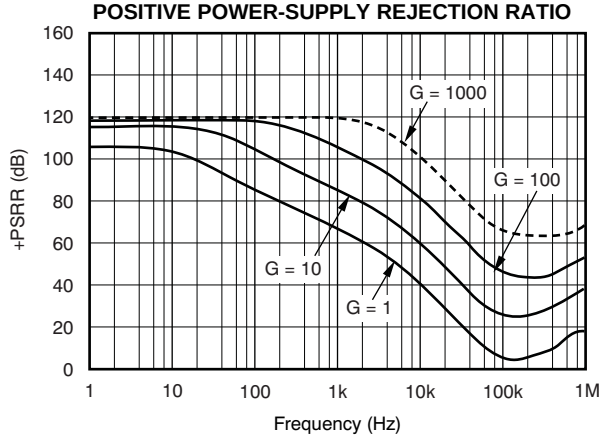


Figure 26.

NEGATIVE POWER-SUPPLY REJECTION RATIO

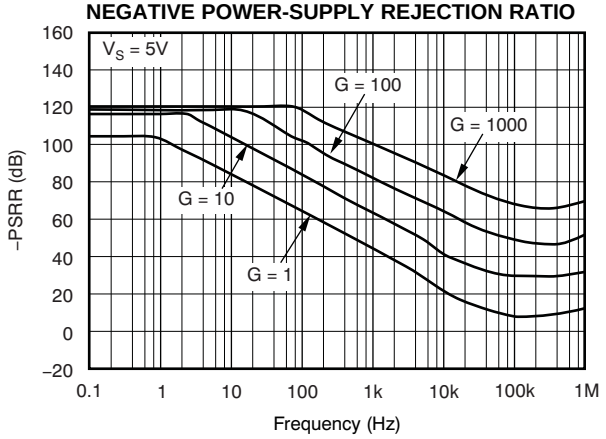


Figure 27.

INPUT BIAS CURRENT vs TEMPERATURE

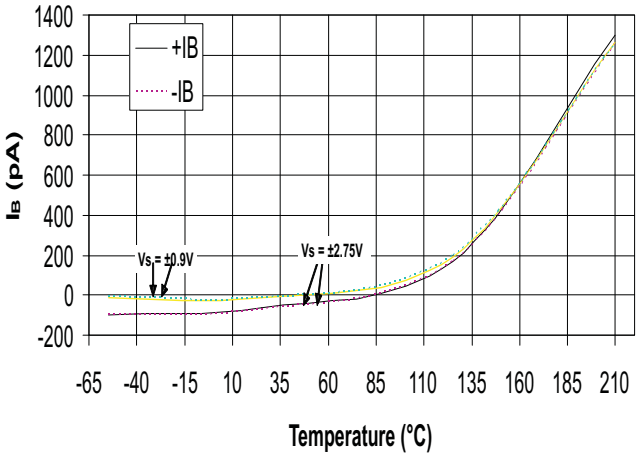


Figure 28.

| INPUT BIAS CURRENT | vs COMMON-MODE VOLTAGE

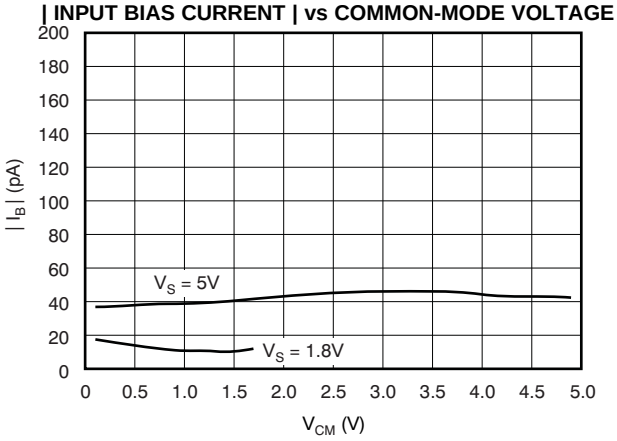


Figure 29.

INPUT OFFSET CURRENT vs TEMPERATURE

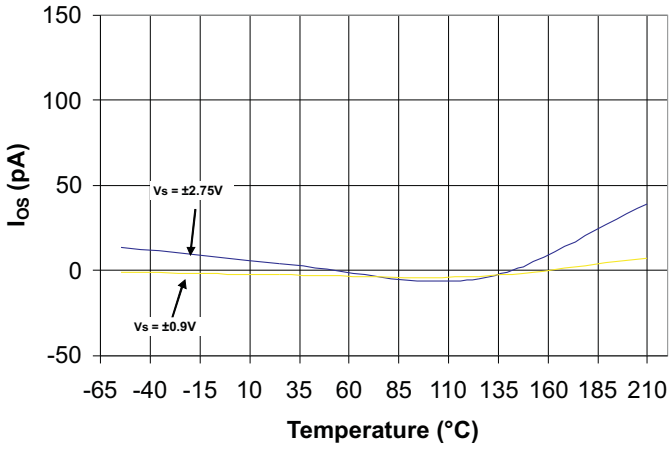


Figure 30.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

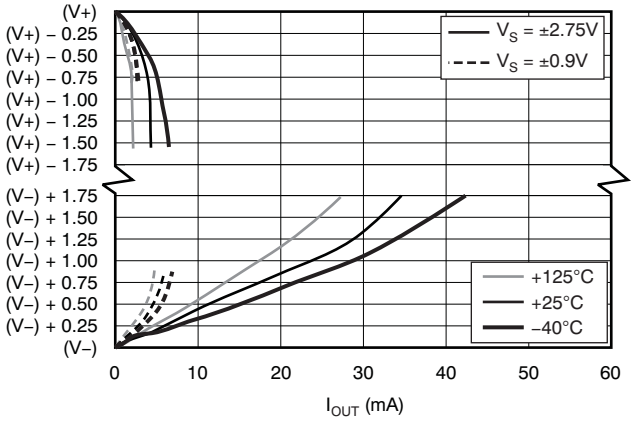


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = 5V, R_L = 10kΩ, V_{REF} = midsupply, and G = 1, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

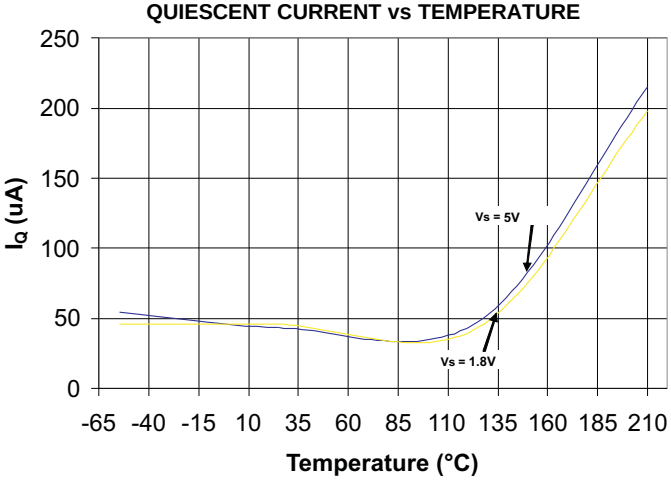


Figure 32.

QUIESCENT CURRENT vs COMMON-MODE VOLTAGE

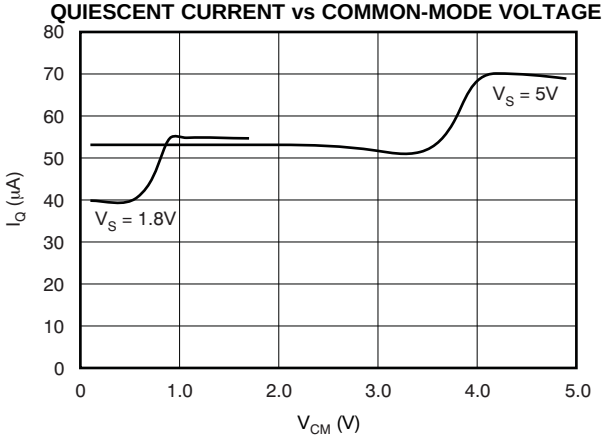


Figure 33.

APPLICATION INFORMATION

Application information below is provided for commercial temperature as a reference and not for high temperature.

It is not recommended to use a gain < 100 for high temperature (210°C) applications. For gains > 100 in such applications, a compensation circuit is needed at pins 1 and 8. The circuit is needed at each pin and consists of a resistor in series with a capacitor referenced to ground. Recommended values for the resistor and capacitor are 3.5 kΩ and 10 nF respectively.

Figure 34 shows the basic connections required for operation of the INA333. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA333 is referred to the output reference (REF) terminal, which is normally grounded. This connection must be low-impedance to assure good common-mode rejection. Although 15 Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

SETTING THE GAIN

Gain of the INA333 is set by a single external resistor, R_G, connected between pins 1 and 8. The value of R_G is selected according to Equation 1:

$$G = 1 + (100\ k\Omega/R_G) \quad (1) \quad (1)$$

Table 2 lists several commonly-used gains and resistor values. The 100 kΩ term in Equation 1 comes from the sum of the two internal feedback resistors of A_1 and A_2. These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA333.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. The contribution of R_G to gain accuracy and drift can be directly inferred from the gain Equation 1. Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at the R_G connections. Careful matching of any parasitics on both R_G pins maintains optimal CMRR over frequency.

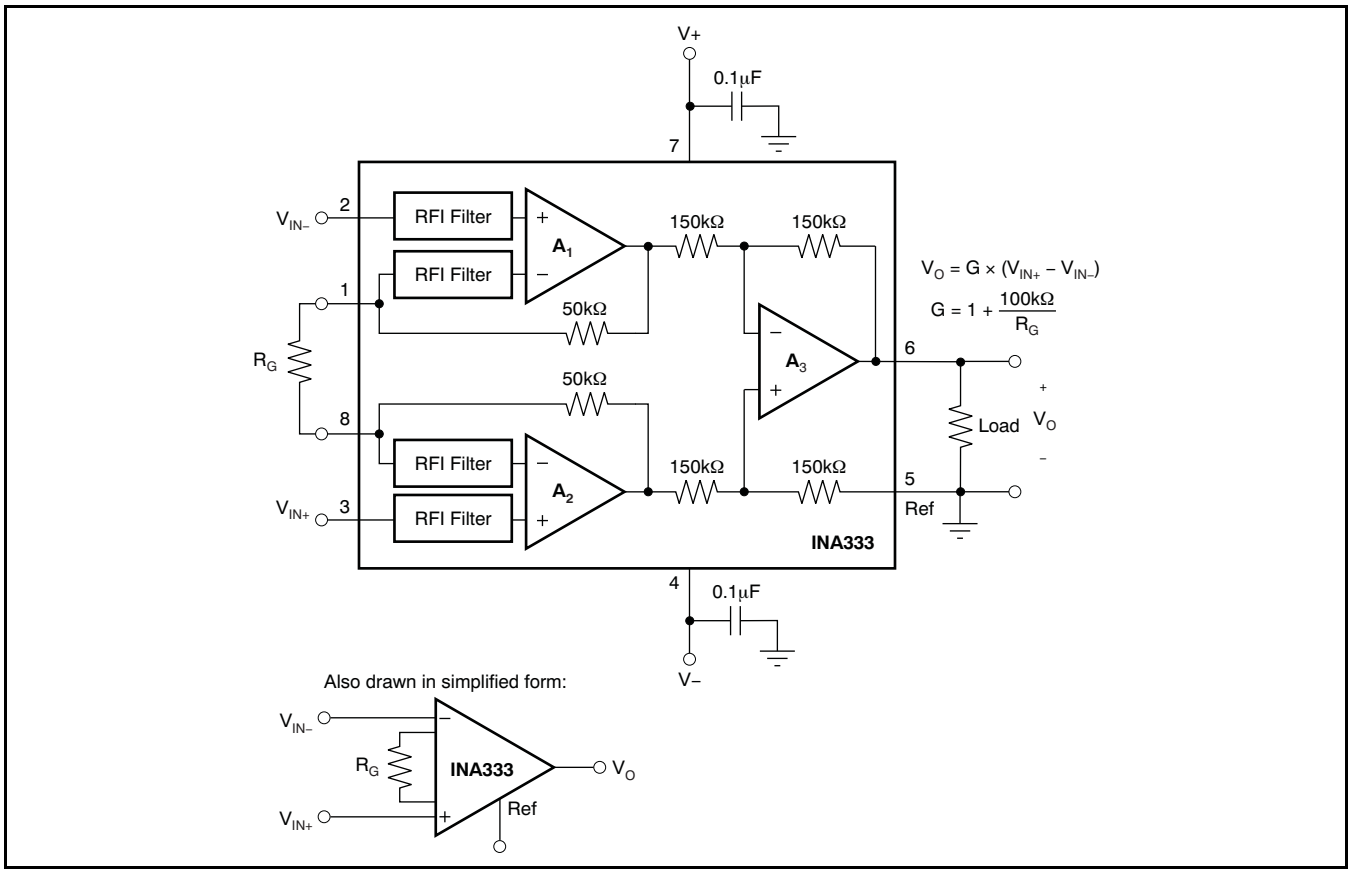


Figure 34. Basic Connections

Table 2. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	NC(1)	NC
2	100k	100k
5	25k	24.9k
10	11.1k	11k
20	5.26k	5.23k
50	2.04k	2.05
100	1.01k	1k
200	502.5	499
500	200.4	200
1000	100.1	100

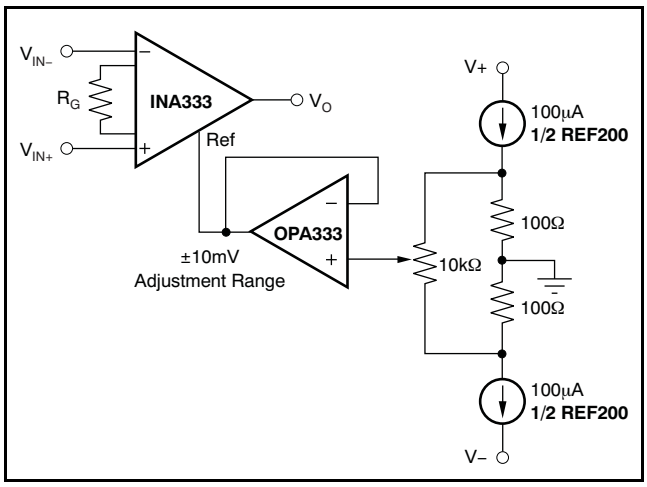
(1) NC denotes no connection. When using the SPICE model, the simulation will not converge unless a resistor is connected to the R_G pins; use a very large resistor value.

INTERNAL OFFSET CORRECTION

The INA333 internal op amps use an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. The amplifier is zero-corrected every 8 µs using a proprietary technique. Upon power-up, the amplifier requires approximately 100 µs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

OFFSET TRIMMING

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF terminal. Figure 35 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF terminal is summed at the output. The op amp buffer provides low impedance at the REF terminal to preserve good common-mode rejection.



(1) REF200 and OPA333 are not tested or characterized at 210°C.

Figure 35. Optional Trimming of Output Offset Voltage

NOISE PERFORMANCE

The auto-calibration technique used by the INA333 results in reduced low frequency noise, typically only 50 nV/√Hz, (G = 100). The spectral noise density can be seen in detail in Figure 10. Low frequency noise of the INA333 is approximately 1 μV_{PP} measured from 0.1 Hz to 10 Hz, (G = 100).

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA333 is extremely high—approximately 100 GΩ. However, a path must be provided for the input bias current of both inputs. This input bias current is typically ±70 pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 36 illustrates various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential that exceeds the common-mode range of the INA333, and the input amplifiers will saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 36). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.

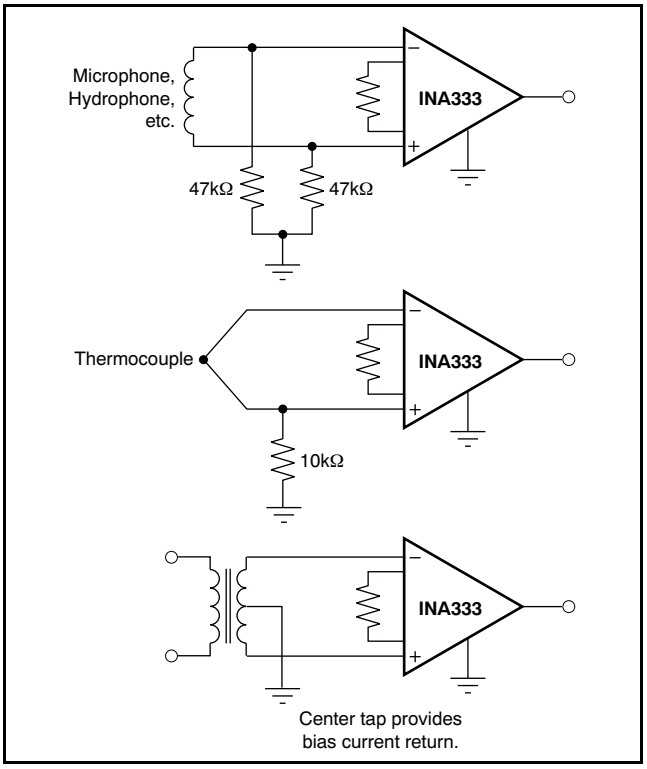


Figure 36. Providing an Input Common-Mode Current Path

INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA333 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers A_1 and A_2. Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see Typical Characteristic curves *Typical Common-Mode Range vs Output Voltage* (Figure 22 to Figure 25).

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333 is near 0 V even though both inputs are overloaded.

OPERATING VOLTAGE

The INA333 operates over a power-supply range of +1.8 V to +5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than +7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

LOW VOLTAGE OPERATION

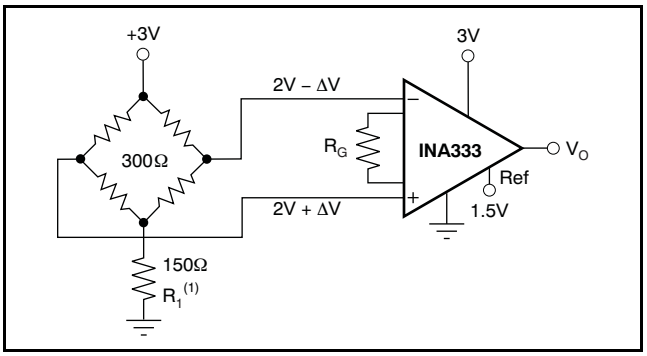
The INA333 can be operated on power supplies as low as ±0.9 V. Most parameters vary only slightly throughout this supply voltage range—see the Typical Characteristics section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The Typical Characteristic curves *Typical Common-Mode Range vs Output Voltage* (Figure 22 to Figure 25) show the range of linear operation for various supply voltages and gains.

SINGLE-SUPPLY OPERATION

The INA333 can be used on single power supplies of +1.8 V to +5.5 V. Figure 37 illustrates a basic single-supply circuit. The output REF terminal is connected to mid-supply. Zero differential input voltage demands an output voltage of mid-supply. Actual output voltage swing is limited to approximately 50 mV above ground, when the load is referred to ground as shown. The typical characteristic curve *Output Voltage Swing vs Output Current* (Figure 31) shows how the output voltage swing varies with output current.

With single-supply operation, V_{IN+} and $V_{IN–}$ must both be 0.1V above ground for linear operation. For instance, the inverting input cannot be connected to ground to measure a voltage connected to the noninverting input.

To illustrate the issues affecting low voltage operation, consider the circuit in Figure 37. It shows the INA333 operating from a single 3-V supply. A resistor in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier inputs.



(1) R_1 creates proper common-mode voltage, only for low-voltage operation—see the *Single-Supply Operation* section.

Figure 37. Single-Supply Bridge Amplifier

INPUT PROTECTION

The input terminals of the INA333 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.3 V, the input signal current should be limited to less than 10 mA to protect the internal clamp diodes. This current limiting can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

GENERAL LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-µF bypass capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

Instrumentation amplifiers vary in the susceptibility to radio-frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The INA333 has been specifically designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the V_{IN+} and $V_{IN–}$ inputs. As a result, the INA333 demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may continue to cause varying offset levels, however, and may require additional shielding.

APPLICATION IDEAS

Additional application ideas are shown in Figure 38 to Figure 41.

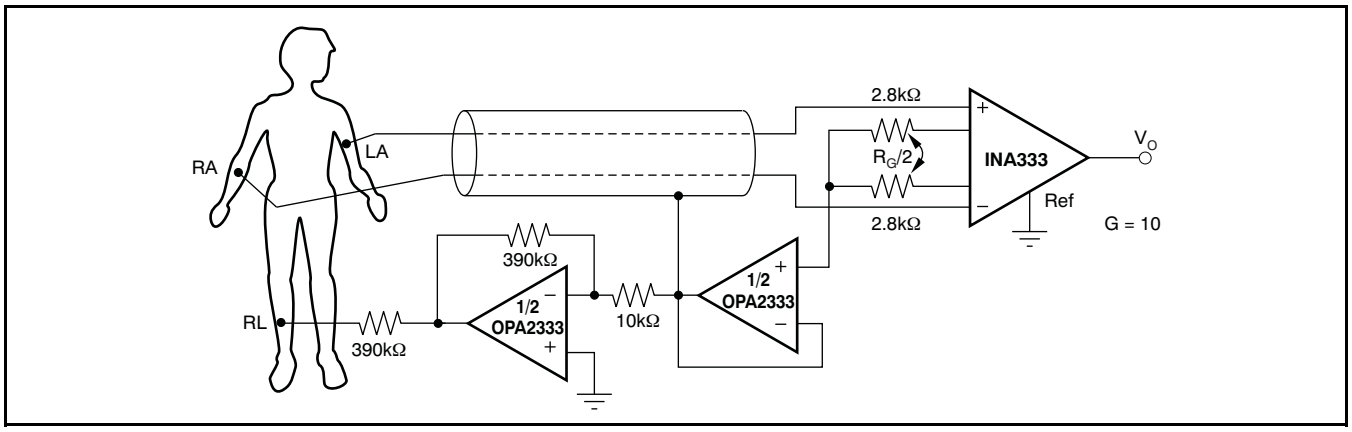
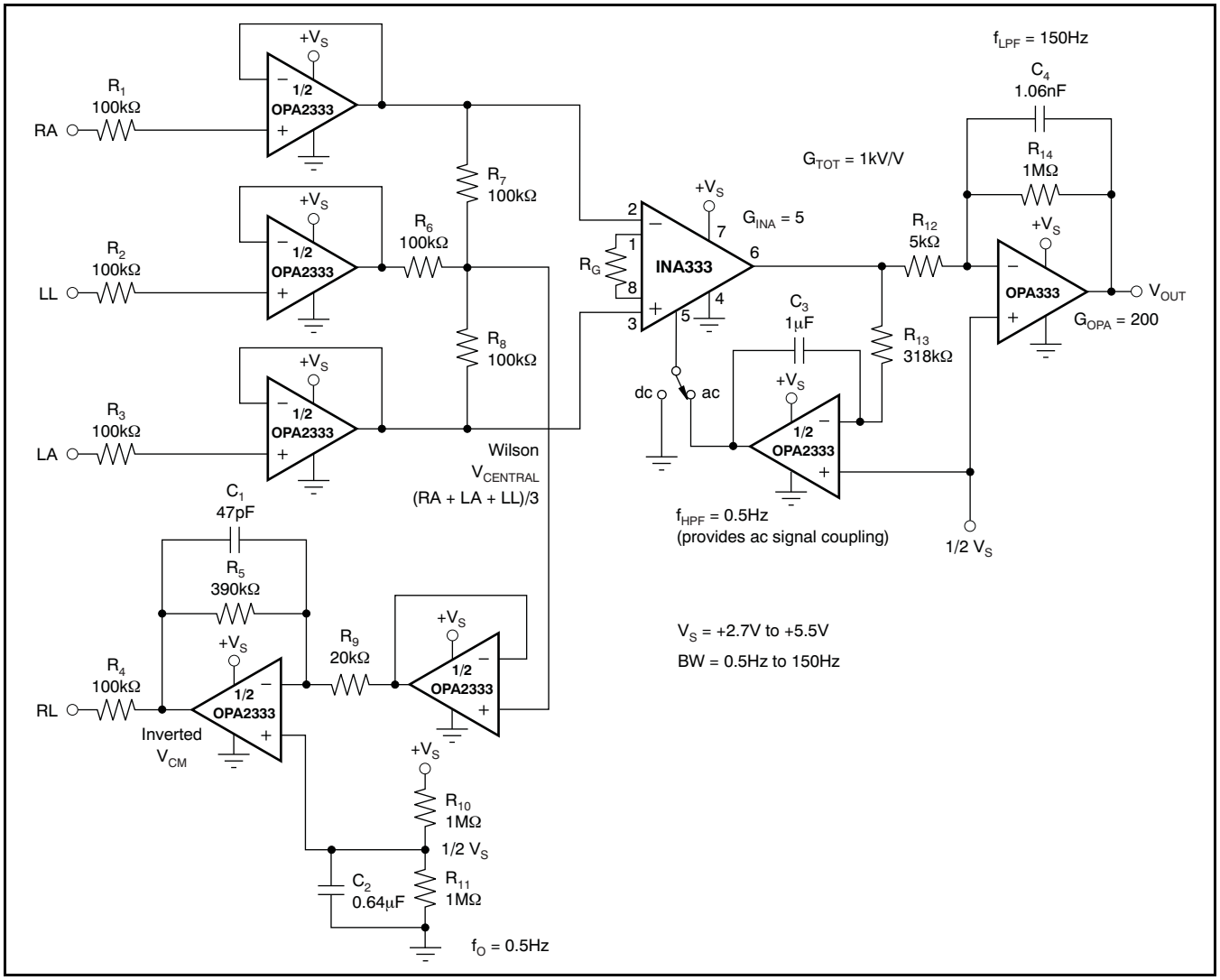


Figure 38. ECG Amplifier With Right-Leg Drive



(1) OPA333 is not tested or characterized at 210°C.

Figure 39. Single-Supply, Very Low Power, ECG Circuit

TINA-TI (FREE DOWNLOAD SOFTWARE)

Using TINA-TI SPICE-Based Analog Simulation Program with the INA333

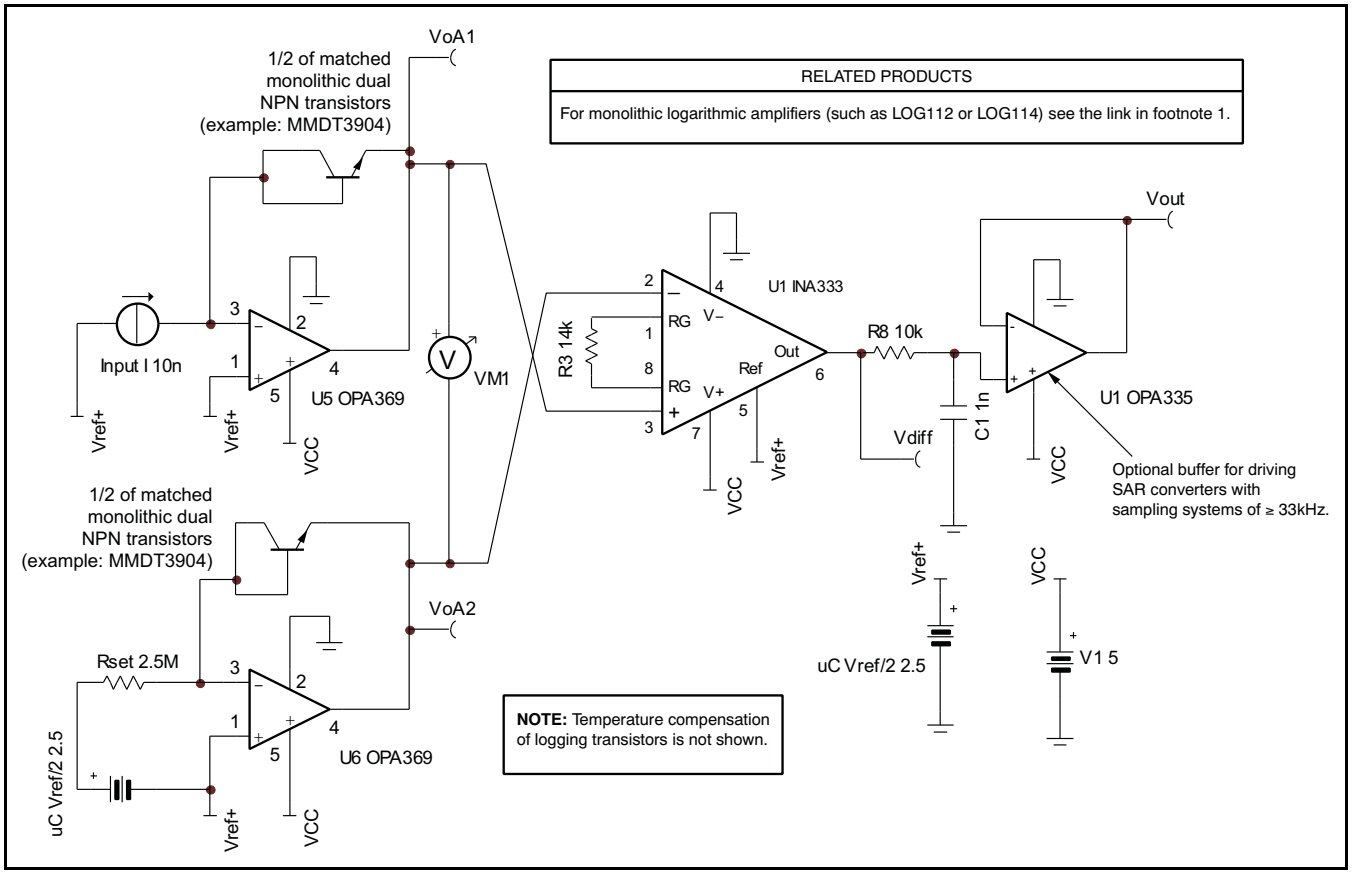
TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. It provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 40 and Figure 41 show example TINA-TI circuits for the INA333 that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

NOTE: these files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

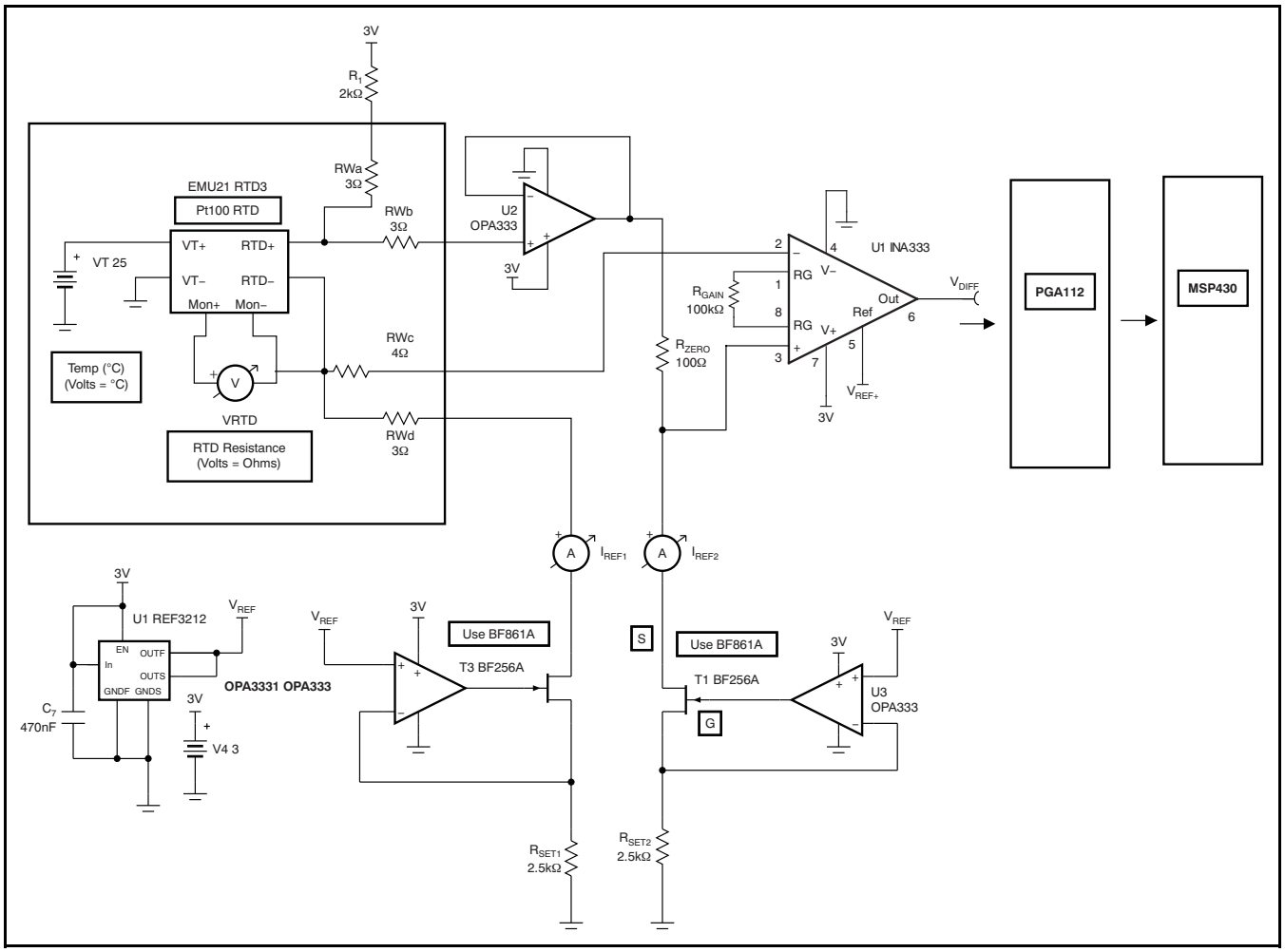


(1) The following link launches the TI logarithmic amplifiers web page: Logarithmic Amplifier Products Home Page

(2) OPA369 and OPA335 are not characterized at 210°C.

Figure 40. Low-Power Log Function Circuit for Portable Battery-Powered Systems (Example Glucose Meter)

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: Log Circuit.



(1) RWa, RWb, RWc, and RWd simulate wire resistance. These resistors are included to show the four-wire sense technique immunity to line mismatches. This method assumes the use of a four-wire RTD.

(2) In this diagram, only INA333 is tested and characterized at 210°C.

Figure 41. Four-Wire, 3V Conditioner for a PT100 RTD With Programmable Gain Acquisition System

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: PT100 RTD.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA333SHKJ	ACTIVE	CFP	HKJ	8	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210	INA333S HKJ	Samples
INA333SHKQ	ACTIVE	CFP	HKQ	8	25	RoHS & Green	AU	N / A for Pkg Type	-55 to 210	INA333S HKQ	Samples
INA333SJD	ACTIVE	CDIP SB	JD	8	45	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210	INA333SJD	Samples
INA333SKGD1	ACTIVE	XCEPT	KGD	0	240	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210		Samples
INA333SKGD2	ACTIVE	XCEPT	KGD	0	10	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

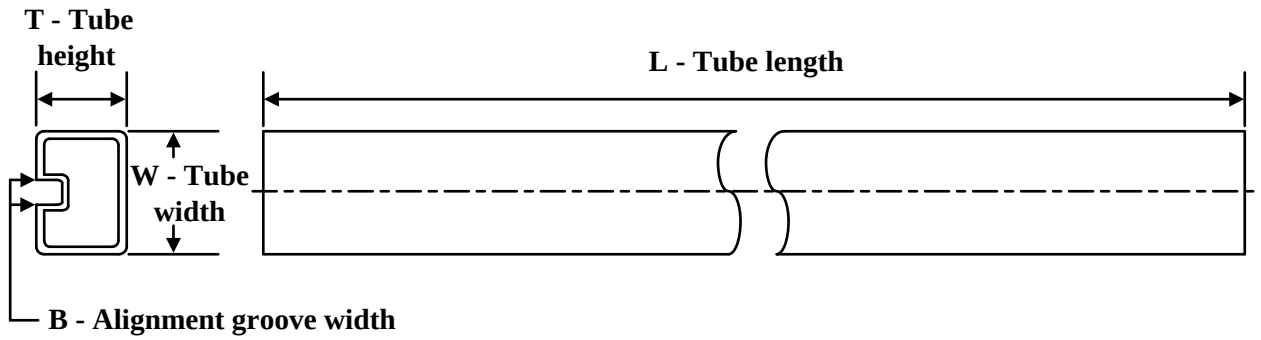
OTHER QUALIFIED VERSIONS OF INA333-HT :

- Catalog : INA333
- Automotive : INA333-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

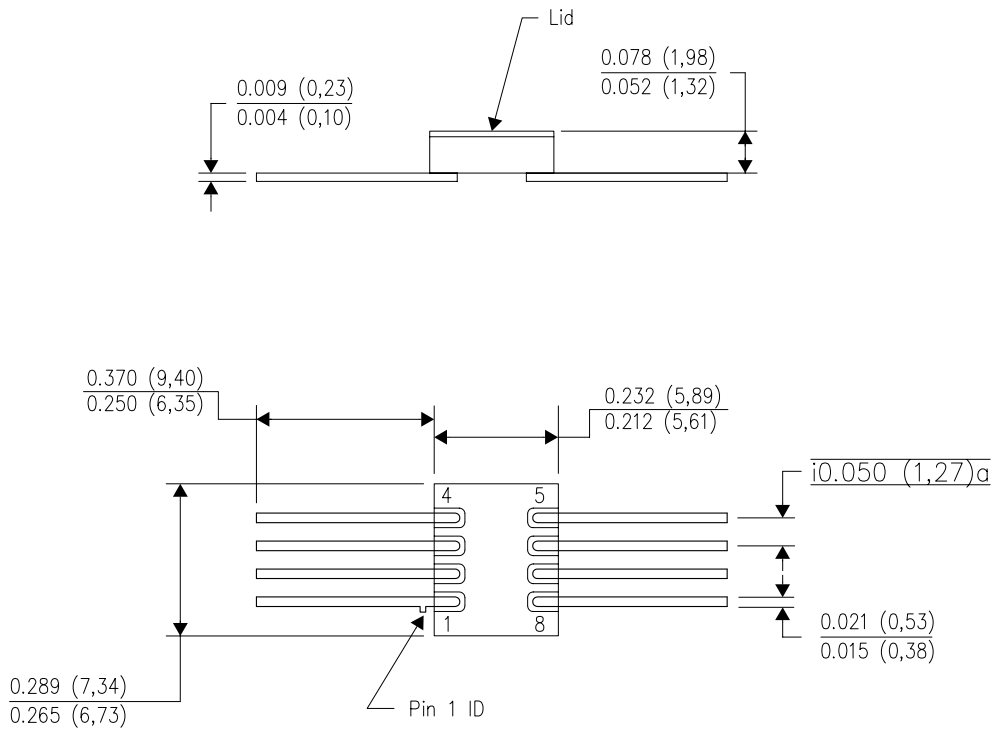
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
INA333SHKJ	HKJ	CFP	8	25	506.98	26.16	6220	NA
INA333SHKQ	HKQ	CFP	8	25	506.98	26.16	6220	NA
INA333SJD	JD	CDIP SB	8	45	506.98	15.24	12290	NA

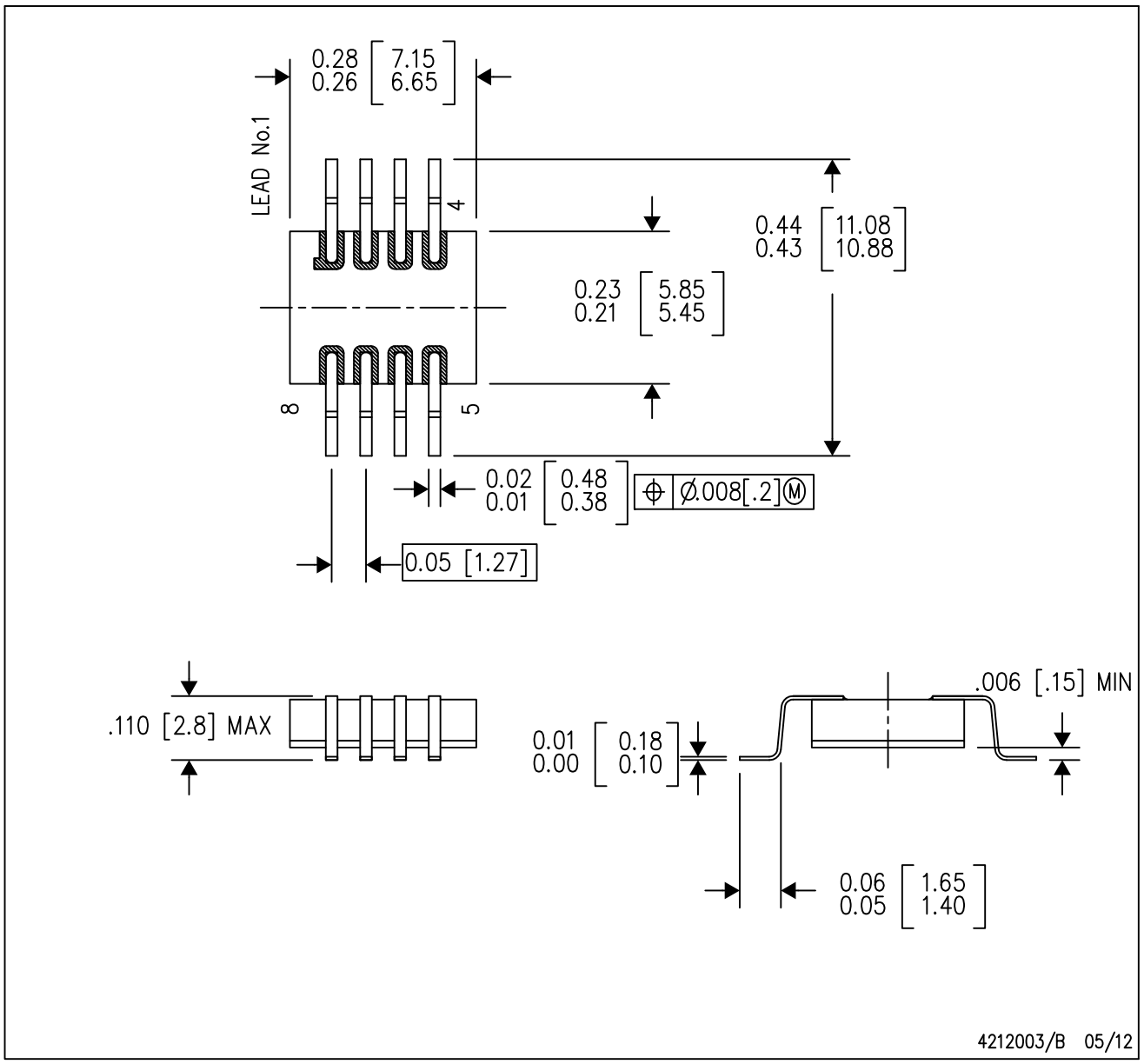
HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



4209892/A 10/08

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

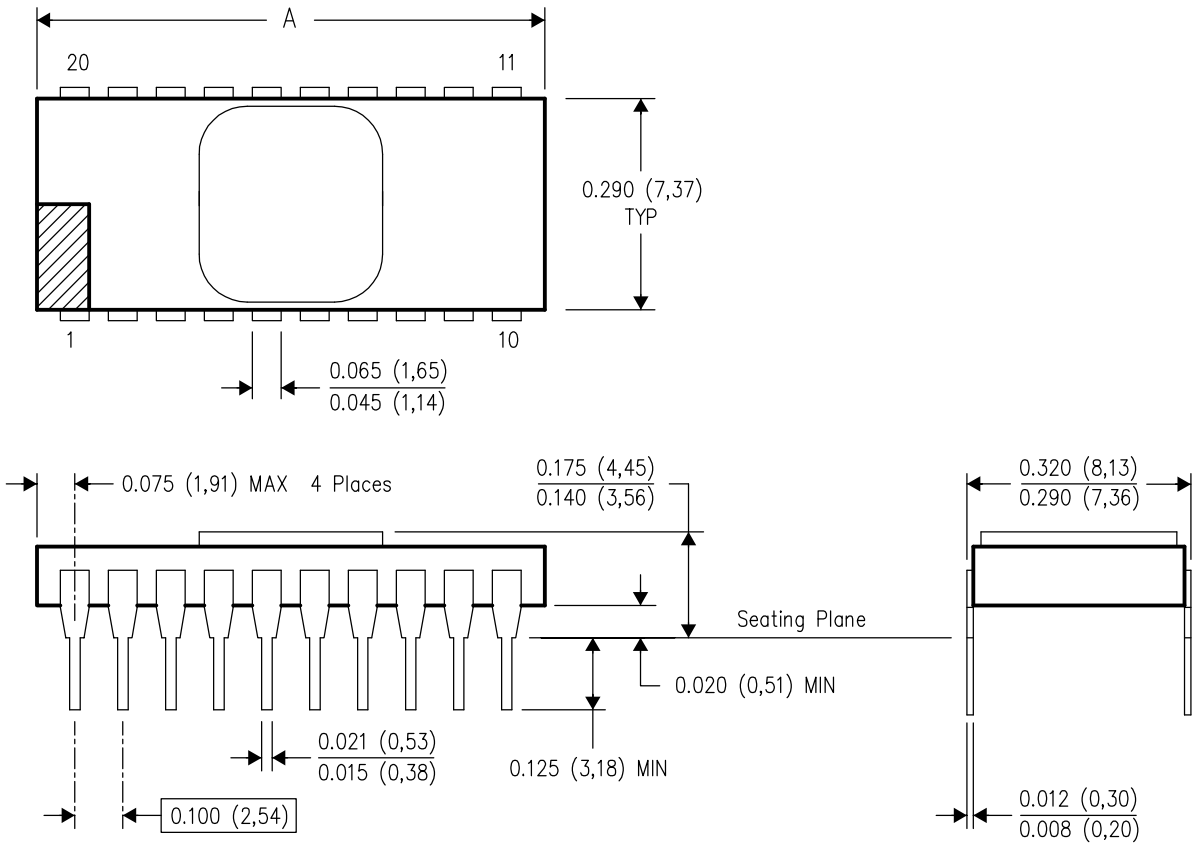
HKQ (R–CDFP–G8) CERAMIC GULL WING



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Lid is not connected to any lead.

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN



DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

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