ISO724x High-Speed, Quad-Channel Digital Isolators

1 Features

- 25 and 150Mbps Signaling Rate Options
  - Low Channel-to-Channel Output Skew; 1ns Maximum
  - Low Pulse-Width Distortion (PWD); 2ns Maximum
  - Low Jitter Content; 1ns Typ at 150Mbps
- Selectable Default Output (ISO7240CF)
- > 25-Year Life at Rated Working Voltage (see Isolation Lifetime Projection)
- 4-kV ESD Protection
- Operates With 3.3V or 5V Supplies
- High Electromagnetic Immunity (see *ISO72x Digital Isolator Magnetic-Field Immunity*)
- –40°C to +125°C Operating Temperature Range
- Safety-Related Certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 61010-1, IEC 62368-1 certifications

2 Applications

- Factory Automation
  - Modbus
  - Profibus™
  - DeviceNet™ Data Buses
- Computer Peripheral Interface
- Servo Control Interface
- Data Acquisition

3 Description

The ISO7240x, ISO7241x, and ISO7242x devices are quad-channel digital isolators with multiple channel configurations and output-enable functions. These devices have logic-input and logic-output buffers separated by Texas Instrument's silicon-dioxide (SiO_2) isolation barrier. Used in conjunction with isolated power supplies, these devices help block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7240x family of devices has all four channels in the same direction. The ISO7241x family of devices has three channels in the same direction and one channel in the opposition direction. The ISO7242x family of devices has two channels in each direction.

The devices with the C suffix (C option) have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device. The devices with the M suffix (M option) have CMOS $V_{CC}/2$ input thresholds and do not have the input noise filter or the additional propagation delay.

The ISO7240CF device has an input disable function on pin 7, and a selectable high or low failsafe-output function with the CTRL pin (pin 10). The failsafe output is a logic high when a logic high is placed on the CTRL pin or the pin is left unconnected. If a logic low signal is applied to the CTRL pin, the failsafe output becomes a logic-low output state. The input disable function of the ISO7240CF device prevents data from being passed across the isolation barrier to the output. When the inputs are disabled or V_{CC1} is powered down, the outputs are set by the CTRL pin.

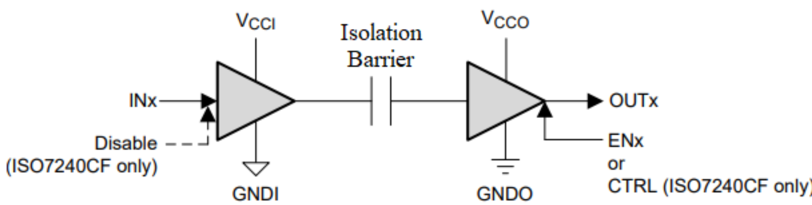
These devices can be powered from 3.3V or 5V supplies on either side, in any combination. The signal input pins are 5V tolerant regardless of the voltage supply level that is used.

These devices are characterized for operation over the ambient temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)	PACKAGE SIZE(2)
ISO7240CF	DW (SOIC, 16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO7240C			
ISO7240M			
ISO7241C			
ISO7241M			
ISO7242C			
ISO7242M			

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



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V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

V_{CCO} and GNDO are supply and ground connections respectively for the output channels.

Simplified Schematic

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4 Pin Configurations and Functions

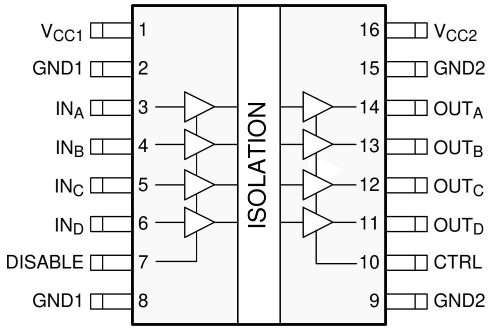


Figure 4-1. ISO7240CF DW Package 16-Pin SOIC Top View

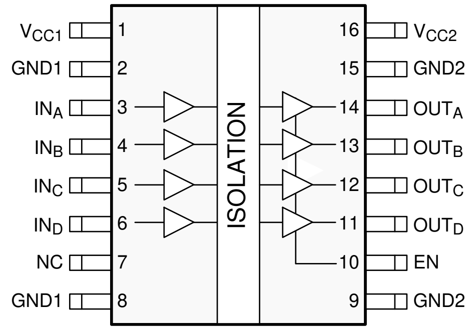


Figure 4-2. ISO7240C and ISO7240M DW Package 16-Pin SOIC Top View

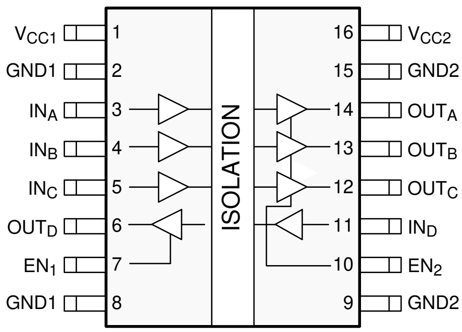


Figure 4-3. ISO7241C and ISO7241M DW Package 16-Pin SOIC Top View

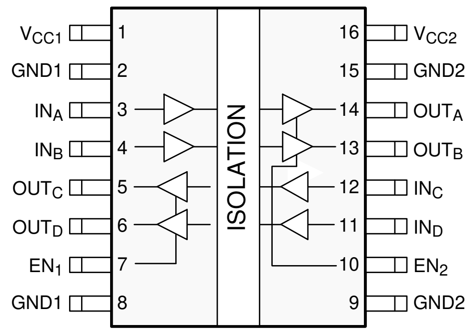


Figure 4-4. ISO7242C and ISO7242M DW Package 16-Pin SOIC Top View

Table 4-1. Pin Functions

PIN					Type[(1)]	DESCRIPTION3
NAME	NO.					
	ISO7240CF	ISO7240C ISO7240M	ISO7241C ISO7241M	ISO7242C ISO7242M		
CTRL	10	—	—	—	I	Failsafe output control. Output state is determined by CTRL pin when DISABLE is high or V_{CC1} is powered down. Output is high when CTRL is high or open and low when CTRL is low.
DISABLE	7	—	—	—	I	Input disable. All input pins are disabled when DISABLE is high and enabled when DISABLE is low or open.
EN	—	10	—	—	I	Output enable. All output pins are enabled when EN is high or open and disabled when EN is low.
EN_1	—	—	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN_1 is high or open and disabled when EN_1 is low.
EN_2	—	—	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN_2 is high or open and disabled when EN_2 is low.
GND1	2, 8	2, 8	2, 8	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	9, 15	9, 15	9, 15	—	Ground connection for V_{CC2}
IN_A	3	3	3	3	I	Input, channel A
IN_B	4	4	4	4	I	Input, channel B
IN_C	5	5	5	12	I	Input, channel C
IN_D	6	6	11	11	I	Input, channel D
NC	—	7	—	—	—	No Connect pins are floating with no internal connection
OUT_A	14	14	14	14	O	Output, channel A
OUT_B	13	13	13	13	O	Output, channel B
OUT_C	12	12	12	5	O	Output, channel C
OUT_D	11	11	6	6	O	Output, channel D
V_{CC1}	1	1	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	16	16	—	Power supply, V_{CC2}

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

See [(1)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage[(2)], V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at IN, OUT, EN, DISABLE, CTRL	–0.5	V_{CC} + 0.5[(3)]	V
I_O	Output current	–15	15	mA
T_J	Maximum junction temperature		170	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage[(2)], V_{CC1}, V_{CC2}		3.15		5.5	V
I_{OH}	High-level output current		–4			mA
I_{OL}	Low-level output current				4	mA
t_{ui}	Input pulse width	ISO724xC	40			ns
		ISO724xM	6.67	5		
$1/t_{ui}$	Signaling rate	ISO724xC	0	30[(1)]	25	Mbps
		ISO724xM	0	200[(1)]	150	
V_{IH}	High-level input voltage (IN)	ISO724xM	0.7 x V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage (IN)		0		0.3 x V_{CC}	V
V_{IH}	High-level input voltage (IN, DISABLE, CTRL, EN on all devices)	ISO724xC	2		5.5	V
V_{IL}	Low-level input voltage (IN, DISABLE, CTRL, EN on all devices)		0		0.8	V
T_J	Junction temperature				150	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification				1000	A/m

(1) Typical value at room temperature and well-regulated power supply.
(2) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.4 Thermal Information

THERMAL METRIC[1]			ISO724xx DW (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K board	168	°C/W
		High-K board	68.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		33.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		33.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter		14.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter		32.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Power Ratings

$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$C, $C_L = 15$ pF, Input a 50% duty cycle 25-Mbps square wave (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation				220	mW

5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0884-17); IEC 60112	≥ 400	V
	Material group		II	
	Overvoltage Category	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17):[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge[3]	Method a: After I/O safety test subgroup 2/3. $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10$ s,	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.3 \times V_{IORM}$, $t_m = 10$ s,	≤5	
		Method b1: At routine test (100% production) $V_{ini} = V_{IOTM}$, $t_{ini} = 1$ s; $V_{pd(m)} = 1.5 \times V_{IORM}$, $t_m = 1$ s,	≤5	
C_{IO}	Barrier capacitance, input to output[4]	$V_I = 0.4\ \sin(2\pi ft)$, f = 1 MHz	2	pF
R_{IO}	Isolation resistance, input to output[4]	$V_{IO} = 500$ V, $T_A = 25°C$	> 10^{12}	Ω
		$V_{IO} = 500$ V, 100°C ≤ T_A ≤ 125°C	>10^{11}	
		$V_{IO} = 500$ V at $T_S = 150°C$	>10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 2500\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 3000\ V_{RMS}$, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of

the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

(3) Apparent charge is electrical discharge caused by a partial discharge (pd).

(4) All pins on each side of the barrier tied together creating a two-terminal device

5.7 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Certificate planned	Certificate planned	Certificate planned

5.8 Safety Limiting Values

Safety limiting[(1)] intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 168°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see Figure 5-2			156	mA
		$R_{\theta JA}$ = 168°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see Figure 5-2			239	
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel		0		μA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 6-1	V_{CCO} – 0.8			V
		I_{OH} = –20 μA, See Figure 6-1	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1			0.4	V
		I_{OL} = 20 μA, See Figure 6-1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN at V_{CCI}			10	μA
I_{IL}	Low-level input current	IN at 0 V	–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f=2MHz		2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-5	25	50		kV/μs

5.10 Supply Current Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7240C/M							
I_{CC1}	Supply current, side 1	Quiescent, All channels, no load, EN at 3 V, V_I = V_{CC} or 0 V			1	3	mA
		25 Mbps, All channels, no load, EN at 3 V, 12.5-MHz input-clock signal			7	10.5	
I_{CC2}	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		15	22	mA
			25 Mbps, 12.5-MHz input-clock signal		17	25	
ISO7241C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6.5	11	mA
			25 Mbps, 12.5-MHz input-clock signal		12	18	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		13	20	mA
			25 Mbps, 12.5-MHz input-clock signal		18	28	
ISO7242C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		10	16	mA
			25 Mbps, 12.5-MHz input-clock signal		15	24	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		10	16	mA
			25 Mbps, 12.5-MHz input-clock signal		15	24	

5.11 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel			0		μA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 6-1	3.3-V side	V_{CCO} – 0.4			V
			5-V side	V_{CCO} – 0.8			
		I_{OH} = –20 μA, See Figure 6-1		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1				0.4	V
		I_{OL} = 20 μA, See Figure 6-1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current	IN at V_{CCI}				10	μA
I_{IL}	Low-level input current	IN at 0 V		–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f=2MHz			2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-5		25	50		kV/μs

5.12 Supply Current Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7240C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		1	3	mA
			25 Mbps, 12.5-MHz input-clock signal		7	10.5	
I_{CC2}	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		9.5	15	mA
			25 Mbps, 12.5-MHz input-clock signal		10.5	17	
ISO7241C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6.5	11	mA
			12.5-MHz input-clock signal		12	18	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		8	13	mA
			25 Mbps, 12.5-MHz input-clock signal		11.5	18	
ISO7242C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		10	16	mA
			12.5-MHz input-clock signal		15	24	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6	10	mA
			25 Mbps, 12.5-MHz input-clock signal		9	14	

5.13 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OFF}	Sleep mode output current	EN at 0 V, Single channel			0		μA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 6-1	3.3-V side	V_{CCO} – 0.4			V
			5-V side	V_{CCO} – 0.8			
		I_{OH} = –20 μA, See Figure 6-1		V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1				0.4	V
		I_{OL} = 20 μA, See Figure 6-1				0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current	IN at V_{CCI}				10	μA
I_{IL}	Low-level input current	IN at 0 V		–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f=2MHz			2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-5		25	50		kV/μs

5.14 Supply Current Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V. For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7240C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		0.5	1.2	mA
			25 Mbps, 12.5-MHz input-clock signal		3	5	
I_{CC2}	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		15	22	mA
			25 Mbps, 12.5-MHz input-clock signal		17	25	
ISO7241C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		4	7	mA
			25 Mbps, 12.5-MHz input-clock signal		6.5	11	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		13	20	mA
			25 Mbps, 12.5-MHz input-clock signal		18	28	
ISO7242C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6	10	mA
			25 Mbps, 12.5-MHz input-clock signal		9	14	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		10	16	mA
			25 Mbps, 12.5-MHz input-clock signal		15	24	

5.15 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OFF}	Sleep mode output current	EN at 0 V, single channel		0		μA
V_{OH}	High-level output voltage	I_{OH} = –4 mA, See Figure 6-1	V_{CCO} – 0.4			V
		I_{OH} = –20 μA, See Figure 6-1	V_{CCO} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, See Figure 6-1			0.4	V
		I_{OL} = 20 μA, See Figure 6-1			0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
I_{IH}	High-level input current	IN at V_{CCI}			10	μA
I_{IL}	Low-level input current	IN at 0 V	–10			
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (2πft), f=2MHz		2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V, See Figure 6-5	25	50		kV/μs

5.16 Supply Current Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

For the 3.3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V. Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ISO7240C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		0.5	1.2	mA
			25 Mbps, 12.5-MHz input-clock signal		3	5	
I_{CC2}	Supply current, side 2	All channels, no load, EN at 3 V	Quiescent, V_I = V_{CC} or 0 V		9.5	15	mA
			25 Mbps, 12.5-MHz input-clock signal		10.5	17	
ISO7241C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		4	7	mA
			25 Mbps, 12.5-MHz input-clock signal		6.5	11	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		8	13	mA
			25 Mbps, 12.5-MHz input-clock signal		11.5	18	
ISO7242C/M							
I_{CC1}	Supply current, side 1	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6	10	mA
			25 Mbps, 12.5-MHz input-clock signal		9	14	
I_{CC2}	Supply current, side 2	All channels, no load, EN_1 at 3 V, EN_2 at 3 V	Quiescent, V_I = V_{CC} or 0 V		6	10	mA
			25 Mbps, 12.5-MHz input-clock signal		9	14	

5.17 Switching Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 6-1	18		42	ns
PWD	Pulse-width distortion[1] $\|t_{PHL} – t_{PLH}\|$	ISO724xC	See Figure 6-1			2.5	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 6-1	8		23	ns
PWD	Pulse-width distortion[1] $\|t_{PHL} – t_{PLH}\|$	ISO724xM	See Figure 6-1		1	2	ns
$t_{sk(pp)}$	Part-to-part skew [2]	ISO724xC				8	ns
$t_{sk(pp)}$	Part-to-part skew [2]	ISO724xM			0	3	ns
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO724xC				2	ns
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 6-1		2.4		ns
t_f	Output signal fall time		See Figure 6-1		2.3		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 6-2		15	25	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 6-2		15	25	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 6-2		15	25	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 6-3		12		μs
t_{wake}	Wake time from input disable		See Figure 6-4		15		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See Figure 6-6		1		ns

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.18 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 6-1	20		50	ns
PWD	Pulse-width distortion [1] $\|t_{PHL} – t_{PLH}\|$	ISO724xC	See Figure 6-1			3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 6-1	8		29	ns
PWD	Pulse-width distortion [1] $\|t_{PHL} – t_{PLH}\|$	ISO724xM	See Figure 6-1		1	2	ns
$t_{sk(pp)}$	Part-to-part skew [2]	ISO724xC				10	ns
$t_{sk(pp)}$	Part-to-part skew [2]	ISO724xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO724xC				3	ns
$t_{sk(o)}$	Channel-to-channel output skew [3]	ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 6-1		2.4		ns
t_f	Output signal fall time		See Figure 6-1		2.3		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 6-2		15	25	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 6-2		15	25	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 6-2		15	25	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 6-3		18		μs
t_{wake}	Wake time from input disable		See Figure 6-4		15		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, Same polarity input on all channels, See Figure 6-6		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.19 Switching Characteristics: V_{CC1} at 3.3-V and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 6-1	22		51	ns
PWD	Pulse-width distortion[(1)] $\|t_{PHL} – t_{PLH}\|$	ISO724xC	See Figure 6-1			3	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 6-1	8		30	ns
PWD	Pulse-width distortion[(1)] $\|t_{PHL} – t_{PLH}\|$	ISO724xM	See Figure 6-1		1	2	ns
$t_{sk(pp)}$	Part-to-part skew [(2)]	ISO724xC				10	ns
$t_{sk(pp)}$	Part-to-part skew [(2)]	ISO724xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew [(3)]	ISO724xC				2.5	ns
$t_{sk(o)}$	Channel-to-channel output skew [(3)]	ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 6-1		2.4		ns
t_f	Output signal fall time		See Figure 6-1		2.3		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 6-2		15	25	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 6-2		15	25	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 6-2		15	25	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 6-3		12		μs
t_{wake}	Wake time from input disable		See Figure 6-4		15		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps NRZ data input, Same polarity input on all channels, See Figure 6-6		1		ns

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.20 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	ISO724xC	See Figure 6-1	25		56	ns
PWD	Pulse-width distortion $\|t_{PHL} – t_{PLH}\|$[(1)]	ISO724xC	See Figure 6-1			4	ns
t_{PLH}, t_{PHL}	Propagation delay	ISO724xM	See Figure 6-1	8		34	ns
PWD	Pulse-width distortion $\|t_{PHL} – t_{PLH}\|$[(1)]	ISO724xM	See Figure 6-1		1	2	ns
$t_{sk(pp)}$	Part-to-part skew [(2)]	ISO724xC				10	ns
$t_{sk(pp)}$	Part-to-part skew [(2)]	ISO724xM			0	5	ns
$t_{sk(o)}$	Channel-to-channel output skew [(3)]	ISO724xC				3.5	ns
$t_{sk(o)}$	Channel-to-channel output skew [(3)]	ISO724xM			0	1	ns
t_r	Output signal rise time		See Figure 6-1		2.4		ns
t_f	Output signal fall time		See Figure 6-1		2.3		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output		See Figure 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output		See Figure 6-2		15	25	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output		See Figure 6-2		15	25	ns
t_{PZL}	Propagation delay, high-impedance-to-low-level output		See Figure 6-2		15	25	ns
t_{fs}	Failsafe output delay time from input power loss		See Figure 6-3		18		μs
t_{wake}	Wake time from input disable		See Figure 6-4		15		μs
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO724xM	150 Mbps PRBS NRZ data input, same polarity input on all channels, See Figure 6-6		1		ns

(1) Also referred to as pulse skew.

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.21 Insulation Characteristics Curves

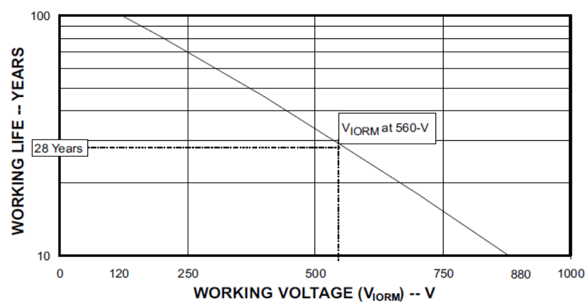


Figure 5-1. Isolation Lifetime Projection

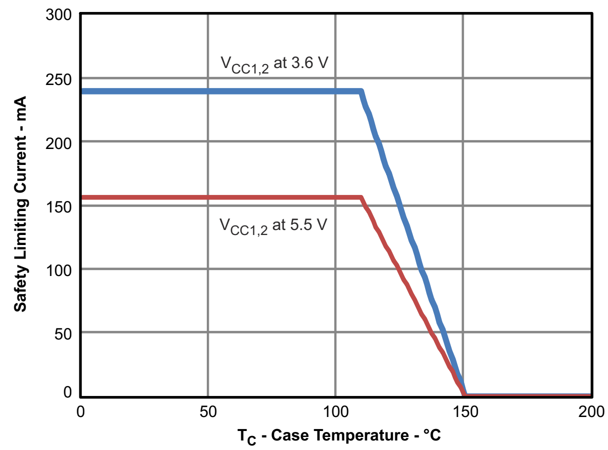
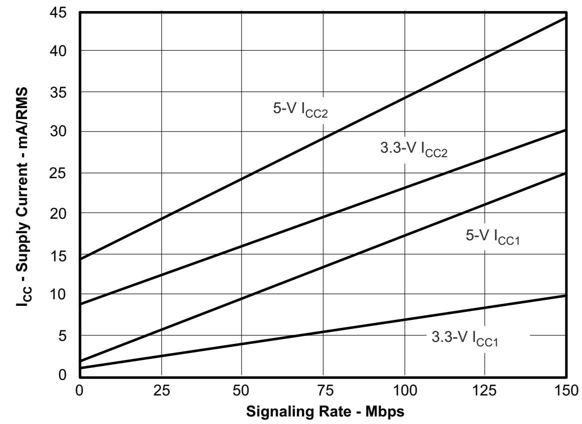


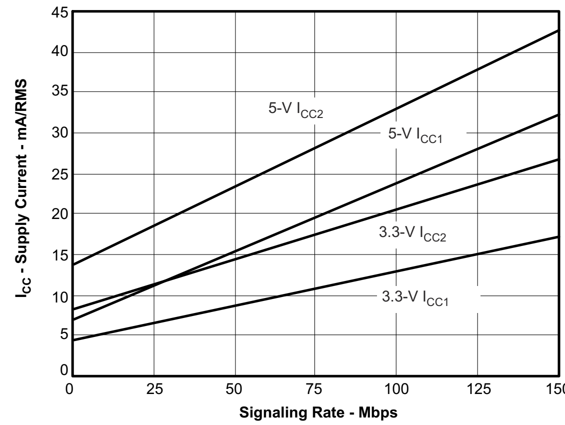
Figure 5-2. Thermal Derating Curve for Limiting Current per VDE

5.22 Typical Characteristics



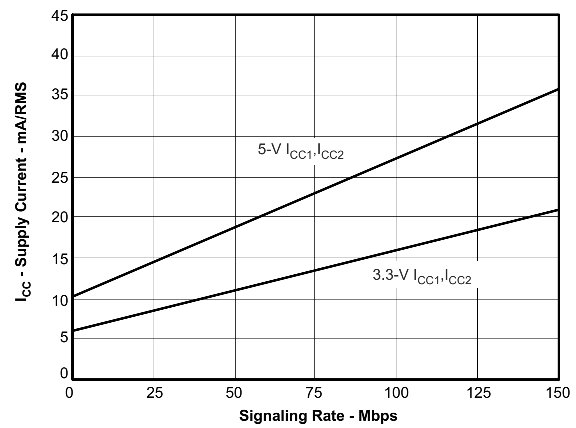
T_A = 25°C Load = 15 pF All Channels

Figure 5-3. ISO7240C/M RMS Supply Current vs Signaling Rate



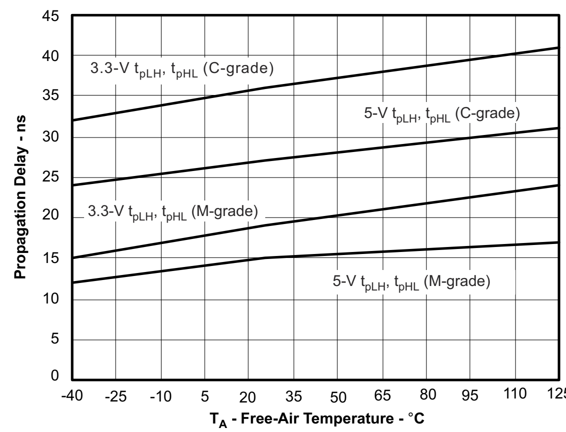
T_A = 25°C Load = 15 pF All Channels

Figure 5-4. ISO7241C/M RMS Supply Current vs Signaling Rate



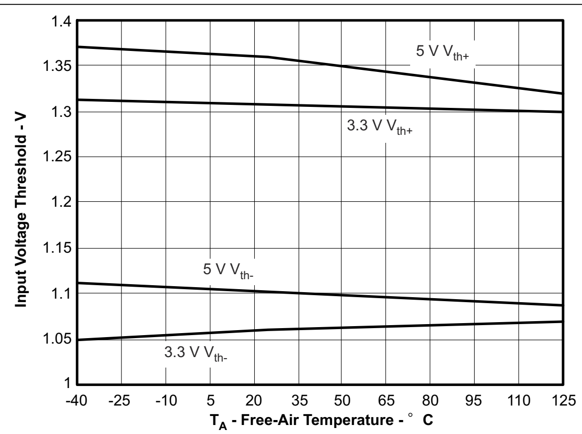
T_A = 25°C Load = 15 pF All Channels

Figure 5-5. ISO7242C/M RMS Supply Current vs Signaling Rate



T_A = 25°C Load = 15 pF All Channels

Figure 5-6. Propagation Delay vs Free-Air Temperature



Air Flow at 7 cf/m Low_K Board

Figure 5-7. Input Voltage Threshold vs Free-Air Temperature

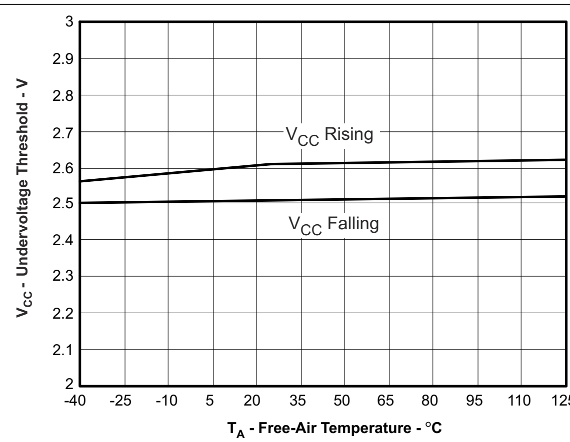
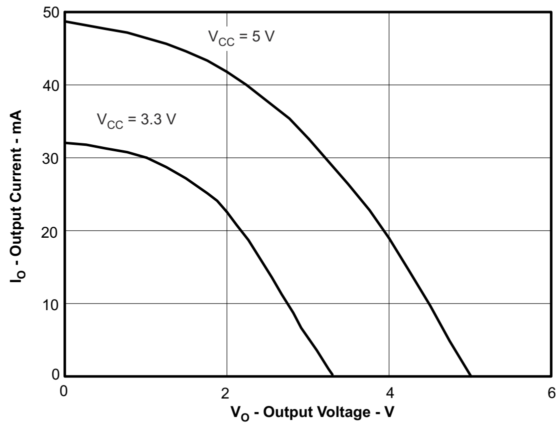


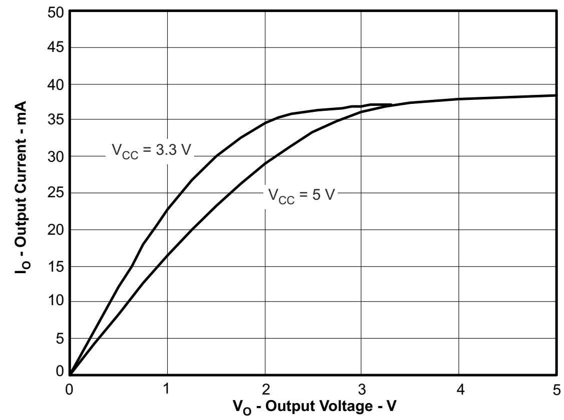
Figure 5-8. V_{CC} Undervoltage Threshold vs Free-Air Temperature

5.22 Typical Characteristics (continued)



T_A = 25°C   Load = 15 pF

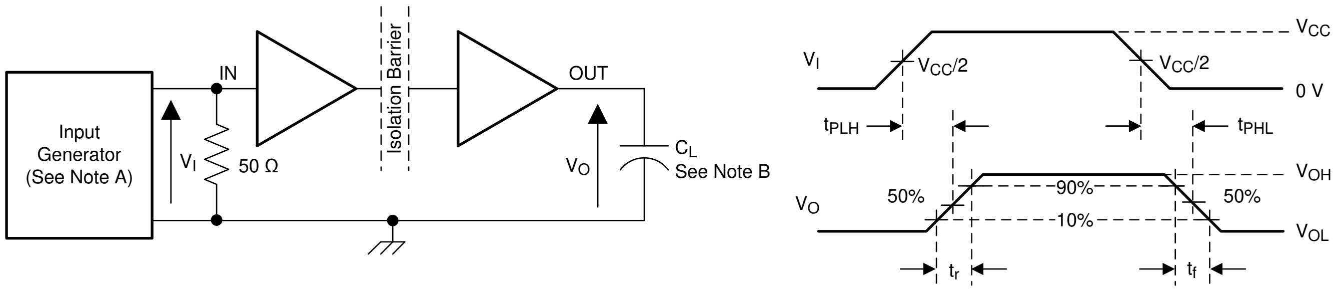
Figure 5-9. High-Level Output Current vs High-Level Output Voltage



T_A = 25°C   Load = 15 pF

Figure 5-10. Low-Level Output Current vs Low-Level Output Voltage

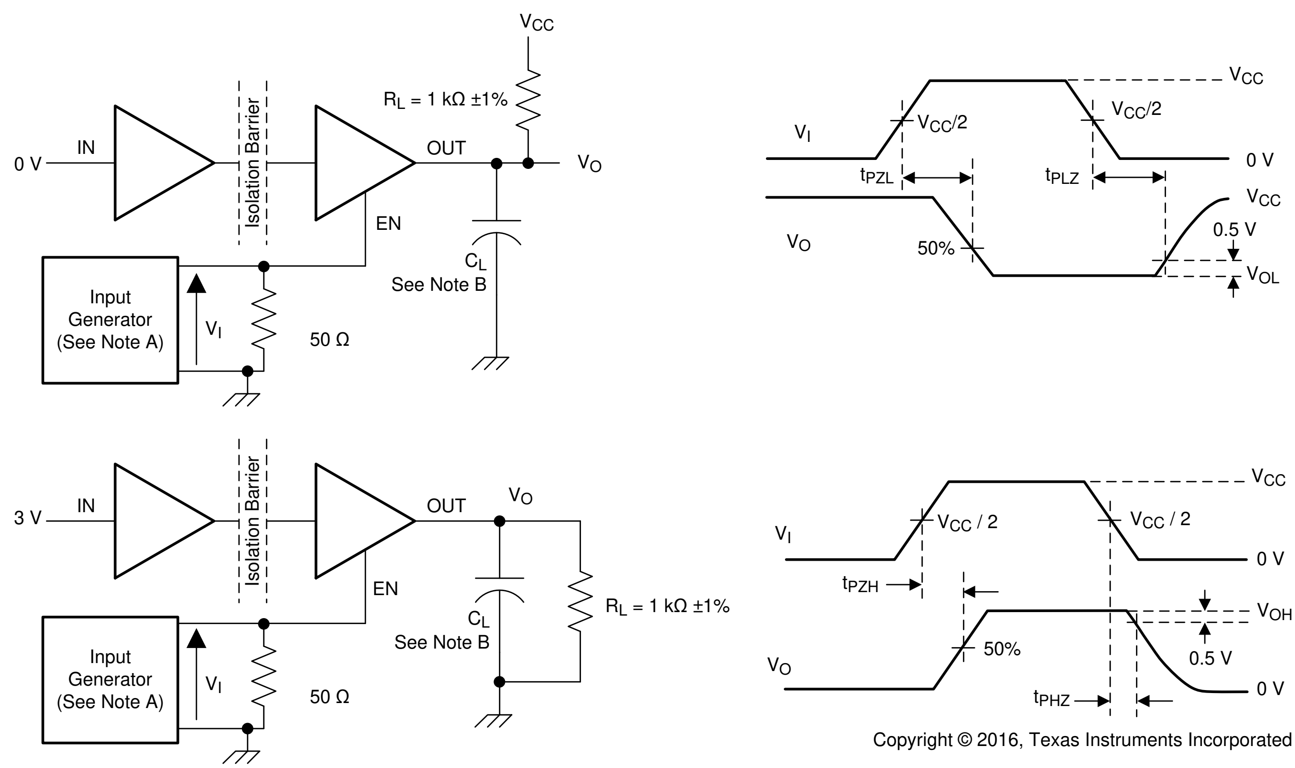
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

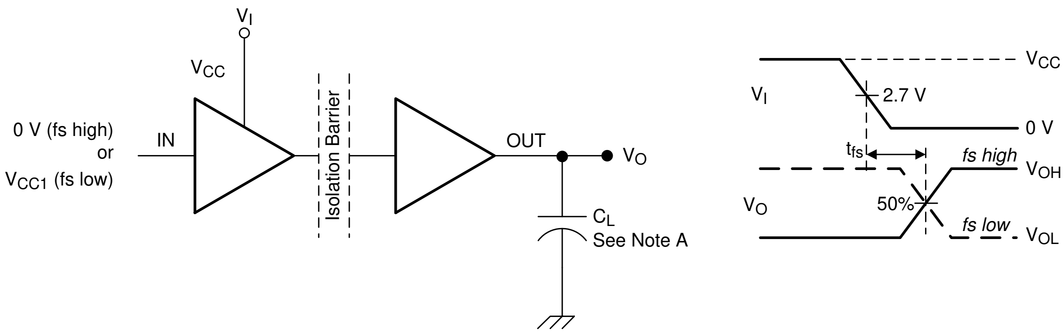
Figure 6-1. Switching Characteristic Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

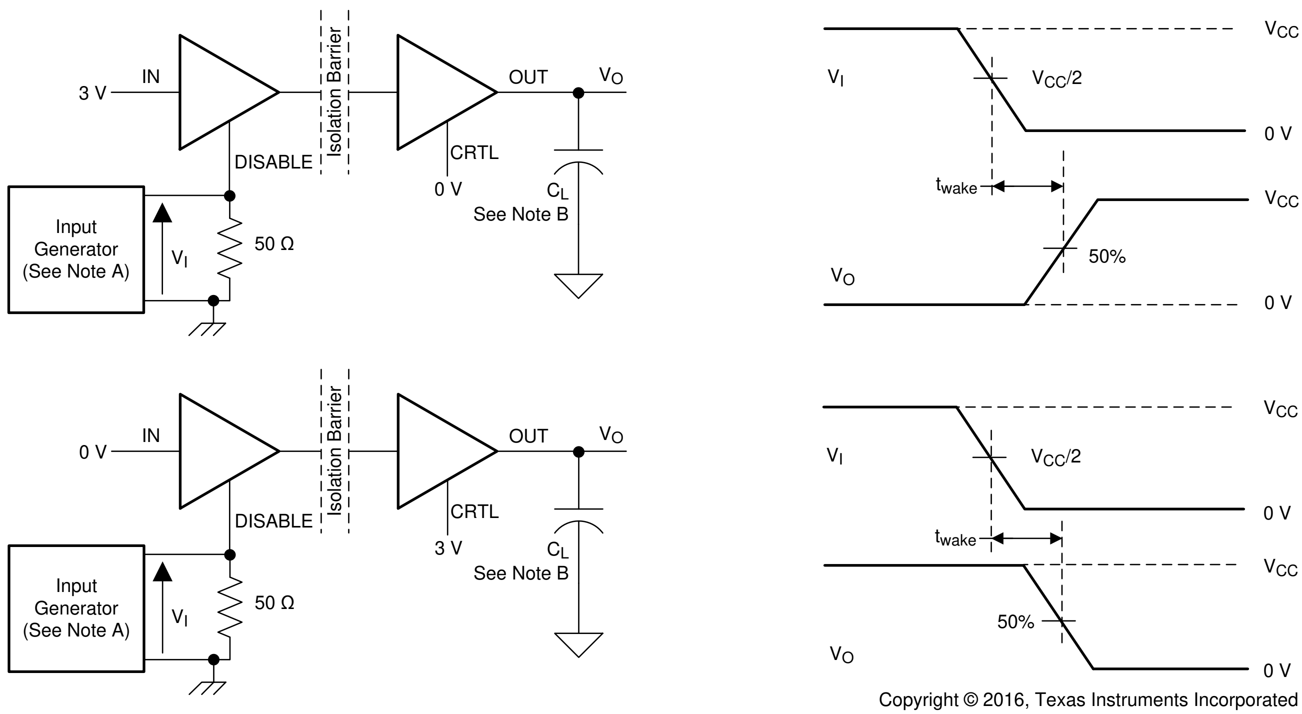
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-2. Enable or Disable Propagation-Delay Time Test Circuit and Waveform



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6-3. Failsafe Delay Time Test Circuit and Voltage Waveforms

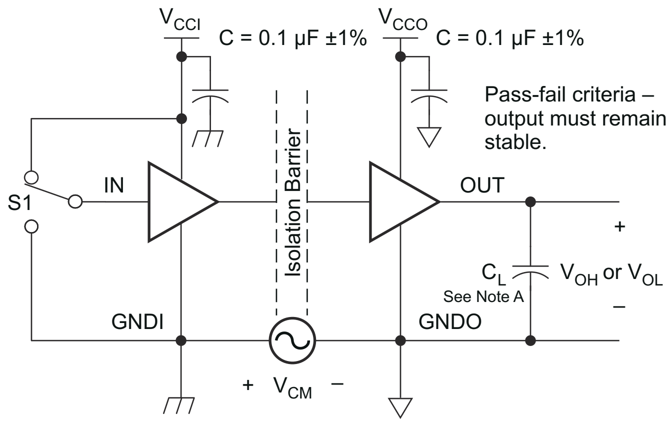


The test that yields the longest time is used in this data sheet.

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

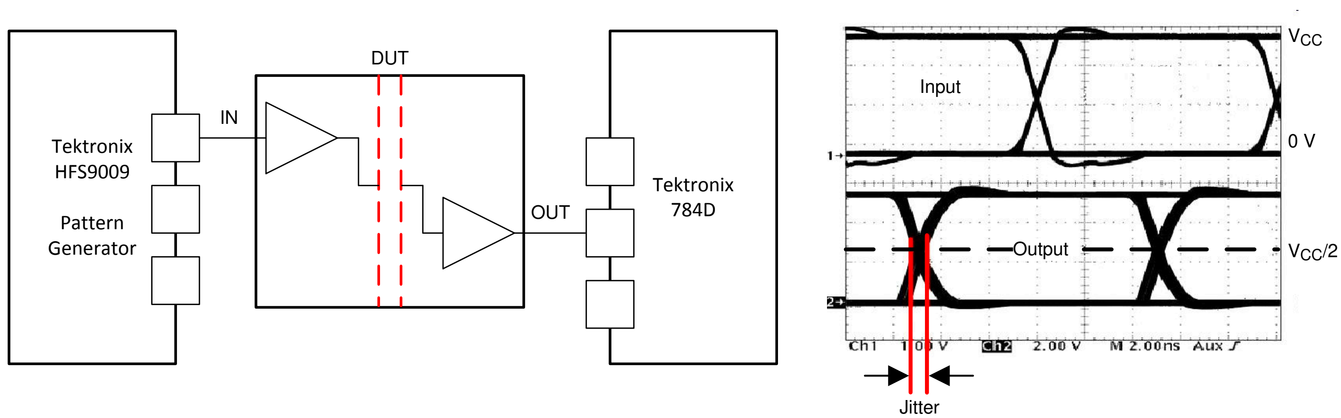
Figure 6-4. Wake Time From Input Disable Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

Figure 6-5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

Figure 6-6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

7 Detailed Description

7.1 Overview

The ISO724x family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

7.2 Functional Block Diagram

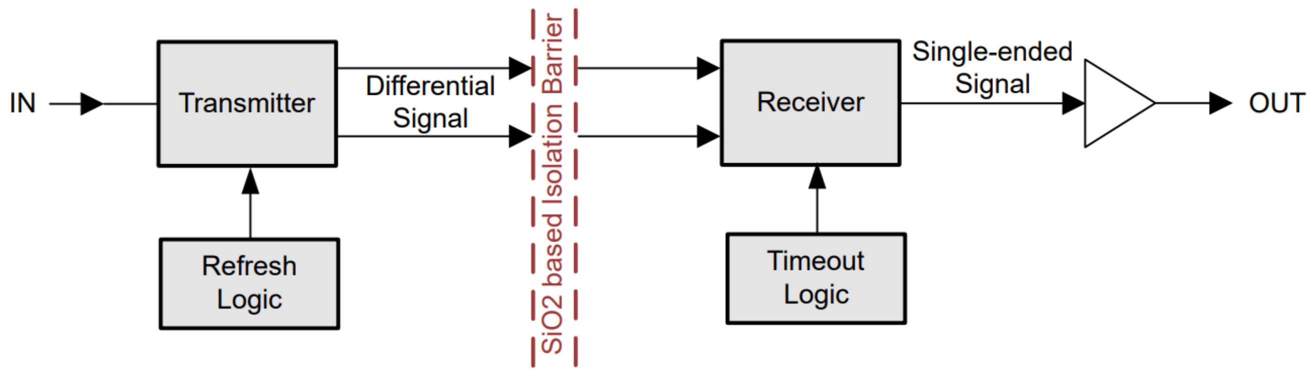


Figure 7-1. Conceptual Block Diagram of a Digital Isolator

7.3 Feature Description

The ISO723xx family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. Table 7-1 lists these device features.

Table 7-1. Device Features

PRODUCT(1)	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION
ISO7230C	25 Mbps	≅1.5 V (TTL)	3/0
ISO7231C	25 Mbps	≅1.5 V (TTL)	2/1
ISO7231M	150 Mbps	V_{CC}/ 2 (CMOS)	

(1) For the most current package and ordering information, see the *Section 11* section, or see the TI website at www.ti.com.

7.4 Device Functional Modes

List of ISO723xx functional modes.

Table 7-2. Device Function Table ISO723x

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

7.4.1 Device I/O Schematics

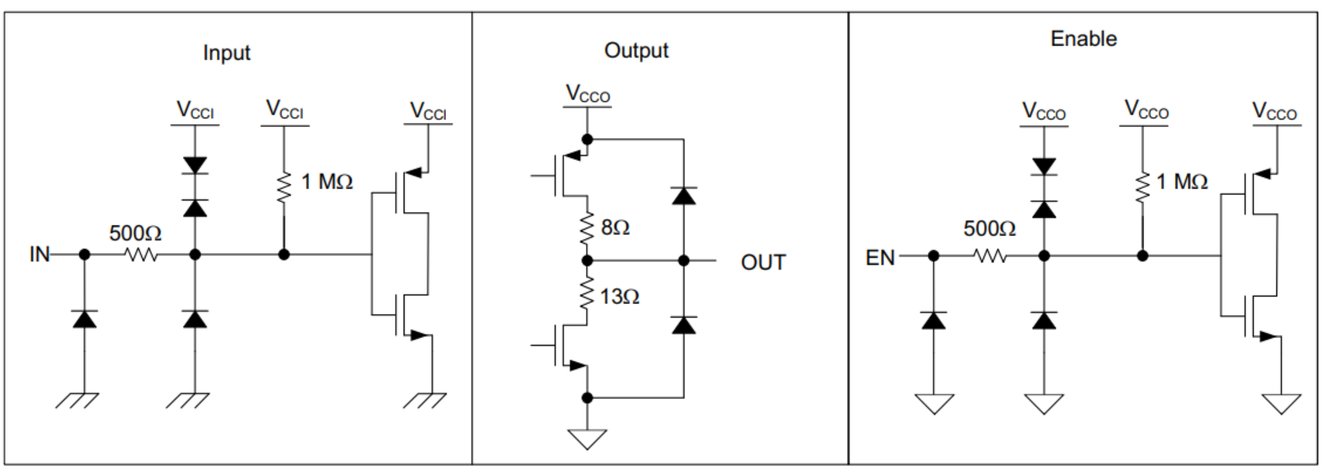


Figure 7-2. Device I/O Schematics

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO724xx family of devices uses a single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3.15 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

8.2.1 Isolated Data Acquisition System for Process Control

The ISO724xx family of devices can be used with Texas Instruments' precision analog-to-digital converter and mixed signal microcontroller to create an advanced isolated data acquisition system as shown in Figure 8-1.

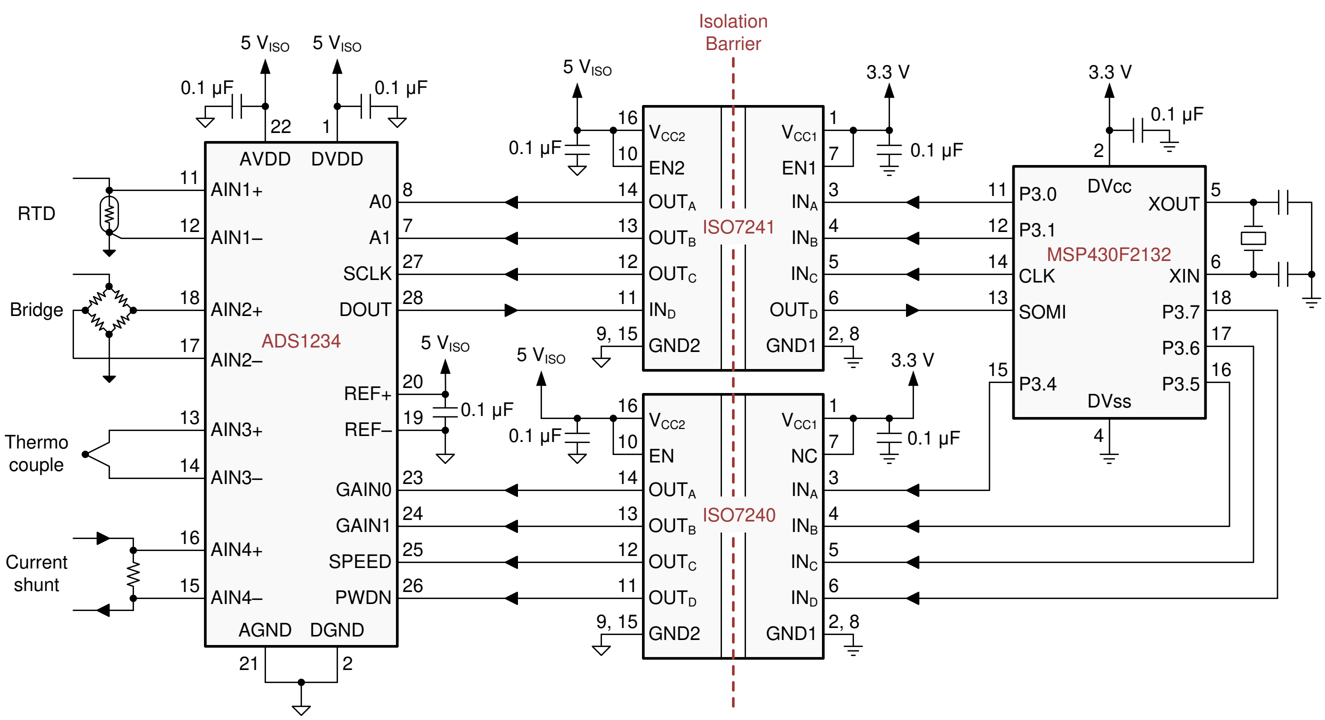


Figure 8-1. Isolated Data Acquisition System for Process Control

8.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO724x family of devices only require two external bypass capacitors to operate.

8.2.1.2 Detailed Design Procedure

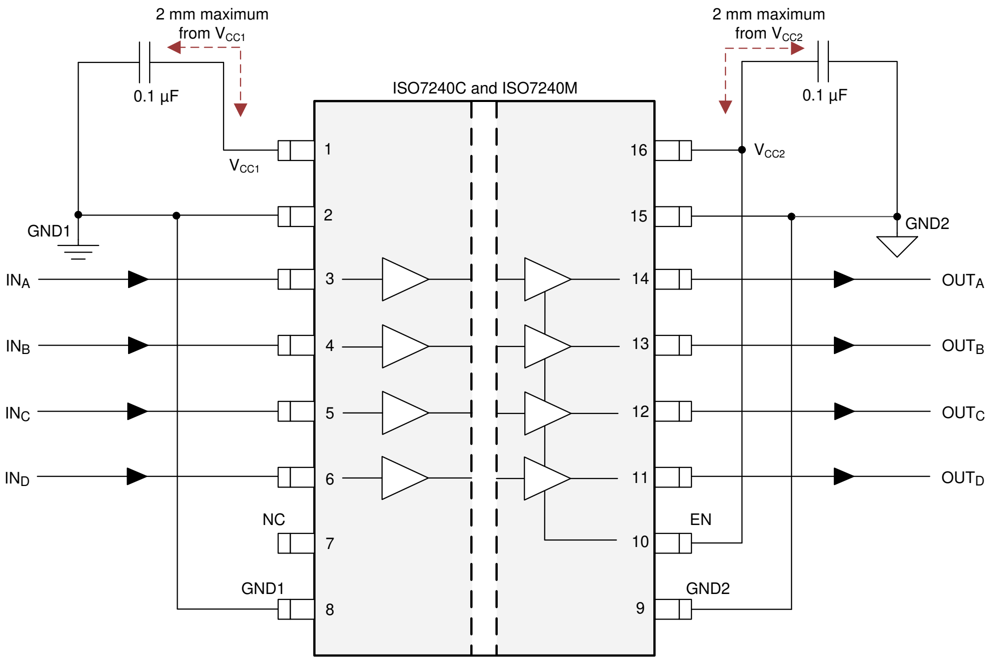


Figure 8-2. ISO7240x Typical Circuit Hook-Up

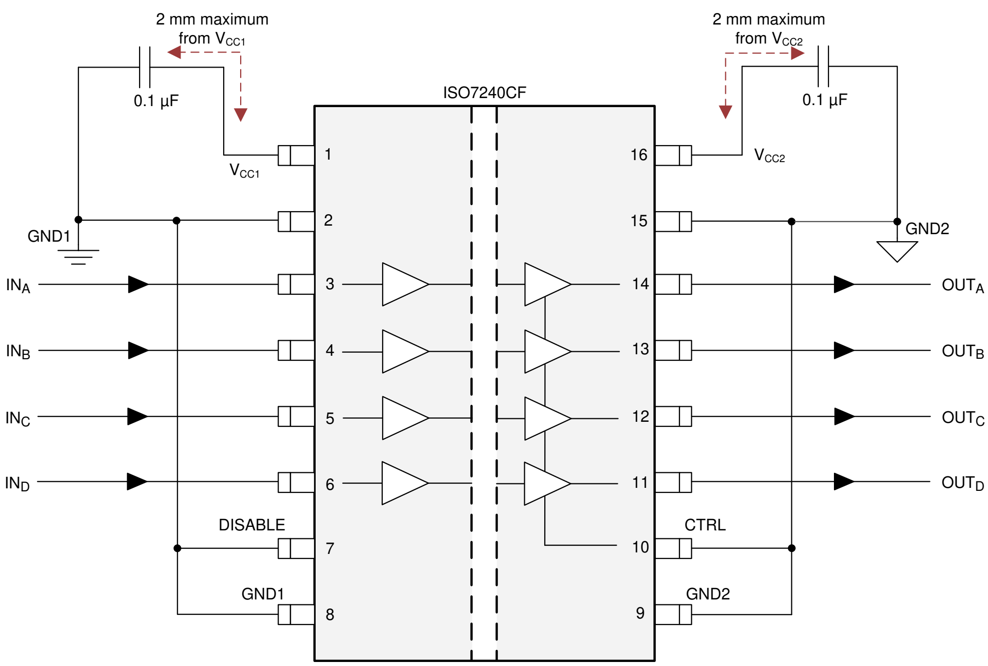


Figure 8-3. ISO7240CF Typical Circuit Hook-Up

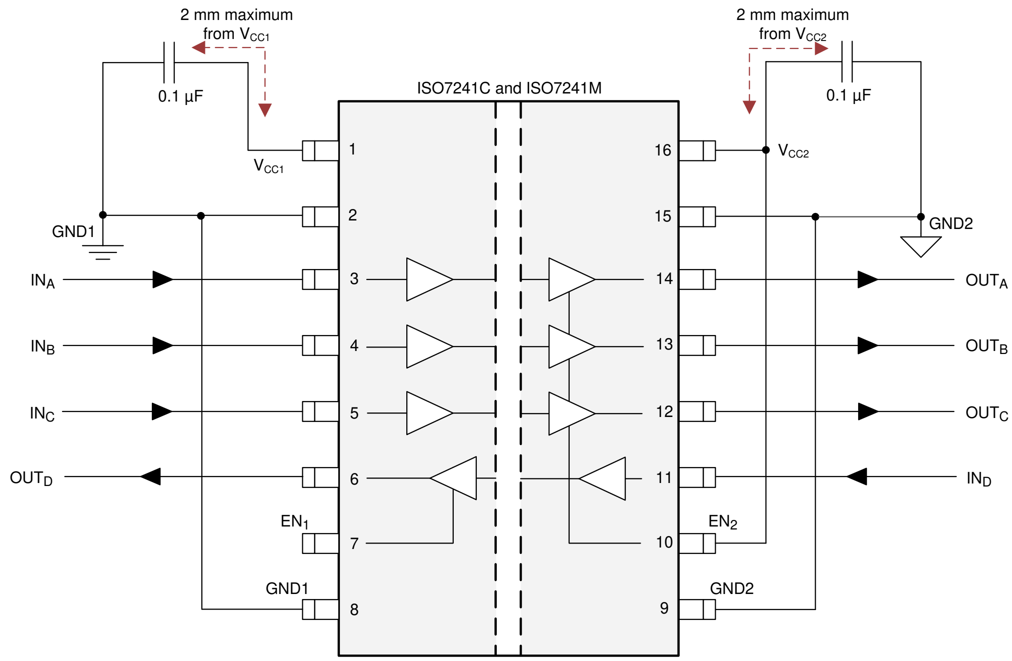


Figure 8-4. ISO7241x Typical Circuit Hook-Up

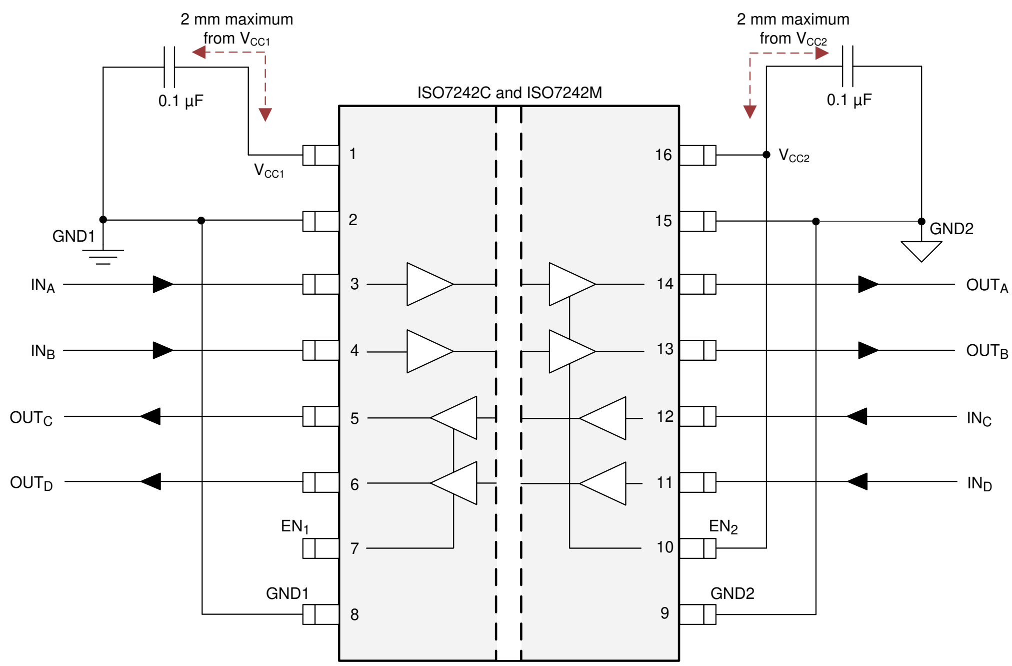


Figure 8-5. ISO7242x Typical Circuit Hook-Up

8.2.1.3 Application Curves

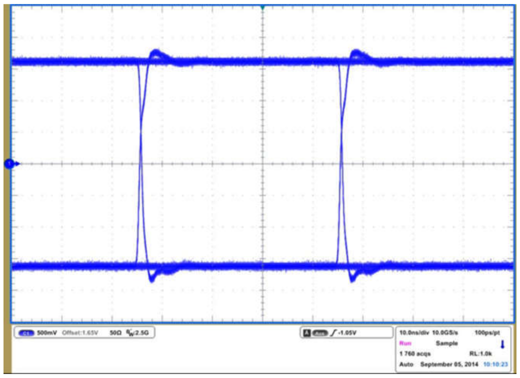


Figure 8-6. ISO7242M Eye Diagram at 25 Mbps, 3.3 V and 25°C

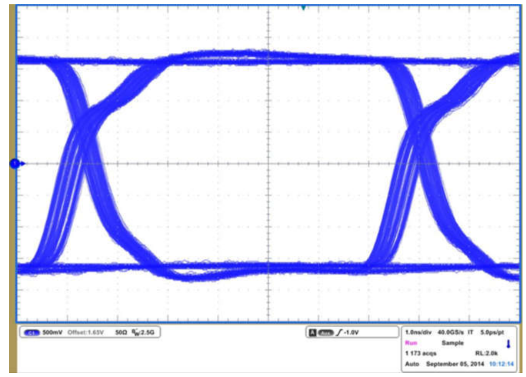


Figure 8-7. ISO7242M Eye Diagram at 150 Mbps, 3.3 V and 25°C

8.2.2 Isolated SPI for an Analog Input Module with 16 Inputs

The ISO7241x family of devices and several other components from Texas Instruments can be used to create an isolated SPI for an input module with 16 inputs.

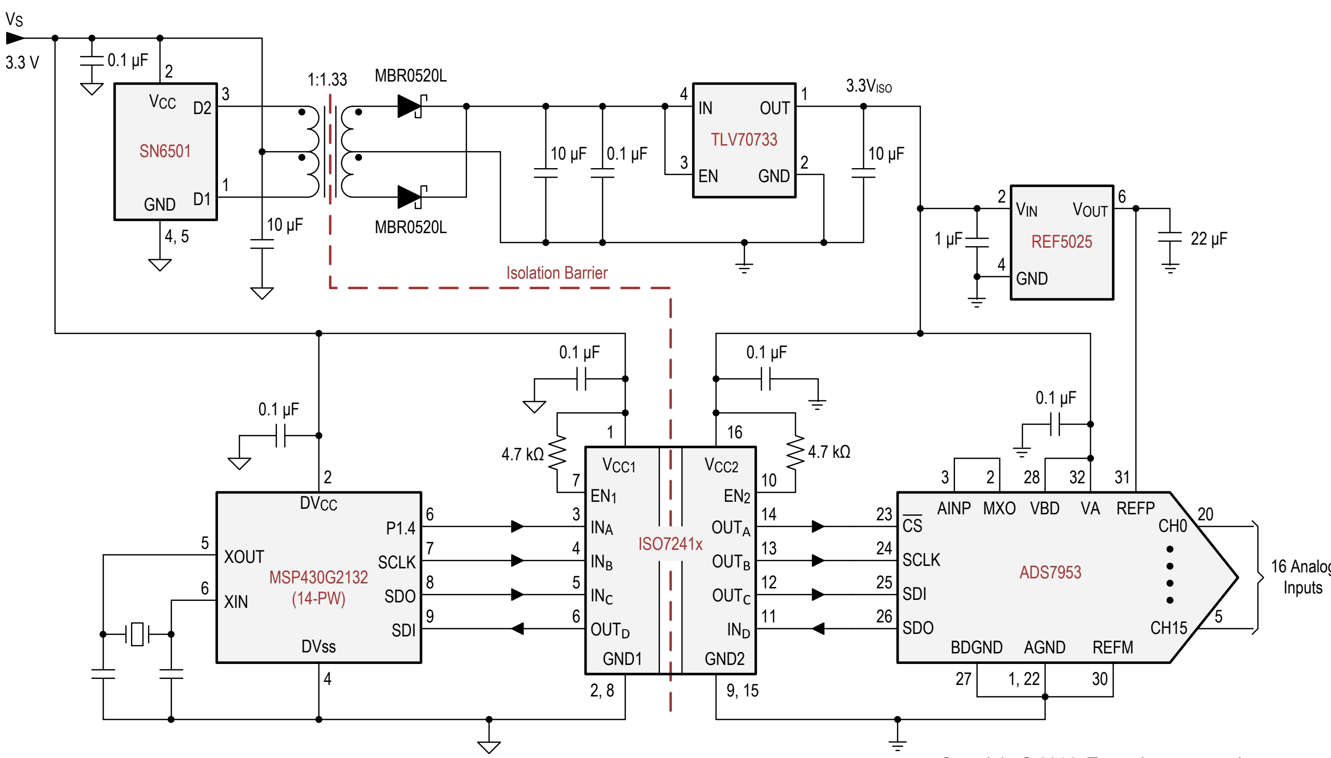


Figure 8-8. Isolated SPI for an Analog Input Module With 16 Inputs

8.2.2.1 Design Requirements

See the *Design Requirements* in *Section 8.2.1*.

8.2.2.2 Detailed Design Procedure

See the *Detailed Design Procedure* in *Section 8.2.1*.

8.2.2.3 Application Curve

See the *Application Curves* in *Section 8.2.1*.

8.2.3 Isolated RS-232 Interface

Figure 8-9 shows a typical isolated RS-232 interface implementation.

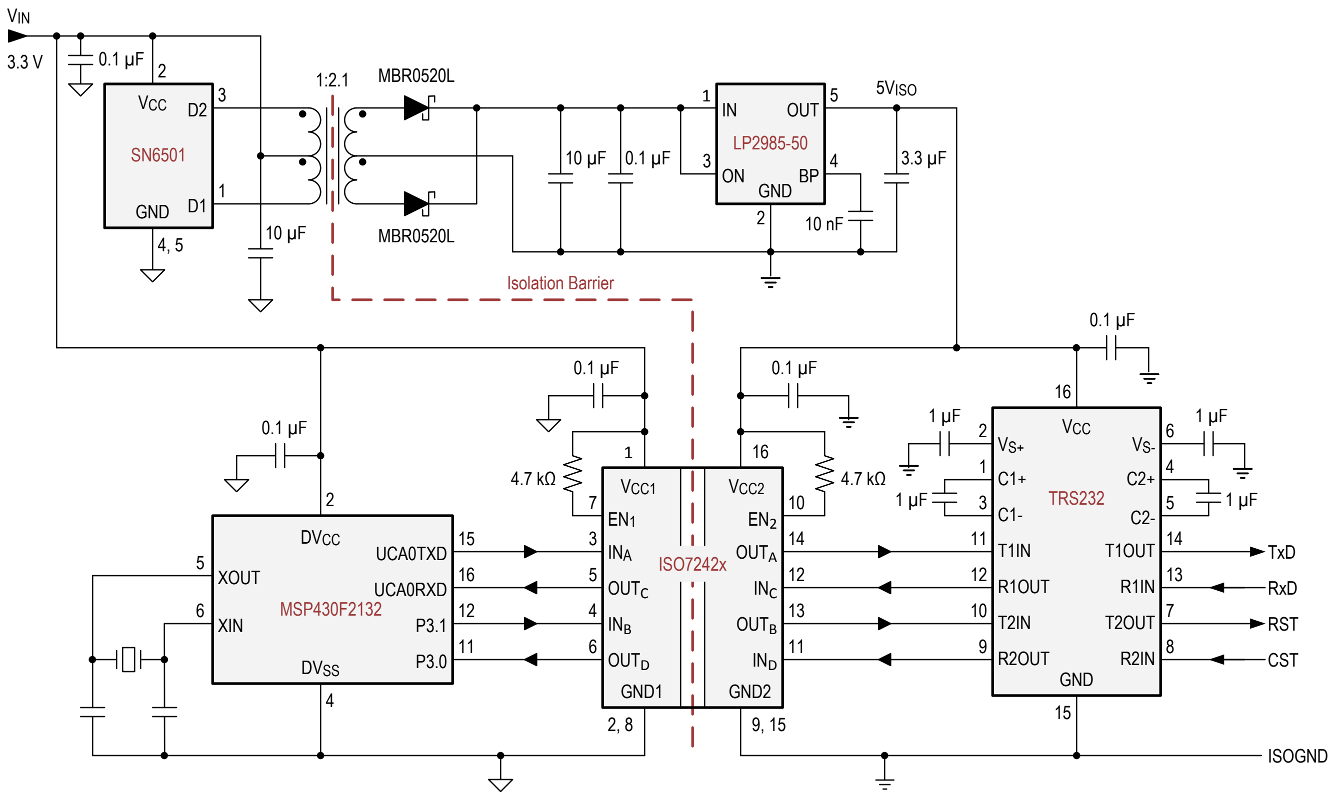


Figure 8-9. Isolated RS-232 Interface

8.2.3.1 Design Requirements

See the *Design Requirements* in *Section 8.2.1*.

8.2.3.2 Detailed Design Procedure

See the *Detailed Design Procedure* in *Section 8.2.1*.

8.2.3.3 Application Curve

See the *Application Curves* in *Section 8.2.1*.

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (VCC1 and VCC2). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies*.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 8-10). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

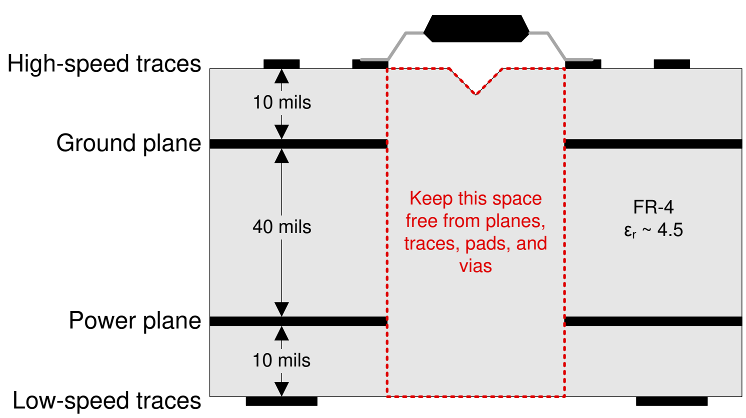


Figure 8-10. Recommended Layer Stack

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- ADS1234 *24-Bit Analog-to-Digital Converter For Bridge Sensors*
- *ADS79xx 12/10/8-Bit, 1 MSPS, 16/12/8/4-Channel, Single-Ended, MicroPower, Serial Interface ADCs*
- *Digital Isolator Design Guide*
- *High-Voltage Lifetime of the ISO72x Family of Digital Isolators*
- *ISO72x Digital Isolator Magnetic-Field Immunity*
- *Isolation Glossary*
- *LP2985 150-mA Low-noise Low-dropout Regulator With Shutdown*
- MSP430F2132 *Mixed Signal Microcontroller*
- *MSP430G2x32, MSP430G2x02 Mixed Signal Microcontroller*
- *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*
- *SN6501 Transformer Driver for Isolated Power Supplies*
- *TLV707, TLV707P 200-mA, Low-IQ, Low-Noise, Low-Dropout Regulator for Portable Devices*
- TRS232 *Dual RS-232 Driver/Receiver With IEC61000-4-2 Protection*

9.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7240CF	Click here	Click here	Click here	Click here	Click here
ISO7240C	Click here	Click here	Click here	Click here	Click here
ISO7240M	Click here	Click here	Click here	Click here	Click here
ISO7241C	Click here	Click here	Click here	Click here	Click here
ISO7241M	Click here	Click here	Click here	Click here	Click here
ISO7242C	Click here	Click here	Click here	Click here	Click here
ISO7242M	Click here	Click here	Click here	Click here	Click here

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

Profibus™ is a trademark of Profibus.
DeviceNet™ is a trademark of Open DeviceNet Vendors Association.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision T (March 2017) to Revision U (October 2024) **Page**

- Updated reference from capacitive isolation to isolation barrier throughout the document................................1
- Updated VDE V 0884-11 to DIN VDE 0884-17 throughout the document.. 1
- Updated the numbering format for tables, figures, and cross-references throughout the document................. 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations..6
- Updated electrical and switching characteristics to match device performance..8

Changes from Revision S (April 2016) to Revision T (March 2017) **Page**

- Added isolation resistance for 100°C ≤ T_A ≤ 125°C in the *Insulation Specifications* table................................6
- Deleted the maximum transient overvoltage from VDE in the *Safety-Related Certifications* table.................... 7
- Added the *Receiving Notification of Documentation Updates* and the *Commnity Resources* section............. 28

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7240CDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7240C	
ISO7240CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240C	Samples
ISO7240CFDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7240CF	
ISO7240CFDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240CF	Samples
ISO7240MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240M	Samples
ISO7240MDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7240M	Samples
ISO7241CDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7241C	
ISO7241CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241C	Samples
ISO7241CDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241C	Samples
ISO7241MDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7241M	
ISO7241MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241M	Samples
ISO7241MDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7241M	Samples
ISO7242CDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7242C	
ISO7242CDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242C	Samples
ISO7242MDW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 125	ISO7242M	
ISO7242MDWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242M	Samples
ISO7242MDWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7242M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7240CF, ISO7241C, ISO7242C :

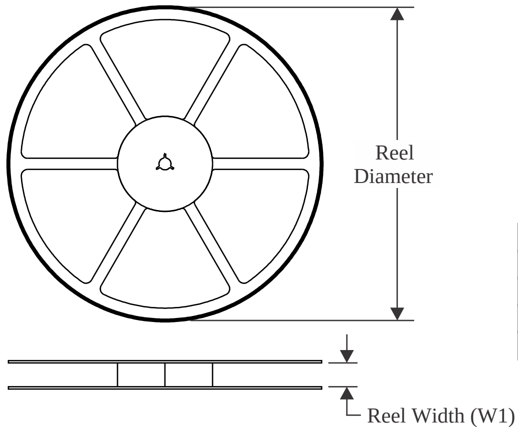
- Automotive : ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1

NOTE: Qualified Version Definitions:

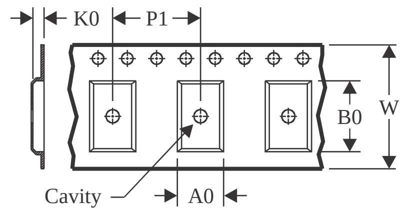
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

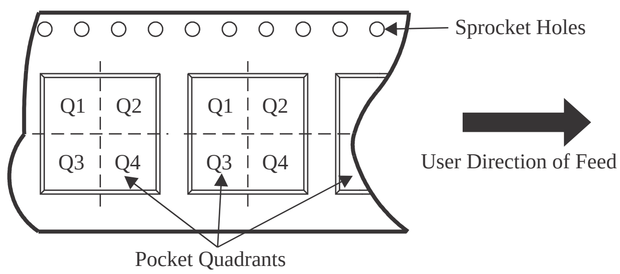


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

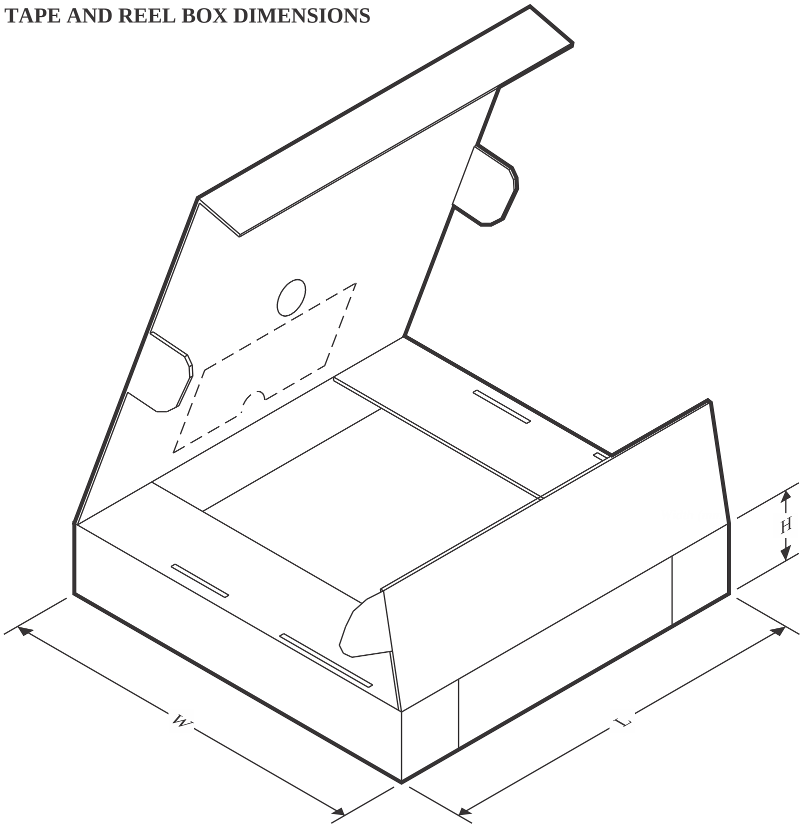
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240CFDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7240MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242MDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

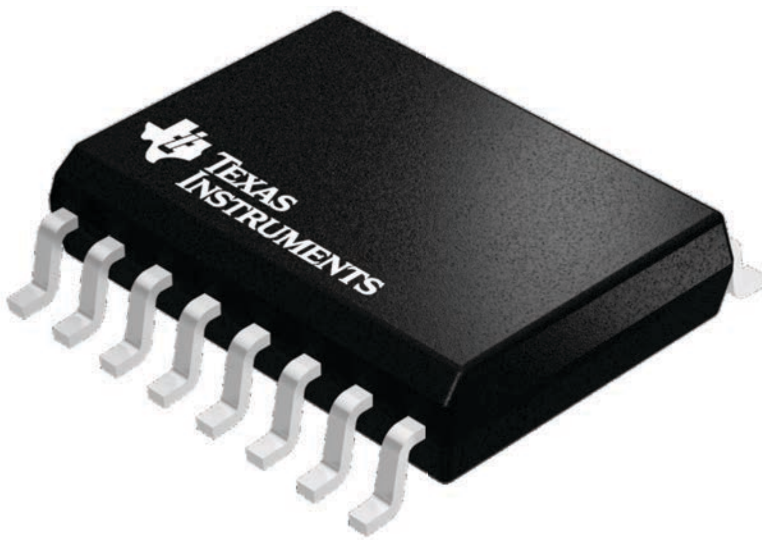
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7240CFDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7240MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241MDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242CDWR	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242MDWR	SOIC	DW	16	2000	350.0	350.0	43.0

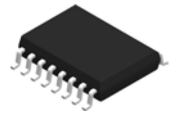
GENERIC PACKAGE VIEW

DW 16 **SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



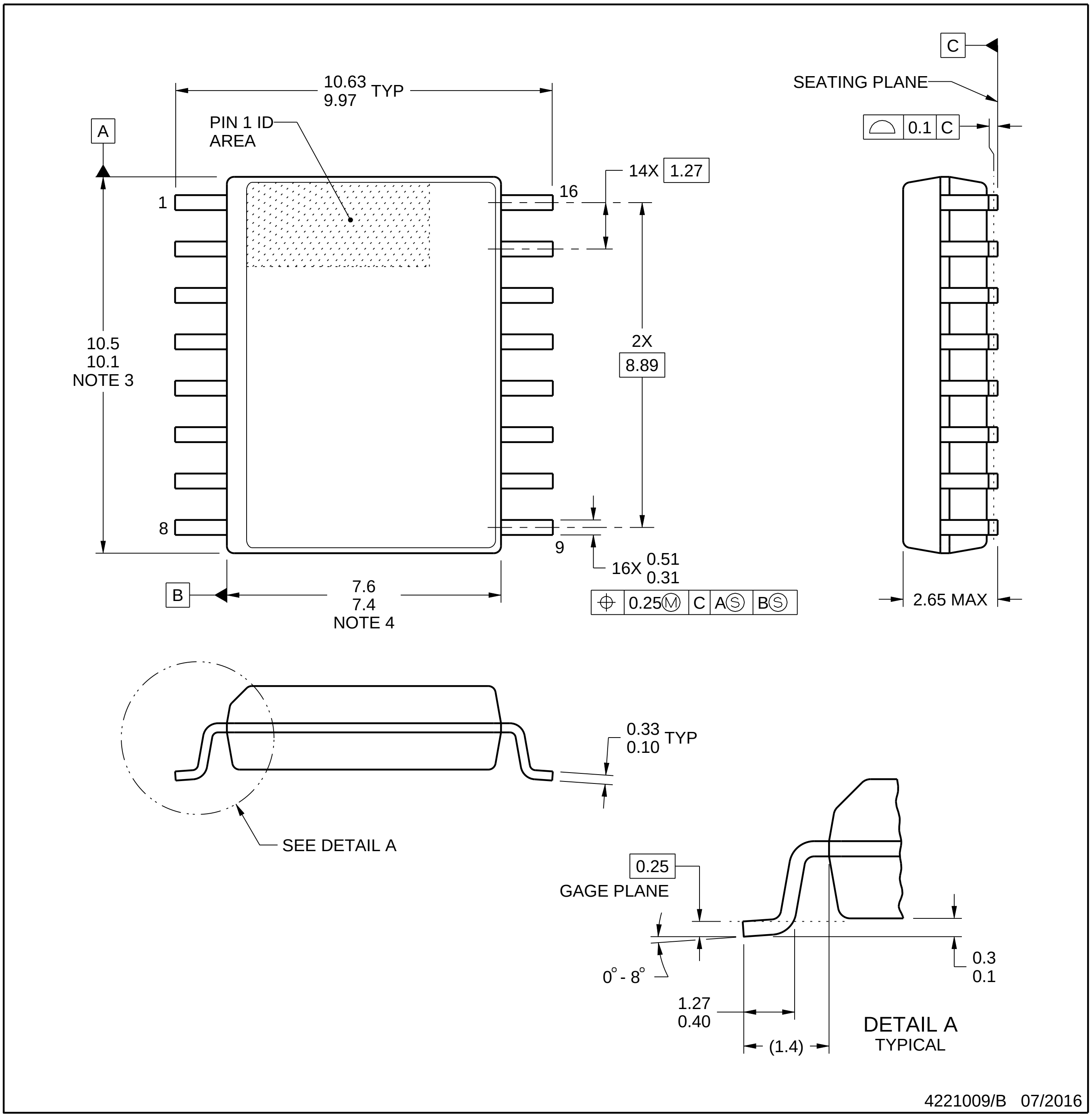


PACKAGE OUTLINE

DW0016B

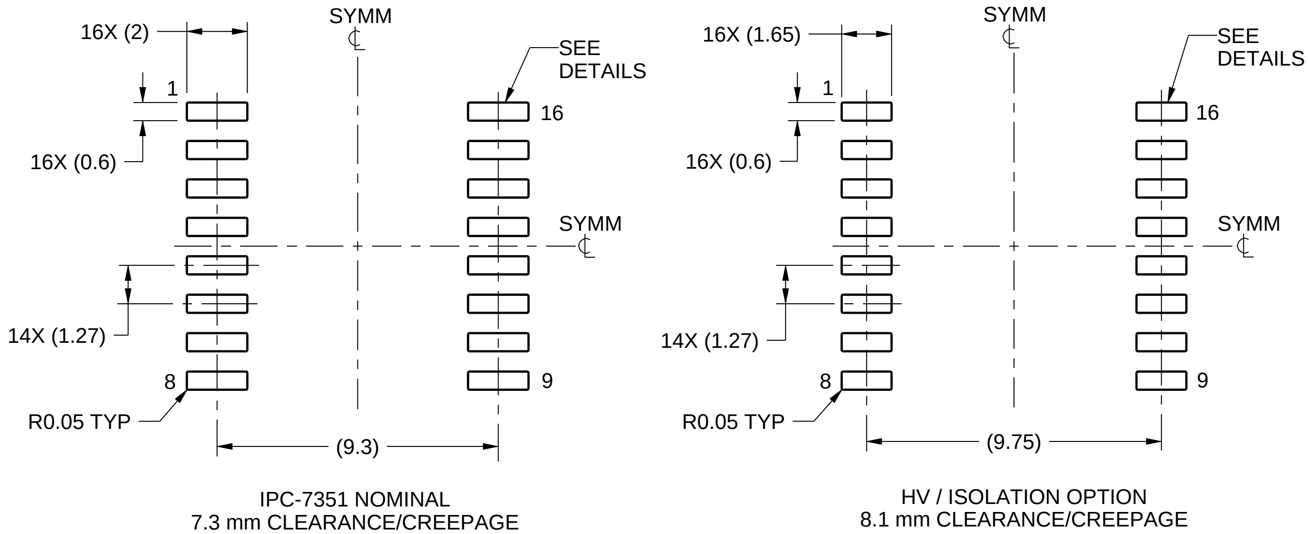
SOIC - 2.65 mm max height

SOIC

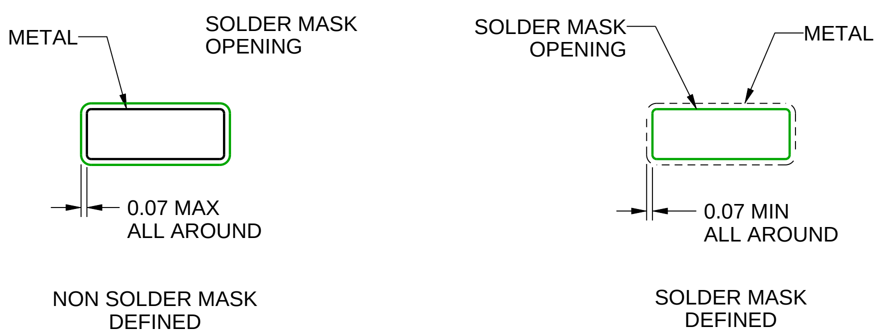


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:4X

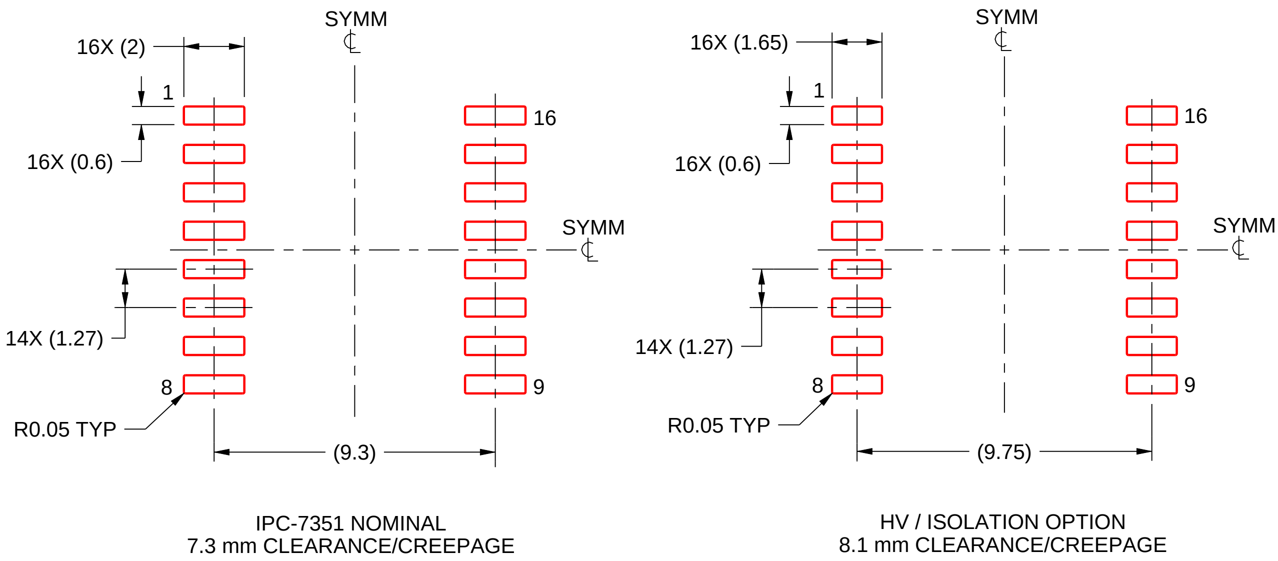


SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.