

# ISOW774x-Q1 Quad-Channel Digital Isolator with Integrated Low-Emissions, Low-Noise DC-DC Converter

## 1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ambient temperature range
- 100 Mbps data rate
- Integrated DC-DC converter with low-emissions, low-noise
  - Emission optimized to meet CISPR25
  - Low frequency power converter at 25 MHz enabling low noise performance
  - Low output ripple: 24 mV
- High efficiency output power
  - Efficiency at max load: 46%
  - Up to 0.55-W output power
  - $V_{\text{ISOOUT}}$  accuracy of 5%
  - 5 V to 5 V: Max available load current = 110 mA
  - 5 V to 3.3 V: Max available load current = 140 mA
  - 3.3 V to 3.3 V: Max available load current = 60 mA
- Independent power supply for channel isolator & power converter
  - Logic supply ( $V_{\text{IO}}$ ): 1.71-V to 5.5-V
  - Power converter supply ( $V_{\text{DD}}$ ): 3-V to 5.5-V
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and surge immunity
  - $\pm 8$  kV IEC 61000-4-2 contact discharge protection across isolation barrier
- Reinforced and Basic isolation options
- High CMTI: 100-kV/ $\mu\text{s}$  (typical)
- Safety Related Certifications:
  - VDE reinforced and basic insulation per DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 component recognition program
  - IEC 62368-1, IEC 61010-1, IEC 60601-1 and GB 4943.1-2011 certifications
  - ISOW774xB devices are planned
- Extended temperature range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- 20-pin wide body SOIC package

## 2 Applications

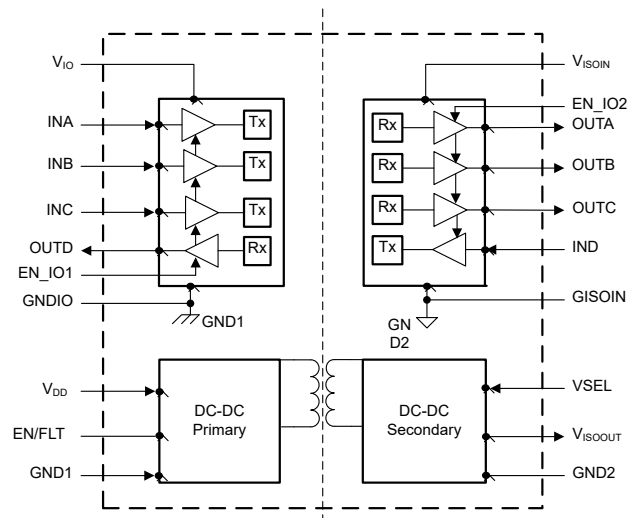
- [Hybrid, electric and power train system \(EV/HEV\)](#)
  - [Battery management system \(BMS\)](#)
  - [On-board charger \(OBC\)](#)
  - [Traction inverter](#)
  - [DC/DC converter](#)

## 3 Description

The ISOW7741-Q1 and ISOW7742-Q1 devices are galvanically-isolated quad-channel digital isolator with an integrated high-efficiency power converter with low emissions. The integrated DC-DC converter provides up to 550 mW of isolated power, eliminating the need for a separate isolated power supply in space-constrained isolated designs.

### Device Information

| FEATURE            | ISOW774x-Q1<br>ISOW774xF-Q1                |
|--------------------|--|
| Surge Test Voltage | 10 kV <sub>PK</sub>                        |
| Isolation Rating   | 5000 V <sub>RMS</sub>                      |
| Working Voltage    | 1000 V <sub>RMS</sub> /1500V <sub>PK</sub> |
| Package            | DFM (20)                                   |
| Body Size (Nom)    | 12.83 mm × 7.5 mm                          |



**ISOW7741-Q1 Simplified Schematic**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE          | REVISION | NOTES            |
|---------------|----------|------------------|
| November 2022 | *        | Initial release. |

## 5 Description (continued)

The high-efficiency of the power converter allows for operation at a wide operating ambient temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . This device provides improved emissions performance, allowing for simplified board design and has provisions for ferrite beads to further attenuate emissions. The ISOW7741-Q1 and ISOW7742-Q1 has been designed with enhanced protection features in mind, including soft-start to limit inrush current, over-voltage and under-voltage lock out, fault detection on the EN/FLT pin, overload and short-circuit protection, and thermal shutdown.

The ISOW7741-Q1 and ISOW7742-Q1 devices provide high electromagnetic immunity while isolating CMOS or LVCMOS digital I/Os. The signal-isolation channel has a logic input and output buffer separated by a double capacitive silicon dioxide ( $\text{SiO}_2$ ) insulation barrier, whereas, power isolation uses on-chip transformers separated by thin film polymer as insulating material. If the input signal is lost, the default output is high for the ISOW7741-Q1 and ISOW7742-Q1 devices without the F suffix and low for the ISOW7741F-Q1 and ISOW7742-Q1 devices with the F suffix. The ISOW774x-Q1 can operate from a single supply voltage of 3 V to 5.5 V by connecting  $V_{\text{IO}}$  and  $V_{\text{DD}}$  together on PCB. If lower logic levels are required, these devices support 1.71 V to 5.5 V logic supply ( $V_{\text{IO}}$ ) that can be independent from the power converter supply ( $V_{\text{DD}}$ ) of 3 V to 5.5 V.  $V_{\text{ISOIN}}$  and  $V_{\text{ISOOUT}}$  needs to be connected on board with either a ferrite bead or fed through a LDO.

These devices help prevent noise currents on data buses, such as CAN and LIN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the device has been significantly enhanced to ease system-level ESD, EFT, surge and emissions compliance. The device is available in a 20-pin SOIC wide-body (SOIC-WB) DFM package.

## 6 Pin Configuration and Functions

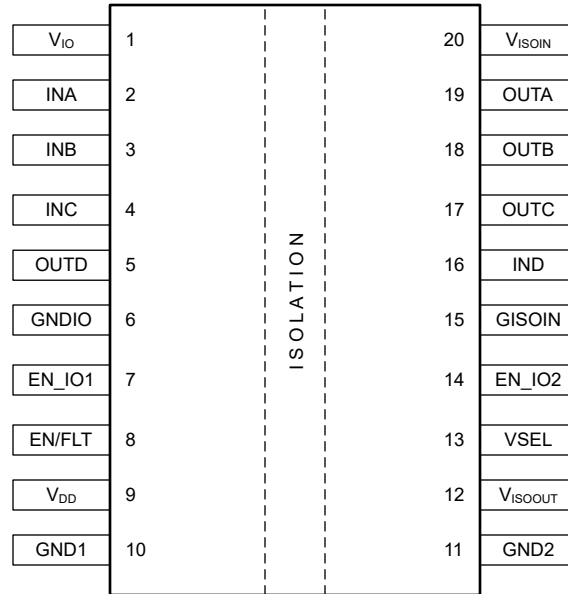


Figure 6-1. ISOW7741-Q1 DFM Package 20-Pin SOIC-WB Top View

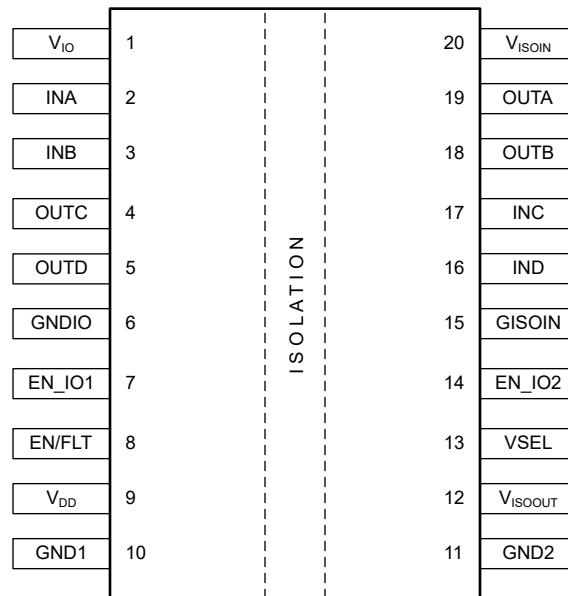


Figure 6-2. ISOW7742-Q1 DFM Package 20-Pin SOIC-WB Top View

| NAME   | PIN         |             | I/O | DESCRIPTION   |
|--------|-------------|-------------|-----|---|
|        | NO.         |             |     |   |
|        | ISOW7741-Q1 | ISOW7742-Q1 |     |   |
| GNDIO  | 6           | 6           | —   | Ground connection for $V_{IO}$ . GND1 and GNDIO needs to be shorted on board.   |
| GND1   | 10          | 10          | —   | Ground connection for $V_{DD}$ . GND1 and GNDIO needs to be shorted on board.   |
| GND2   | 11          | 11          | —   | Ground connection for $V_{ISOOUT}$ . GND2 and GISOIN pins can be shorted on board or connected through a ferrite bead. See the <a href="#">Layout Section</a> for more information. |
| GISOIN | 15          | 15          | —   | Ground connection for $V_{ISOIN}$ . GND2 and GISOIN pins can be shorted on board or connected through a ferrite bead. See the <a href="#">Layout Section</a> for more information.  |
| INA    | 2           | 2           | I   | Input channel A   |

| NAME         | PIN         |             | I/O | DESCRIPTION  |
|--------------|-------------|-------------|-----|--|
|              | NO.         |             |     |  |
|              | ISOW7741-Q1 | ISOW7742-Q1 |     |  |
| INB          | 3           | 3           | I   | Input channel B  |
| INC          | 4           | 17          | I   | Input channel C  |
| IND          | 16          | 16          | I   | Input channel D  |
| OUTA         | 19          | 19          | O   | Output channel A   |
| OUTB         | 18          | 18          | O   | Output channel B   |
| OUTC         | 17          | 4           | O   | Output channel C   |
| OUTD         | 5           | 5           | O   | Output channel D   |
| EN_IO1       | 7           | 7           | I   | Output Enable 1: When EN_IO1 is high or open then the channel output pins on side 1 are enabled. When EN_IO1 is low then the channel output pins on side 1 are in a high impedance state and the transmitter of the channel input pins on side 1 are disabled.   |
| EN_IO2       | 14          | 14          | I   | Output Enable 2: When EN_IO2 is high or open then the channel output pins on side 2 are enabled. When EN_IO2 is low then the channel output pins on side 2 are in a high impedance state and the transmitter of the channel input pins on side 2 are disabled.   |
| EN/FLT       | 8           | 8           | I/O | Multi-function power converter enable input pin or fault output pin. Can only be used as either an input pin or an output pin.<br>Power converter enable input pin: enables and disables the integrated DC-DC power converter. Connect directly to microcontroller or through a series current limiting resistor to use as an enable input pin. DC-DC power converted is enabled when EN/FLT is high to the $V_{IO}$ voltage level and disabled when low at GND1 voltage level.<br>Fault output pin: Alert signal if power converter is not operating properly. This pin is active low. Connect to microcontroller through a 5 k $\Omega$ or greater pull-up resistor in order to use as a fault outpin pin.<br>See <a href="#">Section 9.3.3</a> for more information |
| VSEL         | 13          | 13          | I   | $V_{ISOOUT}$ selection pin. $V_{ISOOUT} = 5\text{ V}$ when VSEL shorted to $V_{ISOOUT}$ . $V_{ISOOUT} = 3.3\text{ V}$ , when VSEL shorted to GND2. For more information see the <a href="#">Device Functional Modes</a> .  |
| $V_{IO}$     | 1           | 1           | —   | Side 1 logic supply.   |
| $V_{DD}$     | 9           | 9           | —   | Side 1 DC-DC converter power supply.   |
| $V_{ISOIN}$  | 20          | 20          | —   | Side 2 supply voltage for isolation channels. $V_{ISOIN}$ and $V_{ISOOUT}$ pins can be shorted on board or connected through a ferrite bead. See <a href="#">Application and Implementation</a> for more information.  |
| $V_{ISOOUT}$ | 12          | 12          | —   | Isolated power converter output voltage. $V_{ISOIN}$ and $V_{ISOOUT}$ pins can be shorted on board or connected through a ferrite bead. See <a href="#">Application and Implementation</a> for more information.   |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup>

|                     |  | MIN  | MAX                       | UNIT |
|---------------------|--|------|---------------------------|------|
| V <sub>DD</sub>     | Power converter supply voltage   | -0.5 | 6                         | V    |
| V <sub>ISOIN</sub>  | Isolated supply voltage, input supply for secondary side isolation channels            | -0.5 | 6                         | V    |
| V <sub>ISOOUT</sub> | Isolated supply voltage, Power converter output<br>VSEL shorted to GND2                | -0.5 | 4                         | V    |
| V <sub>ISOOUT</sub> | Isolated supply voltage, Power converter output<br>VSEL shorted to V <sub>ISOOUT</sub> | -0.5 | 6                         | V    |
| V <sub>IO</sub>     | Primary side logic supply voltage  | -0.5 | 6                         | V    |
| V                   | Voltage at INx, OUTx, EN_IOx <sup>(3)</sup>  | -0.5 | V <sub>SI</sub> + 0.5     | V    |
|                     | Voltage at EN/FLT  | -0.5 | V <sub>SI</sub> + 0.5     | V    |
|                     | Voltage at VSEL  | -0.5 | V <sub>ISOOUT</sub> + 0.5 | V    |
| I <sub>O</sub>      | Maximum output current through data channels   | -15  | 15                        | mA   |
| T <sub>J</sub>      | Junction temperature   | -40  | 150                       | °C   |
| T <sub>stg</sub>    | Storage temperature  | -65  | 150                       | °C   |

- Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- V<sub>DD</sub>, V<sub>ISOIN</sub>, V<sub>ISOOUT</sub>, and V<sub>IO</sub> are with respect to the local ground pin (GND1 or GND2). All voltage values except differential I/O bus voltages are peak voltage values.
- V<sub>SI</sub> = input side supply; Cannot exceed 6 V.

### 7.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup><br>HBM ESD Classification Level 2 | ±3000 | V    |
|                    |                         | Charged-device model (CDM), per AEC Q100-011<br>CDM ESD Classification Level C6           | ±1500 |      |
|                    |                         | Contact discharge per IEC 61000-4-2 <sup>(2)</sup><br>Isolation barrier withstand test    | ±8000 |      |

- AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.

### 7.3 Recommended Operating Conditions

Over recommended operating conditions, typical values are at  $V_{DD} = V_{IO} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ , GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

|                                    |   |   | MIN                 | NOM                 | MAX      | UNIT             |
|------------------------------------|---|---|---------------------|---------------------|----------|------------------|
| <b>Power Converter</b>             |   |   |                     |                     |          |                  |
| $V_{DD}$                           | Power converter supply voltage                            | 3.3 V operation   | 2.97                | 3.3                 | 3.63     | V                |
|                                    |   | 5 V operation   | 4.5                 | 5                   | 5.5      | V                |
| $V_{DD(UVLO+)}$                    | Positive threshold when power converter supply is rising  | Positive threshold when power converter supply is rising  |                     | 2.7                 | 2.95     | V                |
| $V_{DD(UVLO-)}$                    | Positive threshold when power converter supply is falling | Positive threshold when power converter supply is falling | 2.40                | 2.55                |          | V                |
| $V_{DD(HYS)}$                      | Power converter supply voltage hysteresis                 | Power converter supply voltage hysteresis                 | 0.15                |                     |          | V                |
| <b>Channel Isolation</b>           |   |   |                     |                     |          |                  |
| $V_{IO}, V_{ISOIN}$ <sup>(3)</sup> | Channel logic supply voltage                              | 1.8 V operation   | 1.71                |                     | 1.89     | V                |
|                                    |   | 2.5 V, 3.3 V, and 5 V operation                           | 2.25                |                     | 5.5      | V                |
| $V_{IO(UVLO+)}$                    | Rising threshold of logic supply voltage                  |   |                     | 1.55                | 1.7      | V                |
| $V_{IO(UVLO-)}$                    | Falling threshold of logic supply voltage                 |   | 1.0                 | 1.41                |          | V                |
| $V_{IO(HYS)}$                      | Logic supply voltage hysteresis                           |   | 75                  |                     |          | mV               |
| $I_{OH}$                           | High level output current <sup>(1)</sup>                  | $V_{ISOIN} = 5\text{ V}$                                  | -4                  |                     |          | mA               |
|                                    |   | $V_{ISOIN} = 3.3\text{ V}$                                | -2                  |                     |          | mA               |
|                                    |   | $V_{ISOIN} = 2.5\text{ V}$                                | -1                  |                     |          | mA               |
|                                    |   | $V_{ISOIN} = 1.8\text{ V}$                                | -1                  |                     |          | mA               |
| $I_{OL}$                           | Low level output current <sup>(1)</sup>                   | $V_{ISOIN} = 5\text{ V}$                                  |                     |                     | 4        | mA               |
|                                    |   | $V_{ISOIN} = 3.3\text{ V}$                                |                     |                     | 2        | mA               |
|                                    |   | $V_{ISOIN} = 2.5\text{ V}$                                |                     |                     | 1        | mA               |
|                                    |   | $V_{ISOIN} = 1.8\text{ V}$                                |                     |                     | 1        | mA               |
| $V_{IH}$                           | High-level input voltage <sup>(2)</sup>                   |   | $0.7 \times V_{SI}$ |                     | $V_{SI}$ | V                |
| $V_{IL}$                           | Low-level input voltage                                   |   | 0                   | $0.3 \times V_{SI}$ |          | V                |
| DR                                 | Data rate   |   |                     |                     | 100      | Mbps             |
| $t_{PWRUP}$                        | Channel isolator ready after power up or EN/FLT high      | $V_{ISOIN} > V_{IO(UVLO+)}$                               | 5                   |                     |          | ms               |
| $T_A$                              | Ambient temperature                                       |   | -40                 |                     | 125      | $^\circ\text{C}$ |

(1) This current is for data output channel.

(2)  $V_{SI}$  = input side supply;  $V_{SO}$  = output side supply

(3) The channel outputs are in undetermined state when  $1.89\text{ V} < V_{SI} < 2.25\text{ V}$  and  $1.05\text{ V} < V_{SI} < 1.71\text{ V}$

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | ISOW774x-Q1 | UNIT |
|-------------------------------|--|-------------|------|
|                               |  | DFM (SOIC)  |      |
|                               |  | 20 PINS     |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 68.5        | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 24.6        | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 53.7        | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 17.1        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 50.9        | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | —           | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 7.5 Power Ratings

$V_{DD} = V_{IO} = 5.5\text{ V}$ ,  $I_{ISO} = 110\text{ mA}$ ,  $T_J = 150^\circ\text{C}$ ,  $T_A \leq 80^\circ\text{C}$ ,  $C_L = 15\text{ pF}$ , input a 50-MHz 50% duty-cycle square wave

| PARAMETER |  | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|-----------|--|--|-----|-----|------|------|
| $P_D$     | Maximum power dissipation (both sides) | $V_{DD} = 5.5\text{ V}$ , $V_{IO} = 5.5\text{ V}$ , $V_{ISOOUT} = V_{ISOIN}$ , $I_{ISOOUT} = 100\text{ mA}$ , $T_J = 150^\circ\text{C}$ , $T_A \leq 80^\circ\text{C}$ , $C_L = 15\text{ pF}$ , input a 50-MHz 50% duty-cycle square wave |     |     | 1.48 | W    |
| $P_{D1}$  | Maximum power dissipation (side-1)     |  |     |     | 0.74 | W    |
| $P_{D2}$  | Maximum power dissipation (side-2)     |  |     |     | 0.74 | W    |



## 7.6 Insulation Specifications

| PARAMETER                                      |   | TEST CONDITIONS  | VALUE              | UNIT             |
|--|---|--|--------------------|------------------|
| <b>GENERAL</b>                                 |   |  |                    |                  |
| CLR  | External clearance <sup>(1)</sup>                   | Shortest terminal-to-terminal distance through air   | >8                 | mm               |
| CPG  | External creepage <sup>(1)</sup>                    | Shortest terminal-to-terminal distance across the package surface  | >8                 | mm               |
| DTI  | Distance through the insulation                     | Minimum internal gap (internal clearance – capacitive signal isolation)  | > 17               | µm               |
|  |   | Minimum internal gap (internal clearance – transformer power isolation)  | >120               |                  |
| CTI  | Comparative tracking index                          | DIN EN 60112 (VDE 0303-11); IEC 60112  | > 600              | V                |
|  | Material group                                      | According to IEC 60664-1   | I                  |                  |
|  | Overvoltage category per IEC 60664-1                | Rated mains voltage ≤ 300 V <sub>RMS</sub>   | I-IV               |                  |
|  |   | Rated mains voltage ≤ 600 V <sub>RMS</sub>   | I-IV               |                  |
|  |   | Rated mains voltage ≤ 1000 V <sub>RMS</sub>  | I-III              |                  |
| <b>DIN VDE V 0884-11:2017-01<sup>(2)</sup></b> |   |  |                    |                  |
| V <sub>IORM</sub>                              | Maximum repetitive peak isolation voltage           | AC voltage (bipolar)   | 1500               | V <sub>PK</sub>  |
| V <sub>IOWM</sub>                              | Maximum working isolation voltage                   | AC voltage; Time dependent dielectric breakdown (TDDB) Test  | 1000               | V <sub>RMS</sub> |
|  |   | DC voltage   | 1500               | V <sub>DC</sub>  |
| V <sub>IOTM</sub>                              | Maximum transient isolation voltage                 | V <sub>TEST</sub> = V <sub>IOTM</sub> ; t = 60 s (qualification);<br>V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> ; t = 1 s (100% production)   | 7071               | V <sub>PK</sub>  |
| V <sub>IOSM</sub>                              | Maximum surge isolation voltage <sup>(3)</sup>      | Test method per IEC 62368-1, 1.2/50 µs waveform,<br>V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 10000 V <sub>PK</sub> (qualification)  | 6250               | V <sub>PK</sub>  |
| q <sub>pd</sub>                                | Apparent charge <sup>(4)</sup>                      | Method a, after input/output safety test subgroup 2/3,<br>V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s;<br>V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s                              | ≤ 5                | pC               |
|  |   | Method a, after environmental tests subgroup 1,<br>V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s  | ≤ 5                |                  |
|  |   | Method b1, at routine test (100% production) and preconditioning (type test),<br>V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s;<br>V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> , t <sub>m</sub> = 1 s | ≤ 5                |                  |
| C <sub>IO</sub>                                | Barrier capacitance, input to output <sup>(5)</sup> | V <sub>IO</sub> = 0.4 × sin(2πft), f = 1 MHz   | ~3.5               | pF               |
| R <sub>IO</sub>                                | Insulation resistance <sup>(5)</sup>                | V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C   | > 10 <sup>12</sup> | Ω                |
|  |   | V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C  | > 10 <sup>11</sup> |                  |
|  |   | V <sub>IO</sub> = 500 V, T <sub>S</sub> = 150°C  | > 10 <sup>9</sup>  |                  |
|  | Pollution degree                                    |  | 2                  |                  |
|  | Climatic category                                   |  | 40/125/21          |                  |
| <b>UL 1577</b>                                 |   |  |                    |                  |
| V <sub>ISO(UL)</sub>                           | Withstand isolation voltage                         | V <sub>TEST</sub> = V <sub>ISO(UL)</sub> = 5000 V <sub>RMS</sub> , t = 60 s (qualification),<br>V <sub>TEST</sub> = 1.2 × V <sub>ISO(UL)</sub> = 6000 V <sub>RMS</sub> , t = 1 s (100% production)                             | 5000               | V <sub>RMS</sub> |

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) ISOW77xx is suitable for *safe electrical insulation* and ISOW77xxB is suitable for *basic electrical insulation* only within the safety ratings.. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).

(5) All pins on each side of the barrier tied together creating a two-terminal device.

## 7.7 Safety-Related Certifications

| VDE  | CSA  | UL   | CQC   | TUV  |
|--|--|--|---|--|
| Certified according to DIN EN IEC 60747-17 (VDE 0884-17)   | Certified according to IEC 62368-1, and IEC 60601-1  | Recognized under UL 1577 Component Recognition Program | Certified according to GB 4943.1-2011   | Certified according to EN 61010-1:2010/A1:2019 and EN 62368-1:2014   |
| Reinforced insulation; Maximum transient isolation voltage, 7071 V <sub>PK</sub> ; Maximum repetitive peak isolation voltage, 1500 V <sub>PK</sub> ; Maximum surge isolation voltage, 6250 V <sub>PK</sub> | CSA 62368-1-19 and IEC 62368-1:2018 Ed. 3 and EN 62368-1:2020. (pollution degree 2, material group I) 600 V <sub>RMS</sub> (Reinforced) maximum working voltage; 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3+A1, 250 V <sub>RMS</sub> maximum working voltage. Temperature rating is 90°C for reinforced insulation and 125°C for basic insulation; see certificate for details. | Single protection, 5000 V <sub>RMS</sub>               | Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V <sub>RMS</sub> maximum working voltage; | 5000 V <sub>RMS</sub> Reinforced insulation per EN 61010-1:2010 up to working voltage of 600 V <sub>RMS</sub> ; 5000 V <sub>RMS</sub> Reinforced insulation per EN 62368-1:2014 up to working voltage of 600 V <sub>RMS</sub> (Reinforced) |
| Certificate #: Pending   | Master Contract#: Pending  | File #: Pending  | Certificate #: Pending  | Client ID: Pending   |

## 7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER      |  | TEST CONDITIONS  | MIN | TYP | MAX  | UNIT |
|----------------|--|--|-----|-----|------|------|
| I <sub>S</sub> | Safety input, output, or supply current <sup>(1)</sup> | R <sub>θJA</sub> = 68.5°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C |     |     | 332  | mA   |
|                |  | R <sub>θJA</sub> = 68.5°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C |     |     | 507  |      |
| P <sub>S</sub> | Safety input, output, or total power <sup>(1)</sup>    | R <sub>θJA</sub> = 68.5°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C                         |     |     | 1825 | mW   |
| T <sub>S</sub> | Maximum safety temperature <sup>(1)</sup>              |  |     |     | 150  | °C   |

(1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use the following equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$ , where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$ , where T<sub>J(max)</sub> is the maximum allowed junction temperature.

$P_S = I_S \times V_I$ , where V<sub>I</sub> is the maximum input voltage.

## 7.9 Electrical Characteristics - Power Converter

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3.3\text{ V} \pm 10\%$  and  $V_{ISOIN}$  power externally, GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER   |   | TEST CONDITIONS   | MIN   | TYP | MAX   | UNIT |
|---|---|---|-------|-----|-------|------|
| <b><math>V_{DD} = 5\text{ V}</math>, <math>V_{ISOOUT} = 5\text{ V}</math>, <math>V_{SEL} = V_{ISOOUT}</math></b>      |   |   |       |     |       |      |
| $V_{ISOOUT}$  | Isolated supply voltage   | External $I_{ISOOUT} = 0$ to 55 mA  | 4.75  | 5   | 5.25  | V    |
| $V_{ISOOUT}$  | Isolated supply voltage   | External $I_{ISOOUT} = 0$ to 110 mA   | 4.5   | 5   | 5.25  | V    |
| $V_{ISOOUT(LINE)}$  | DC line regulation  | $I_{ISOOUT} = 55\text{ mA}$ , $V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$   |       | 2   |       | mV/V |
| $V_{ISOOUT(LOAD)}$  | DC load regulation  | $I_{ISOOUT} = 0$ to 110 mA  |       | 1%  |       |      |
| EFF   | Efficiency at maximum load current <sup>(3)</sup>                   | $I_{ISOOUT} = 110\text{ mA}$ , $C_{LOAD} = 0.01\text{ }\mu\text{F} \parallel 10\text{ }\mu\text{F}$ ; $V_I = V_{DD}$ (ISOW774x-Q1); $V_I = 0\text{ V}$ (ISOW774x-Q1 with F suffix). |       | 46% |       |      |
| $V_{ISOOUT(RIP)}$   | Output ripple on isolated supply (pk-pk)                            | 20-MHz bandwidth, $C_{LOAD} = 0.01\text{ }\mu\text{F} \parallel 20\text{ }\mu\text{F}$ , $I_{ISOOUT} = 110\text{ mA}$   |       | 24  |       | mV   |
| $I_{ISOOUT\_SC}$  | DC current from $V_{DD}$ supply under short circuit on $V_{ISOOUT}$ | $V_{ISOOUT}$ shorted to GND2  |       | 250 |       | mA   |
| <b><math>V_{DD} = 5\text{ V}</math>, <math>V_{ISOOUT} = 3.3\text{ V}</math>, <math>V_{SEL} = \text{GND2}</math></b>   |   |   |       |     |       |      |
| $V_{ISOOUT}$  | Isolated supply voltage   | External $I_{ISOOUT} = 0$ to 70 mA  | 3.135 | 3.3 | 3.465 | V    |
| $V_{ISOOUT}$  | Isolated supply voltage   | External $I_{ISOOUT} = 0$ to 140 mA   | 3.135 | 3.3 | 3.465 | V    |
| $V_{ISOOUT(LINE)}$  | DC line regulation  | $I_{ISOOUT} = 70\text{ mA}$ , $V_{DD} = 4.5\text{ V}$ to $5.5\text{ V}$   |       | 2   |       | mV/V |
| $V_{ISOOUT(LOAD)}$  | DC load regulation  | $I_{ISOOUT} = 0$ to 140 mA  |       | 1%  |       |      |
| EFF   | Efficiency at maximum load current <sup>(3)</sup>                   | $I_{ISOOUT} = 140\text{ mA}$ , $C_{LOAD} = 0.01\text{ }\mu\text{F} \parallel 10\text{ }\mu\text{F}$ ; $V_I = V_{DD}$ (ISOW774x-Q1); $V_I = 0\text{ V}$ (ISOW774x-Q1 with F suffix). |       | 36% |       |      |
| $V_{ISOOUT(RIP)}$   | Output ripple on isolated supply (pk-pk)                            | 20-MHz bandwidth, $C_{LOAD} = 0.01\text{ }\mu\text{F} \parallel 20\text{ }\mu\text{F}$ , $I_{ISOOUT} = 110\text{ mA}$   |       | 30  |       | mV   |
| $I_{ISOOUT\_SC}$  | DC current from $V_{DD}$ supply under short circuit on $V_{ISOOUT}$ | $V_{ISOOUT}$ shorted to GND2  |       | 250 |       | mA   |
| <b><math>V_{DD} = 3.3\text{ V}</math>, <math>V_{ISOOUT} = 3.3\text{ V}</math>, <math>V_{SEL} = \text{GND2}</math></b> |   |   |       |     |       |      |
| $V_{ISOOUT}$  | Isolated supply voltage   | External $I_{ISOOUT} = 0$ to 30 mA  | 3.135 | 3.3 | 3.465 | V    |
| $V_{ISOOUT}$  | Isolated supply voltage   | External $I_{ISOOUT} = 0$ to 60 mA  | 3.135 | 3.3 | 3.465 | V    |
| $V_{ISOOUT(LINE)}$  | DC line regulation  | $I_{ISOOUT} = 30\text{ mA}$ , $V_{DD} = 3.0\text{ V}$ to $3.6\text{ V}$   |       | 2   |       | mV/V |
| $V_{ISOOUT(LOAD)}$  | DC load regulation  | $I_{ISOOUT} = 0$ to 60 mA   |       | 1%  |       |      |
| EFF   | Efficiency at maximum load current <sup>(3)</sup>                   | $I_{ISOOUT} = 60\text{ mA}$ , $C_{LOAD} = 0.01\text{ }\mu\text{F} \parallel 10\text{ }\mu\text{F}$ ; $V_I = V_{DD}$ (ISOW774x-Q1); $V_I = 0\text{ V}$ (ISOW774x-Q1 with F suffix).  |       | 43% |       |      |
| $V_{ISOOUT(RIP)}$   | Output ripple on isolated supply (pk-pk)                            | 20-MHz bandwidth, $C_{LOAD} = 0.01\text{ }\mu\text{F} \parallel 20\text{ }\mu\text{F}$ , $I_{ISOOUT} = 60\text{ mA}$  |       | 14  |       | mV   |
| $I_{ISOOUT\_SC}$  | DC current from $V_{DD}$ supply under short circuit on $V_{ISOOUT}$ | $V_{ISOOUT}$ shorted to GND2  |       | 185 |       | mA   |

- (1) Power converter  $I_{LOAD}$  = current required to power the secondary side.  $I_{LOAD}$  does not take into account the channel isolator current. See Supply Current Characteristics Channel Isolator section for details.

## 7.10 Supply Current Characteristics - Power Converter

$V_{DD} = 5\text{ V} \pm 10\%$  or  $3.3\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions unless otherwise noted).

| PARAMETER                                     | TEST CONDITIONS                                   |                            | SUPPLY CURRENT | MIN | TYP  | MAX  | UNIT |
|---|---|----------------------------|----------------|-----|------|------|------|
| <b>Power Converter Disabled</b>               |   |                            |                |     |      |      |      |
| Power converter supply current                | EN/FLT = GND1, $V_{ISOOUT} = \text{No } I_{LOAD}$ |                            | $I_{DD}$       |     | 0.28 | 0.45 | mA   |
| Logic supply current                          | EN/FLT = GND1                                     |                            | $I_{IO}$       |     | 0.27 | 0.57 | mA   |
| <b>Power Converter Enabled</b>                |   |                            |                |     |      |      |      |
| Power converter supply current input          | $V_{DD} = 5\text{ V}$ , $V_{SEL} = V_{ISOOUT}$    | $I_{LOAD} = 55\text{ mA}$  | $I_{DD}$       |     | 115  | 171  | mA   |
|   | $V_{DD} = 5\text{ V}$ , $V_{SEL} = V_{ISOOUT}$    | $I_{LOAD} = 110\text{ mA}$ |                |     | 225  | 316  | mA   |
|   | $V_{DD} = 5\text{ V}$ , $V_{SEL} = \text{GND2}$   | $I_{LOAD} = 70\text{ mA}$  |                |     | 127  | 169  | mA   |
|   | $V_{DD} = 5\text{ V}$ , $V_{SEL} = \text{GND2}$   | $I_{LOAD} = 140\text{ mA}$ |                |     | 250  | 310  | mA   |
|   | $V_{DD} = 3.3\text{ V}$ , $V_{SEL} = \text{GND2}$ | $I_{LOAD} = 30\text{ mA}$  |                |     | 74   | 112  | mA   |
|   | $V_{DD} = 3.3\text{ V}$ , $V_{SEL} = \text{GND2}$ | $I_{LOAD} = 60\text{ mA}$  |                |     | 143  | 216  | mA   |
| Power converter output current <sup>(1)</sup> | $V_{DD} = 5\text{ V}$                             | $V_{SEL} = V_{ISOOUT}$     | $I_{ISOOUT}$   |     | 110  |      | mA   |
|   | $V_{DD} = 5\text{ V}$                             | $V_{SEL} = \text{GND2}$    |                |     | 140  |      | mA   |
|   | $V_{DD} = 3.3\text{ V}$                           | $V_{SEL} = \text{GND2}$    |                |     | 60   |      | mA   |

(1)  $I_{LOAD}$  does not take into account the channel isolator current. See Supply Current Characteristics Channel Isolator section for details.

### 7.11 Electrical Characteristics Channel Isolator - $V_{IO}, V_{ISOIN} = 5\text{-V}$

$V_{IO}, V_{ISOIN} = 5\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                |                                      | TEST CONDITIONS   | MIN                  | TYP | MAX                 | UNIT          |
|--------------------------|--------------------------------------|---|----------------------|-----|---------------------|---------------|
| <b>Channel Isolation</b> |                                      |   |                      |     |                     |               |
| $V_{ITH}$                | Input pin rising threshold           |   |                      |     | $0.7 \times V_{SI}$ | V             |
| $V_{ITL}$                | Input pin falling threshold          |   | $0.3 \times V_{SI}$  |     |                     | V             |
| $V_{I(HYS)}$             | Input pin threshold hysteresis (INx) |   | $0.1 \times V_{SI}$  |     |                     | V             |
| $I_{IL}$                 | Low level input current              | $V_{IL} = 0$ at INx   | -25                  |     |                     | $\mu\text{A}$ |
| $I_{IH}$                 | High level input current             | $V_{IH} = V_{SI}^{(1)}$ at INx  |                      |     | 25                  | $\mu\text{A}$ |
| $V_{OH}$                 | High level output voltage            | $I_O = -4\text{ mA}$ , see <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>                     | $V_{SO}^{(1)} - 0.4$ |     |                     | V             |
| $V_{OL}$                 | Low level output voltage             | $I_O = 4\text{ mA}$ , see <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>                      |                      |     | 0.4                 | V             |
| CMTI                     | Common mode transient immunity       | $V_I = V_{SI}$ or $0\text{ V}$ , $V_{CM} = 1000\text{ V}$ ; see <a href="#">Common-Mode Transient Immunity Test Circuit</a> | 85                   | 100 |                     | kV/us         |

(1)  $V_{SI}$  = input side supply;  $V_{SO}$  = output side supply

### 7.12 Supply Current Characteristics Channel Isolator - $V_{IO}, V_{ISOIN} = 5\text{-V}$

$V_{IO}, V_{ISOIN} = 5\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                                 | TEST CONDITIONS   | SUPPLY CURRENT | MIN          | TYP | MAX  | UNIT |    |
|---|---|----------------|--------------|-----|------|------|----|
| <b>ISOW7741-Q1 Channel Supply Current</b> |   |                |              |     |      |      |    |
| Supply current - Disable                  | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = V_{CCI}^{(1)}$ (ISOW7741-Q1);<br>$V_I = 0\text{ V}$ (ISOW7741-Q1 with F suffix) | $I_{DD\_IO}$   |              | 2.8 | 4.1  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 4.3 | 6.3  | mA   |    |
|   | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = 0\text{ V}$ (ISOW7741-Q1);<br>$V_I = V_{CCI}$ (ISOW7741-Q1 with F suffix)       | $I_{DD\_IO}$   |              | 2.8 | 4.1  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 4.3 | 6.3  | mA   |    |
| Channel Supply current - DC signal        | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = V_{CCI}$ (ISOW7741-Q1);<br>$V_I = 0\text{ V}$ (ISOW7741-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 2.8 | 4.1  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 4.3 | 6.3  | mA   |    |
|   | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = 0\text{ V}$ (ISOW7741-Q1);<br>$V_I = V_{CCI}$ (ISOW7741-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 6.1 | 8.4  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 5.5 | 7.9  | mA   |    |
| Channel Supply current - AC signal        | All channels switching with square wave clock input; $C_L = 15\text{ pF}$   | 1 Mbps         | $I_{DD\_IO}$ |     | 4.4  | 6.3  | mA |
|   |   |                | $I_{ISOIN}$  |     | 4.9  | 7.1  | mA |
|   |   | 10 Mbps        | $I_{DD\_IO}$ |     | 5    | 7    | mA |
|   |   |                | $I_{ISOIN}$  |     | 6.3  | 8.9  | mA |
|   |   | 100 Mbps       | $I_{DD\_IO}$ |     | 12.2 | 14.2 | mA |
|   |   |                | $I_{ISOIN}$  |     | 25   | 32   | mA |
| <b>ISOW7742-Q1 Channel Supply Current</b> |   |                |              |     |      |      |    |
| Supply current - Disable                  | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = V_{CCI}^{(1)}$ (ISOW7742-Q1);<br>$V_I = 0\text{ V}$ (ISOW7742-Q1 with F suffix) | $I_{DD\_IO}$   |              | 3.1 | 4.7  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.9 | 5.6  | mA   |    |
|   | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix)       | $I_{DD\_IO}$   |              | 3.1 | 4.7  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.9 | 5.6  | mA   |    |
| Channel Supply current - DC signal        | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = V_{CCI}$ (ISOW7742-Q1);<br>$V_I = 0\text{ V}$ (ISOW7742-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 3.1 | 4.7  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.9 | 5.6  | mA   |    |
|   | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 5.4 | 7.7  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 6.2 | 8.5  | mA   |    |

$V_{IO}, V_{ISOIN} = 5\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                          | TEST CONDITIONS   | SUPPLY CURRENT | MIN          | TYP   | MAX | UNIT |
|------------------------------------|---|----------------|--------------|-------|-----|------|
| Channel Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15\text{ pF}$ | 1 Mbps         | $I_{DD\_IO}$ | 4.2   | 6.3 | mA   |
|                                    |   |                | $I_{ISOIN}$  | 5.1   | 7.2 | mA   |
|                                    |   | 10 Mbps        | $I_{DD\_IO}$ | 5.5   | 7.6 | mA   |
|                                    |   |                | $I_{ISOIN}$  | 6.3   | 8.3 | mA   |
|                                    |   | 100 Mbps       | $I_{DD\_IO}$ | 16.7  | 20  | mA   |
|                                    |   |                | $I_{ISOIN}$  | 17.33 | 22  | mA   |

(1)  $V_{CCI} = V_{IO}$  or  $V_{ISOIN}$

### 7.13 Electrical Characteristics Channel Isolator - $V_{IO}, V_{ISOIN} = 3.3\text{-V}$

$V_{IO}, V_{ISOIN} = 3.3\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                |                                      | TEST CONDITIONS   | MIN                  | TYP                 | MAX | UNIT          |
|--------------------------|--------------------------------------|---|----------------------|---------------------|-----|---------------|
| <b>Channel Isolation</b> |                                      |   |                      |                     |     |               |
| $V_{ITH}$                | Input pin rising threshold           |   |                      | $0.7 \times V_{SI}$ |     | V             |
| $V_{ITL}$                | Input pin falling threshold          |   | $0.3 \times V_{SI}$  |                     |     | V             |
| $V_{I(HYS)}$             | Input pin threshold hysteresis (INx) |   | $0.1 \times V_{SI}$  |                     |     | V             |
| $I_{IL}$                 | Low level input current              | $V_{IL} = 0$ at INx   | -25                  |                     |     | $\mu\text{A}$ |
| $I_{IH}$                 | High level input current             | $V_{IH} = V_{SI}^{(1)}$ at INx  |                      |                     | 25  | $\mu\text{A}$ |
| $V_{OH}$                 | High level output voltage            | $I_O = -2\text{ mA}$ , see <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>                     | $V_{SO}^{(1)} - 0.3$ |                     |     | V             |
| $V_{OL}$                 | Low level output voltage             | $I_O = 2\text{ mA}$ , see <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>                      |                      |                     | 0.3 | V             |
| CMTI                     | Common mode transient immunity       | $V_I = V_{SI}$ or $0\text{ V}$ , $V_{CM} = 1000\text{ V}$ ; see <a href="#">Common-Mode Transient Immunity Test Circuit</a> | 85                   | 100                 |     | kV/us         |

(1)  $V_{SI}$  = input side supply;  $V_{SO}$  = output side supply

### 7.14 Supply Current Characteristics Channel Isolator - $V_{IO}, V_{ISOIN} = 3.3\text{-V}$

$V_{IO}, V_{ISOIN} = 3.3\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                                 | TEST CONDITIONS   | SUPPLY CURRENT | MIN          | TYP | MAX  | UNIT |    |
|---|---|----------------|--------------|-----|------|------|----|
| <b>ISOW7741-Q1 Channel Supply Current</b> |   |                |              |     |      |      |    |
| Supply current - Disable                  | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = V_{CCI}^{(1)}$ (ISOW7741-Q1);<br>$V_I = 0\text{ V}$ (ISOW7741-Q1 with F suffix) | $I_{DD\_IO}$   |              | 2.8 | 4    | mA   |    |
|   |   | $I_{ISOIN}$    |              | 4.2 | 6.3  | mA   |    |
|   | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = 0\text{ V}$ (ISOW7741-Q1);<br>$V_I = V_{CCI}$ (ISOW7741-Q1 with F suffix)       | $I_{DD\_IO}$   |              | 2.8 | 4    | mA   |    |
|   |   | $I_{ISOIN}$    |              | 4.2 | 6.3  | mA   |    |
| Channel Supply current - DC signal        | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = V_{CCI}$ (ISOW7741-Q1);<br>$V_I = 0\text{ V}$ (ISOW7741-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 2.8 | 4    | mA   |    |
|   |   | $I_{ISOIN}$    |              | 4.2 | 6.3  | mA   |    |
|   | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = 0\text{ V}$ (ISOW7741-Q1);<br>$V_I = V_{CCI}$ (ISOW7741-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 6.1 | 8.3  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 5.5 | 7.9  | mA   |    |
| Channel Supply current - AC signal        | All channels switching with square wave clock input; $C_L = 15\text{ pF}$   | 1 Mbps         | $I_{DD\_IO}$ |     | 4.4  | 6.3  | mA |
|   |   |                | $I_{ISOIN}$  |     | 4.9  | 7.1  | mA |
|   |   | 10 Mbps        | $I_{DD\_IO}$ |     | 4.8  | 6.7  | mA |
|   |   |                | $I_{ISOIN}$  |     | 5.9  | 8.3  | mA |
|   |   | 100 Mbps       | $I_{DD\_IO}$ |     | 9.4  | 12   | mA |
|   |   |                | $I_{ISOIN}$  |     | 17.5 | 25   | mA |
| <b>ISOW7742-Q1 Channel Supply Current</b> |   |                |              |     |      |      |    |
| Supply current - Disable                  | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = V_{CCI}^{(1)}$ (ISOW7742-Q1);<br>$V_I = 0\text{ V}$ (ISOW7742-Q1 with F suffix) | $I_{DD\_IO}$   |              | 3.1 | 4.6  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.9 | 5.5  | mA   |    |
|   | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix)       | $I_{DD\_IO}$   |              | 3.1 | 4.6  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.9 | 5.5  | mA   |    |
| Channel Supply current - DC signal        | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = V_{CCI}$ (ISOW7742-Q1);<br>$V_I = 0\text{ V}$ (ISOW7742-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 3.1 | 4.6  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.9 | 5.5  | mA   |    |
|   | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 5.4 | 7.6  | mA   |    |
|   |   | $I_{ISOIN}$    |              | 6.2 | 8.5  | mA   |    |

$V_{IO}, V_{ISOIN} = 3.3\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                          | TEST CONDITIONS   | SUPPLY CURRENT | MIN          | TYP  | MAX  | UNIT |
|------------------------------------|---|----------------|--------------|------|------|------|
| Channel Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15\text{ pF}$ | 1 Mbps         | $I_{DD\_IO}$ | 4.2  | 6.3  | mA   |
|                                    |   |                | $I_{ISOIN}$  | 5.1  | 7.2  | mA   |
|                                    |   | 10 Mbps        | $I_{DD\_IO}$ | 4.9  | 7    | mA   |
|                                    |   |                | $I_{ISOIN}$  | 5.7  | 7.9  | mA   |
|                                    |   | 100 Mbps       | $I_{DD\_IO}$ | 13   | 16.6 | mA   |
|                                    |   |                | $I_{ISOIN}$  | 13.7 | 17.5 | mA   |

(1)  $V_{CCI} = V_{IO}$  or  $V_{ISOIN}$



### 7.15 Electrical Characteristics Channel Isolator - $V_{IO}, V_{ISOIN} = 2.5\text{-V}$

$V_{IO}, V_{ISOIN} = 2.5\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                |                                      | TEST CONDITIONS   | MIN                  | TYP | MAX                 | UNIT          |
|--------------------------|--------------------------------------|---|----------------------|-----|---------------------|---------------|
| <b>Channel Isolation</b> |                                      |   |                      |     |                     |               |
| $V_{ITH}$                | Input pin rising threshold           |   |                      |     | $0.7 \times V_{SI}$ | V             |
| $V_{ITL}$                | Input pin falling threshold          |   | $0.3 \times V_{SI}$  |     |                     | V             |
| $V_{I(HYS)}$             | Input pin threshold hysteresis (INx) |   | $0.1 \times V_{SI}$  |     |                     | V             |
| $I_{IL}$                 | Low level input current              | $V_{IL} = 0$ at INx   | -25                  |     |                     | $\mu\text{A}$ |
| $I_{IH}$                 | High level input current             | $V_{IH} = V_{SI}^{(1)}$ at INx  |                      |     | 25                  | $\mu\text{A}$ |
| $V_{OH}$                 | High level output voltage            | $I_O = -1\text{ mA}$ , see <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>                     | $V_{SO}^{(1)} - 0.1$ |     |                     | V             |
| $V_{OL}$                 | Low level output voltage             | $I_O = 1\text{ mA}$ , see <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>                      |                      |     | 0.1                 | V             |
| CMTI                     | Common mode transient immunity       | $V_I = V_{SI}$ or $0\text{ V}$ , $V_{CM} = 1000\text{ V}$ ; see <a href="#">Common-Mode Transient Immunity Test Circuit</a> | 85                   | 100 |                     | kV/us         |

(1)  $V_{SI}$  = input side supply;  $V_{SO}$  = output side supply

### 7.16 Supply Current Characteristics Channel Isolator - $V_{IO}, V_{ISOIN} = 2.5\text{-V}$

$V_{IO}, V_{ISOIN} = 2.5\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER  | TEST CONDITIONS   | SUPPLY CURRENT | MIN          | TYP | MAX  | UNIT |    |
|--|---|----------------|--------------|-----|------|------|----|
| <b>ISOW7741-Q1 Channel Supply Current</b>  |   |                |              |     |      |      |    |
| Supply current - Disable   | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = V_{CCI}^{(1)}$ (ISOW7741-Q1);<br>$V_I = 0\text{ V}$ (ISOW7741-Q1 with F suffix) | $I_{DD\_IO}$   |              | 2.7 | 4.3  | mA   |    |
|  |   | $I_{ISOIN}$    |              | 4.2 | 6.3  | mA   |    |
| Channel Supply current - DC signal   | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = 0\text{ V}$ (ISOW7741-Q1);<br>$V_I = V_{CCI}$ (ISOW7741-Q1 with F suffix)       | $I_{DD\_IO}$   |              | 2.7 | 4.3  | mA   |    |
|  |   | $I_{ISOIN}$    |              | 4.2 | 6.3  | mA   |    |
|  | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = 0\text{ V}$ (ISOW7741-Q1);<br>$V_I = V_{CCI}$ (ISOW7741-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 6.1 | 8.3  | mA   |    |
|  |   | $I_{ISOIN}$    |              | 5.4 | 7.9  | mA   |    |
| Channel Supply current - AC signal   | All channels switching with square wave clock input; $C_L = 15\text{ pF}$   | 1 Mbps         | $I_{DD\_IO}$ |     | 4.4  | 6.3  | mA |
|  |   |                | $I_{ISOIN}$  |     | 4.9  | 7.1  | mA |
|  |   | 10 Mbps        | $I_{DD\_IO}$ |     | 4.7  | 8.3  | mA |
|  |   |                | $I_{ISOIN}$  |     | 5.6  | 7.9  | mA |
|  |   | 100 Mbps       | $I_{DD\_IO}$ |     | 8.2  | 11.2 | mA |
|  |   |                | $I_{ISOIN}$  |     | 14.6 | 18.8 | mA |
| <b>ISOW7742-Q1 Channel Supply Current</b>  |   |                |              |     |      |      |    |
| Supply current - Disable   | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = V_{CCI}^{(1)}$ (ISOW7742-Q1);<br>$V_I = 0\text{ V}$ (ISOW7742-Q1 with F suffix) | $I_{DD\_IO}$   |              | 3.1 | 4.6  | mA   |    |
|  |   | $I_{ISOIN}$    |              | 3.8 | 5.5  | mA   |    |
| Channel Supply current - DC signal   | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix)       | $I_{DD\_IO}$   |              | 3.1 | 4.6  | mA   |    |
|  |   | $I_{ISOIN}$    |              | 3.8 | 5.5  | mA   |    |
|  | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 3.1 | 4.6  | mA   |    |
|  |   | $I_{ISOIN}$    |              | 3.8 | 5.4  | mA   |    |
| $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix) | $I_{DD\_IO}$  |                | 5.3          | 7.5 | mA   |      |    |
|  | $I_{ISOIN}$   |                | 6.1          | 8.4 | mA   |      |    |

$V_{IO}, V_{ISOIN} = 2.5\text{ V} \pm 10\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                          | TEST CONDITIONS   | SUPPLY CURRENT | MIN          | TYP  | MAX  | UNIT |
|------------------------------------|---|----------------|--------------|------|------|------|
| Channel Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15\text{ pF}$ | 1 Mbps         | $I_{DD\_IO}$ | 4.2  | 6.3  | mA   |
|                                    |   |                | $I_{ISOIN}$  | 5.1  | 7.2  | mA   |
|                                    |   | 10 Mbps        | $I_{DD\_IO}$ | 4.7  | 6.8  | mA   |
|                                    |   |                | $I_{ISOIN}$  | 5.6  | 7.7  | mA   |
|                                    |   | 100 Mbps       | $I_{DD\_IO}$ | 10.9 | 14.5 | mA   |
|                                    |   |                | $I_{ISOIN}$  | 11.7 | 15.5 | mA   |

(1)  $V_{CCI} = V_{IO}$  or  $V_{ISOIN}$

### 7.17 Electrical Characteristics Channel Isolator - $V_{IO}$ , $V_{ISOIN} = 1.8\text{-V}$

$V_{IO}$ ,  $V_{ISOIN} = 1.8\text{ V} \pm 5\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                |                                      | TEST CONDITIONS   | MIN                  | TYP | MAX                 | UNIT          |
|--------------------------|--------------------------------------|---|----------------------|-----|---------------------|---------------|
| <b>Channel Isolation</b> |                                      |   |                      |     |                     |               |
| $V_{ITH}$                | Input pin rising threshold           |   |                      |     | $0.7 \times V_{SI}$ | V             |
| $V_{ITL}$                | Input pin falling threshold          |   | $0.3 \times V_{SI}$  |     |                     | V             |
| $V_{I(HYS)}$             | Input pin threshold hysteresis (INx) |   | $0.1 \times V_{SI}$  |     |                     | V             |
| $I_{IL}$                 | Low level input current              | $V_{IL} = 0$ at INx   | -25                  |     |                     | $\mu\text{A}$ |
| $I_{IH}$                 | High level input current             | $V_{IH} = V_{SI}^{(1)}$ at INx  |                      |     | 25                  | $\mu\text{A}$ |
| $V_{OH}$                 | High level output voltage            | $I_O = -1\text{ mA}$ , see <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>                     | $V_{SO}^{(1)} - 0.1$ |     |                     | V             |
| $V_{OL}$                 | Low level output voltage             | $I_O = 1\text{ mA}$ , see <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>                      |                      |     | 0.1                 | V             |
| CMTI                     | Common mode transient immunity       | $V_I = V_{SI}$ or $0\text{ V}$ , $V_{CM} = 1000\text{ V}$ ; see <a href="#">Common-Mode Transient Immunity Test Circuit</a> | 85                   | 100 |                     | kV/us         |

(1)  $V_{SI}$  = input side supply;  $V_{SO}$  = output side supply

### 7.18 Supply Current Characteristics Channel Isolator - $V_{IO}$ , $V_{ISOIN} = 1.8\text{-V}$

$V_{IO}$ ,  $V_{ISOIN} = 1.8\text{ V} \pm 5\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                                 | TEST CONDITIONS   | SUPPLY CURRENT | MIN          | TYP | MAX | UNIT |    |
|---|---|----------------|--------------|-----|-----|------|----|
| <b>ISOW7741-Q1 Channel Supply Current</b> |   |                |              |     |     |      |    |
| Supply current - Disable                  | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = V_{CCI}^{(1)}$ (ISOW7741-Q1);<br>$V_I = 0\text{ V}$ (ISOW7741-Q1 with F suffix) | $I_{DD\_IO}$   |              | 2.4 | 3.6 | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.8 | 5.6 | mA   |    |
| Channel Supply current - DC signal        | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = 0\text{ V}$ (ISOW7741-Q1);<br>$V_I = V_{CCI}$ (ISOW7741-Q1 with F suffix)       | $I_{DD\_IO}$   |              | 2.4 | 3.6 | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.8 | 5.6 | mA   |    |
| Channel Supply current - AC signal        | All channels switching with square wave clock input; $C_L = 15\text{ pF}$   | 1 Mbps         | $I_{DD\_IO}$ |     | 4   | 5.7  | mA |
|   |   |                | $I_{ISOIN}$  |     | 4.4 | 6.5  | mA |
|   |   | 10 Mbps        | $I_{DD\_IO}$ |     | 4.2 | 6    | mA |
|   |   |                | $I_{ISOIN}$  |     | 5.2 | 7.3  | mA |
|   |   | 100 Mbps       | $I_{DD\_IO}$ |     | 6.9 | 9.6  | mA |
|   |   |                | $I_{ISOIN}$  |     | 12  | 15.8 | mA |
| <b>ISOW7742-Q1 Channel Supply Current</b> |   |                |              |     |     |      |    |
| Supply current - Disable                  | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = V_{CCI}^{(1)}$ (ISOW7742-Q1);<br>$V_I = 0\text{ V}$ (ISOW7742-Q1 with F suffix) | $I_{DD\_IO}$   |              | 2.8 | 4.3 | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.4 | 5.1 | mA   |    |
| Channel Supply current - DC signal        | $EN_{IO1} = EN_{IO2} = 0\text{ V}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix)       | $I_{DD\_IO}$   |              | 2.8 | 4.3 | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.4 | 5.1 | mA   |    |
| Channel Supply current - DC signal        | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = V_{CCI}$ (ISOW7742-Q1);<br>$V_I = 0\text{ V}$ (ISOW7742-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 2.8 | 4.3 | mA   |    |
|   |   | $I_{ISOIN}$    |              | 3.4 | 5.1 | mA   |    |
| Channel Supply current - DC signal        | $EN_{IO1} = EN_{IO2} = V_{CCI}$ ; $V_I = 0\text{ V}$ (ISOW7742-Q1);<br>$V_I = V_{CCI}$ (ISOW7742-Q1 with F suffix)          | $I_{DD\_IO}$   |              | 5   | 7.4 | mA   |    |
|   |   | $I_{ISOIN}$    |              | 5.6 | 8.1 | mA   |    |

$V_{IO}, V_{ISOIN} = 1.8\text{ V} \pm 5\%$  GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions, unless otherwise specified)

| PARAMETER                          | TEST CONDITIONS   | SUPPLY CURRENT | MIN          | TYP | MAX  | UNIT |
|------------------------------------|---|----------------|--------------|-----|------|------|
| Channel Supply current - AC signal | All channels switching with square wave clock input; $C_L = 15\text{ pF}$ | 1 Mbps         | $I_{DD\_IO}$ | 4.2 | 6.3  | mA   |
|                                    |   |                | $I_{ISOIN}$  | 4.5 | 7.2  | mA   |
|                                    |   | 10 Mbps        | $I_{DD\_IO}$ | 4.3 | 6.6  | mA   |
|                                    |   |                | $I_{ISOIN}$  | 5.0 | 7.5  | mA   |
|                                    |   | 100 Mbps       | $I_{DD\_IO}$ | 9.1 | 12.5 | mA   |
|                                    |   |                | $I_{ISOIN}$  | 9.7 | 13.3 | mA   |

(1)  $V_{CCI} = V_{IO}$  or  $V_{ISOIN}$

## 7.19 Switching Characteristics - 5-V Supply

$V_{ISOIN} = 5\text{ V} \pm 10\%$ ,  $V_{IO} = 5\text{ V} \pm 10\%$ , GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions unless otherwise noted)

| PARAMETER                            |   | TEST CONDITIONS   | MIN | TYP  | MAX   | UNIT    |
|--------------------------------------|---|---|-----|------|-------|---------|
| $t_{PLH}$ , $t_{PHL}$                | Propagation delay time  | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  | 7.6 | 10.7 | 15.7  | ns      |
| PWD                                  | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $                                   |   |     | 0.9  | 5     | ns      |
| $ENIO\_t_{PLH}$ ,<br>$ENIO\_t_{PHL}$ | ENIO propagation delay time (opposite side)   | See <a href="#">Enable/Disable Propagation Delay Time Test Circuit and Waveform</a>   |     | 210  | 473.8 | ns      |
| $t_{sk(o)}$                          | Channel-to-channel output skew time <sup>(2)</sup>  | Same-direction channels   |     |      | 4     | ns      |
| $t_{sk(pp)}$                         | Part-to-part skew time <sup>(3)</sup>   |   |     |      | 5.5   | ns      |
| $t_r$                                | Output signal rise time   | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  |     | 2.5  | 3.6   | ns      |
| $t_f$                                | Output signal fall time   | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  |     | 2.4  | 3.5   | ns      |
| $t_{PHZ}$                            | Channel disable propagation delay, high-to-high impedance output                              | See <a href="#">Enable/Disable Propagation Delay Time Test Circuit and Waveform</a>   |     | 217  | 286   | ns      |
| $t_{PLZ}$                            | Channel disable propagation delay, low-to-high impedance output                               |   |     | 217  | 286   | ns      |
| $t_{PZH}$                            | Channel enable propagation delay, high impedance-to-high output for ISOW774x-Q1               |   |     | 237  | 333   | ns      |
|                                      | Channel enable propagation delay, high impedance-to-high output for ISOW774x-Q1 with F suffix |   |     | 237  | 333   | ns      |
| $t_{PZL}$                            | Channel enable propagation delay, high impedance-to-low output for ISOW774x-Q1                |   |     | 237  | 333   | ns      |
|                                      | Channel enable propagation delay, high impedance-to-low output for ISOW774x-Q1 with F suffix  |   |     | 237  | 333   | ns      |
| $t_{DO}$                             | Default output delay time from input power loss   | Measured from the time $V_{IO}$ or $V_{ISOIN}$ goes below 1.6 V at 10 mV/ns. See <a href="#">Default Output Delay Time Test Circuit and Voltage Waveforms</a> |     | 0.1  | 0.3   | $\mu$ s |
| $t_{ie}$                             | Time interval error   | $2^{16} - 1$ PRBS data at 100 Mbps  |     | 0.7  |       | ns      |

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 7.20 Switching Characteristics - 3.3-V Supply

$V_{ISOIN} = 3.3\text{ V} \pm 10\%$ ,  $V_{IO} = 3.3\text{ V} \pm 10\%$ , GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions unless otherwise noted)

| PARAMETER                            |   | TEST CONDITIONS   | MIN | TYP  | MAX   | UNIT    |
|--------------------------------------|---|---|-----|------|-------|---------|
| $t_{PLH}$ , $t_{PHL}$                | Propagation delay time  | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  | 6   | 11   | 16.2  | ns      |
| PWD                                  | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $                                   |   |     | 0.6  | 4.7   | ns      |
| ENIO_ $t_{PLH}$ ,<br>ENIO_ $t_{PHL}$ | ENIO propagation delay time (opposite side)   | See <a href="#">Enable/Disable Propagation Delay Time Test Circuit and Waveform</a>   |     | 220  | 474   | ns      |
| $t_{sk(o)}$                          | Channel-to-channel output skew time <sup>(2)</sup>  | Same-direction channels   |     |      | 4.1   | ns      |
| $t_{sk(pp)}$                         | Part-to-part skew time <sup>(3)</sup>   |   |     |      | 4.5   | ns      |
| $t_r$                                | Output signal rise time   | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  |     | 1.8  | 2.7   | ns      |
| $t_f$                                | Output signal fall time   |   |     | 1.6  | 2.4   | ns      |
| $t_{PHZ}$                            | Channel disable propagation delay, high-to-high impedance output                              | See <a href="#">Enable/Disable Propagation Delay Time Test Circuit and Waveform</a>   |     | 230  | 300.4 | ns      |
| $t_{PLZ}$                            | Channel disable propagation delay, low-to-high impedance output                               |   |     | 230  | 299.6 | ns      |
| $t_{PZH}$                            | Channel enable propagation delay, high impedance-to-high output for ISOW774x-Q1               |   |     | 226  | 318.9 | ns      |
|                                      | Channel enable propagation delay, high impedance-to-high output for ISOW774x-Q1 with F suffix |   |     | 226  | 319.1 | ns      |
| $t_{PZL}$                            | Channel enable propagation delay, high impedance-to-low output for ISOW774x-Q1                |   |     | 225  | 317.9 | ns      |
|                                      | Channel enable propagation delay, high impedance-to-low output for ISOW774x-Q1 with F suffix  |   |     | 225  | 317.6 | ns      |
| $t_{DO}$                             | Default output delay time from input power loss   | Measured from the time $V_{IO}$ or $V_{ISOIN}$ goes below 1.6 V at 10 mV/ns. See <a href="#">Default Output Delay Time Test Circuit and Voltage Waveforms</a> |     | 0.1  | 0.3   | $\mu$ s |
| $t_{ie}$                             | Time interval error   | $2^{16} - 1$ PRBS data at 100 Mbps  |     | 0.65 |       | ns      |

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 7.21 Switching Characteristics - 2.5-V Supply

$V_{ISOIN} = 2.5\text{ V} \pm 10\%$ ,  $V_{IO} = 2.5\text{ V} \pm 10\%$ , GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions unless otherwise noted)

| PARAMETER                            |   | TEST CONDITIONS   | MIN | TYP  | MAX  | UNIT    |
|--------------------------------------|---|---|-----|------|------|---------|
| $t_{PLH}$ , $t_{PHL}$                | Propagation delay time  | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  | 7.5 | 12   | 18   | ns      |
| PWD                                  | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $                                   |   |     | 0.36 | 5.1  | ns      |
| $ENIO\_t_{PLH}$ ,<br>$ENIO\_t_{PHL}$ | ENIO propagation delay time (opposite side)   | See <a href="#">Enable/Disable Propagation Delay Time Test Circuit and Waveform</a>   |     | 225  | 478  | ns      |
| $t_{sk(o)}$                          | Channel-to-channel output skew time <sup>(2)</sup>  | Same-direction channels   |     |      | 4.1  | ns      |
| $t_{sk(pp)}$                         | Part-to-part skew time <sup>(3)</sup>   |   |     |      | 6    | ns      |
| $t_r$                                | Output signal rise time   | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  |     | 2    | 3.26 | ns      |
| $t_f$                                | Output signal fall time   |   |     | 1.8  | 3.2  | ns      |
| $t_{PHZ}$                            | Channel disable propagation delay, high-to-high impedance output                              | See <a href="#">Enable/Disable Propagation Delay Time Test Circuit and Waveform</a>   |     | 237  | 326  | ns      |
| $t_{PLZ}$                            | Channel disable propagation delay, low-to-high impedance output                               |   |     | 236  | 325  | ns      |
| $t_{PZH}$                            | Channel enable propagation delay, high impedance-to-high output for ISOW774x-Q1               |   |     | 228  | 360  | ns      |
|                                      | Channel enable propagation delay, high impedance-to-high output for ISOW774x-Q1 with F suffix |   |     | 228  | 360  | ns      |
| $t_{PZL}$                            | Channel enable propagation delay, high impedance-to-low output for ISOW774x-Q1                |   |     | 227  | 350  | ns      |
|                                      | Channel enable propagation delay, high impedance-to-low output for ISOW774x-Q1 with F suffix  |   |     | 227  | 350  | ns      |
| $t_{DO}$                             | Default output delay time from input power loss   | Measured from the time $V_{IO}$ or $V_{ISOIN}$ goes below 1.6 V at 10 mV/ns. See <a href="#">Default Output Delay Time Test Circuit and Voltage Waveforms</a> |     | 0.1  | 0.3  | $\mu$ s |
| $t_{ie}$                             | Time interval error   | $2^{16} - 1$ PRBS data at 100 Mbps  |     | 0.7  |      | ns      |

(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 7.22 Switching Characteristics - 1.8-V Supply

$V_{ISOIN} = 1.8\text{ V} \pm 5\%$ ,  $V_{IO} = 1.8\text{ V} \pm 5\%$ , GND1 = GNDIO, GND2 = GISOIN (over recommended operating conditions unless otherwise noted)

| PARAMETER                            |   | TEST CONDITIONS   | MIN | TYP | MAX  | UNIT    |
|--------------------------------------|---|---|-----|-----|------|---------|
| $t_{PLH}$ , $t_{PHL}$                | Propagation delay time  | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  | 7.5 | 15  | 21.5 | ns      |
| PWD                                  | Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $                                   |   |     | 0   | 5.8  | ns      |
| ENIO_ $t_{PLH}$ ,<br>ENIO_ $t_{PHL}$ | ENIO propagation delay time (opposite side)   | See <a href="#">Enable/Disable Propagation Delay Time Test Circuit and Waveform</a>   |     | 243 | 475  | ns      |
| $t_{sk(o)}$                          | Channel-to-channel output skew time <sup>(2)</sup>  | Same-direction channels   |     |     | 4.1  | ns      |
| $t_{sk(pp)}$                         | Part-to-part skew time <sup>(3)</sup>   |   |     |     | 8.6  | ns      |
| $t_r$                                | Output signal rise time   | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  |     | 1.9 | 3    | ns      |
| $t_f$                                | Output signal fall time   | See <a href="#">Switching Characteristics Test Circuit and Voltage Waveforms</a>  |     | 1.8 | 3    | ns      |
| $t_{PHZ}$                            | Channel disable propagation delay, high-to-high impedance output                              | See <a href="#">Enable/Disable Propagation Delay Time Test Circuit and Waveform</a>   |     | 260 | 410  | ns      |
| $t_{PLZ}$                            | Channel disable propagation delay, low-to-high impedance output                               |   |     | 260 | 406  | ns      |
| $t_{PZH}$                            | Channel enable propagation delay, high impedance-to-high output for ISOW774x-Q1               |   |     | 240 | 444  | ns      |
|                                      | Channel enable propagation delay, high impedance-to-high output for ISOW774x-Q1 with F suffix |   |     | 240 | 444  | ns      |
| $t_{PZL}$                            | Channel enable propagation delay, high impedance-to-low output for ISOW774x-Q1                |   |     | 237 | 439  | ns      |
|                                      | Channel enable propagation delay, high impedance-to-low output for ISOW774x-Q1 with F suffix  |   |     | 237 | 439  | ns      |
| $t_{DO}$                             | Default output delay time from input power loss   | Measured from the time $V_{IO}$ or $V_{ISOIN}$ goes below 1.6 V at 10 mV/ns. See <a href="#">Default Output Delay Time Test Circuit and Voltage Waveforms</a> |     | 0.1 | 0.3  | $\mu$ s |
| $t_{ie}$                             | Time interval error   | $2^{16} - 1$ PRBS data at 100 Mbps  |     | 0.7 |      | ns      |

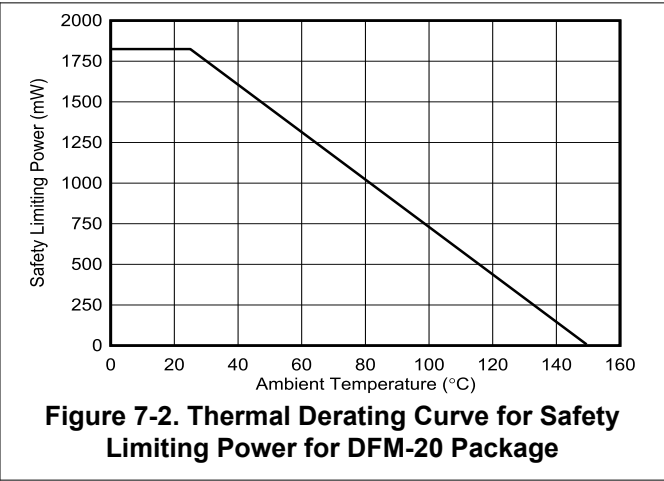
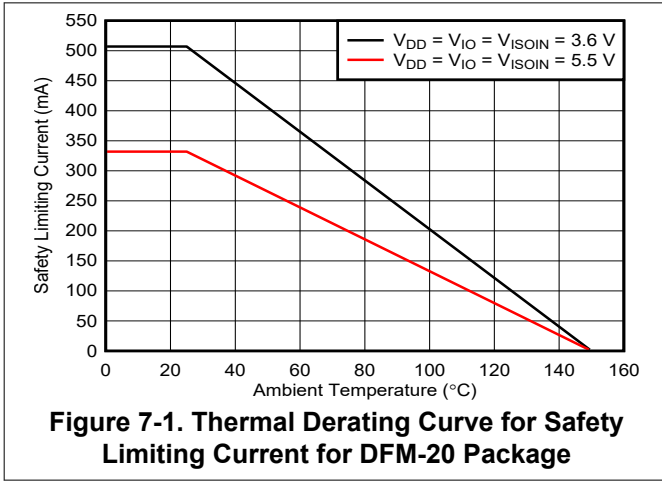
(1) Also known as pulse skew.

(2)  $t_{sk(o)}$  is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

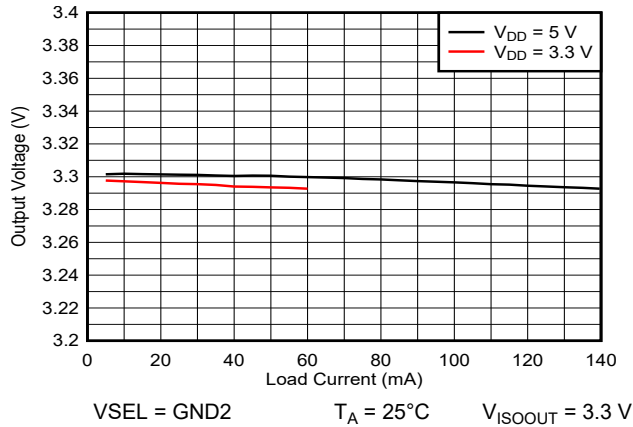
(3)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.



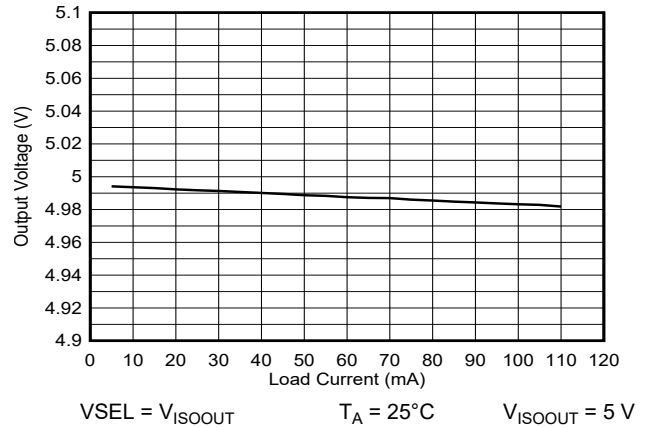
### 7.23 Insulation Characteristics Curves



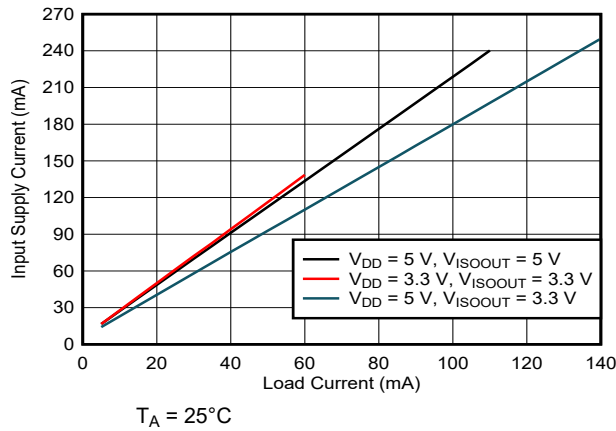
## 7.24 Typical Characteristics



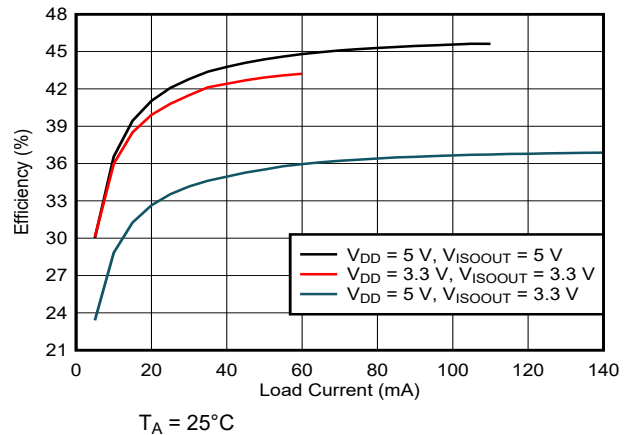
**Figure 7-3. Isolated Supply Voltage ( $V_{ISOOUT}$ ) vs Load Current ( $I_{ISOOUT}$ )**



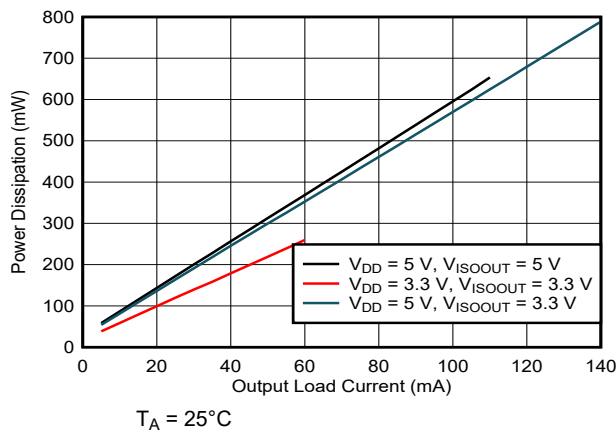
**Figure 7-4. Isolated Supply Voltage ( $V_{ISOOUT}$ ) vs Load Current ( $I_{ISOOUT}$ )**



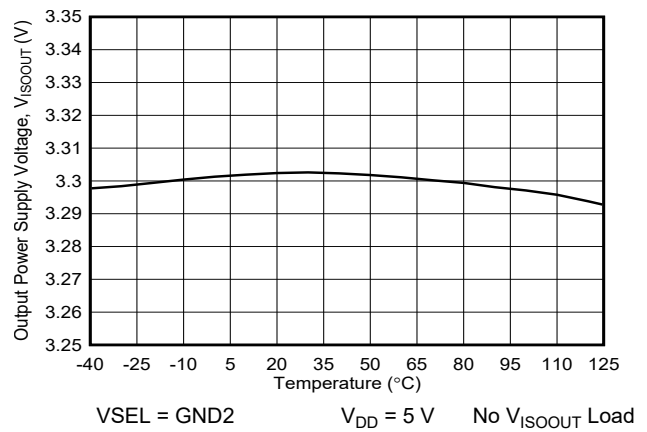
**Figure 7-5. Supply Current ( $I_{DD}$ ) vs Load Current ( $I_{ISOOUT}$ )**



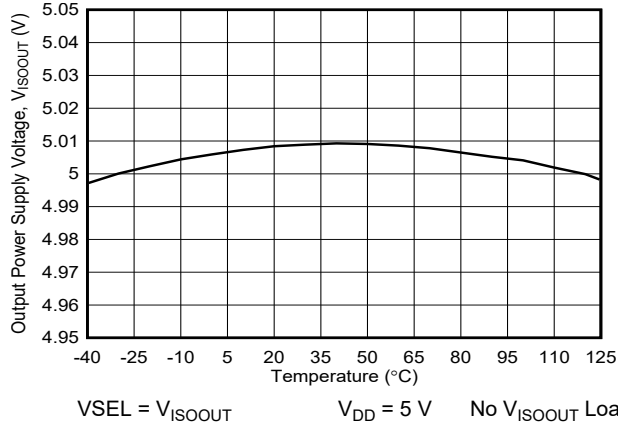
**Figure 7-6. Efficiency vs Load Current ( $I_{ISOOUT}$ )**



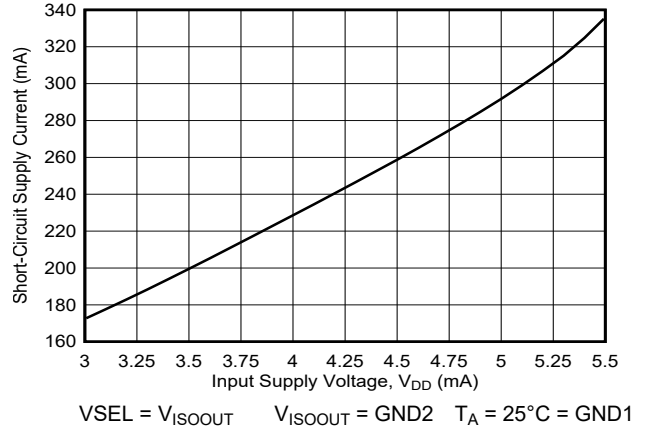
**Figure 7-7. Power Dissipation vs Load Current ( $I_{ISOOUT}$ )**



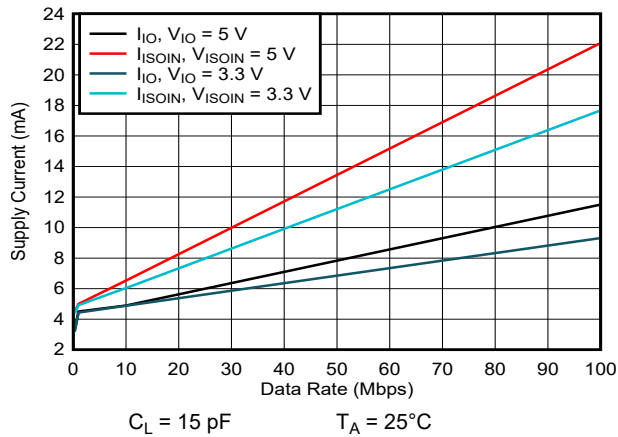
**Figure 7-8. 3.3-V Isolated Supply Voltage ( $V_{ISOOUT}$ ) vs Free-Air Temperature**



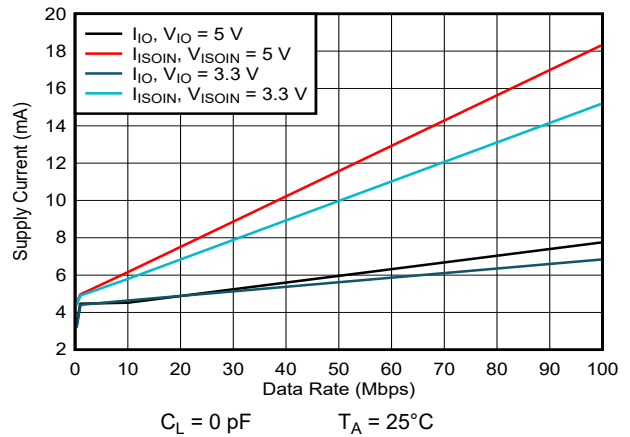
**Figure 7-9. 5-V Isolated Supply Voltage ( $V_{ISOOUT}$ ) vs Free-Air Temperature**



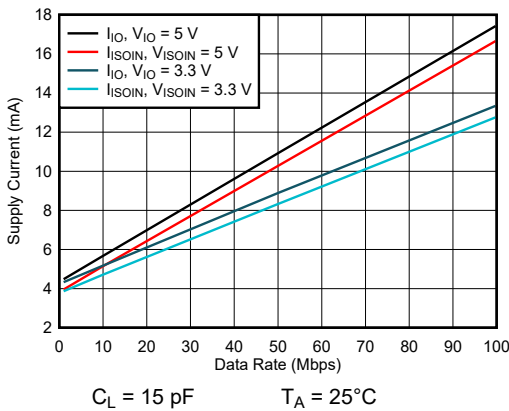
**Figure 7-10. Short-Circuit Supply Current ( $I_{CC}$ ) vs Supply Voltage ( $V_{CC}$ )**



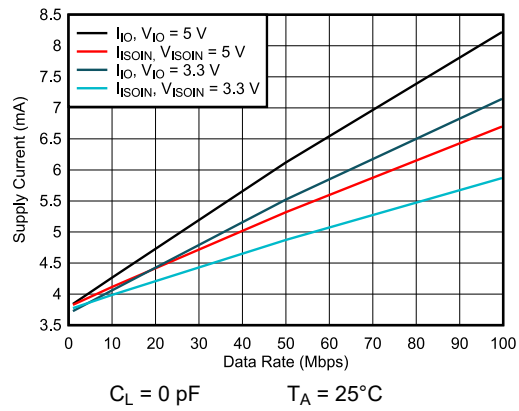
**Figure 7-11. ISOW7741-Q1 Channel Supply Currents vs Data Rate For  $C_L = 15$  pF**



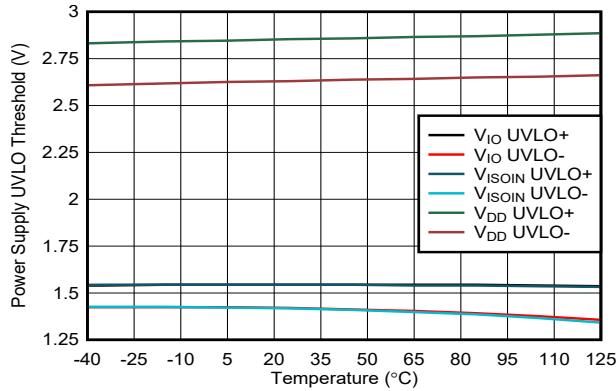
**Figure 7-12. ISOW7741-Q1 Channel Supply Currents vs Data Rate For  $C_L = 0$  pF**



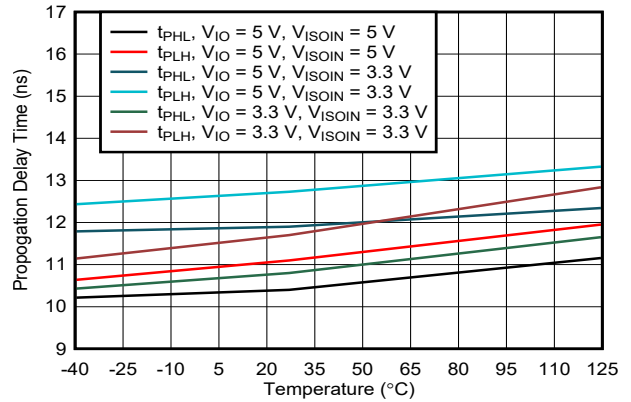
**Figure 7-13. ISOW7742-Q1 Channel Supply Currents vs Data Rate For  $C_L = 15$  pF**



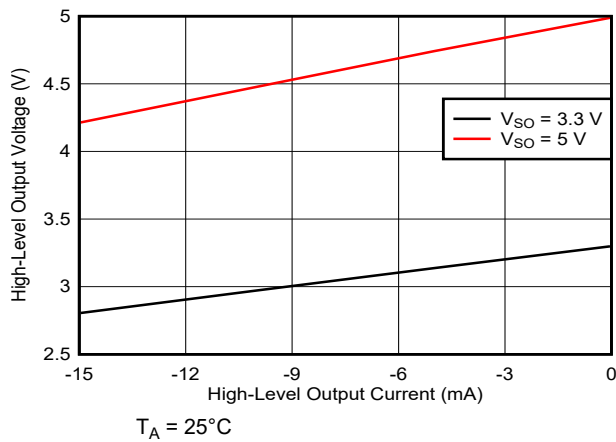
**Figure 7-14. ISOW7742-Q1 Channel Supply Currents vs Data Rate For  $C_L = 0$  pF**



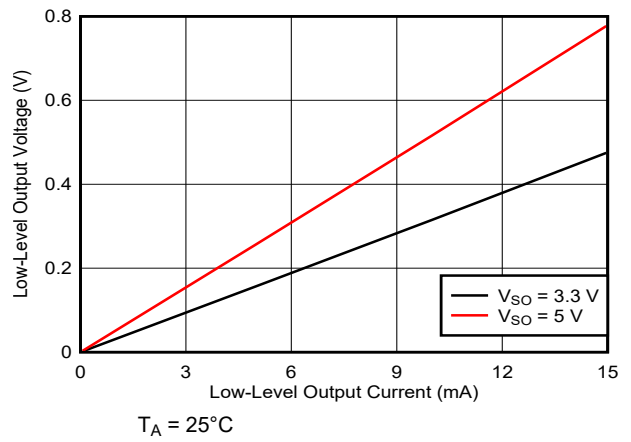
**Figure 7-15. Power-Supply Undervoltage Threshold vs Free Air Temperature**



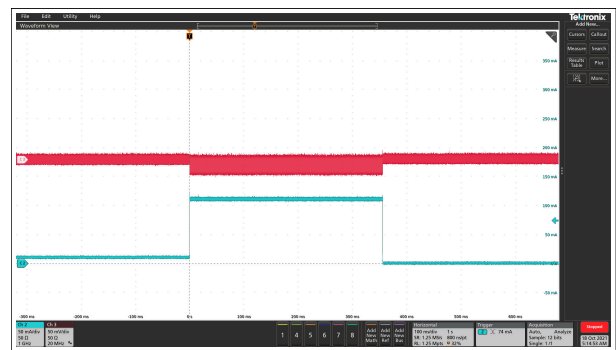
**Figure 7-16. Propagation Delay Time vs Free-Air Temperature**



**Figure 7-17. High-Level Output Voltage vs High-Level Output Current**

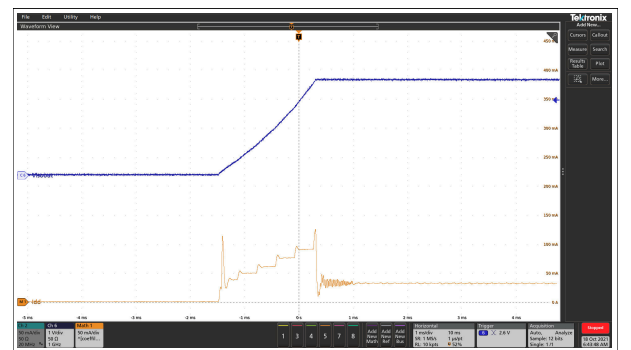


**Figure 7-18. Low-Level Output Voltage vs Low-Level Output Current**



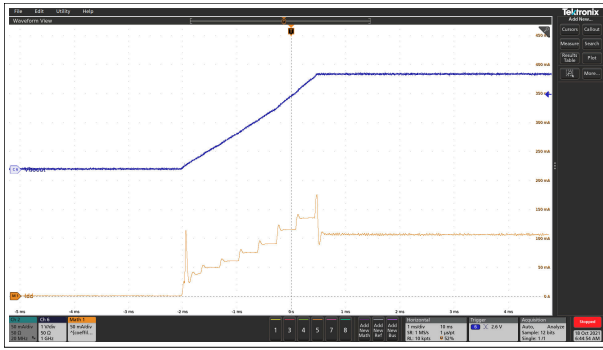
V<sub>DD</sub> = 5 V V<sub>ISOOUT</sub> = 3.3 V T<sub>A</sub> = 25°C

**Figure 7-19. 10-mA to 110-mA Load Transient Response**



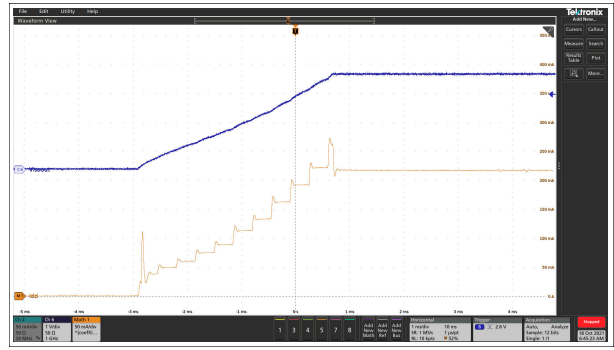
V<sub>DD</sub> = 5 V V<sub>ISOOUT</sub> = 3.3 V 10 uF Capacitor on V<sub>ISOOUT</sub>

**Figure 7-20. Soft Start at 10-mA Load For V<sub>ISOOUT</sub> = 3.3 V**



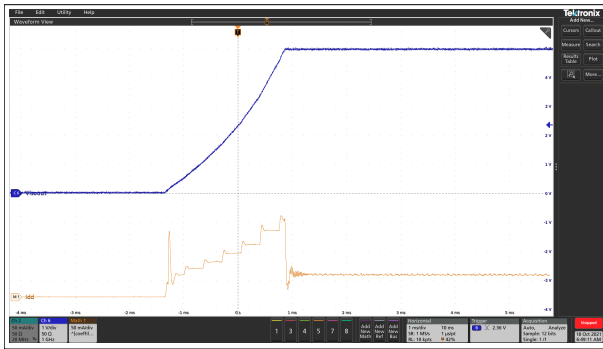
$V_{DD} = 5\text{ V}$   $V_{ISOOUT} = 3.3\text{ V}$   $10\text{ }\mu\text{F}$   
Capacitor on  $V_{ISOOUT}$

**Figure 7-21. Soft Start at 50-mA Load For  $V_{ISOOUT} = 3.3\text{ V}$**



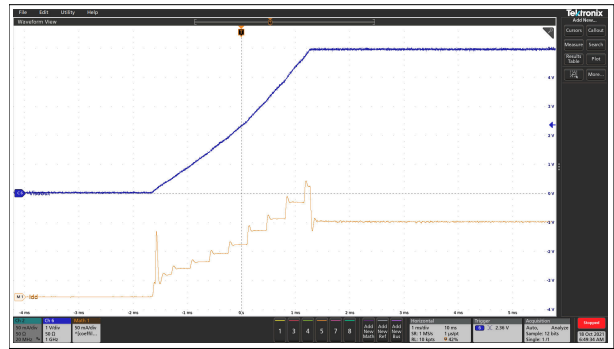
$V_{DD} = 5\text{ V}$   $V_{ISOOUT} = 3.3\text{ V}$   $10\text{ }\mu\text{F}$   
Capacitor on  $V_{ISOOUT}$

**Figure 7-22. Soft Start at 110-mA Load For  $V_{ISOOUT} = 3.3\text{ V}$**



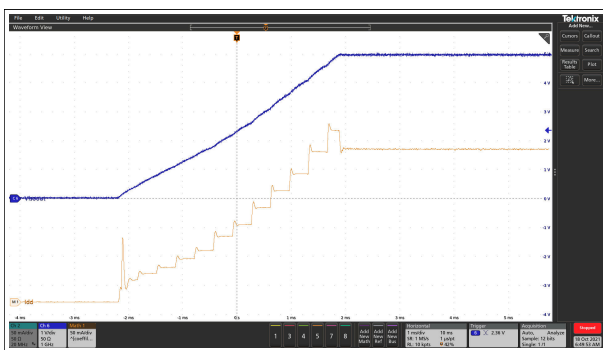
$V_{DD} = 5\text{ V}$   $V_{ISOOUT} = 5\text{ V}$   $10\text{ }\mu\text{F}$   
Capacitor on  $V_{ISOOUT}$

**Figure 7-23. Soft Start at 10-mA Load For  $V_{ISOOUT} = 5\text{ V}$**



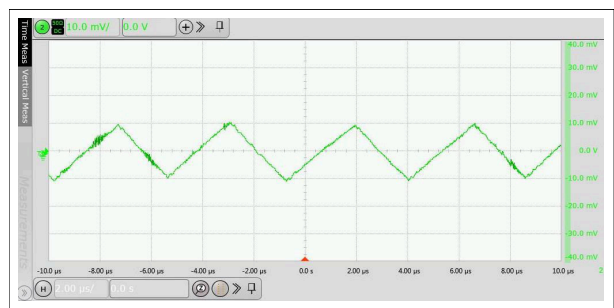
$V_{DD} = 5\text{ V}$   $V_{ISOOUT} = 5\text{ V}$   $10\text{ }\mu\text{F}$   
Capacitor on  $V_{ISOOUT}$

**Figure 7-24. Soft Start at 50-mA Load For  $V_{ISOOUT} = 5\text{ V}$**



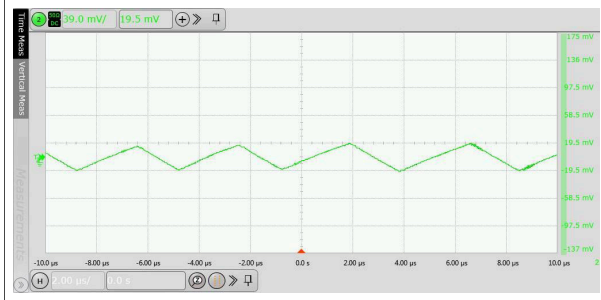
$V_{DD} = 5\text{ V}$   $V_{ISOOUT} = 5\text{ V}$   $10\text{ }\mu\text{F}$   
Capacitor on  $V_{ISOOUT}$

**Figure 7-25. Soft Start at 110-mA Load For  $V_{ISOOUT} = 5\text{ V}$**



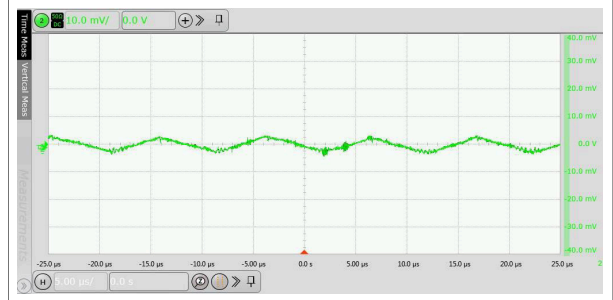
$V_{DD} = 3.3\text{ V}$   $V_{ISOOUT} = 3.3\text{ V}$   $10\text{ }\mu\text{F}$   
Capacitor on  $V_{ISOOUT}$

**Figure 7-26.  $V_{ISOOUT}$  Ripple Voltage at 3.3 V with 10  $\mu\text{F}$  Capacitor and 60 mA load**



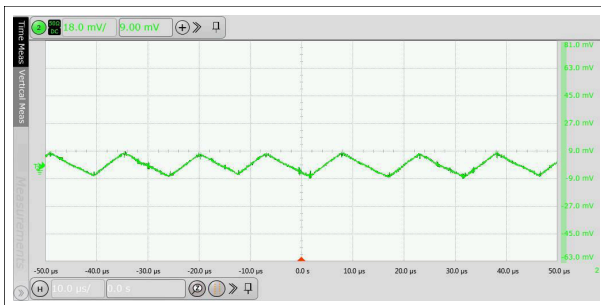
$V_{DD} = 5\text{ V}$   $V_{ISOOUT} = 5\text{ V}$  10  $\mu\text{F}$   
Capacitor on  
 $V_{ISOOUT}$

**Figure 7-27.  $V_{ISOOUT}$  Ripple Voltage at 5 V with 10  $\mu\text{F}$  Capacitor and 110 mA load**



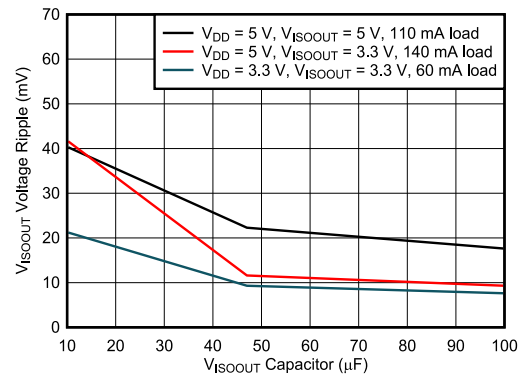
$V_{DD} = 3.3\text{ V}$   $V_{ISOOUT} = 3.3\text{ V}$  100  $\mu\text{F}$   
V Capacitor on  
 $V_{ISOOUT}$

**Figure 7-28.  $V_{ISOOUT}$  Ripple Voltage at 3.3 V with 100  $\mu\text{F}$  Capacitor and 60 mA load**



$V_{DD} = 5\text{ V}$   $V_{ISOOUT} = 5\text{ V}$  100  $\mu\text{F}$   
Capacitor on  
 $V_{ISOOUT}$

**Figure 7-29.  $V_{ISOOUT}$  Ripple Voltage at 5 V with 100  $\mu\text{F}$  Capacitor and 110 mA load**

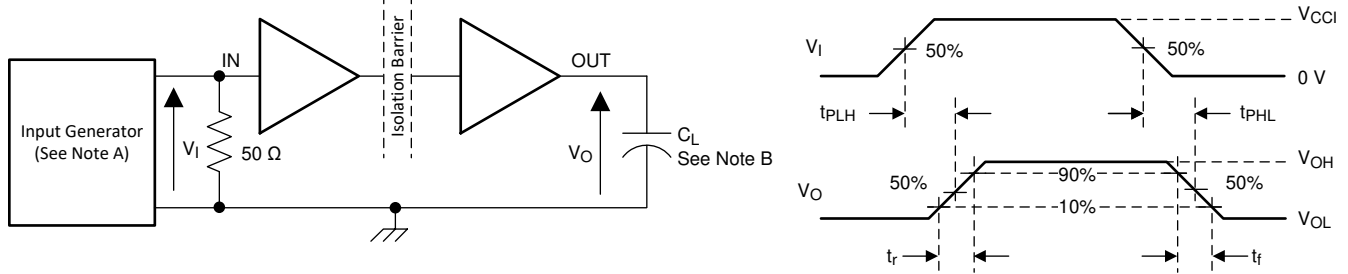


$T_A = 25^\circ\text{C}$

**Figure 7-30.  $V_{ISOOUT}$  Ripple Voltage vs Load Capacitor**

## 8 Parameter Measurement Information

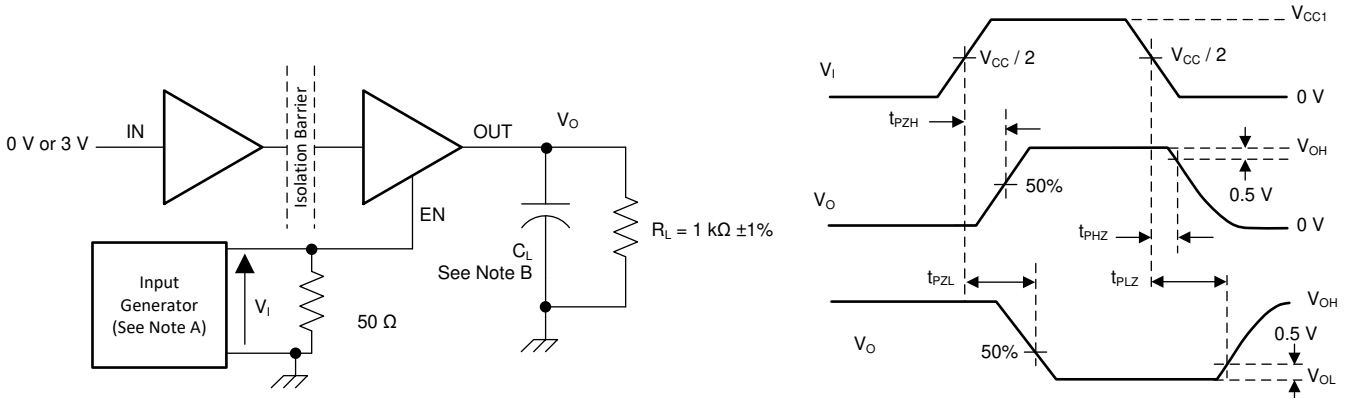
In the below images,  $V_{CC1}$  and  $V_{CC0}$  refers to the power supplies  $V_{IO}$  and  $V_{ISOIN}$ , respectively.



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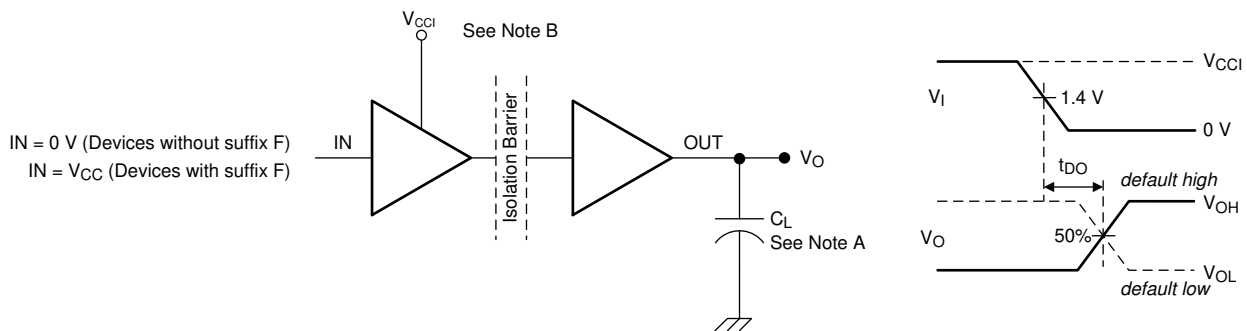
- A.  $C_L = 15$  pF and The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 50$  kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_0 = 50 \Omega$ . At the input,  $50 \Omega$  resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms**



- A. A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq 50$  kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_0 = 50 \Omega$ . At the input,  $50 \Omega$  resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 8-2. Enable/Disable Propagation Delay Time Test Circuit and Waveform**



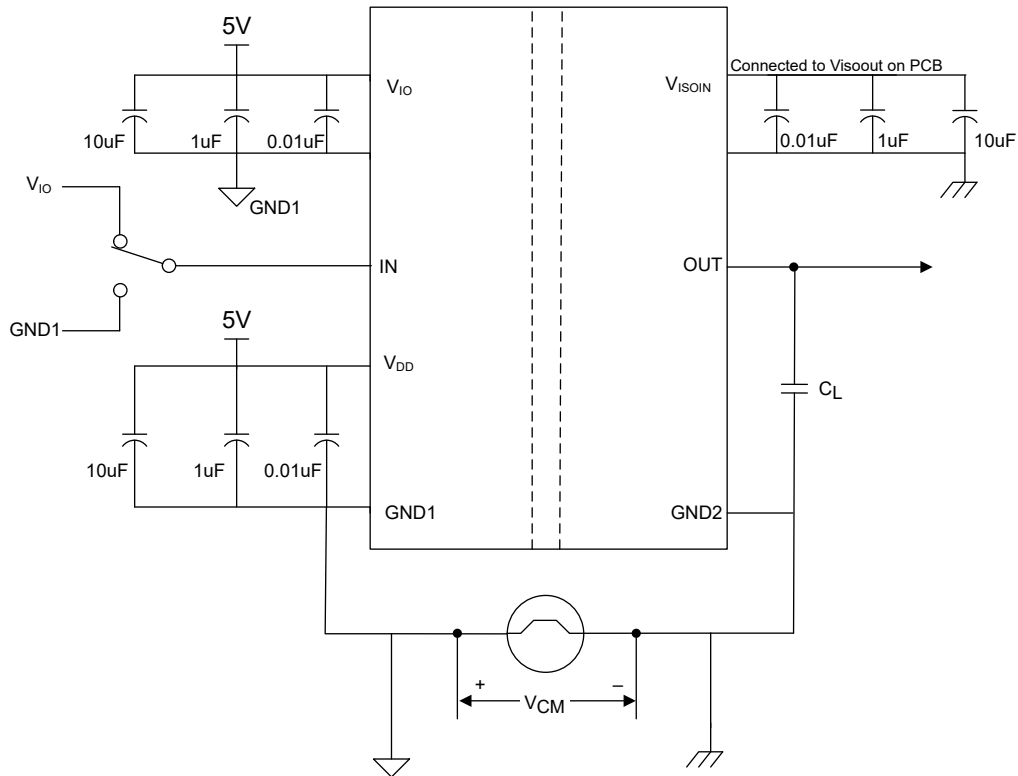
**Note**

A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Note**

B. Power Supply Ramp Rate = 10 mV/ns.

**Figure 8-3. Default Output Delay Time Test Circuit and Voltage Waveforms**



**Note**

C<sub>L</sub> = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Note**

Pass-fail criteria: Outputs must remain stable.

**Figure 8-4. Common-Mode Transient Immunity Test Circuit**



## 9 Detailed Description

### 9.1 Overview

The ISOW774x-Q1 family of devices have low-noise, low-emissions isolated DC-DC converter, and four high-speed isolated data channels. [Section 9.2](#) shows the functional block diagram of the ISOW774x device.

#### 9.1.1 Power Isolation

The integrated isolated DC-DC converter uses advanced circuit and on-chip layout techniques to reduce radiated emissions and achieve upto 46% typical efficiency. The integrated transformer uses thin film polymer as the insulation barrier. Output voltage of power converter can be controlled to 3.3 V or 5 V using  $V_{SEL}$  pin. The DC-DC converter can be switched off using the EN/FLT pin to save power. The output voltage,  $V_{ISOOUT}$ , is monitored and feedback information is conveyed to the primary side through a dedicated isolation channel.  $V_{ISOOUT}$  needs to be connected to  $V_{ISOIN}$  to ensure the feedback channel is properly powered to regulate the DC-DC converter. This can be achieved by connecting the pins directly or through an LDO that remains powered up at all times. A ferrite bead is recommended between  $V_{ISOOUT}$  and  $V_{ISOIN}$  to further reduce emissions. See the [Section 10.2](#) section. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the  $V_{IO}$ ,  $V_{DD}$  and  $V_{ISOIN}$  supplies which ensures robust fails-safe system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

#### 9.1.2 Signal Isolation

The integrated signal isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. [Figure 9-1](#) shows a functional block diagram of a typical signal isolation channel. In order to keep any noise coupling from power converter away from signal path, power supplies on side 1 for power converter ( $V_{DD}$ ) and signal path ( $V_{IO}$ ) are kept separate. Similarly on side 2, power converter output ( $V_{ISOOUT}$ ) needs to be connected to  $V_{ISOIN}$  externally on PCB. Emissions can be further improved by placing a ferrite bead between  $V_{ISOOUT}$  and  $V_{ISOIN}$  as well as between the GND2 pins. For more details, refer to the [Layout Guidelines section](#).

## 9.2 Functional Block Diagram

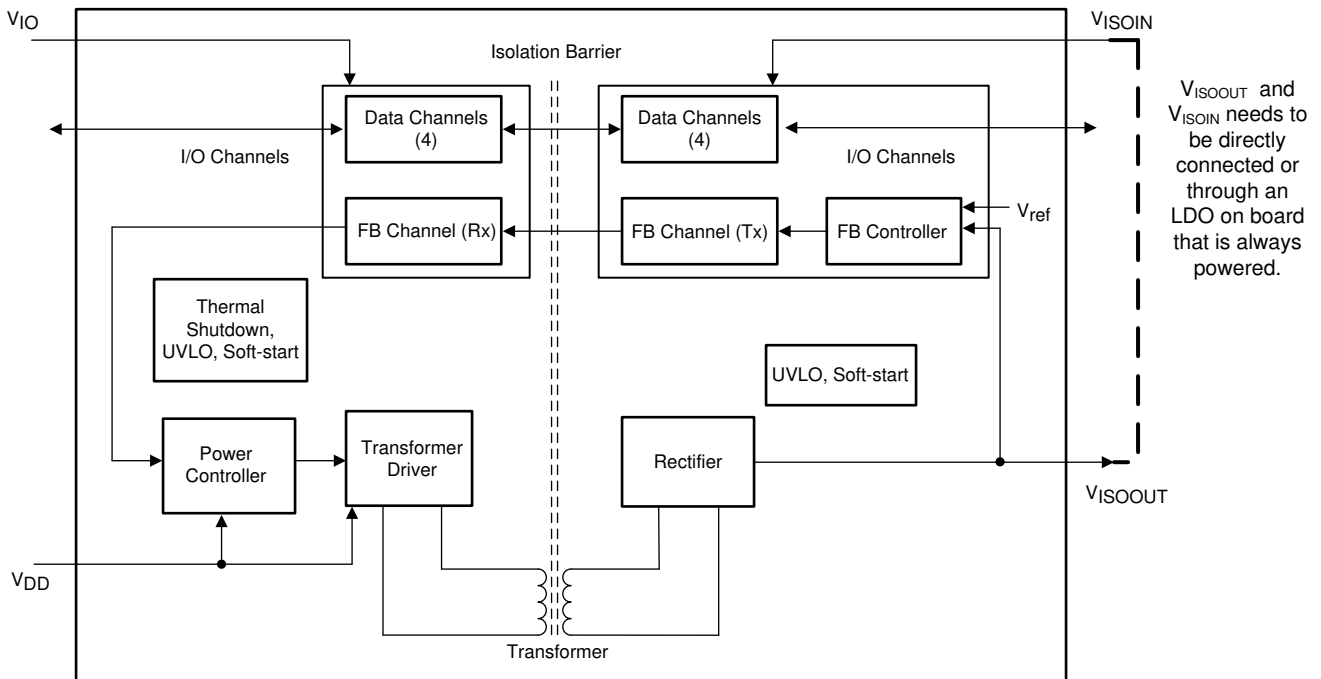


Figure 9-1. Block Diagram

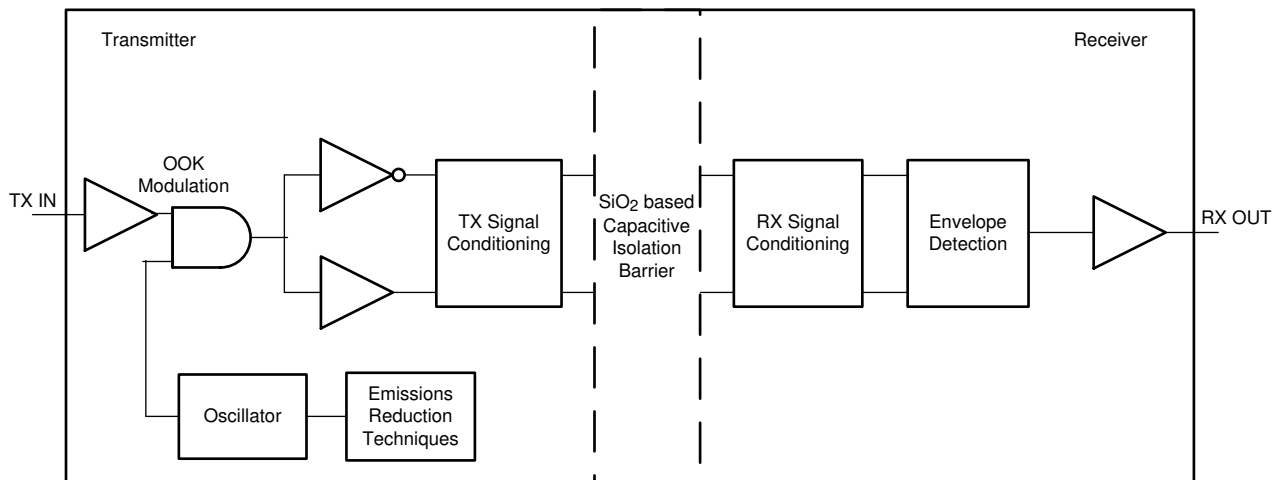
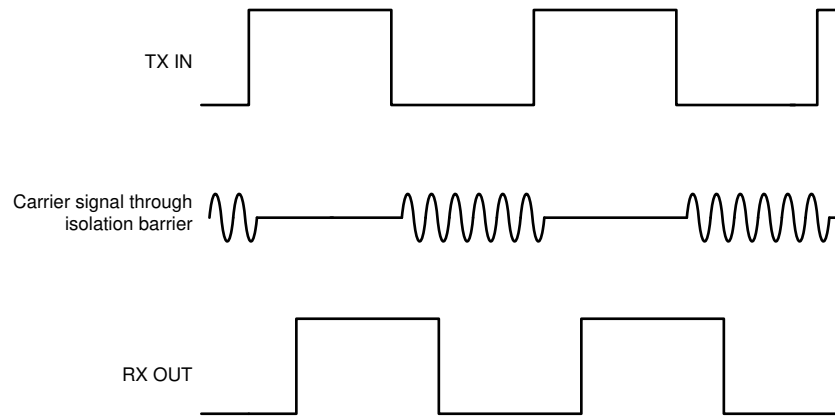


Figure 9-2. Conceptual Block Diagram of a Capacitive Data Channel

Figure 9-3 shows a conceptual detail of how the OOK scheme works.



**Figure 9-3. On-Off Keying (OOK) Based Modulation Scheme**

### 9.3 Feature Description

Table 9-1 shows an overview of the device features.

**Table 9-1. Device Features**

| PART NUMBER <sup>(1)</sup> | CHANNEL DIRECTION    | MAXIMUM DATA RATE | DEFAULT OUTPUT STATE | RATED ISOLATION <sup>(2)</sup>             |
|----------------------------|----------------------|-------------------|----------------------|--|
| ISOW7741-Q1                | 3 forward, 1 reverse | 100 Mbps          | High                 | 5 kV <sub>RMS</sub> / 7071 V <sub>PK</sub> |
| ISOW7741-Q1 with F suffix  |                      |                   | Low                  |  |
| ISOW7742-Q1                | 2 forward, 2 reverse |                   | High                 |  |
| ISOW7742-Q1 with F suffix  |                      |                   | Low                  |  |

(1) The F suffix is part of the orderable part number. See the [Section 14](#) section for the full orderable part number.

(2) For detailed isolation ratings, see the [Section 7.7](#) table.

#### 9.3.1 Electromagnetic Compatibility (EMC) Considerations

The ISOW7741-Q1 and ISOW7742-Q1 devices use emissions reduction schemes for the internal oscillator and advanced internal layout scheme to minimize radiated emissions at the system level.

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 32. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISOW7741-Q1 and ISOW7742-Q1 devices incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.
- Power path and signal path separated to minimize internal high frequency coupling and allowing for an external filtering knob using ferrite beads available to further reduce emissions
- Reduced power converter switching frequency to 25 Mhz to reduce strength of high frequency components in emissions spectrum



- Thermal protection is also integrated to help prevent the device from getting damaged during overload and short-circuit conditions on the isolated output. Under these conditions, the device temperature starts to increase. When the temperature goes above 165°C, thermal shutdown activates and the primary controller turns off which removes the energy supplied to the  $V_{ISOOUT}$  load, which causes the device to cool off. When the junction temperature goes below 150°C, the device starts to function normally. If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care should be taken in the design to prevent the device junction temperatures from reaching such high values.

## 9.4 Device Functional Modes

Table 9-2 lists the supply configurations for these devices.

**Table 9-2. Supply Configuration Function Table**

| $V_{DD}^{(1)}$    | $V_{IO}$          | VSEL                                 | $V_{ISOOUT}^{(3)}$ |
|-------------------|-------------------|--------------------------------------|--------------------|
| $< V_{DD(UVLO+)}$ | $> V_{IO(UVLO+)}$ | X                                    | OFF                |
| $> V_{DD(UVLO+)}$ | $< V_{IO(UVLO+)}$ | X                                    | OFF                |
| 5 V               | 1.71 V to 5.5 V   | High (shorted to $V_{ISOOUT}$ )      | 5 V                |
| 5 V or 3.3 V      | 1.71 V to 5.5 V   | Low (shorted to GND2) <sup>(2)</sup> | 3.3 V              |

- (1)  $V_{DD} = 3.3$  V, VSEL shorted to  $V_{ISOOUT}$  (essentially  $V_{ISOOUT} = 5$  V) is not the recommended mode of operation  
 (2) The VSEL pin has a weak pulldown internally. Therefore for  $V_{ISOOUT} = 3.3$  V, the VSEL pin should be strongly connected to the GND2 pin in noisy system scenarios.  
 (3)  $V_{ISOOUT}$  shorted to  $V_{ISOIN}$  on PCB and both GND2 pins are shorted to each other and EN=High

Table 9-3 lists the channel isolators functional modes for these devices.

**Table 9-3. Channel Isolator Function Table**

| CHANNEL INPUT SUPPLY ( $V_{CCI}$ ) <sup>(1)</sup> | CHANNEL OUTPUT SUPPLY ( $V_{CCO}$ ) <sup>(1)</sup> | INPUT (INx) | IO ENABLE (EN_IOx) | OUTPUT (OUTx) | COMMENTS  |
|---|--|-------------|--------------------|---------------|---|
| PU  | PU   | H           | H or Open          | H             | Normal Operation: A channel output assumes the logic state of its input.  |
|   |  | L           | H or Open          | L             |   |
|   |  | Open        | H or Open          | Default       | Default mode <sup>(2)</sup> : When INx is open, the corresponding channel output goes to its default logic state.   |
|   |  | X           | L                  | Z and Default | A low value of output enable causes the outputs of the same side to be high impedance and the output of opposite side to be fail-safe default state.  |
| PD  | PU   | X           | H or Open          | Default       | Default mode <sup>(2)</sup> : When $V_{CCI}$ is unpowered, a channel output assumes the logic state based on the selected default option. When $V_{CCI}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When $V_{CCI}$ transitions from powered-up to unpowered, channel output assumes the selected default state. |

- (1)  $V_{CCI}$  = Input-side  $V_{IO}$  or  $V_{ISOIN}$ ;  $V_{CCO}$  = Output-side  $V_{IO}$  or  $V_{ISOIN}$ ; PU = Powered up ( $V_{IO} > 1.7$  V,  $V_{ISOIN} > 1.7$  V); PD = Powered down ( $V_{IO} < 1$  V,  $V_{ISOIN} < 1$  V); X = Irrelevant; H = High level; L = Low level.  
 (2) In the default condition, the output is high for the ISOW774x-Q1 device and low with the F suffix.

9.4.1 Device I/O Schematics

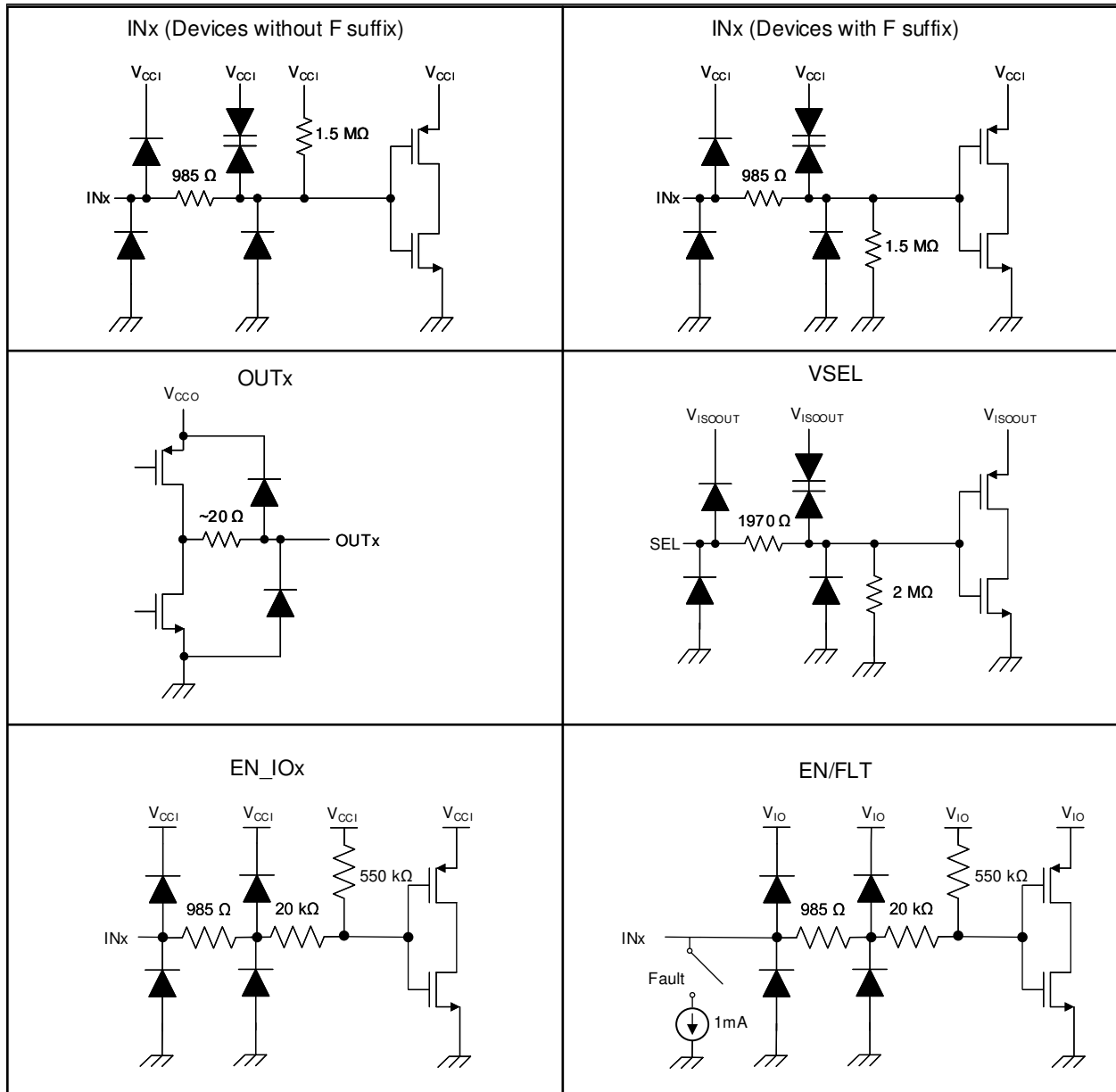


Figure 9-5. Device I/O Schematics

## 10 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The device is a high-performance, quad channel digital isolator with integrated DC-DC converter. Typically digital isolators require two power supplies isolated from each other to power up both sides of device. Due to the integrated DC-DC converter in the device, the isolated supply is generated inside the device that can be used to power isolated side of the device and peripherals on isolated side, thus saving board space. The device uses single-ended CMOS-logic switching technology. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is Microcontroller or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

The device is suitable for applications that have limited board space and desire more integration. The device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

### 10.2 Typical Application

Figure 10-1 shows the typical schematic for SPI isolation.

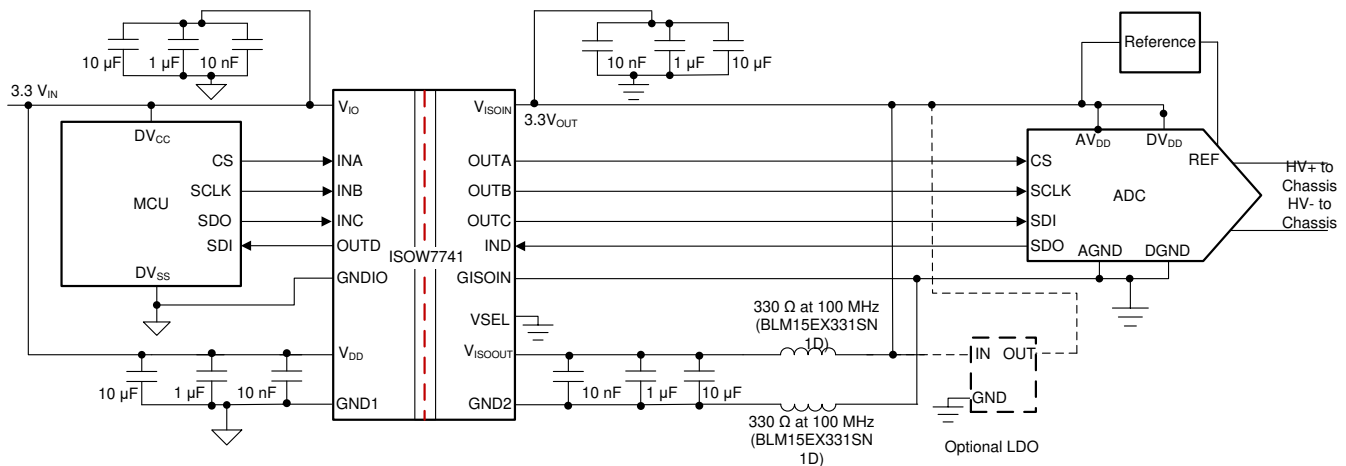


Figure 10-1. Isolated Power and SPI for ADC Sensing Application with ISOW7741-Q1



### 10.2.1 Design Requirements

To design with this device, use the parameters listed in [Table 10-1](#).

**Table 10-1. Design Parameters**

| PARAMETER                                   | VALUE   |
|---|---|
| $V_{DD}$ input voltage                      | 3 V to 5.5 V  |
| $V_{IO}$ input voltage                      | 1.71 V to 5.5 V   |
| $V_{ISOIN}$ input voltage                   | 1.71 V to 5.5 V   |
| $V_{DD}$ decoupling capacitors              | 10 $\mu$ F + 1 $\mu$ F + 0.01 $\mu$ F + optional additional capacitance |
| $V_{IO}$ decoupling capacitors              | 0.1 $\mu$ F + optional additional capacitance                           |
| $V_{ISOIN}$ decoupling capacitors           | 0.1 $\mu$ F + optional additional capacitance                           |
| $V_{ISOOUT}$ decoupling capacitors          | 10 $\mu$ F + 1 $\mu$ F + 0.01 $\mu$ F + optional additional capacitance |
| $V_{ISOOUT}$ to $V_{ISOIN}$ series inductor | BLM15ELX9331SN1D  |
| GND2 to GISOIN series inductor              | BLM15ELX9331SN1D  |
| $V_{IO}$ series inductor                    | BLM15ELX9331SN1D  |
| $V_{DD}$ series inductor                    | BLM15ELX9331SN1D  |
| GND1 to GNDIO series inductor               | BLM15ELX9331SN1D  |

Because of very-high current flowing through the ISOW7741-Q1 device  $V_{DD}$  and  $V_{ISOOUT}$  supplies, higher decoupling capacitors typically provide better noise and ripple performance. Although a 10- $\mu$ F capacitor is adequate, higher decoupling capacitors (such as 47  $\mu$ F) on both the  $V_{DD}$  and  $V_{ISOOUT}$  pins to the respective grounds are strongly recommended to achieve the best performance.

### 10.2.2 Detailed Design Procedure

The devices requires specific placement of external bypass capacitors and ferrite beads to operate at high performance. These low-ESR ceramic bypass capacitors must be placed as close to the chip pads as possible.

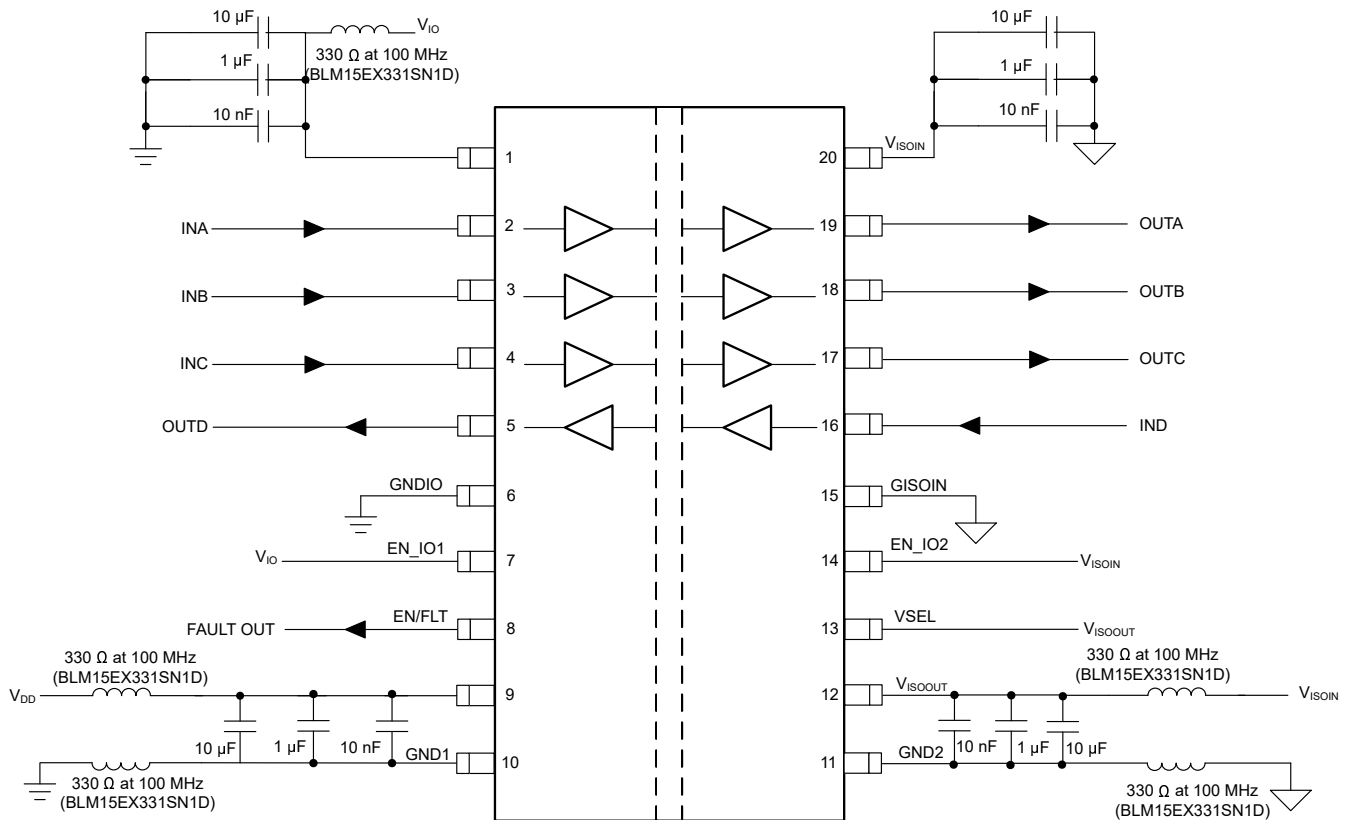


Figure 10-2. Typical ISOW7741-Q1 Circuit Hook-Up

### 10.2.3 Application Curve

The following typical eye diagrams of the ISOW774x-Q1 device indicates low jitter and wide open eye at the data rate of 50 Mbps.

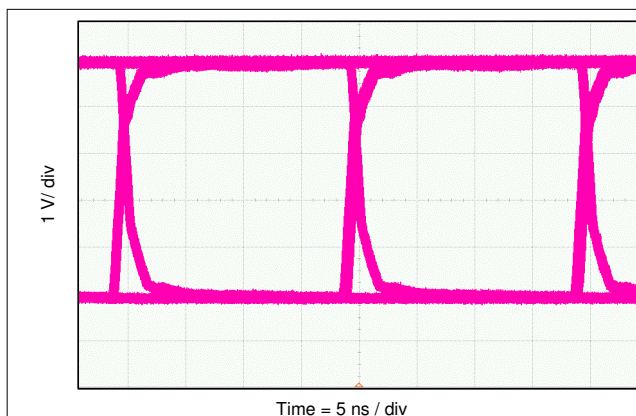


Figure 10-3. Eye Diagram at 50 Mbps PRBS  $2^{16} - 1$ , 5 V and 25°C

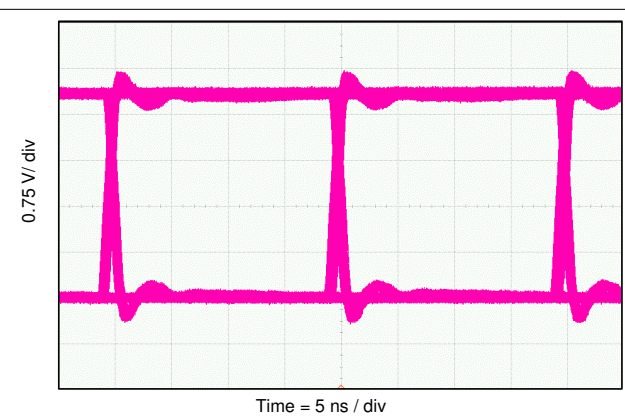


Figure 10-4. Eye Diagram at 50 Mbps PRBS  $2^{16} - 1$ , 3.3 V and 25°C

### 10.2.4 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 10-5 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million

(ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 10-6 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1000 V<sub>RMS</sub> with a lifetime of 1184 years.

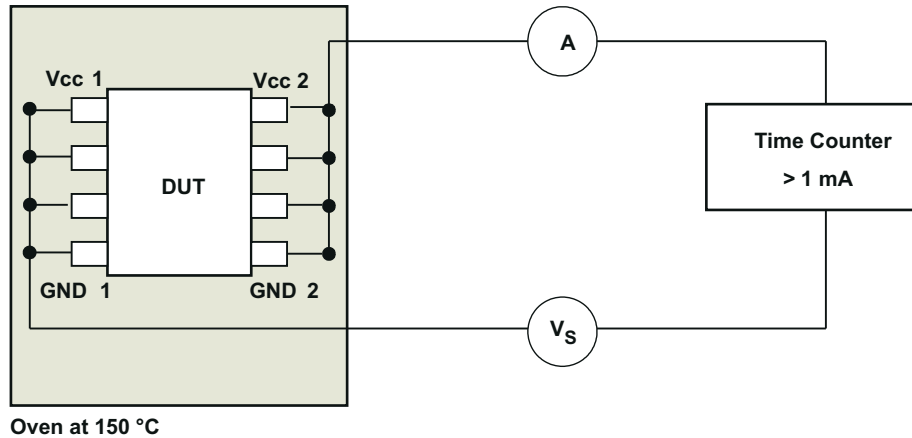


Figure 10-5. Test Setup for Insulation Lifetime Measurement

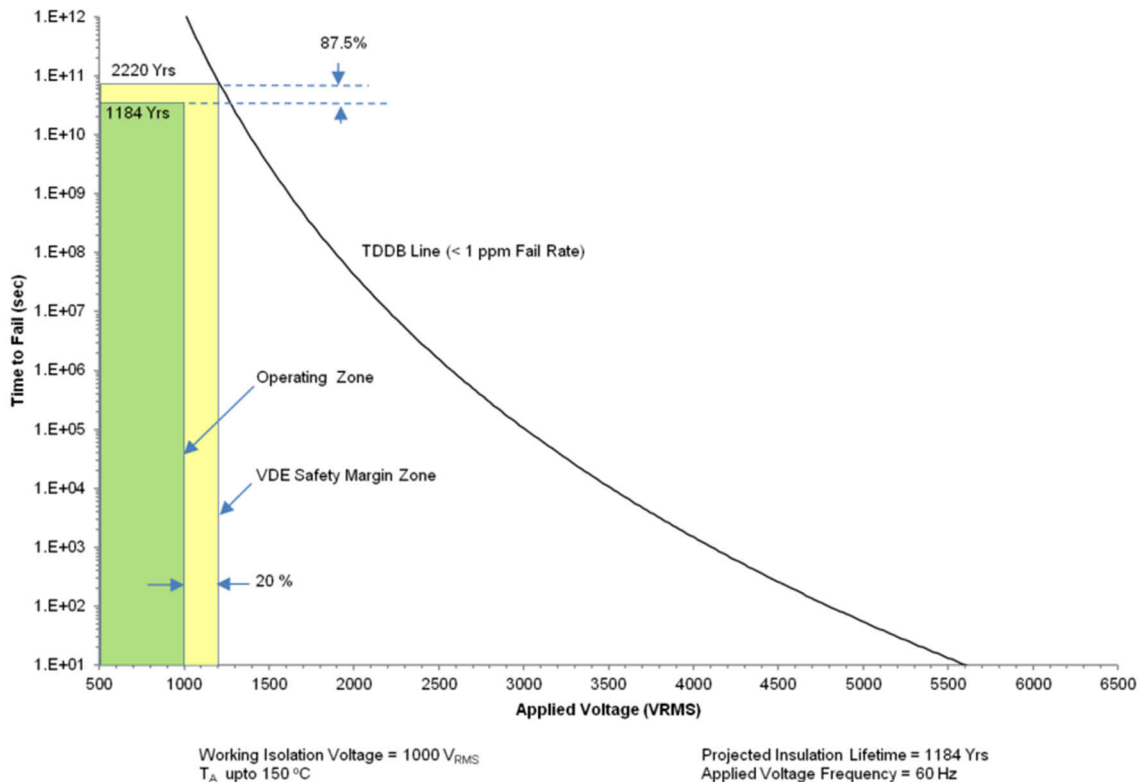


Figure 10-6. Insulation Lifetime Projection Data

## 11 Power Supply Recommendations

To help make sure that operation is reliable at data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible.  $V_{ISOOUT}$  needs to be connected to  $V_{ISOIN}$  to ensure the feedback channel is properly powered to regulate the DC-DC converter. If  $V_{ISOOUT}$  and  $V_{ISOIN}$  are not connected, the DC-DC converter will run open loop and the  $V_{ISOOUT}$  voltage will drift until the over-voltage clamp clamps at 6 V. There are two ways to connect  $V_{ISOOUT}$  and  $V_{ISOIN}$ :

- 1) connect  $V_{ISOOUT}$  and  $V_{ISOIN}$  directly with a ferrite bead. A ferrite bead is recommended between  $V_{ISOOUT}$  and  $V_{ISOIN}$  to further reduce emissions.
- 2) connect  $V_{ISOOUT}$  and  $V_{ISOIN}$  with a ferrite bead through an LDO that remains powered up at all times. If the LDO has an EN pin then keep the EN high at all times.

The input supply ( $V_{IO}$  and  $V_{DD}$ ) must have an appropriate current rating to support output load and switching at the maximum data rate required by the end application. For more information, refer to the [Section 10.2](#) section.

For an output load current of 110 mA, it is recommended to have >600 mA of input current limit and for lower output load currents, the input current limit can be proportionally lower.

## 12 Layout

### 12.1 Layout Guidelines

A low cost two layer PCB should be sufficient to achieve good EMC performance:

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Because the device has no thermal pad to dissipate heat, the device dissipates heat through the respective GND pins. Ensure that enough copper is present on both GND pins to prevent the internal junction temperature of the device from rising to unacceptable levels.

Figure 12-1 shows the recommended placement and routing of device bypass capacitors. Below guidelines must be followed to meet application EMC requirements:

- High frequency bypass capacitors 10 nF must be placed close to  $V_{DD}$  and  $V_{ISOOUT}$  pins, less than 1 mm distance away from device pins. This is very essential for optimised radiated emissions performance. Ensure that these capacitors are 0402 size so that they offer least inductance (ESL).
- Bulk capacitors of at least 10  $\mu$ F must be placed on power converter input ( $V_{DD}$ ) and output ( $V_{ISOOUT}$ ) supply pins.
- Traces on  $V_{DD}$  and GND1 must be symmetric till bypass capacitors. Similarly traces on  $V_{ISOOUT}$  and GND2 must be symmetric.
- Place two 0402 size Ferrite beads (Part number: BLM15EX331SN1) on  $V_{ISOOUT}$  and GND2 path so that any high frequency noise from power converter output sees a high impedance before it goes to other components on PCB.
- Do not have any metal traces or ground pour within 4 mm of power converter output terminals  $V_{ISOOUT}$  pin12 and GND2 pin11. VSEL pin is also in  $V_{ISOOUT}$  domain and should be shorted to either pin 11 or pin 12 for output voltage selection.
- Following the layout guidelines of EVM as much as possible is highly recommended for a low radiated emissions design.

#### 12.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

## 12.2 Layout Example

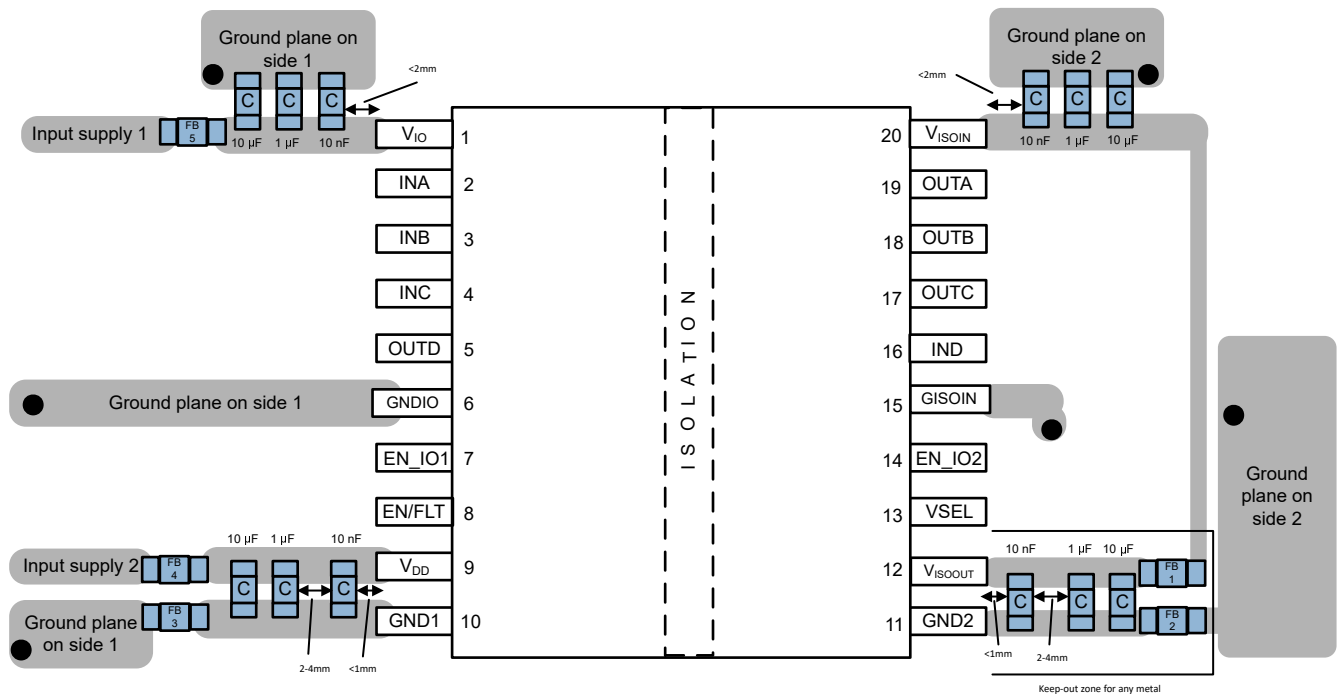


Figure 12-1. Layout Example

## 13 Device and Documentation Support

### 13.1 Device Support

### 13.2 Documentation Support

#### 13.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Digital Isolator Design Guide](#)
- Texas Instruments, [Isolation Glossary](#)

### 13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 13.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 13.5 Trademarks

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### 13.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 13.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## **14 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

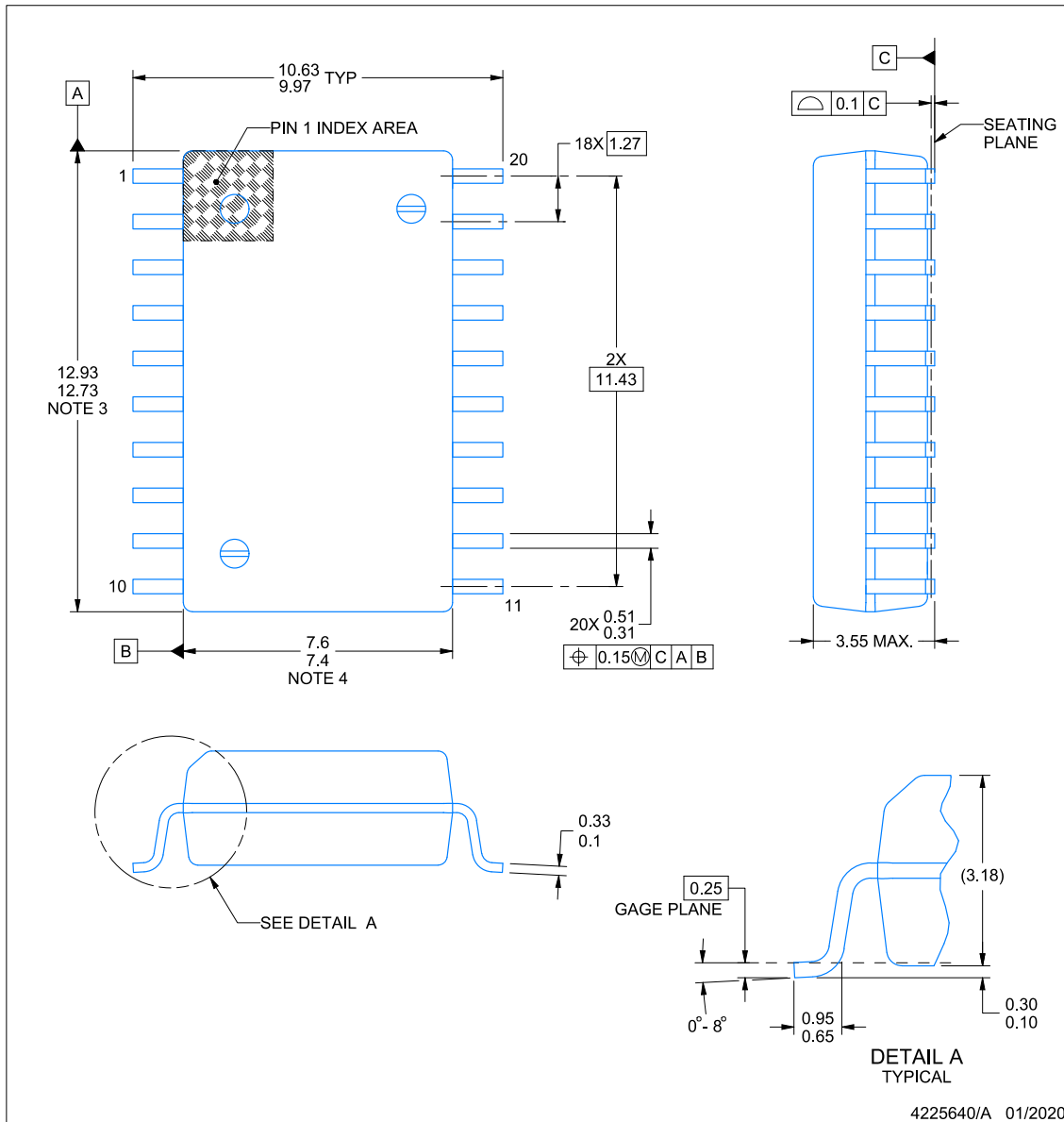


**PACKAGE OUTLINE**

**DFM0020A**

**SOIC - 3.55 mm max height**

SMALL OUTLINE PACKAGE



NOTES:

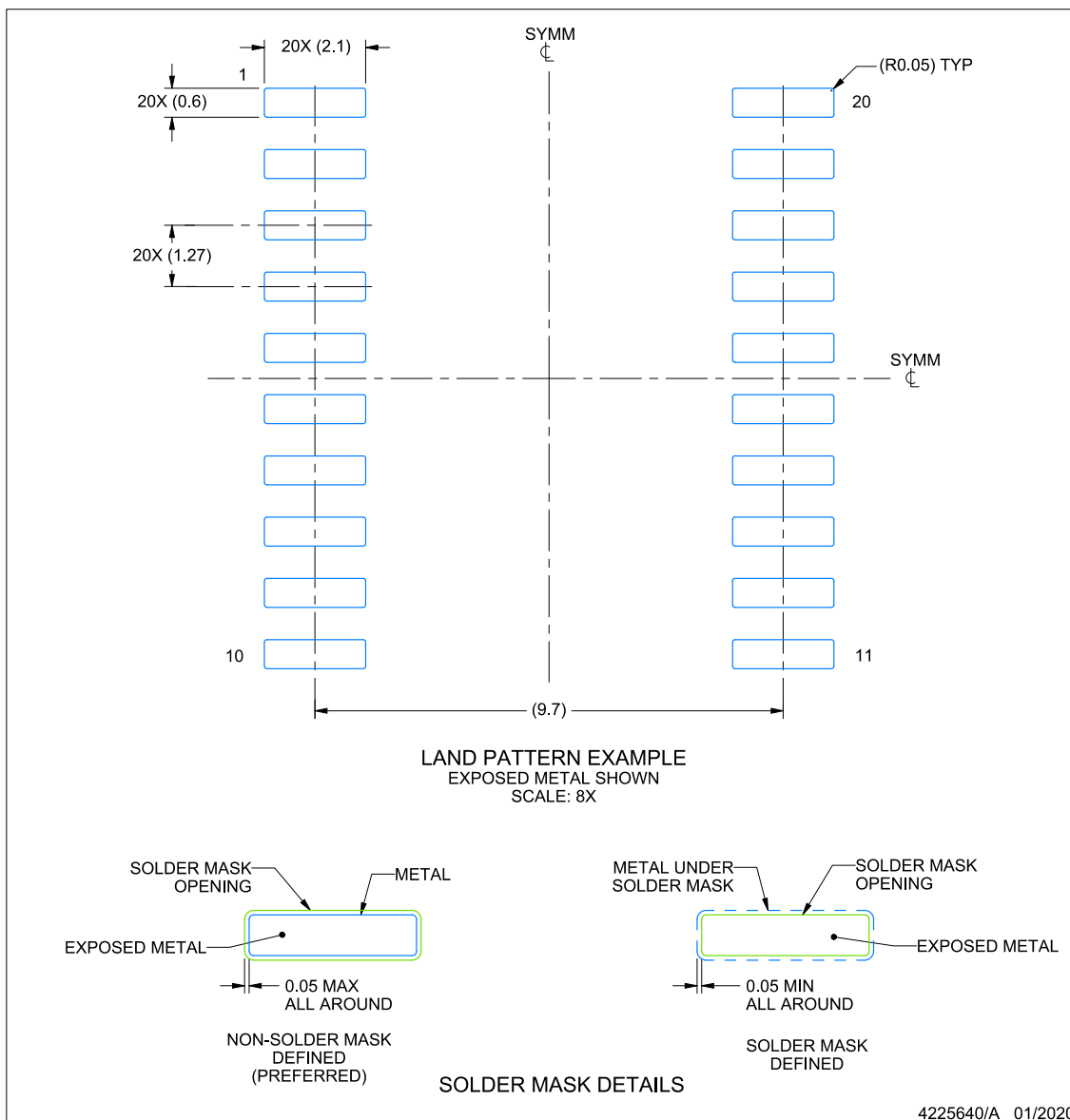
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

## EXAMPLE BOARD LAYOUT

**DFM0020A**

**SOIC - 3.55 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

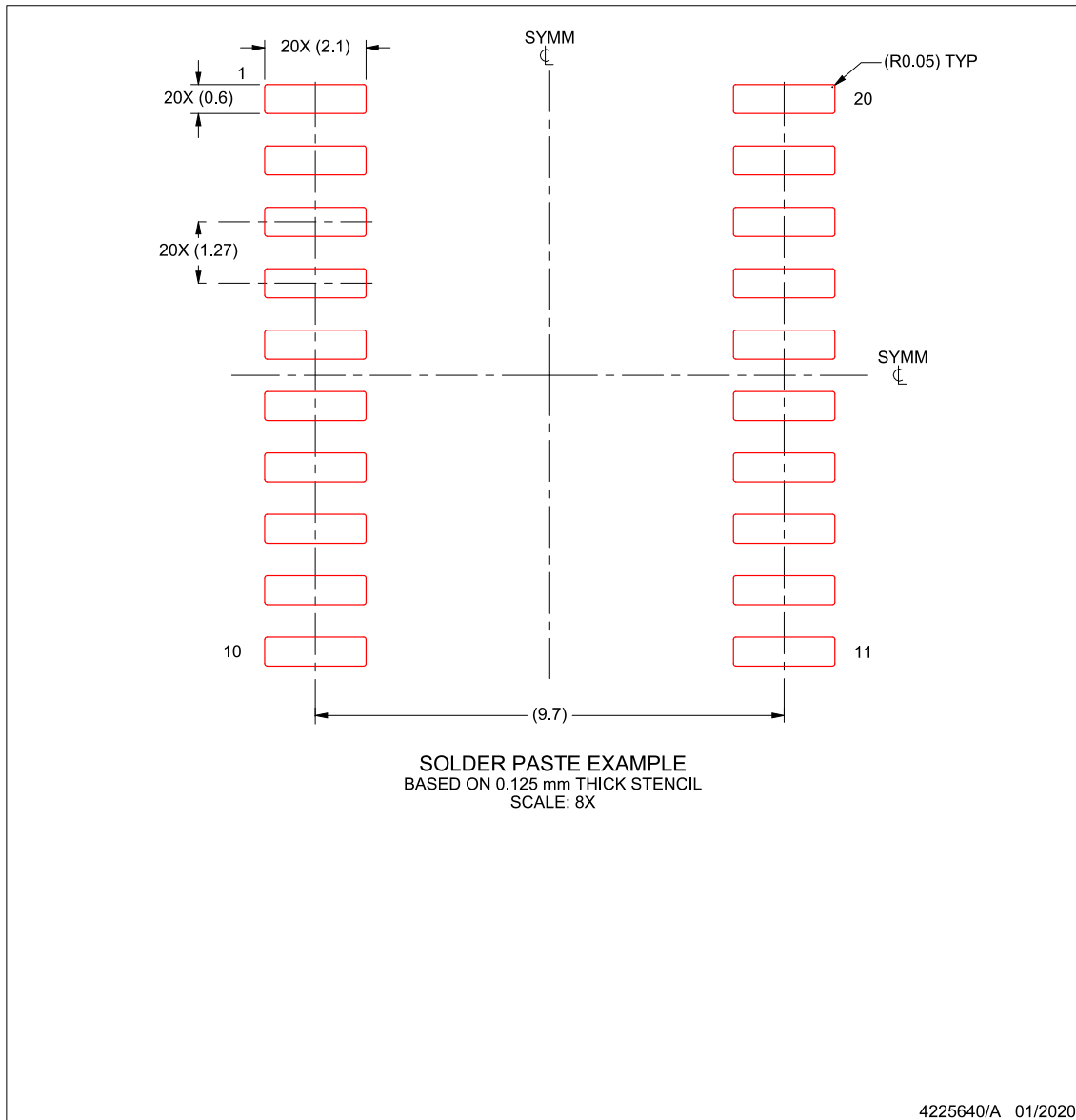
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DFM0020A**

**SOIC - 3.55 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

**PACKAGING INFORMATION**

| Orderable part number            | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">ISOW7741FQDFMRQ1</a> | Active        | Production           | SOIC (DFM)   20 | 850   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | ISOW7741F           |
| ISOW7741FQDFMRQ1.A               | Active        | Production           | SOIC (DFM)   20 | 850   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | ISOW7741F           |
| <a href="#">ISOW7741QDFMRQ1</a>  | Active        | Production           | SOIC (DFM)   20 | 850   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | ISOW7741            |
| ISOW7741QDFMRQ1.A                | Active        | Production           | SOIC (DFM)   20 | 850   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | ISOW7741            |
| <a href="#">ISOW7742FQDFMRQ1</a> | Active        | Production           | SOIC (DFM)   20 | 850   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | ISOW7742F           |
| ISOW7742FQDFMRQ1.A               | Active        | Production           | SOIC (DFM)   20 | 850   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | ISOW7742F           |
| <a href="#">ISOW7742QDFMRQ1</a>  | Active        | Production           | SOIC (DFM)   20 | 850   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | ISOW7742            |
| ISOW7742QDFMRQ1.A                | Active        | Production           | SOIC (DFM)   20 | 850   LARGE T&R       | Yes         | NIPDAU                               | Level-3-260C-168 HR               | -40 to 125   | ISOW7742            |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ISOW7741-Q1, ISOW7742-Q1 :**

- Catalog : [ISOW7741](#), [ISOW7742](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ISOW7741FQDFMRQ1 | SOIC         | DFM             | 20   | 850 | 330.0              | 24.4               | 10.85   | 13.4    | 4.0     | 16.0    | 24.0   | Q1            |
| ISOW7741QDFMRQ1  | SOIC         | DFM             | 20   | 850 | 330.0              | 24.4               | 10.85   | 13.4    | 4.0     | 16.0    | 24.0   | Q1            |
| ISOW7742FQDFMRQ1 | SOIC         | DFM             | 20   | 850 | 330.0              | 24.4               | 10.85   | 13.4    | 4.0     | 16.0    | 24.0   | Q1            |
| ISOW7742QDFMRQ1  | SOIC         | DFM             | 20   | 850 | 330.0              | 24.4               | 10.85   | 13.4    | 4.0     | 16.0    | 24.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

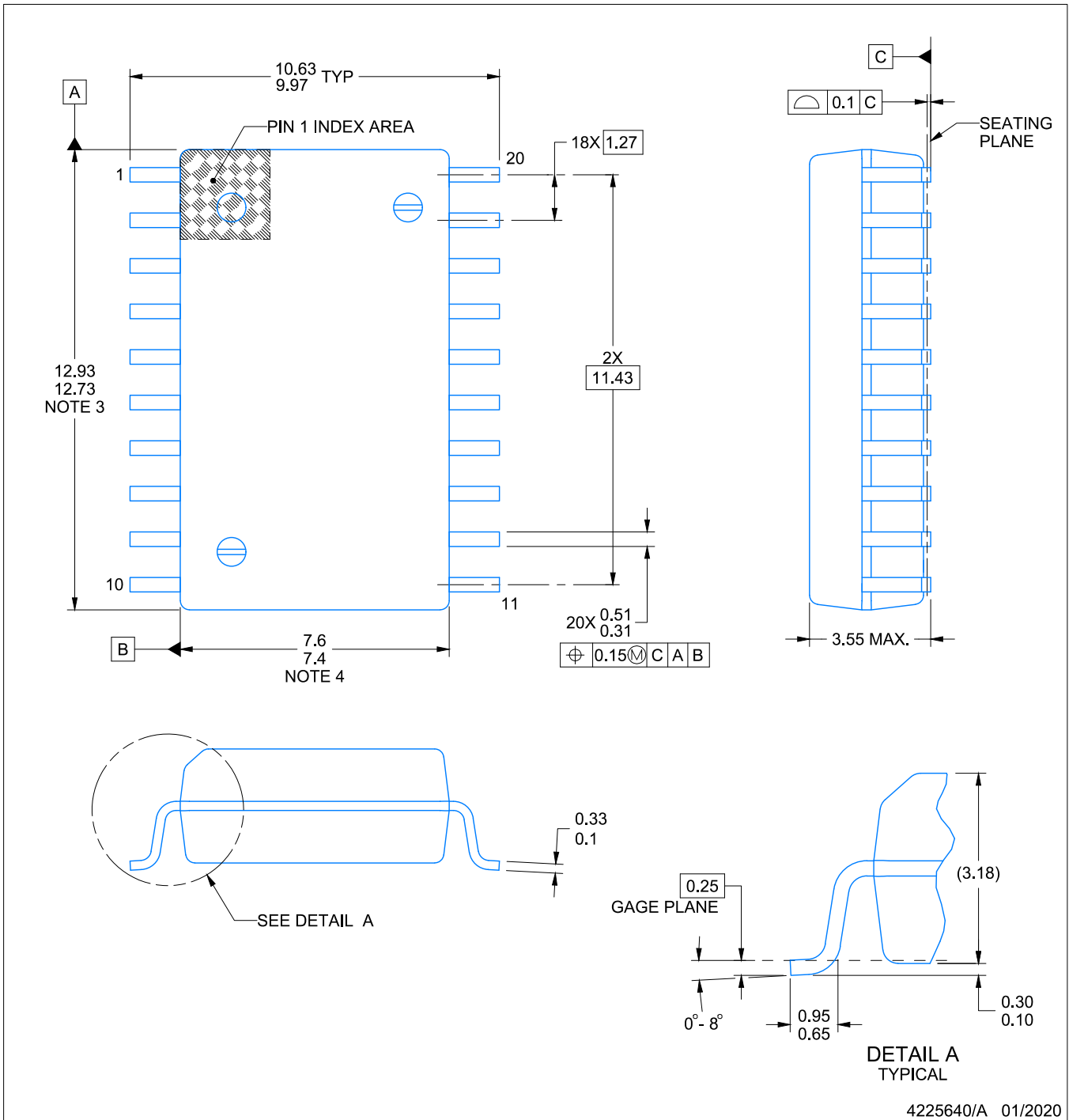
| Device           | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| ISOW7741FQDFMRQ1 | SOIC         | DFM             | 20   | 850 | 350.0       | 350.0      | 43.0        |
| ISOW7741QDFMRQ1  | SOIC         | DFM             | 20   | 850 | 350.0       | 350.0      | 43.0        |
| ISOW7742FQDFMRQ1 | SOIC         | DFM             | 20   | 850 | 350.0       | 350.0      | 43.0        |
| ISOW7742QDFMRQ1  | SOIC         | DFM             | 20   | 850 | 350.0       | 350.0      | 43.0        |

# PACKAGE OUTLINE

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



4225640/A 01/2020

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

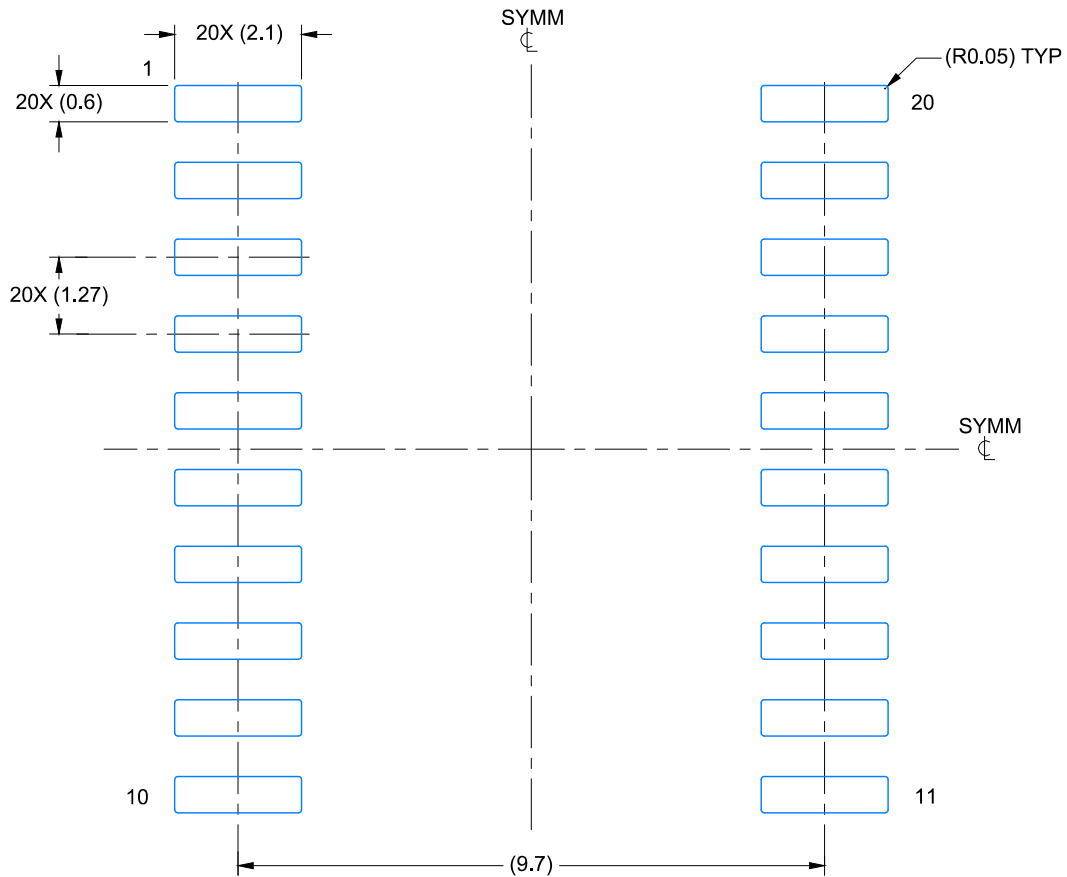


# EXAMPLE BOARD LAYOUT

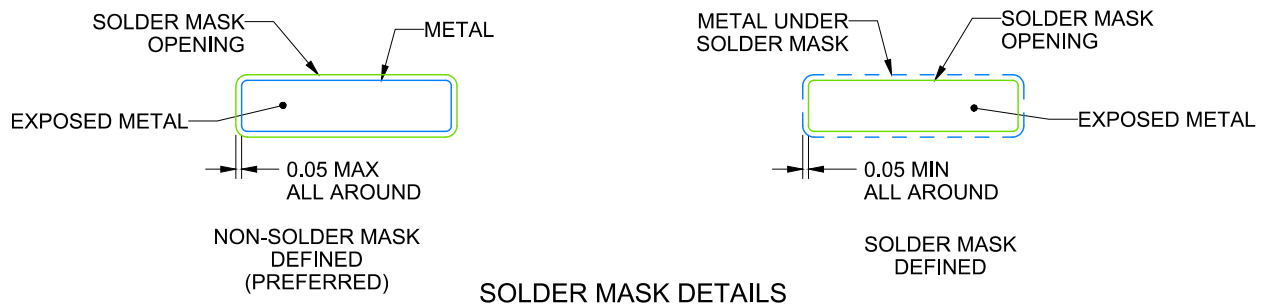
DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 8X



SOLDER MASK DETAILS

4225640/A 01/2020

NOTES: (continued)

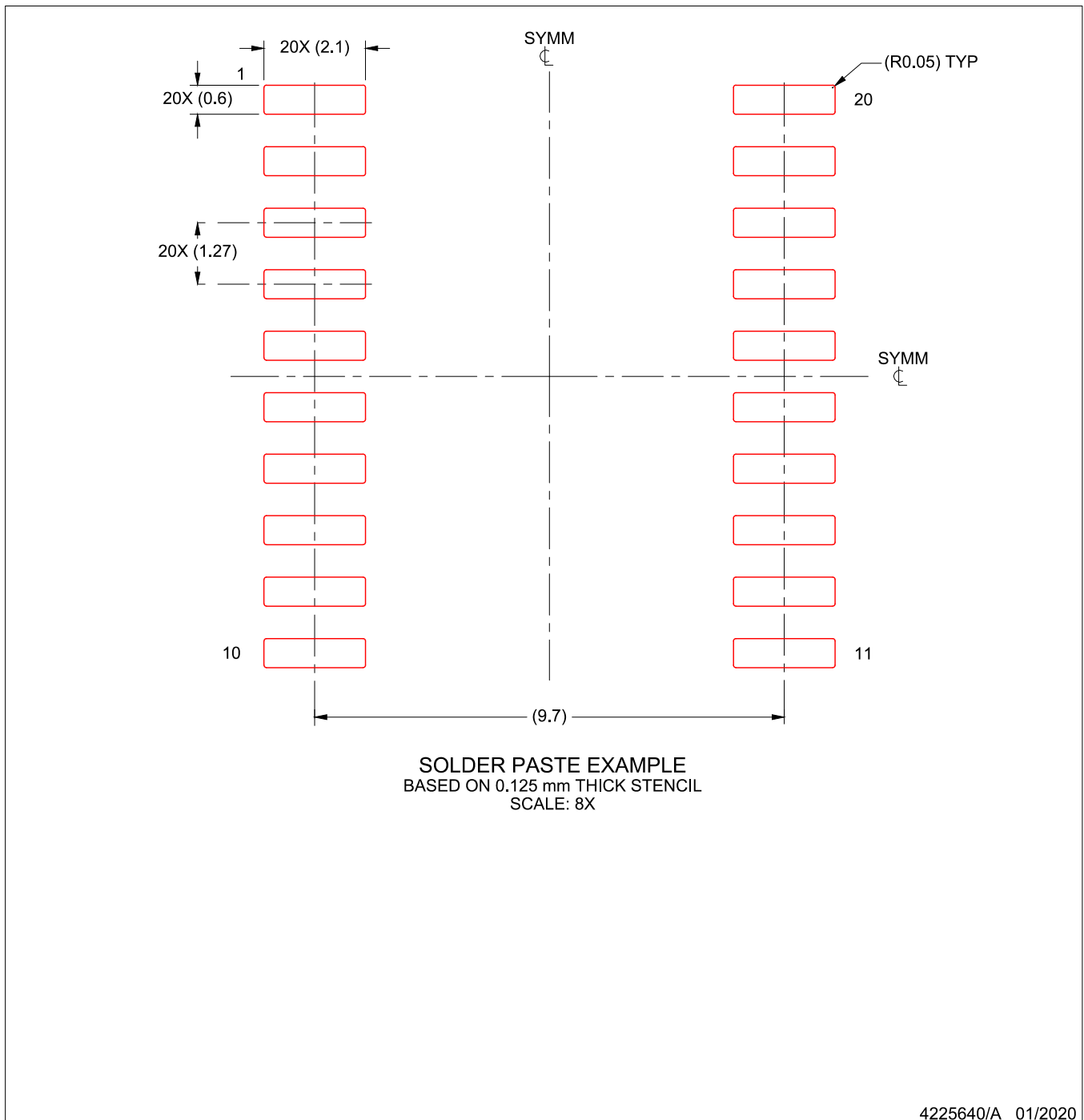
5. Publication IPC-7351 may have alternate designs.
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# EXAMPLE STENCIL DESIGN

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

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8. Board assembly site may have different recommendations for stencil design.

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