LM2105 107-V, 0.5-A, 0.8-A Half-Bridge Driver with 5-V UVLO and Integrated Bootstrap Diode

1 Features

- Drives two N-channel MOSFETs in half-bridge configuration
- Integrated bootstrap diode
- 5-V typical undervoltage lockout on GVDD
- 107-V absolute maximum voltage on BST
- –19.5-V absolute maximum negative transient voltage handling on SH
- 0.5-A/0.8-A peak source/sink currents
- 115-ns typical propagation delay

2 Applications

- Brushless-DC (BLDC) motors
- Permanent magnet synchronous motors (PMSM)
- Cordless vacuum cleaners
- Cordless garden and power tools
- E-bikes and e-scooters
- Battery test equipment
- Offline uninterruptible power supply (UPS)
- General-purpose MOSFET or IGBT driver

3 Description

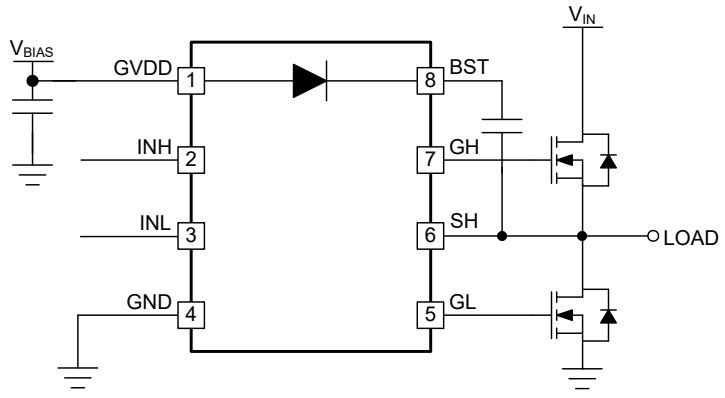
The LM2105 is a compact, high-voltage gate driver designed to drive both the high-side and the low-side N-channel MOSFETs in a synchronous buck or a half-bridge configuration. The integrated bootstrap diode saves board space and reduces system cost by eliminating the need for an external discrete diode.

The –1-V DC and –19.5-V transient negative voltage handling on the SH pin improve the system robustness in high noise applications. The small, thermally-enhanced 8-pin WSON package improves PCB layout by allowing the driver to be placed closer to the motor phases. The LM2105 is also available in an 8-pin SOIC package compatible with industry standard pinouts. Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails for protection during power up and power down.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
LM2105	D (SOIC, 8)	4.90 mm × 3.91 mm
	DSG (WSON, 8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2023) to Revision C (September 2023)	Page
• Changed title from 105-V to 107-V	1
• Changed LM2105DSG from Advance Information to Production Data	1

Changes from Revision A (March 2023) to Revision B (May 2023)	Page
• Changed D package from Advance Information to Production Data and DSG package from Product Preview to Advance Information	1

Changes from Revision * (January 2023) to Revision A (March 2023)	Page
• Changed from Private to Public Advance Information Release	1

5 Pin Configuration and Functions

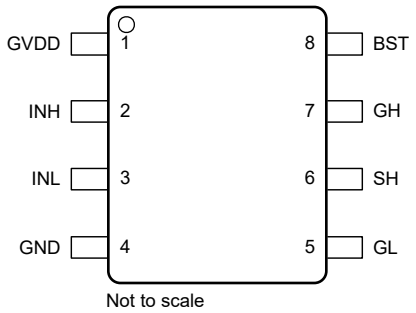


Figure 5-1. D Package, 8-Pin SOIC (Top View)

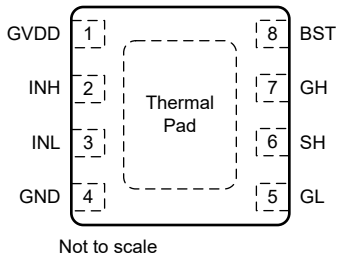


Figure 5-2. DSG Package, 8-Pin WSON (Top View)

Table 5-1. Pin Functions

PIN			DESCRIPTION
NO.(1)	NAME	TYPE(2)	
1	GVDD	P	Gate driver positive supply rail. Locally decouple to ground using low ESR and ESL capacitor located as close to IC as possible.
2	INH	I	High-side control input. The INH input is compatible with TTL and CMOS input thresholds. Unused INH input must be tied to ground and not left open.
3	INL	I	Low-side control input. The INL input is compatible with TTL and CMOS input thresholds. Unused INL input must be tied to ground and not left open.
4	GND	G	Ground. All signals are referenced to this ground.
5	GL	O	Low-side gate driver output. Connect to the gate of the low-side MOSFET or one end of external gate resistor, when used.
6	SH	P	High-side source connection. Connect to the negative terminal of the bootstrap capacitor and to the source of the high-side MOSFET.
7	GH	O	High-side gate driver output. Connect to the gate of the high-side MOSFET or one end of external gate resistor, when used.
8	BST	P	High-side gate driver positive supply rail. Connect the positive terminal of the bootstrap capacitor to BST and the negative terminal of the bootstrap capacitor to SH. The bootstrap capacitor must be placed as close to IC as possible.

(1) For 8-pin WSON package, TI recommends that the exposed pad on the bottom of the package be soldered to ground plane on the PCB and the ground plane must extend out from underneath the package to improve heat dissipation.
(2) G = Ground, I = Input, O = Output, and P = Power

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range and all voltages are with respect to GND (unless otherwise noted).(1)

			MIN	MAX	UNIT
V_{GVDD}	Low-side supply voltage		–0.3	19.5	V
V_{BST} to V_{SH}	High-side supply voltage		–0.3	19.5	V
V_{INL}, V_{INH}	Input voltages on INL and INH		–0.3	19.5	V
V_{GL}	Output voltage on GL		–0.3	GVDD + 0.3	V
V_{GH}	Output voltage on GH		V_{SH}– 0.3	V_{BST} + 0.3	V
V_{SH}	Voltage on SH	DC	–1	95	V
		Repetitive pulse < 100 ns(2)	–19.5	95	
V_{BST}	Voltage on BST		V_{SH}	107	V
T_J	Junction temperature		–40	125	°C
T_{stg}	Storage temperature	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Values are verified by characterization and are not production tested.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range and all voltages are with respect to GND (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{GVDD}	Supply voltage	5	12	18	V
$V_{INL,}$ V_{INH}	Input voltage range	0		V_{GVDD} + 0.3	V
V_{BST}	Voltage on BST	V_{SH} + 5.0		105	V
V_{SH}	Voltage on SH (DC)	–1		V_{BST} – V_{GVDD}	V
V_{SH}	Voltage on SH (repetitive pulse < 100 ns)(1)	–18		V_{BST} – V_{GVDD}	V
SR_{SH}	Voltage slew rate on SH			2	V/ns
T_J	Operating junction temperature	–40		125	°C

(1) Values are verified by characterization and are not production tested.

6.4 Thermal Information

THERMAL METRIC(1)		LM2105 D (SOIC) 8 PINS	LM2105 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.2	78.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.2	97.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.7	44.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	25.5	4.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	75.9	44.6	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		LM2105 D (SOIC) 8 PINS	LM2105 DSG (WSON) 8 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	9.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

V_{GVDD} = V_{BST} = 12 V, GND = V_{SH} = 0 V, No Load on GL or GH, T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{GVDD}	GVDD quiescent current	V_{INL} = V_{INH} = 0 V		430		µA
I_{DDO}	GVDD operating current	f = 50 kHz, C_{LOAD} = 0		0.56		mA
I_{BST}	Total BST quiescent current	V_{INL} = V_{INH} = 0 V, VDD = 12 V		130		µA
I_{BSTO}	Total BST operating current	f = 50 kHz, C_{LOAD} = 0		0.16		mA
I_{BSTS}	BST to GND quiescent current	V_{SH} = V_{BST} = 95 V, GVDD = 12 V		33.3		µA
I_{BSTSO}	BST to GND operating current	f = 50 kHz, C_{LOAD} = 0		0.07		mA
INPUT						
V_{HIT}	Input voltage high threshold	-40°C to 125°C		1.45	2	V
V_{LIT}	Input voltage low threshold	-40°C to 125°C	0.8	1.3		V
V_{IHYS}	Input voltage hysteresis			0.15		V
R_{IN}	Input pulldown resistance	V_{IN} = 3 V		200		kΩ
UNDERVOLTAGE PROTECTION (UVLO)						
V_{GVDDR}	GVDD rising threshold	V_{GVDDR} = V_{GVDD} - GND, -40°C to 125°C		4.6	4.8	V
V_{GVDDF}	GVDD falling threshold	V_{GVDDF} = V_{GVDD} - GND, -40°C to 125°C	4	4.3		V
V_{DDHYS}	GVDD threshold hysteresis			0.3		V
V_{BSTR}	VBST rising threshold	V_{BSTR} = V_{BST} - V_{SH}, -40°C to 125°C		4.25	4.7	V
V_{BSTF}	VBST falling threshold	V_{BSTF} = V_{BST} - V_{SH}, -40°C to 125°C	3.4	4		V
V_{BSTHYS}	VBST threshold hysteresis			0.25		V
BOOTSTRAP DIODE						
V_F	Low-current forward voltage	I_{BOOT} = 100 uA		0.6		V
V_{FI}	High-current forward voltage	I_{BOOT} = 100 mA		2.1		V
R_{BOOT}	Bootstrap dynamic resistance	I_{BOOT} = 100 mA and 80 mA		12.5		Ω
GL GATE DRIVER						
V_{GL_L}	Low level output voltage	I_{GL} = 100 mA, V_{GL_L} = V_{GL} – GND		0.25		V
V_{GL_H}	High level output voltage	I_{GL} = -100 mA, V_{GL_H} = V_{GVDD} – V_{GL}		0.8		V
	Peak pullup current[1]	V_{GL} = 0V		0.5		A
	Peak pulldown current[1]	V_{GL} = 12V		0.8		A
GH GATE DRIVER						
V_{GH_L}	Low level output voltage	I_{GH} = 100 mA, V_{GH_L} = V_{GH} – V_{SH}		0.25		V
V_{GH_H}	High level output voltage	I_{GH} = –100 mA, V_{GH_H} = V_{BST} – V_{GH}		0.8		V
	Peak pullup current[1]	V_{GH} = 0V		0.5		A
	Peak pulldown current[1]	V_{GH} = 12V		0.8		A

(1) Parameter not tested in production.

6.6 Switching Characteristics

V_{GVDD} = V_{BST} = 12 V, GND = V_{SH} = 0 V, No Load on GL or GH, T_J = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROPAGATION DELAYS					

6.6 Switching Characteristics (continued)

V_{GVDD} = V_{BST} = 12 V, GND = V_{SH} = 0 V, No Load on GL or GH, T_J = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLFF}	VINL falling to VGL falling	V_{INH} = V_{INL} = 0-3 V, C_{LOAD} = 0 pF. Time from 50% of the input to 90% of the output.		115		ns
t_{DHFF}	VINH falling to VGH falling	V_{INH} = $V_{IN\ L}$ = 0-3 V, C_{LOAD} = 0 pF. Time from 50% of the input to 90% of the output.		115		ns
t_{DLRR}	VINL rising to VGL rising	V_{INH} = V_{INL} = 0-3 V, C_{LOAD} = 0 pF. Time from 50% of the input to 10% of the output.		115		ns
t_{DHRR}	VINH rising to VGH rising	V_{INH} = V_{INL} = 0-3 V, C_{LOAD} = 0 pF. Time from 50% of the input to 10% of the output.		115		ns
DELAY MATCHING						
t_{MON}	Delay from GL on to GH off	INL ON, INH OFF, V_{INH} = V_{INL} = 0-3 V			30	ns
t_{MOFF}	Delay from GL off to GH on	INL OFF, INH ON, V_{INH} = V_{INL} = 0-3 V			30	ns
OUTPUT RISE AND FALL TIME						
t_{R_GL}	GL	C_{LOAD} = 1000 pF, V_{INH} = V_{INL} = 0-3 V		28		ns
t_{R_GH}	GH	C_{LOAD} = 1000 pF, V_{INH} = V_{INL} = 0-3 V		28		ns
t_{F_GL}	GL	C_{LOAD} = 1000 pF, V_{INH} = V_{INL} = 0-3 V		18		ns
t_{F_GH}	GH	C_{LOAD} = 1000 pF, V_{INH} = V_{INL} = 0-3 V		18		ns

6.7 Timing Diagrams

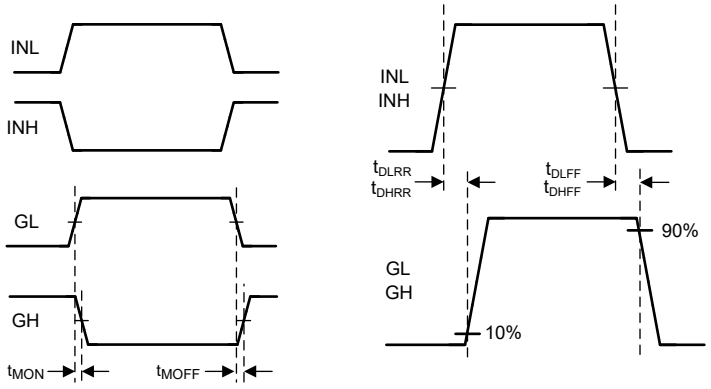


Figure 6-1. Timing Definition Diagram

6.8 Typical Characteristics

Unless otherwise specified, V_{GVDD} = V_{BST} = 12 V, GND = V_{SH} = 0 V, No Load on GL or GH, T_J = 25°C.

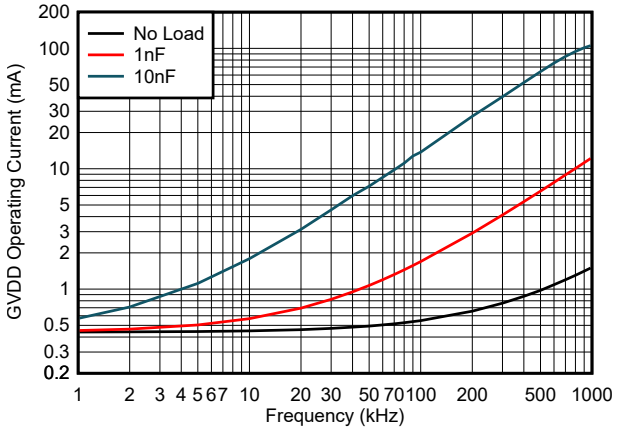


Figure 6-2. GVDD Operating Current vs Frequency

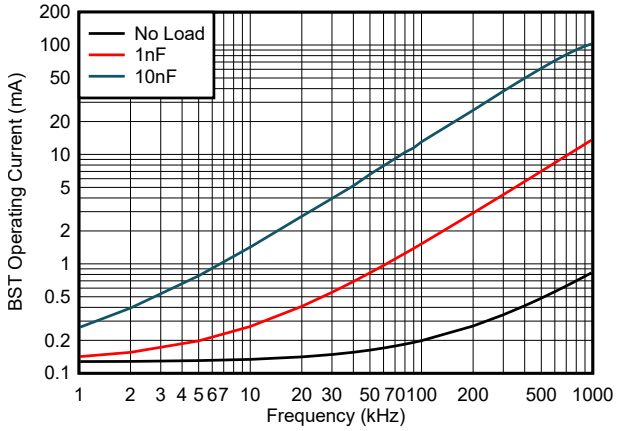


Figure 6-3. BST Operating Current vs Frequency

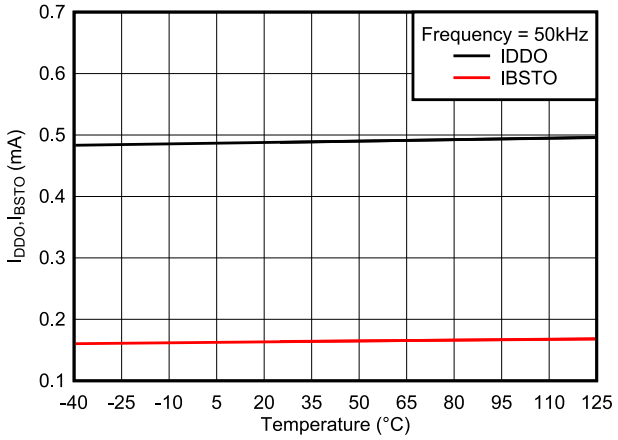


Figure 6-4. Operating Currents vs Temperature

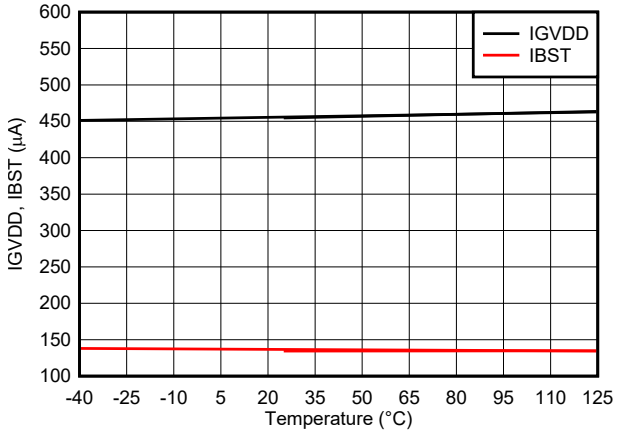


Figure 6-5. Quiescent Currents vs Temperature

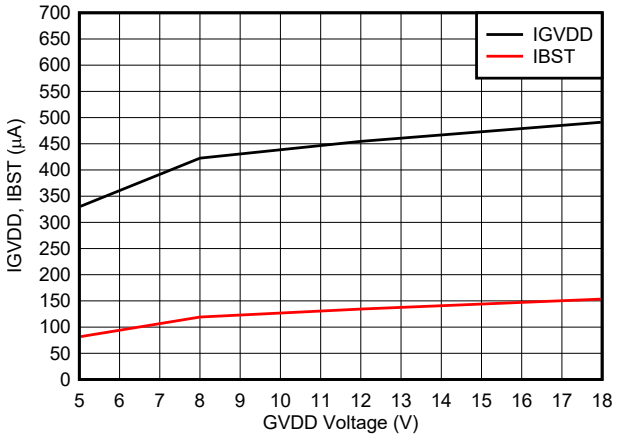


Figure 6-6. Quiescent Currents vs Supply Voltage

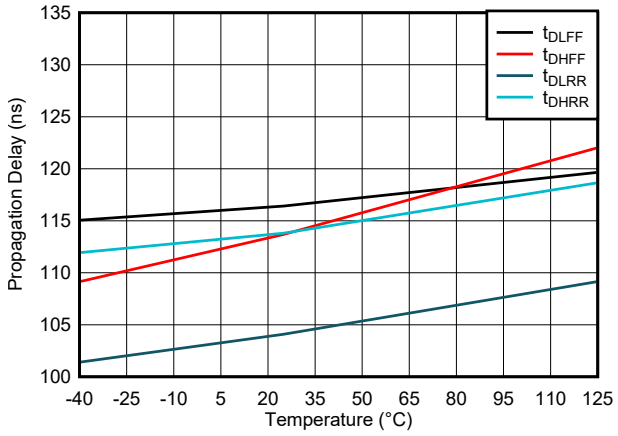


Figure 6-7. Propagation Delays vs Temperature

6.8 Typical Characteristics (continued)

Unless otherwise specified, V_{GVDD} = V_{BST} = 12 V, GND = V_{SH} = 0 V, No Load on GL or GH, T_J = 25°C.

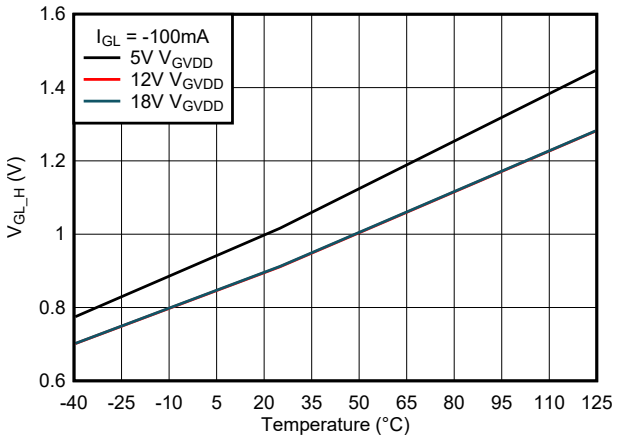


Figure 6-8. GL Output High Voltage vs Temperature

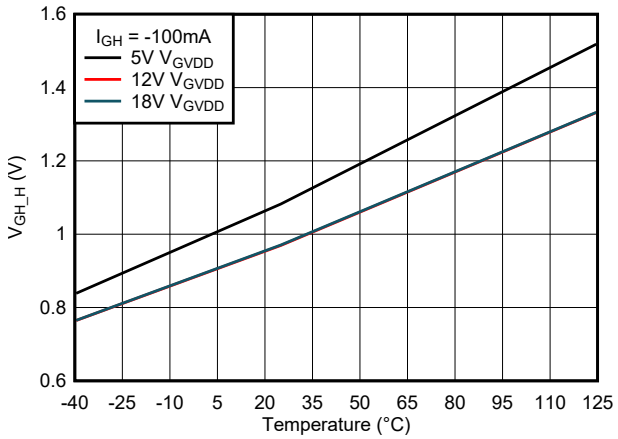


Figure 6-9. GH Output High Voltage vs Temperature

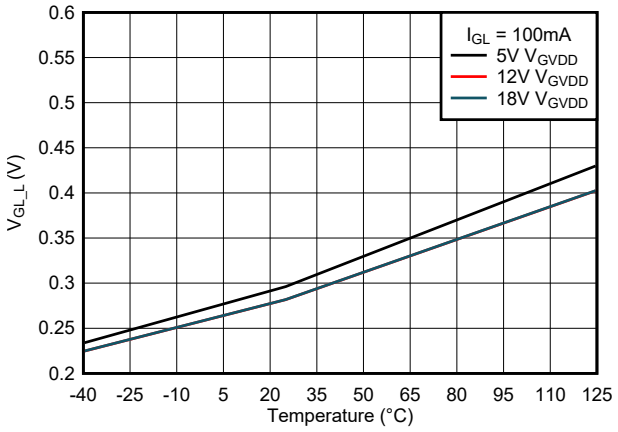


Figure 6-10. GL Output Low Voltage vs Temperature

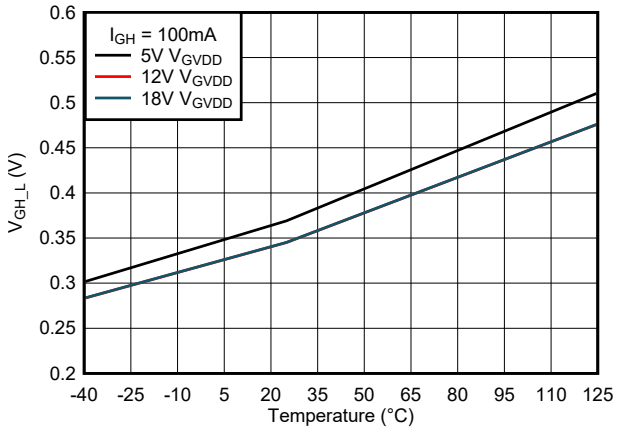


Figure 6-11. GH Output Low Voltage vs Temperature

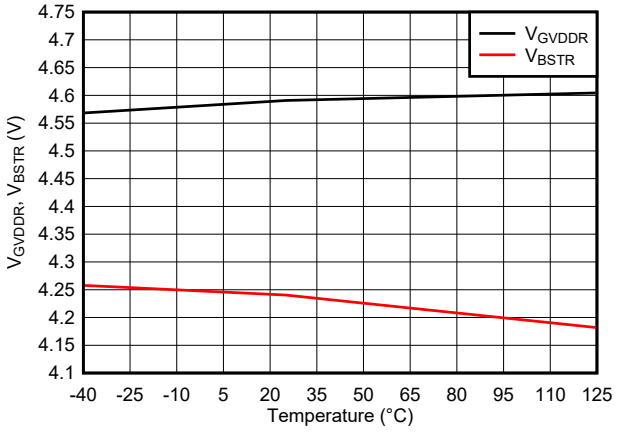


Figure 6-12. GVDD and BST UVLO Thresholds vs Temperature

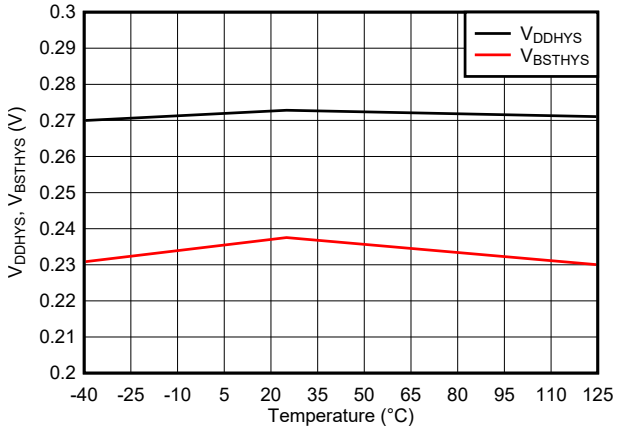


Figure 6-13. GVDD and BST UVLO Hysteresis vs Temperature

6.8 Typical Characteristics (continued)

Unless otherwise specified, V_{GVDD} = V_{BST} = 12 V, GND = V_{SH} = 0 V, No Load on GL or GH, T_J = 25°C.

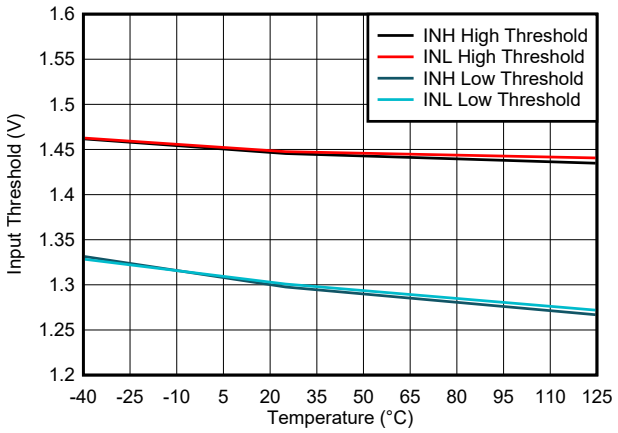


Figure 6-14. Input Voltage Thresholds vs Temperature

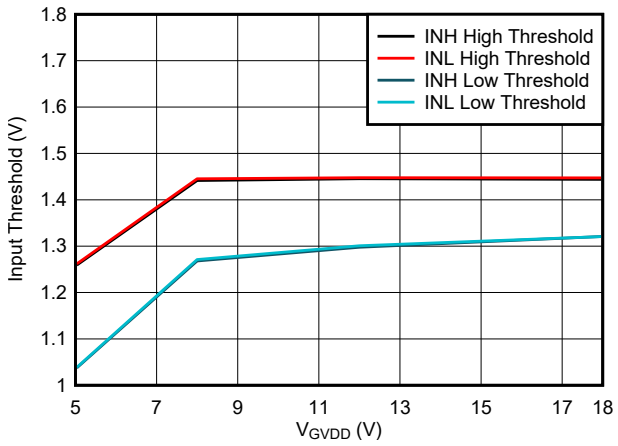


Figure 6-15. Input Voltage Thresholds vs Supply Voltage

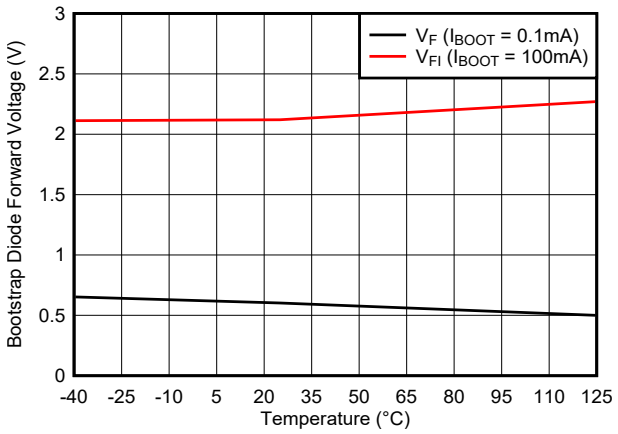


Figure 6-16. Bootstrap Diode Forward Voltage vs Supply Voltage

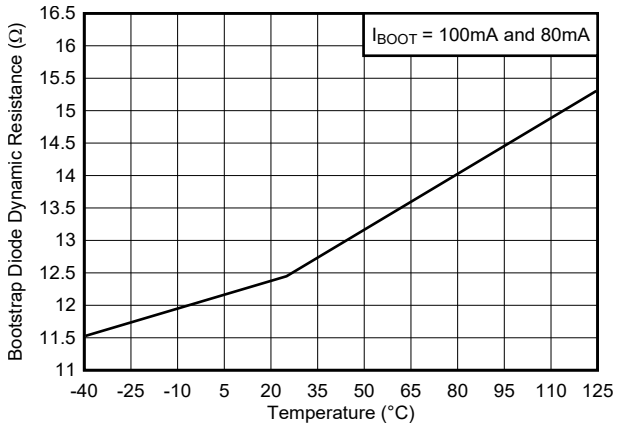


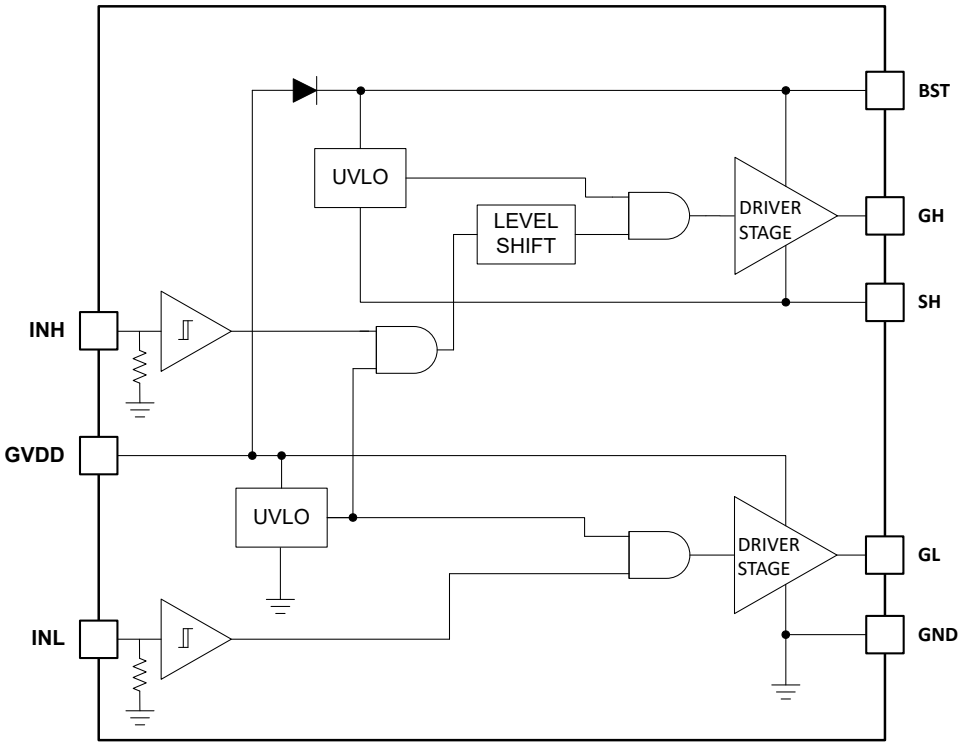
Figure 6-17. Bootstrap Diode Dynamic Resistance

7 Detailed Description

7.1 Overview

The LM2105 is a high-voltage gate driver designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The two outputs are independently controlled with two TTL-compatible input signals. The device can also work with CMOS type control signals at its inputs as long as the signals meet the turn-on and turn-off threshold specifications of the LM2105. The floating high-side driver is capable of working with a recommended BST voltage up to 105 V. A bootstrap diode is integrated in the LM2105 device to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Start-Up and UVLO

Both the high-side and the low-side driver stages include UVLO protection circuitry which monitors the supply voltage (V_{GVDD}) and the bootstrap capacitor voltage (V_{BST-SH}). The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the GVDD pin of the device, both outputs are held low until V_{GVDD} exceeds the UVLO threshold, typically 4.6 V. Any UVLO condition on the bootstrap capacitor ($V_{BST–SH}$) disables only the high-side output (GH).

Table 7-1. GVDD UVLO Logic Operation

CONDITION ($V_{BST-SH} > V_{BSTR}$)	INH	INL	GH	GL
V_{GVDD} – GND < V_{GVDDR} during device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

Table 7-1. GVDD UVLO Logic Operation (continued)

CONDITION ($V_{BST-SH} > V_{BSTR}$)	INH	INL	GH	GL
$V_{GVDD} – GND < V_{GVDDR} – V_{DDHYS}$ after device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

Table 7-2. BST UVLO Logic Operation

CONDITION ($V_{GVDD} > V_{GVDDR}$)	INH	INL	GH	GL
$V_{BST-SH} < V_{BSTR}$ during device start-up	H	L	L	L
	L	H	L	H
	H	H	L	H
	L	L	L	L
$V_{BST-SH} < V_{BSTR} – V_{BSTHYS}$ after device start-up	H	L	L	L
	L	H	L	H
	H	H	L	H
	L	L	L	L

7.3.2 Input Stages

The INL and INH inputs operate independent of each other. There is no fixed time de-glitch filter implemented at the inputs and therefore propagation delay and delay matching are not sacrificed. In other words, there is no built-in dead time. If the dead time between two outputs is desired then that shall be programmed through the microcontroller. A small filter at each of the inputs of the driver further improves system robustness in noise-prone applications. The inputs have internal pulldown resistors with typical value of 200 kΩ. Thus, when the inputs are floating, the outputs are held low.

7.3.3 Level Shift

The level shift circuit is the interface from the high-side input, which is a GND referenced signal, to the high-side driver stage, which is referenced to the switch node (SH). The level shift allows control of the GH output which is referenced to the SH pin and provides excellent delay matching with the low-side driver.

7.3.4 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to GND and the high-side is referenced to SH.

7.3.5 SH Transient Voltages Below Ground

In most applications, the body diode of the external low-side power MOSFET clamps the SH node to ground. In some situations, board capacitance and inductance can cause the SH node to transiently swing several volts below ground, before the body diode of the external low-side MOSFET clamps this swing. The SH pin in the LM2105 is allowed to swing below ground as long as specifications are not violated and conditions mentioned in this section are followed.

SH must always be at a lower potential than GH. Pulling GH more negative than specified conditions can activate parasitic transistors which may result in excessive current flow from the BST supply. This may result in damage to the device. The same relationship is true with GL and GND. If necessary, a Schottky diode can be placed externally between GH and SH or GL and GND to protect the device from this type of transient. The diode must be placed as close to the device pins as possible in order to be effective.

Low ESR bypass capacitors from BST to SH and from GVDD to GND are essential for proper operation of the gate driver device. The capacitor should be located at the leads of the device to minimize series inductance. The peak currents from GL and GH can be quite large. Any series inductance with the bypass capacitor causes voltage ringing at the leads of the device which must be avoided for reliable operation.

7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See Section 7.3.1 for more information on UVLO operation mode. In normal mode, when the V_{GVDD} and $V_{BST–SH}$ are above UVLO threshold, the output stage is dependent on the states of the INH and INL pins. The outputs GH and GL will be low if input state is floating.

Table 7-3. Input/Output Logic in Normal Mode of Operation

INH	INL	GH(1)	GL(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
Floating	Floating	L	L

(1) GH is measured with respect to SH.
(2) GL is measured with respect to GND.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

To operate power MOSFETs at high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level-shift circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers can also minimize the effect of high-frequency switching noise by being placed physically close to the power switch. Additionally, gate drivers can drive gate-drive transformers and control floating power-device gates, reducing the controller's power dissipation and thermal stress by moving the gate-charge power losses into the driver.

8.2 Typical Application

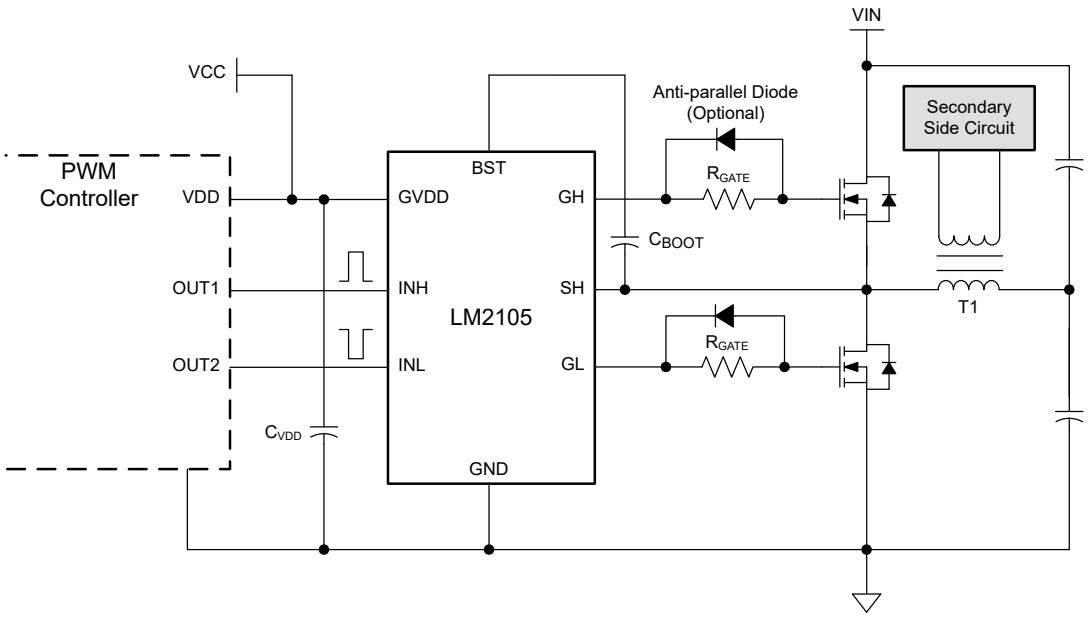


Figure 8-1. LM2105 Driving MOSFETs in a Half-Bridge Converter

8.2.1 Design Requirements

Table 8-1 lists the design parameters of the LM2105.

Table 8-1. Design Example

PARAMETER	VALUE
Gate Driver	LM2105
MOSFET	CSD19534KCS
V_{DD}	10 V
Q_G	17 nC
f_{SW}	50 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Select Bootstrap and GVDD Capacitor

The bootstrap capacitor must maintain the V_{BST-SH} voltage above the UVLO threshold for normal operation. Calculate the maximum allowable drop across the bootstrap capacitor with Equation 1.

$$\Delta V_{BST} = V_{GVDD} - V_{DH} - V_{BSTL} = 10V - 2.1V - 4.45V = 3.45V \quad (1)$$

where

- V_{GVDD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- V_{BSTL} = BST falling threshold ($V_{BSTR(max)}$ - V_{BSTHYS})

Then, the total charge needed per switching cycle is estimated by Equation 2.

$$Q_{TOTAL} = Q_G + I_{BSTS} \times \frac{D_{MAX}}{f_{SW}} + \frac{I_{BST}}{f_{SW}} = 17nC + 33.3\mu A \times \frac{0.95}{50kHz} + \frac{130\mu A}{50kHz} = 20nC \quad (2)$$

where

- Q_G = Total MOSFET gate charge
- I_{BSTS} = BST to VSS leakage current
- D_{Max} = Converter maximum duty cycle
- I_{BST} = BST quiescent current

Next, use Equation 3 to estimate the minimum bootstrap capacitor value.

$$C_{BOOT\ (MIN)} = \frac{Q_{TOTAL}}{\Delta V_{BST}} = \frac{20nC}{3.45V} = 5.8nF \quad (3)$$

In practice, the value of the C_{Boot} capacitor must be greater than calculated to allow for situations where the power stage may skip pulse due to load transients. Equation 4 can be used to estimate the recommended bootstrap capacitance based on the maximum bootstrap voltage ripple desired for a specific application.

$$C_{BOOT} > \frac{Q_{TOTAL}}{\Delta V_{BST\_RIPPLE}} \quad (4)$$

where

- ΔV_{BST_RIPPLE} = Maximum allowable voltage drop across the bypass capacitor based on system requirements

TI recommends having enough margins and to place the bootstrap capacitor as close to the BST and SH pins as possible.

$$C_{BOOT} = 100\ nF \quad (5)$$

As a general rule, the local V_{GVDD} bypass capacitor must be 10 times greater than the value of C_{BOOT}, as shown in Equation 6.

$$C_{GVDD} = 1\ \mu F \quad (6)$$

The bootstrap and bias capacitors must be ceramic types with X7R dielectric. The voltage rating must be twice that of the maximum V_{GVDD} considering capacitance tolerances once the devices have a DC bias voltage across them and to ensure long-term reliability.

8.2.2.2 Select External Gate Driver Resistor

The external gate driver resistor, R_{GATE}, is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver.

The peak GH pullup current is calculated in Equation 7.

$$I_{GHH} = \frac{V_{GVDD} - V_{DH}}{R_{GHH} + R_{GATE} + R_{GFET\_INT}} \quad (7)$$

where

- I_{GHH} = GH Peak pullup current
- V_{DH} = Bootstrap diode forward voltage drop
- R_{GHH} = Gate driver internal GH pullup resistance, estimated from the testing conditions, that is $R_{GHH} = V_{GH\_H} / I_{GH}$
- R_{GATE} = External gate drive resistance
- R_{GFET_INT} = MOSFET internal gate resistance, provided by transistor data sheet

Similarly, the peak GH pulldown current is shown in Equation 8.

$$I_{GHL} = \frac{V_{GVDD} - V_{DH}}{R_{GHL} + R_{GATE} + R_{GFET\_INT}} \quad (8)$$

where

- R_{GHL} is the GH pulldown resistance

The peak GL pullup current is shown in Equation 9.

$$I_{GLH} = \frac{V_{GVDD}}{R_{GLH} + R_{GATE} + R_{GFET\_INT}} \quad (9)$$

where

- R_{GLH} is the GL pullup resistance

The peak GL pulldown current is shown in Equation 10.

$$I_{GLL} = \frac{V_{GVDD}}{R_{GLL} + R_{GATE} + R_{GFET\_INT}} \quad (10)$$

where

- R_{GLL} is the GL pulldown resistance

For some scenarios, if the applications require fast turnoff, an anti-paralleled diode on R_{Gate} could be used to bypass the external gate drive resistor and speed up turnoff transition.

8.2.2.3 Estimate the Driver Power Loss

The total driver IC power dissipation can be estimated through the following components.

1. Static power losses, P_{QC}, due to quiescent currents I_{GVDD} and I_{BST} is shown in Equation 11.

$$P_{QC} = V_{GVDD} \times I_{GVDD} + (V_{GVDD} - V_F) \times I_{BST} = 10V \times 0.43mA + (10V - 0.6V) \times 0.13mA = 5.52mW \quad (11)$$

2. Level-shifter losses, P_{IBSTS}, due high-side leakage current I_{BSTS} is shown in Equation 12.

$$P_{IBSTS} = V_{BST} \times I_{BSTS} \times D = 72V \times 0.033mA \times 0.95 = 2.26mW \quad (12)$$

where

- D is the high-side switch duty cycle

3. Dynamic losses, $P_{QG1\&2}$, due to the FETs gate charge Q_G as shown in Equation 13.

$$P_{QG1\&2} = 2 \times V_{GVDD} \times Q_G \times f_{SW} \times \frac{R_{GD\_R}}{R_{GD\_R} + R_{GATE} + R_{GFET\_INT}} = 2 \times 10V \times 17nC \times 50kHz \times \frac{5.25\Omega}{5.25\Omega + 4.7\Omega + 2.2\Omega} = 7.35mW \quad (13)$$

where

- Q_G = Total FETs gate charge
- f_{SW} = Switching frequency
- R_{GD_R} = Average value of pullup and pulldown resistor
- R_{GATE} = External gate drive resistor
- R_{GFET_INT} = Internal FETs gate resistor

4. Level-shifter dynamic losses, P_{LS}, during high-side switching due to required level-shifter charge on each switching cycle. For this example it is assumed that value of parasitic charge Q_P is 2.5 nC, as shown in Equation 14.

$$P_{LS} = V_{BST} \times Q_P \times f_{SW} = 72V \times 2.5nC \times 50kHz = 9mW \quad (14)$$

In this example, the sum of all the losses is 24 mW as a total gate driver loss. For gate drivers that include bootstrap diode, one should also estimate losses in the bootstrap diode. Diode forward conduction loss is computed as product of average forward voltage drop and average forward current.

Equation 15 estimates the maximum allowable power loss of the device for a given ambient temperature.

$$P_{MAX} = \frac{T_J - T_A}{R_{\theta JA}} \quad (15)$$

where

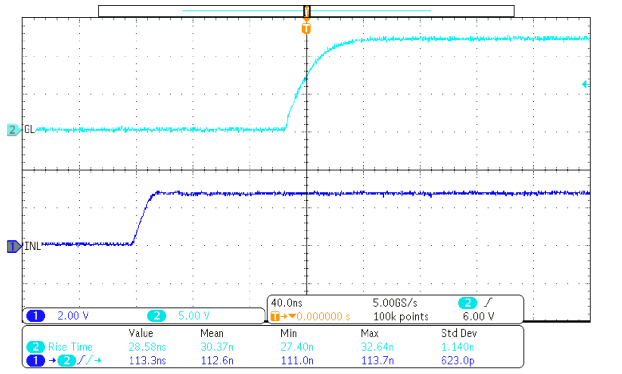
- P_{MAX} = Maximum allowed power dissipation in the gate driver device
- T_J = Junction temperature
- T_A = Ambient temperature
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance

The thermal metrics for the driver package is summarized in the *Thermal Information* table of the data sheet. For detailed information regarding the thermal information table, refer to the Texas Instruments application note entitled *Semiconductor and IC Package Thermal Metrics*.

8.2.3 Application Curves

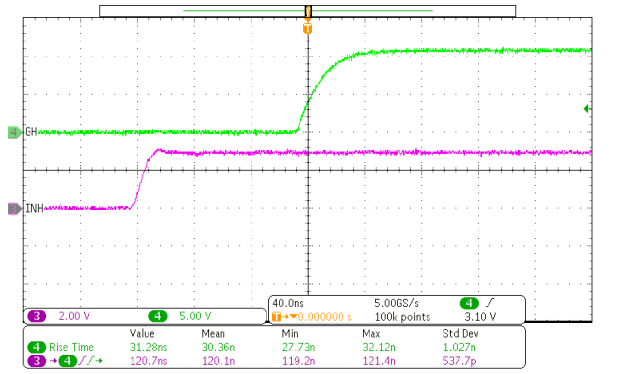
Figure 8-2 and Figure 8-3 show the rise times and turn-on propagation delays for the low side driver and the high side driver respectively. Likewise, Figure 8-4 and Figure 8-5 show the fall times and turn-off propagation delays. Each channel (INH, INL, GH, and GL) is labeled and displayed on the left hand of the waveforms.

The testing condition: load capacitance is 1 nF, gate resistor is 4 Ω, V_{DD} = 12 V, f_{SW} = 50 kHz.



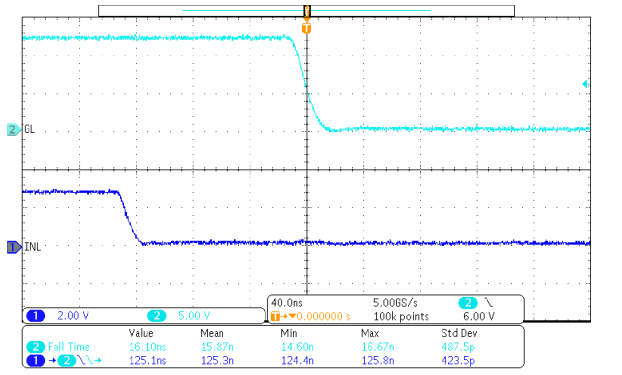
C_L = 1 nF R_G = 4 Ω | V_{GVDD} = 12 V f_{SW} = 50 kHz

Figure 8-2. GL Rise Time and INL to GL Turn-on Propagation Delay



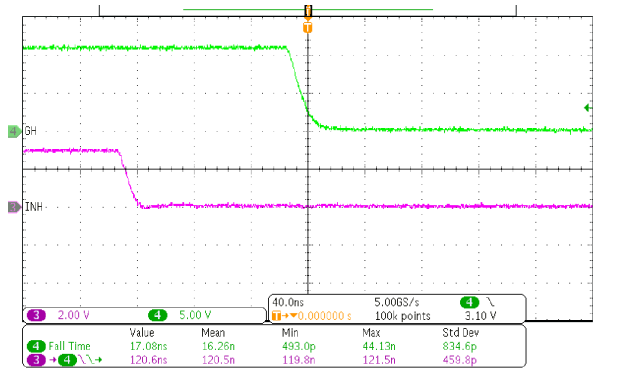
C_L = 1 nF R_G = 4 Ω | V_{GVDD} = 12 V f_{SW} = 50 kHz

Figure 8-3. GH Rise Time and INH to GH Turn-on Propagation Delay



C_L = 1 nF R_G = 4 Ω | V_{DD} = 12 V f_{SW} = 50 kHz

Figure 8-4. GL Fall Time and INL to GL Turn-off Propagation Delay



C_L = 1 nF R_G = 4 Ω | V_{DD} = 12 V f_{SW} = 50 kHz

Figure 8-5. GH Fall Time and INH to GH Turn-off Propagation Delay

9 Power Supply Recommendations

The recommended bias supply voltage range for LM2105 is from 5 V to 18 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the V_{GVDD} supply circuit blocks. The upper end of this range is driven by the 18-V recommended maximum voltage rating of the GVDD pin. It is recommened that the voltage on GVDD pin is lower than the maximum recommended voltage to account for transient voltage spikes.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the V_{GVDD} voltage drops, the device continues to operate in normal mode as long as the voltage drop does not exceed the hysteresis specification, V_{DDHYS}. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 5-V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of LM2105 to avoid triggering device-shutdown.

A local bypass capacitor must be placed between the GVDD and GND pins and this capacitor must be located as close to the device as possible. A low-ESR, ceramic surface mount capacitor is recommended.

TI recommends using 2 capacitors across GVDD and GND: a low capacitance ceramic surface-mount capacitor for high-frequency filtering placed very close to GVDD and GND pins, and another high capacitance value surface-mount capacitor for IC bias requirements. In a similar manner, the current pulses delivered by the GH pin are sourced from the BST pin. Therefore, a local decoupling capacitor is recommended between the BST and SH pins.

10 Layout

10.1 Layout Guidelines

Optimum performance of half-bridge gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low-ESR and low-ESL capacitors must be connected close to the IC between GVDD and GND pins and between BST and SH pins to support high peak currents being drawn from GVDD and BST during the turn-on of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low-ESR electrolytic capacitor and a good-quality ceramic capacitor must be connected between the MOSFET drain and ground (GND).
3. To avoid large negative transients on the switch node (SH) pin, the parasitic inductances between the source of the top MOSFET and the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver must be placed as close as possible to the MOSFETs.
   - The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced GVDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

10.2 Layout Example

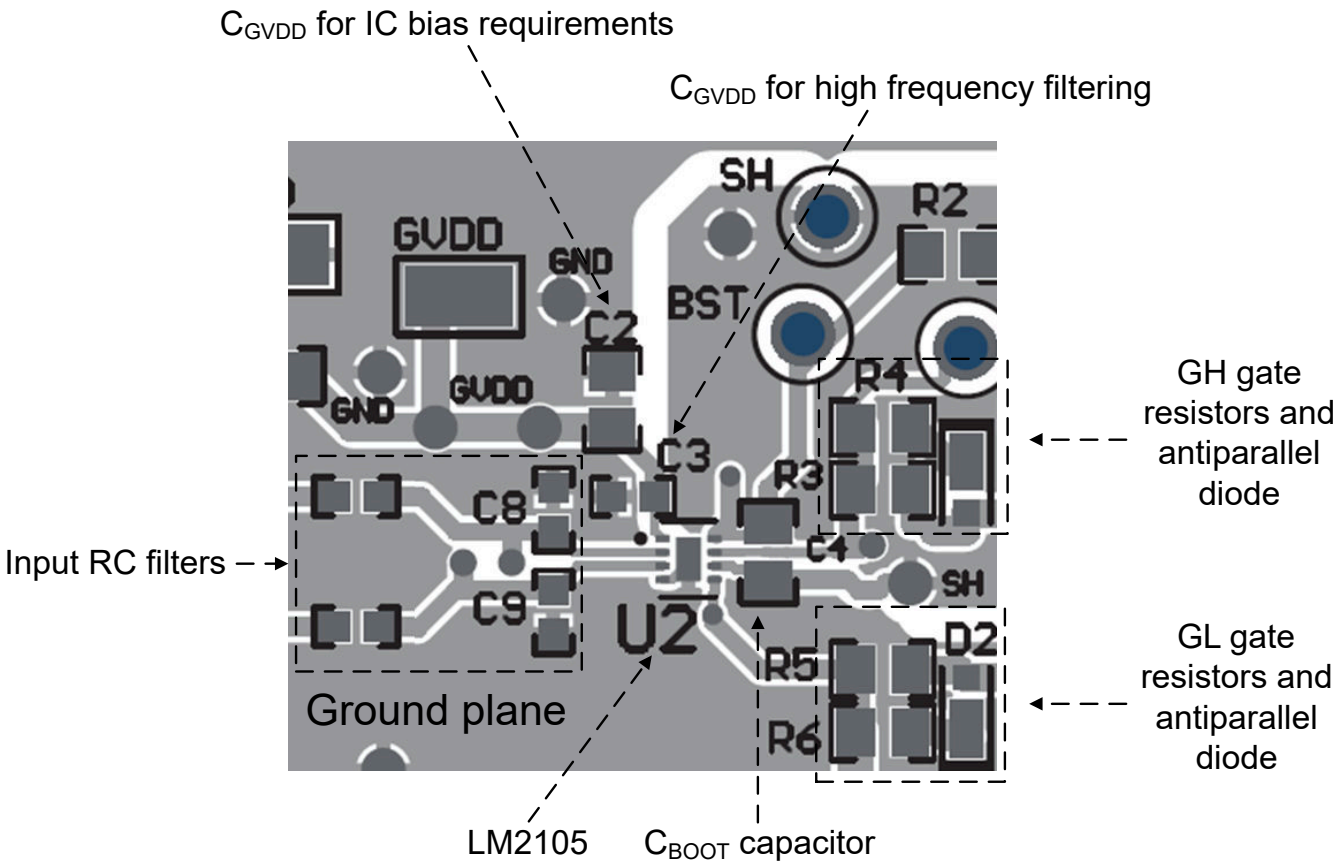


Figure 10-1. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Packaging Thermal Metrics*, SPRA953

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2105DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2105	Samples
LM2105DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L105	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

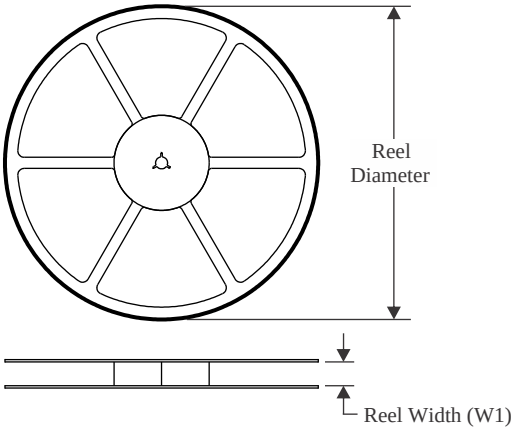
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

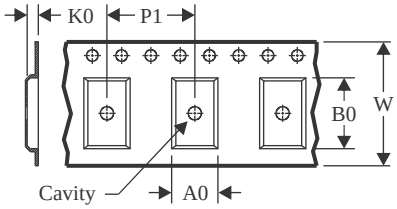
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

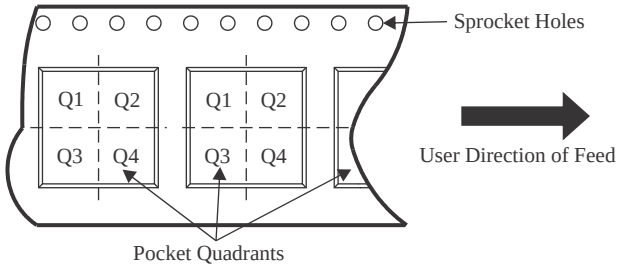


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

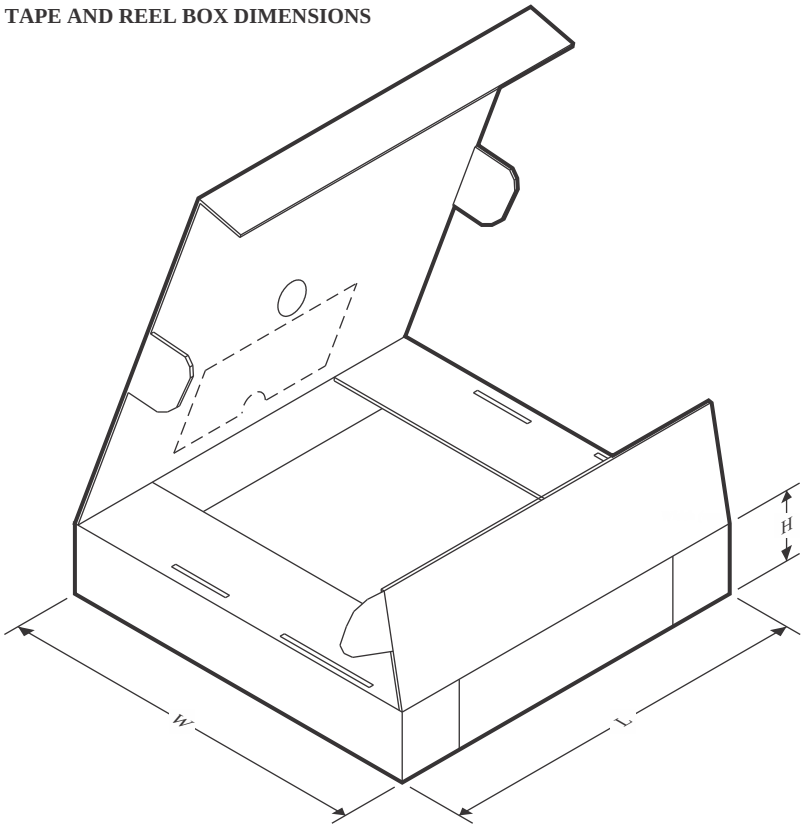
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

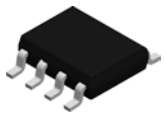
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2105DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2105DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2105DR	SOIC	D	8	3000	356.0	356.0	35.0
LM2105DSGR	WSON	DSG	8	3000	210.0	185.0	35.0

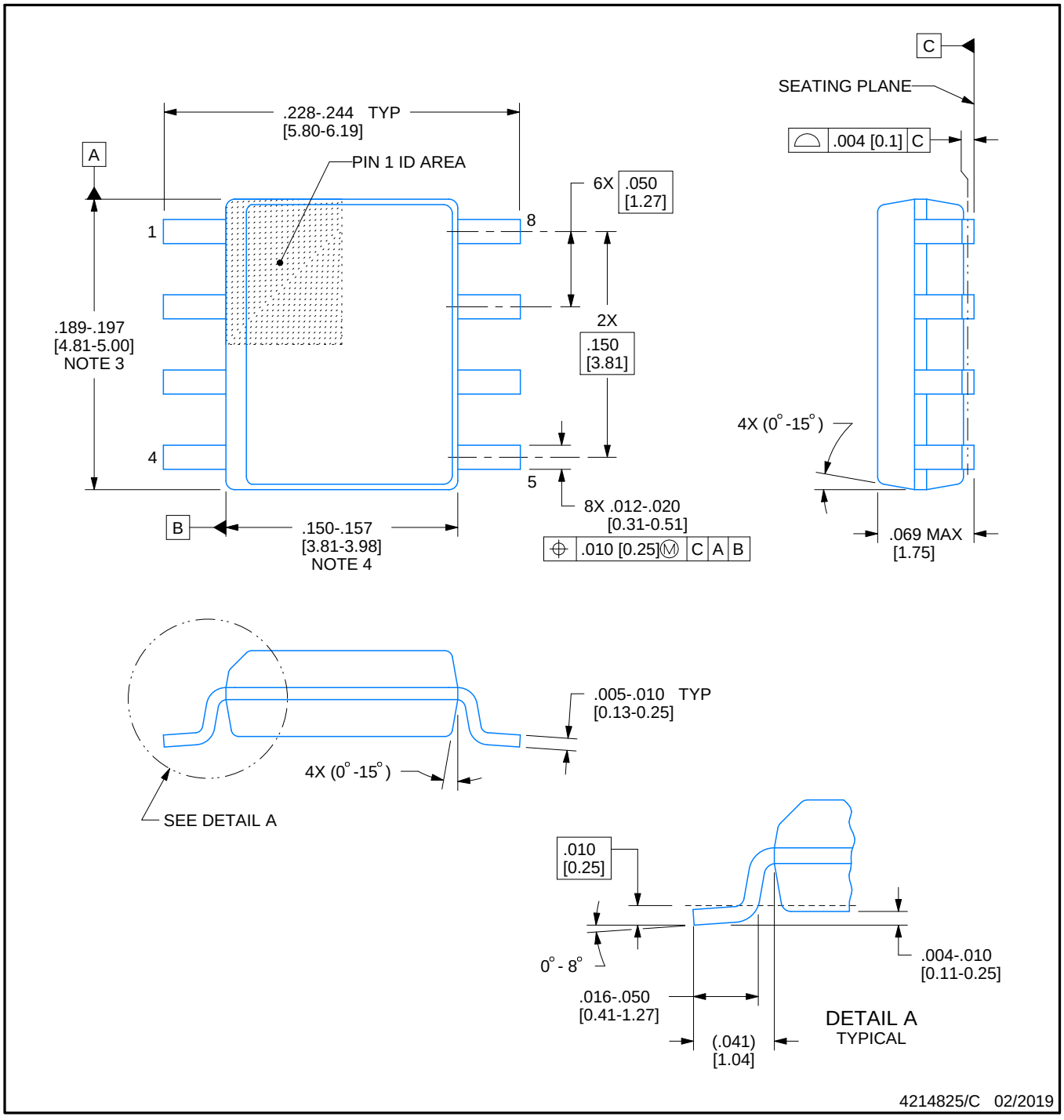


PACKAGE OUTLINE

D0008A

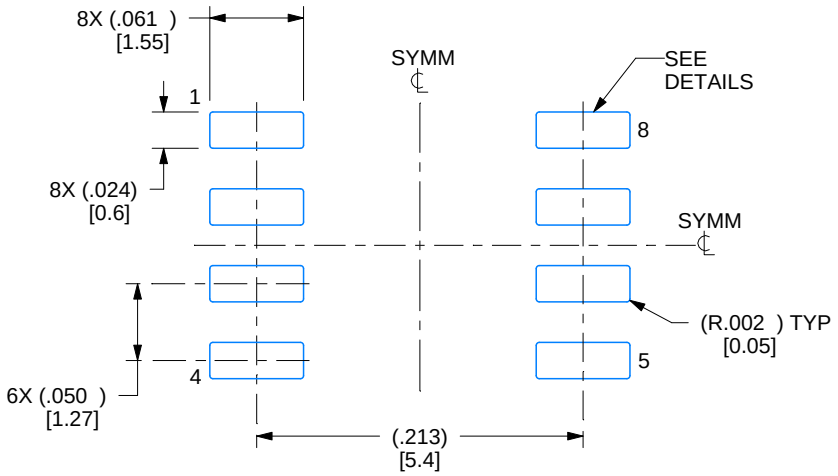
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

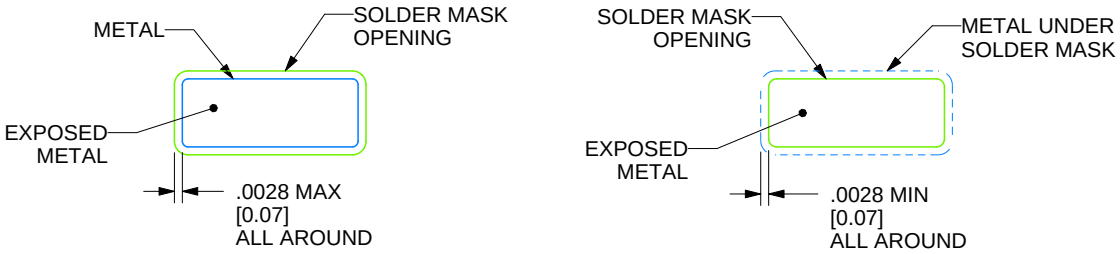


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

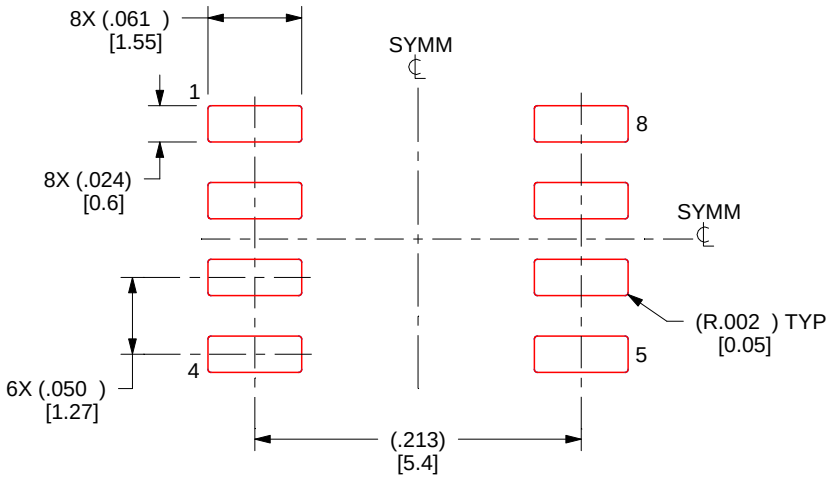
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

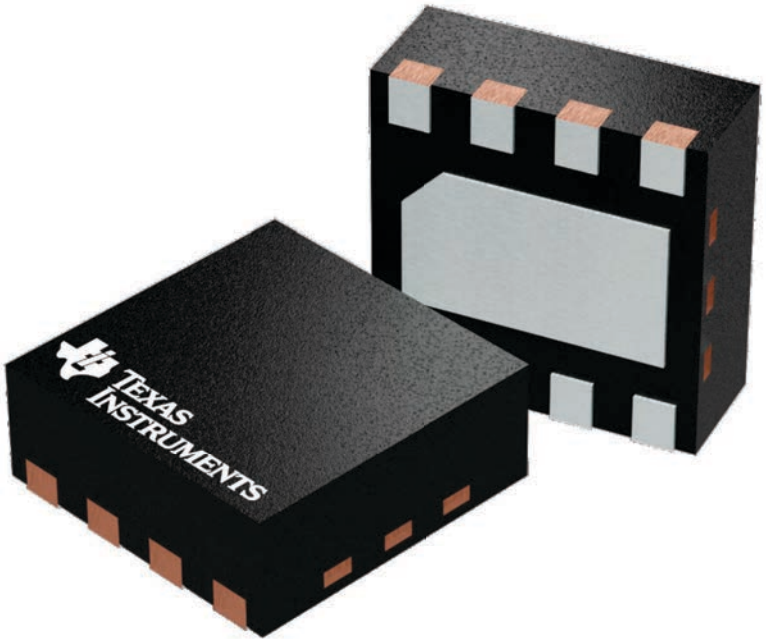
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



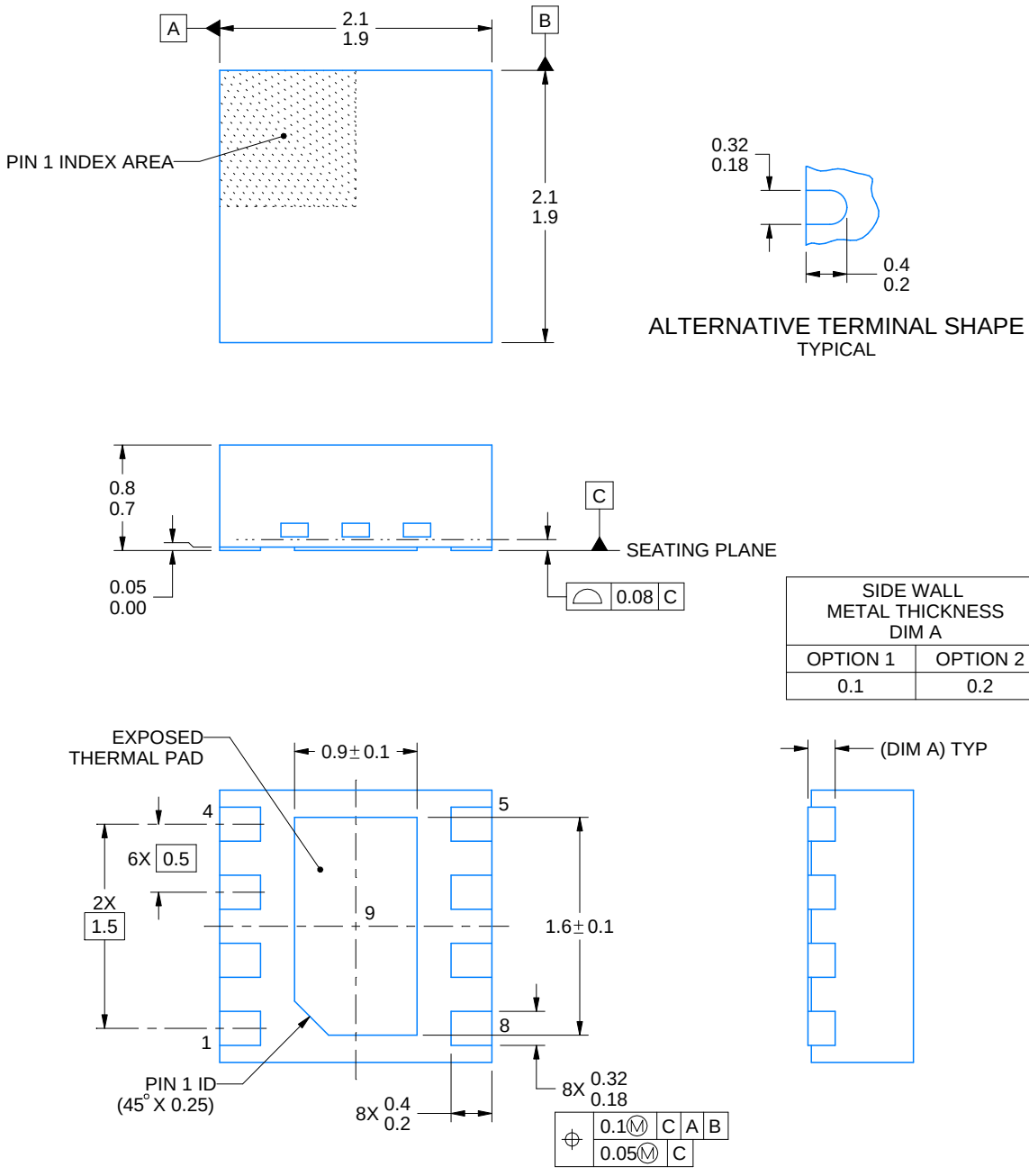
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

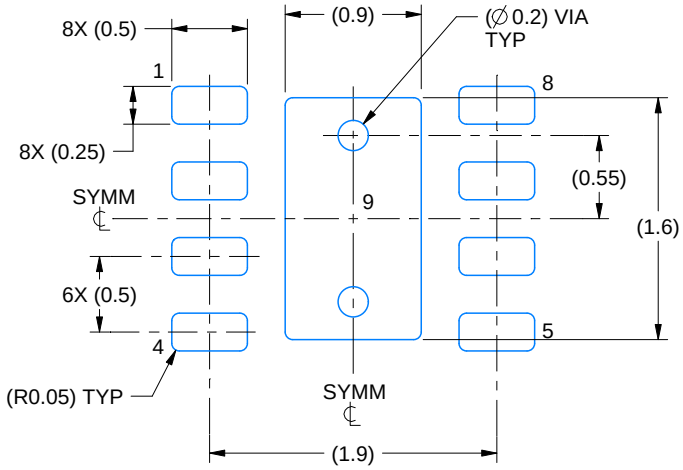
PLASTIC SMALL OUTLINE - NO LEAD



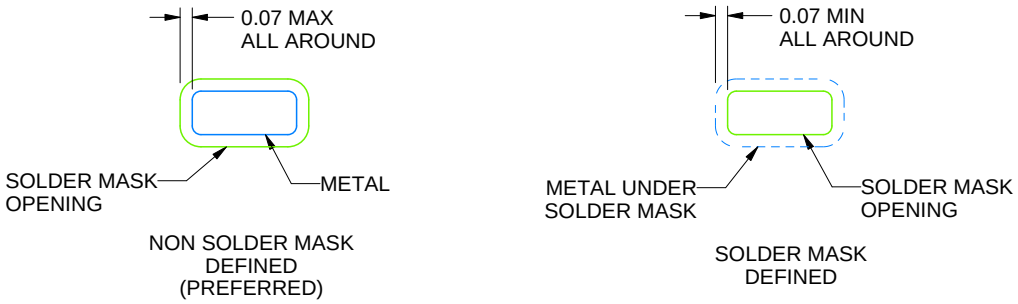
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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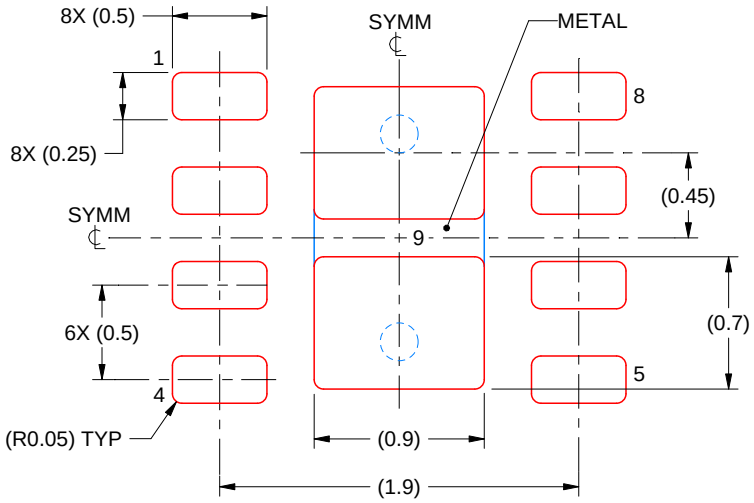
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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