## LM2700 600kHz/1.25MHz, 2.5A, Step-up PWM DC/DC Converter

**Check for Samples: LM2700**

## FEATURES

- **3.6A, 0.08Ω, Internal Switch**
- **Operating Input Voltage Range of 2.2V to 12V**
- **Input Undervoltage Protection**
- **Adjustable Output Voltage up to 17.5V**
- **600kHz/1.25MHz Pin Selectable Frequency Operation**
- **Over Temperature Protection**
- **Small 14-Lead TSSOP or WSON Package**

## APPLICATIONS

- **LCD Bias Supplies**
- **Handheld Devices**
- **Portable Applications**
- **GSM/CDMA Phones**
- **Digital Cameras**

## DESCRIPTION

The LM2700 is a step-up DC/DC converter with a 3.6A, 80mΩ internal switch and pin selectable operating frequency. With the ability to produce 500mA at 8V from a single Lithium Ion battery, the LM2700 is an ideal part for biasing LCD displays. The LM2700 can be operated at switching frequencies of 600kHz and 1.25MHz allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. The LM2700 features continuous switching at light loads and operates with a switching quiescent current of 2.0mA at 600kHz and 3.0mA at 1.25MHz. The LM2700 is available in a low profile 14-lead TSSOP package or a 14-lead WSON package.
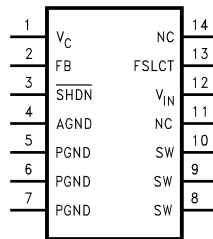
**Typical Application Circuit**
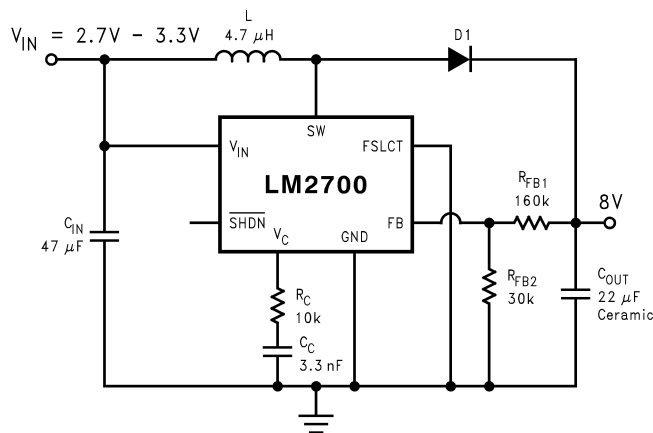


**Figure 1. 600 kHz Operation**

## Connection Diagram



**Figure 2. Top View**
**14-Lead TSSOP or WSON**

## PIN DESCRIPTION

| Pin | Name | Function |
|-----|------|----------|
| 1 | $V_C$ | Compensation network connection. Connected to the output of the voltage error amplifier. |
| 2 | FB | Output voltage feedback input. |
| 3 | $\overline{SHDN}$ | Shutdown control input, active low. |
| 4 | AGND | Analog ground. |
| 5 | PGND | Power ground. PGND pins must be connected together directly at the part. |
| 6 | PGND | Power ground. PGND pins must be connected together directly at the part. |
| 7 | PGND | Power ground. PGND pins must be connected together directly at the part. |
| 8 | SW | Power switch input. Switch connected between SW pins and PGND pins. |
| 9 | SW | Power switch input. Switch connected between SW pins and PGND pins. |
| 10 | SW | Power switch input. Switch connected between SW pins and PGND pins. |
| 11 | NC | Pin not connected internally. |
| 12 | $V_{IN}$ | Analog power input. |
| 13 | FSLCT | Switching frequency select input. $V_{IN}$ = 1.25MHz. Ground = 600kHz. |
| 14 | NC | Connect to ground. |

Product Folder Links: *LM2700*
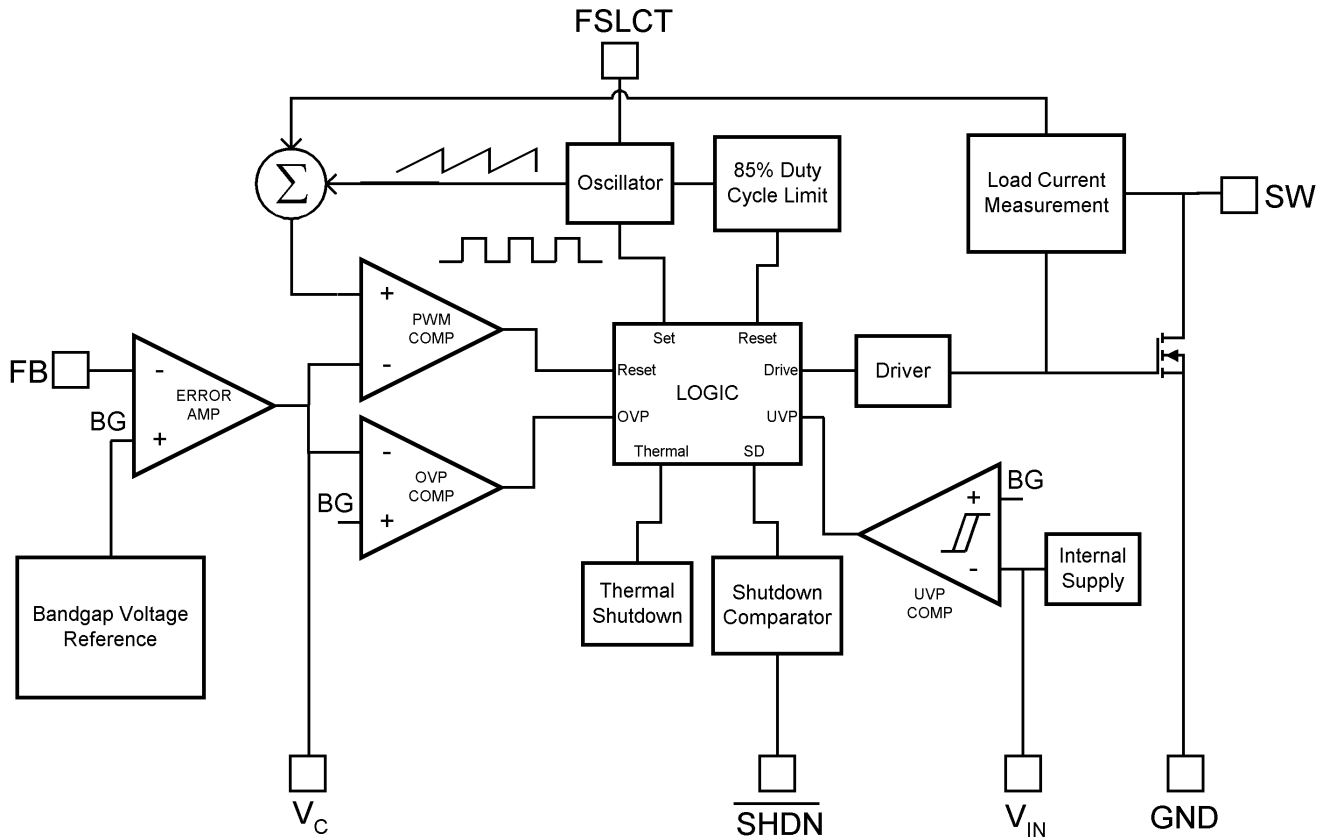
## Block Diagram



## Detailed Description

The LM2700 utilizes a PWM control scheme to regulate the output voltage over all load conditions. The operation can best be understood referring to the block diagram and Figure 17 of the Operation section. At the start of each cycle, the oscillator sets the driver logic and turns on the NMOS power device conducting current through the inductor, cycle 1 of Figure 17(a). During this cycle, the voltage at the $V_C$ pin controls the peak inductor current. The $V_C$ voltage will increase with larger loads and decrease with smaller. This voltage is compared with the summation of the SW voltage and the ramp compensation. The ramp compensation is used in PWM architectures to eliminate the sub-harmonic oscillations that occur during duty cycles greater than 50%. Once the summation of the ramp compensation and switch voltage equals the $V_C$ voltage, the PWM comparator resets the driver logic turning off the NMOS power device. The inductor current then flows through the schottky diode to the load and output capacitor, cycle 2 of Figure 17(b). The NMOS power device is then set by the oscillator at the end of the period and current flows through the inductor once again.

The LM2700 has dedicated protection circuitry running during normal operation to protect the IC. The Thermal Shutdown circuitry turns off the NMOS power device when the die temperature reaches excessive levels. The UVP comparator protects the NMOS power device during supply power startup and shutdown to prevent operation at voltages less than the minimum input voltage. The OVP comparator is used to prevent the output voltage from rising at no loads allowing full PWM operation over all load conditions. The LM2700 also features a shutdown mode decreasing the supply current to 5µA.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings[(1)(2)]

| | | |
|---|---|---|
| $V_{IN}$ | | 12V |
| SW Voltage | | 18V |
| FB Voltage | | 7V |
| $V_C$ Voltage | | $0.965V \le V_C \le 1.565V$ |
| $\overline{SHDN}$ Voltage[(3)] | | 7V |
| FSLCT[(3)] | | 12V |
| Maximum Junction Temperature | | 150°C |
| Power Dissipation[(4)] | | Internally Limited |
| Lead Temperature | | 300°C |
| Vapor Phase (60 sec.) | | 215°C |
| Infrared (15 sec.) | | 220°C |
| ESD Susceptibility[(5)] | Human Body Model | 2kV |
| | Machine Model | 200V |

(1)   Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2)   If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3)   This voltage should never exceed $V_{IN}$.
(4)   The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D (MAX) = (T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(5)   The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

## Operating Conditions

| | |
|---|---|
| Operating Junction Temperature Range[(1)] | −40°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Supply Voltage | 2.2V to 12V |
| SW Voltage | 17.5V |

(1)   All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or ensured through statistical analysis. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
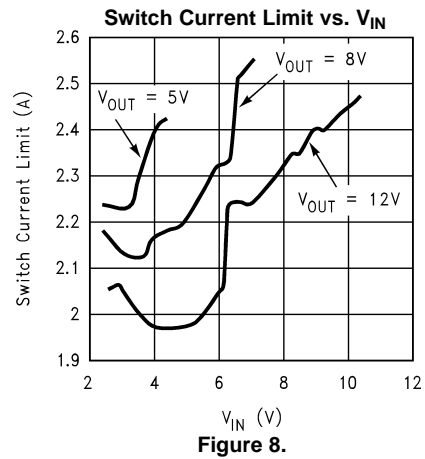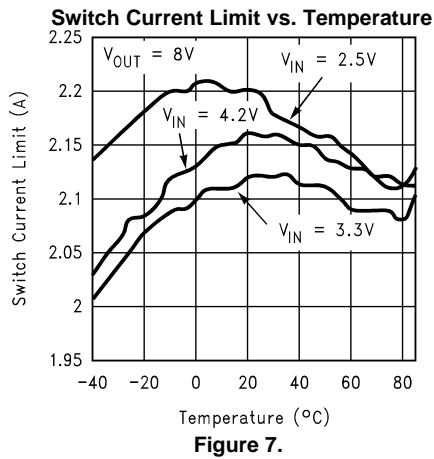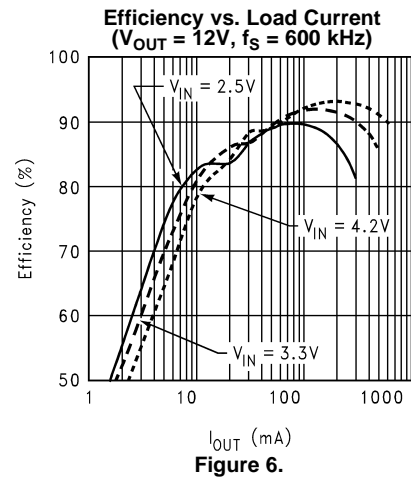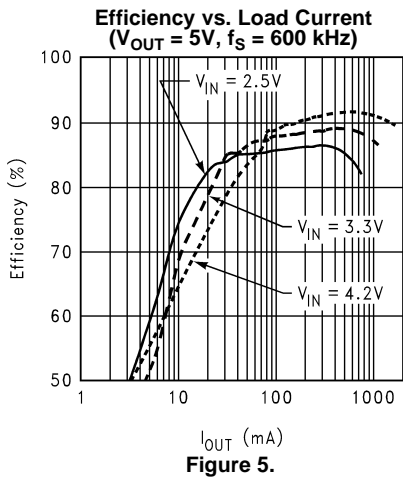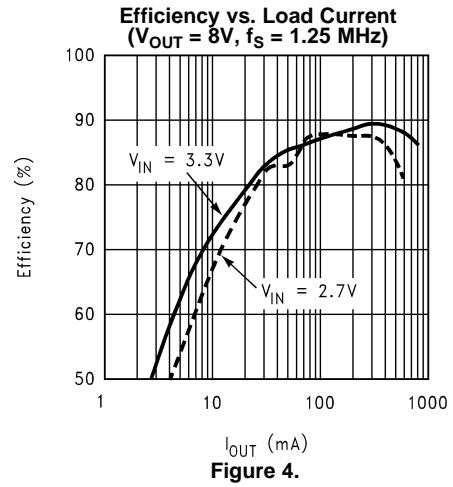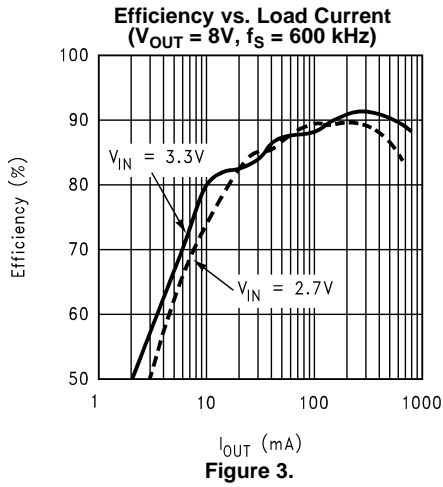
Product Folder Links: *LM2700*

## Electrical Characteristics

Specifications in standard type face are for $T_J$ = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** ($T_J$ = −40°C to +125°C) Unless otherwise specified. $V_{IN}$ =2.2V and $I_L$ = 0A, unless otherwise specified.

| Symbol | Parameter | Conditions | Min (1) | Typ (2) | Max (1) | Units |
|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent Current | FB = 2.2V (Not Switching) FSLCT = 0V | | 1.2 | **2** | mA |
| | | FB = 2.2V (Not Switching) FSLCT = $V_{IN}$ | | 1.3 | **2** | mA |
| | | $V_{\overline{SHDN}}$ = 0V | | 5 | **20** | µA |
| $V_{FB}$ | Feedback Voltage | | **1.2285** | 1.26 | **1.2915** | V |
| $I_{CL}$ (3) | Switch Current Limit | $V_{IN}$ = 2.7V (4) | **2.55** | 3.6 | **4.3** | A |
| %$V_{FB}$/Δ$V_{IN}$ | Feedback Voltage Line Regulation | 2.2V ≤ $V_{IN}$ ≤ 12.0V | | 0.02 | **0.07** | %/V |
| $I_B$ | FB Pin Bias Current (5) | | | 0.5 | **40** | nA |
| $V_{IN}$ | Input Voltage Range | | **2.2** | | **12** | V |
| $g_m$ | Error Amp Transconductance | ΔI = 5µA | **40** | 155 | **290** | µmho |
| $A_V$ | Error Amp Voltage Gain | | | 135 | | V/V |
| $D_{MAX}$ | Maximum Duty Cycle | FSLCT = Ground | **78** | 85 | | % |
| $D_{MIN}$ | Minimum Duty Cycle | FSLCT = Ground | | 15 | | % |
| | | FSLCT = $V_{IN}$ | | 30 | | |
| $f_S$ | Switching Frequency | FSLCT = Ground | **480** | 600 | **720** | kHz |
| | | FSLCT = $V_{IN}$ | **1** | 1.25 | **1.5** | MHz |
| $I_{\overline{SHDN}}$ | Shutdown Pin Current | $V_{\overline{SHDN}}$ = $V_{IN}$ | | 0.008 | **1** | µA |
| | | $V_{\overline{SHDN}}$ = 0V | | −0.5 | **−1** | |
| $I_L$ | Switch Leakage Current | $V_{SW}$ = 18V | | 0.02 | **20** | µA |
| $R_{DSON}$ | Switch $R_{DSON}$ (6) | $V_{IN}$ = 2.7V, $I_{SW}$ = 2A | | 80 | **150** | mΩ |
| $Th_{SHDN}$ | $\overline{SHDN}$ Threshold | Output High | **0.9** | 0.6 | | V |
| | | Output Low | | 0.6 | **0.3** | V |
| UVP | On Threshold | | **1.95** | 2.05 | **2.2** | V |
| | Off Threshold | | **1.85** | 1.95 | **2.1** | V |
| $θ_{JA}$ | Thermal Resistance (7) | TSSOP, package only | | 150 | | °C/W |
| | | WSON, package only | | 45 | | |

(1)  All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or ensured through statistical analysis. All limits at temperature extremes are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2)  Typical numbers are at 25°C and represent the most likely norm.
(3)  Duty cycle affects current limit due to ramp generator.
(4)  Current limit at 0% duty cycle. See Typical Performance Characteristics section for Switch Current Limit vs. $V_{IN}$
(5)  Bias current flows into FB pin.
(6)  Does not include the bond wires. Measured directly at the die.
(7)  Refer to Texas Instrument's packaging website for more detailed thermal information and mounting techniques for the WSON and TSSOP packages.

## Typical Performance Characteristics

**Efficiency vs. Load Current**
**($V_{OUT}$ = 8V, $f_S$ = 600 kHz)**



Figure 3.

**Efficiency vs. Load Current**
**($V_{OUT}$ = 8V, $f_S$ = 1.25 MHz)**



Figure 4.

**Efficiency vs. Load Current**
**($V_{OUT}$ = 5V, $f_S$ = 600 kHz)**



Figure 5.

**Efficiency vs. Load Current**
**($V_{OUT}$ = 12V, $f_S$ = 600 kHz)**



Figure 6.

**Switch Current Limit vs. Temperature**



Figure 7.

**Switch Current Limit vs. $V_{IN}$**



Figure 8.

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# Typical Performance Characteristics (continued)

**R$_{DSON}$ vs. V$_{IN}$ (I$_{SW}$ = 2A)**



Figure 9.

**I$_Q$ vs. V$_{IN}$ (600 kHz, not switching)**



Figure 10.

**I$_Q$ vs. V$_{IN}$ (600 kHz, switching)**



Figure 11.

**I$_Q$ vs. V$_{IN}$ (1.25 MHz, not switching)**



Figure 12.

**I$_Q$ vs. V$_{IN}$ (1.25 MHz, switching)**



Figure 13.

**I$_Q$ vs. V$_{IN}$ (In shutdown)**



Figure 14.

## Typical Performance Characteristics (continued)

**Frequency vs. V$_{IN}$
(600 kHz)**



**Figure 15.**

**Frequency vs. V$_{IN}$
(1.25 MHz)**



**Figure 16.**

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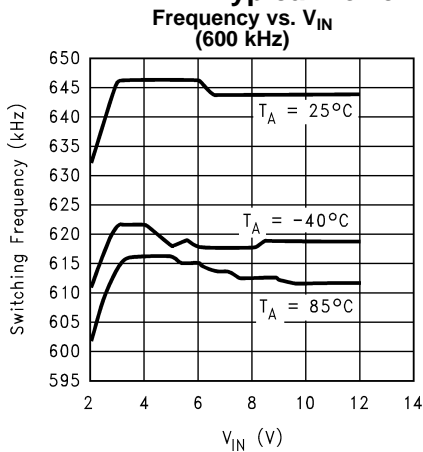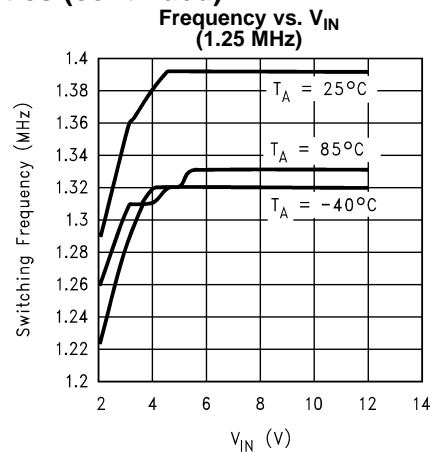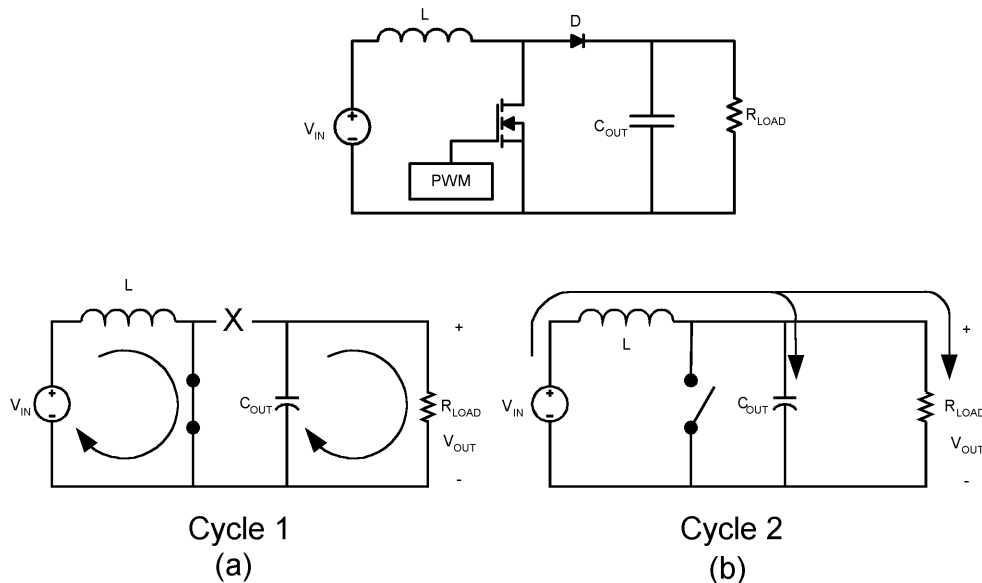**Operation**



**Figure 17. Simplified Boost Converter Diagram**
**(a) First Cycle of Operation (b) Second Cycle Of Operation**

## CONTINUOUS CONDUCTION MODE

The LM2700 is a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in Figure 17(a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by $C_{OUT}$.

The second cycle is shown in Figure 17(b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1\text{-}D} \ , \ D' = (1\text{-}D) = \frac{V_{IN}}{V_{OUT}}$$

(1)

where D is the duty cycle of the switch, D and D′ will be required for design calculations.

## SETTING THE OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in Figure 19. The feedback pin voltage is 1.26V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R_{FB1} = R_{FB2} \ x \ \frac{V_{OUT} \text{-} 1.26}{1.26} \ \Omega$$

(2)

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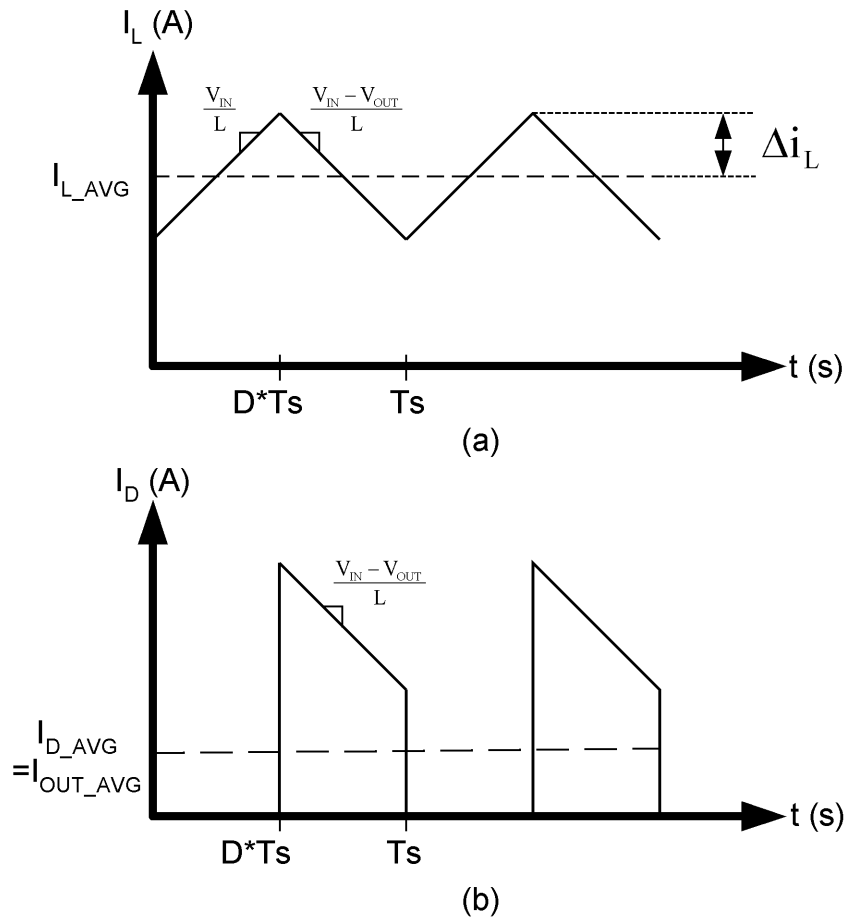
## INTRODUCTION TO COMPENSATION



**Figure 18. (a) Inductor current. (b) Diode current.**

The LM2700 is a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see Figure 18(a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. A 4.7µH inductor is recommended for most 600 kHz applications, while a 2.2µH inductor may be used for most 1.25 MHz applications. If the duty cycle is approaching the maximum of 85%, it may be necessary to increase the inductance by as much as 2X. See *Inductor and Diode Selection* for more detailed inductor sizing.

The LM2700 provides a compensation pin ($V_C$) to customize the voltage loop feedback. It is recommended that a series combination of $R_C$ and $C_C$ be used for the compensation network, as shown in Figure 19. For any given application, there exists a unique combination of $R_C$ and $C_C$ that will optimize the performance of the LM2700 circuit in terms of its transient response. The series combination of $R_C$ and $C_C$ introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz} \tag{3}$$

$$f_{PC} = \frac{1}{2\pi (R_C + R_O) C_C} \text{ Hz} \tag{4}$$

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where $R_O$ is the output impedance of the error amplifier, approximately 850kΩ. For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ $R_C$ ≤ 20kΩ ($R_C$ can be up to 200kΩ if $C_{C2}$ is used, see *High Output Capacitor ESR Compensation*) and 680pF ≤ $C_C$ ≤ 4.7nF. Refer to the Application Information section for recommended values for specific circuits and conditions. Refer to the COMPENSATION section for other design requirement.

## COMPENSATION

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation (loads greater than approximately 100mA), in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

## INDUCTOR AND DIODE SELECTION

Although the inductor sizes mentioned earlier are fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN}R_{DSON}}{0.144 \text{ fs}} \left[ \frac{\left(\frac{D}{D'}\right)^2 - 1}{\left(\frac{D}{D'}\right) + 1} \right] \text{ (in H)}$$

(5)

where fs is the switching frequency, D is the duty cycle, and $R_{DSON}$ is the ON resistance of the internal switch taken from the graph "$R_{DSON}$ vs. $V_{IN}$" in the Typical Performance Characteristics section. This equation is only good for duty cycles greater than 50% (D>0.5), for duty cycles less than 50% the recommended values may be used. The corresponding inductor current ripple as shown in Figure 18(a) is given by:

$$\Delta i_L = \frac{V_{IN}D}{2Lfs} \text{ (in Amps)}$$

(6)

The inductor ripple current is important for a few reasons. One reason is because the peak switch current will be the average inductor current (input current or $I_{LOAD}/D'$) plus $\Delta i_L$. As a side note, discontinuous operation occurs when the inductor current falls to zero during a switching cycle, or $\Delta i_L$ is greater than the average inductor current. Therefore, continuous conduction mode occurs when $\Delta i_L$ is less than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in Figure 18(b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

## DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45°) is desired for the best stability and transient response. For the purpose of stabilizing the LM2700, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin. A discussion of the right half plane zero and checking the crossover using the DC gain will follow.

## INPUT AND OUTPUT CAPACITOR SELECTION

The switching action of a boost regulator causes a triangular voltage waveform at the input. A capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used is dependant on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used for the less stressful condtions while a 33µF or 47µF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series Resistance, denoted $R_{ESR}$) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \cong 2\Delta i_L R_{ESR} \text{ (in Volts)} \tag{7}$$

A minimum value of 10µF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR} + R_L)C_{OUT}} \text{ (in Hz)} \tag{8}$$

$$f_{Z1} = \frac{1}{2\pi R_{ESR}C_{OUT}} \text{ (in Hz)} \tag{9}$$

Where $R_L$ is the minimum load resistance corresponding to the maximum load current. The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the HIGH OUTPUT CAPACITOR ESR COMPENSATION section.

## RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90° in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$RHPzero = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD}L} \text{ (in Hz)} \tag{10}$$

where $I_{LOAD}$ is the maximum load current.

## SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components $R_C$ and $C_C$ is to set a dominant low frequency pole in the control loop. Simply choose values for $R_C$ and $C_C$ within the ranges given in the INTRODUCTION TO COMPENSATION section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ (in Hz)} \tag{11}$$

where $R_O$ is the output impedance of the error amplifier, approximately 850kΩ. Since $R_C$ is generally much less than $R_O$, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero $f_{ZC}$. $f_{ZC}$ is created to cancel out the pole created by the output capacitor, $f_{P1}$. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of $f_{P1}$ over the expected loads and then set the zero $f_{ZC}$ to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)} \tag{12}$$

Now $R_C$ can be chosen with the selected value for $C_C$. Check to make sure that the pole $f_{PC}$ is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range. After checking the design at the end of this section, these values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of $R_C$ should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimal performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

## HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, $C_{C2}$, directly from the compensation pin $V_C$ to ground, in parallel with the series combination of $R_C$ and $C_C$. The pole should be placed at the same frequency as $f_{Z1}$, the ESR zero. The equation for this pole follows:

$$f_{PC2} = \frac{1}{2\pi C_{C2}(R_C // R_O)} \ \text{(in Hz)} \tag{13}$$

To ensure this equation is valid, and that $C_{C2}$ can be used without negatively impacting the effects of $R_C$ and $C_C$, $f_{PC2}$ must be greater than $10f_{ZC}$.

## CHECKING THE DESIGN

The final step is to check the design. This is to ensure a bandwidth of ½ or less of the frequency of the RHP zero. This is done by calculating the open-loop DC gain, $A_{DC}$. After this value is known, you can calculate the crossover visually by placing a −20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding $C_{C2}$ as discussed earlier in the section. The equation for $A_{DC}$ is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)\frac{g_m R_O D'}{R_{DSON}}\{[(\omega cLeff)// R_L]//R_L\}\right\rangle \ \text{(in dB)} \tag{14}$$

$$\omega c \cong \frac{2fs}{nD'} \ \text{(in rad/s)} \tag{15}$$

$$Leff = \frac{L}{(D')^2} \tag{16}$$

$$n = 1+ \frac{2mc}{m1} \ \text{(no unit)} \tag{17}$$

$$mc \cong 0.072fs \ \text{(in V/s)} \tag{18}$$

$$m1 \cong \frac{V_{IN}R_{DSON}}{L} \ \text{(in V/s)} \tag{19}$$

where $R_L$ is the minimum load resistance, $V_{IN}$ is the minimum input voltage, $g_m$ is the error amplifier transconductance found in the *Electrical Characteristics* table, and $R_{DSON}$ is the value chosen from the graph "$R_{DSON}$ vs. $V_{IN}$" in the Typical Performance Characteristics section.

## LAYOUT CONSIDERATIONS

The LM2700 uses two separate ground connections, PGND for the driver and NMOS power device and AGND for the sensitive analog control circuitry. The AGND and PGND pins should be tied directly together at the package. The feedback and compensation networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the AGND pin. If no analog ground plane is available then the ground connections of the feedback and compensation networks must tie directly to the AGND pin. Connecting these networks to the PGND can inject noise into the system and effect performance.

The input bypass capacitor $C_{IN}$, as shown in Figure 19, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with $C_{IN}$, close to the $V_{IN}$ pin, to shunt any high frequency noise to ground. The output capacitor, $C_{OUT}$, should also be placed close to the IC. Any copper trace connections for the $C_{OUT}$ capacitor can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors $R_{FB1}$ and $R_{FB2}$, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. For more detail on switching power supply layout considerations see Application Note AN-1149: *Layout Guidelines for Switching Power Supplies* (literature number SNVA021).

Product Folder Links: *LM2700*
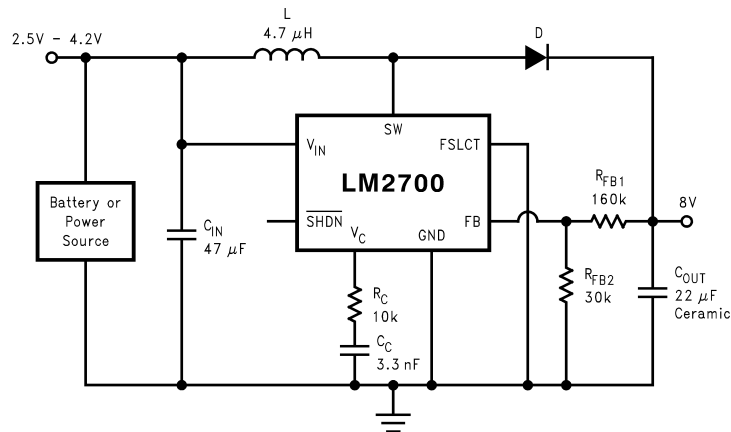
## APPLICATION INFORMATION



**Figure 19.  600 kHz operation, 8V output**
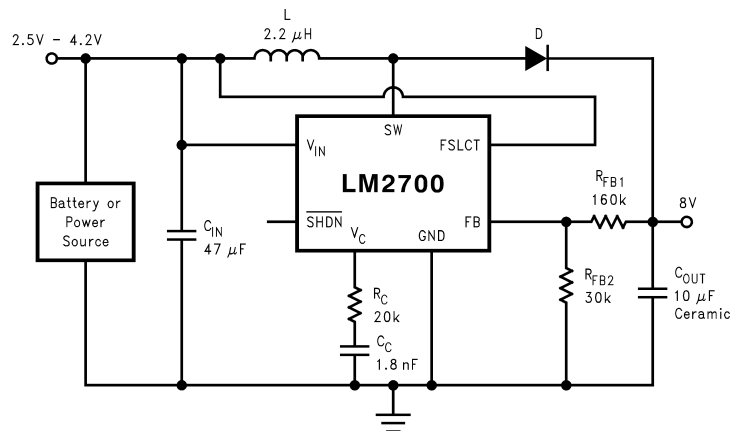


**Figure 20.  1.25 MHz operation, 8V output**
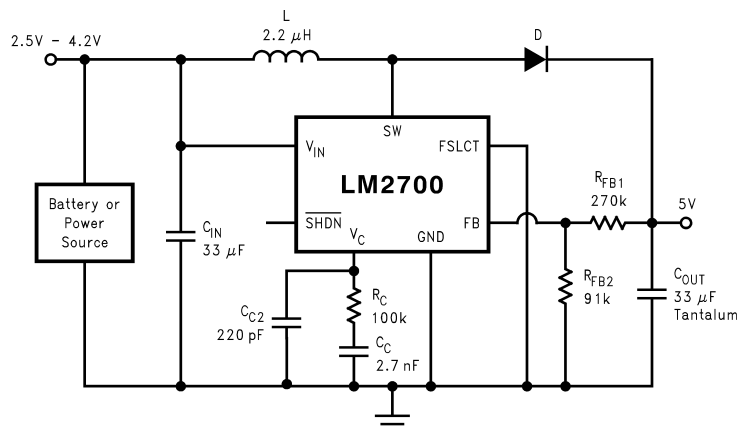


**Figure 21.  600 kHz operation, 5V output**

Product Folder Links: *LM2700*
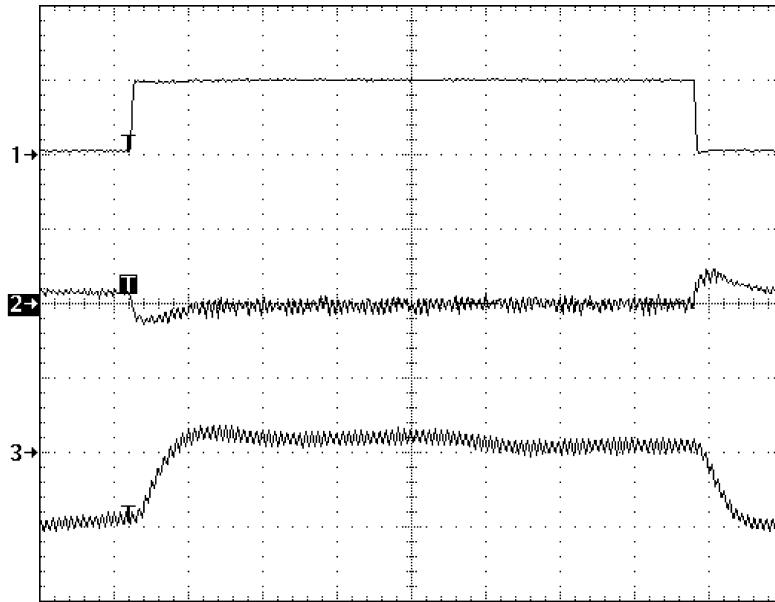
$V_{IN}$ = 3.3V, $I_{OUT}$ = 200mA ⤳ 700mA ⤳ 200mA
CH1: $I_{OUT}$ 0.5A/div DC Coupled
CH2: $V_{OUT}$ 500mV/div AC Coupled
CH3: Inductor Current 1A/div DC Coupled
20µs/div
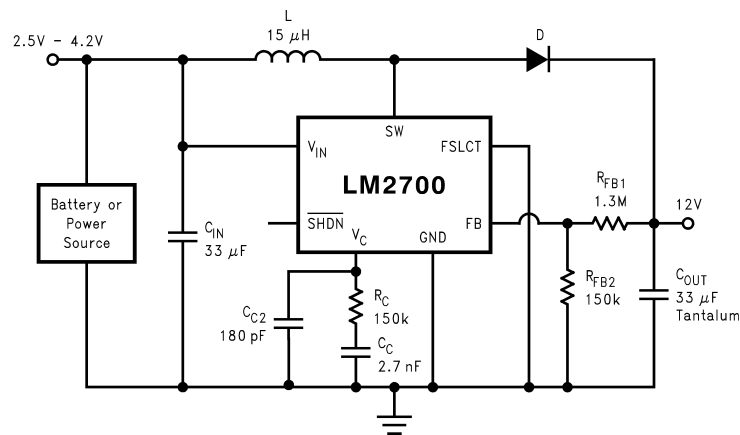
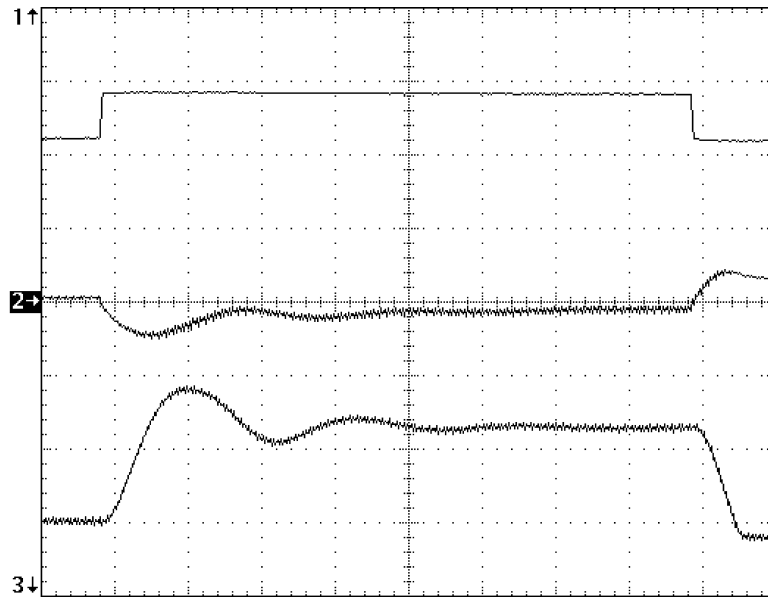**Figure 22. Load Transient for Figure 21**



**Figure 23. 600 kHz operation, 12V output**

Product Folder Links: *LM2700*

$V_{IN}$ = 3.3V, $I_{OUT}$ = 50mA ↝ 350mA ↝ 50mA
CH1: $I_{OUT}$ 0.5A/div DC Coupled
CH2: $V_{OUT}$ 500mV/div AC Coupled
CH3: Inductor Current 1A/div DC Coupled
50µs/div

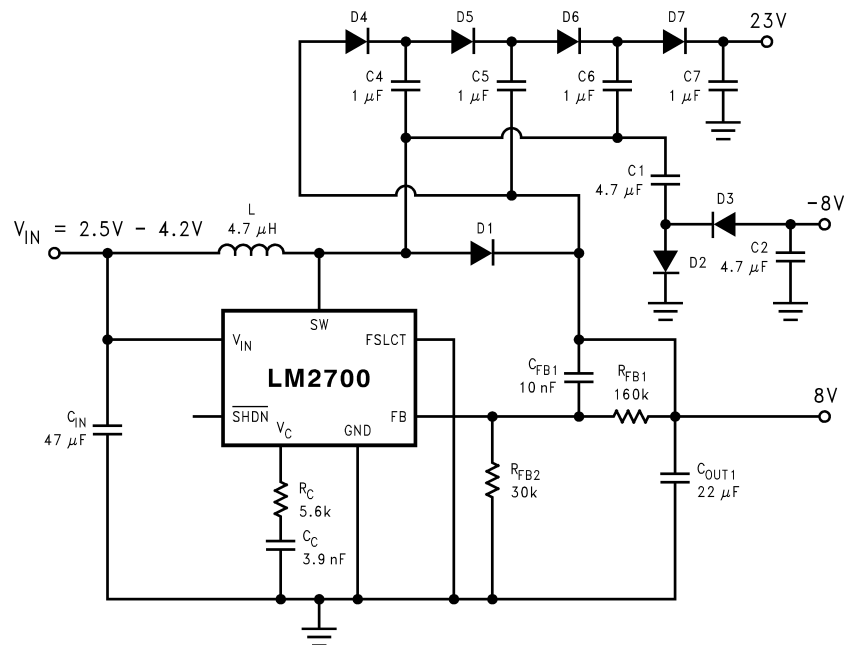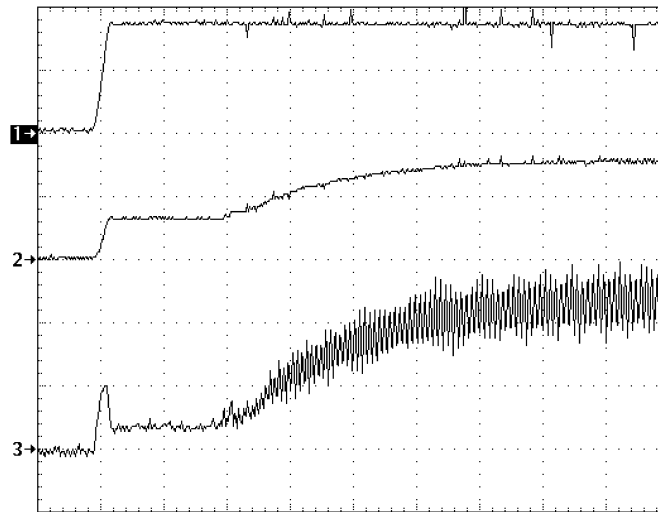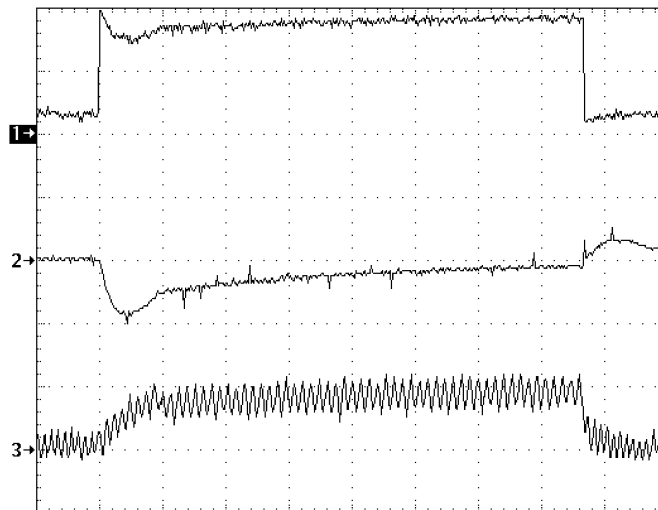**Figure 24.  Load Transient for Figure 23**



**Figure 25.  Triple Output TFT Bias (600 kHz operation)**

$V_{IN}$ = 3.3V, $I_{OUT}$ = 500mA
CH1: $V_{IN}$ 2V/div DC Coupled
CH2: $V_{OUT}$ 5V/div DC Coupled
CH3: Inductor Current 500mA/div DC Coupled
1ms/div

**Figure 26. Start Up Waveform for Figure 25**



$V_{IN}$ = 3.3V, $I_{OUT}$ = 50mA ⤳ 375mA ⤳ 50mA
CH1: $I_{OUT}$ 0.2A/div DC Coupled
CH2: $V_{OUT}$ 2V/div AC Coupled
CH3: Inductor Current 1A/div DC Coupled
500µs/div

**Figure 27. Load Transient for Figure 25, 8V Output**

Product Folder Links: *LM2700*

# REVISION HISTORY

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM2700LD-ADJ/NOPB | ACTIVE | WSON | NHE | 14 | 1000 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 125 | S00001B | Samples |
| LM2700MT-ADJ | LIFEBUY | TSSOP | PW | 14 | 94 | Non-RoHS & Green | Call TI | Level-1-260C-UNLIM | -40 to 125 | 2700MT -ADJ | |
| LM2700MT-ADJ/NOPB | ACTIVE | TSSOP | PW | 14 | 94 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | 2700MT -ADJ | Samples |
| LM2700MTX-ADJ/NOPB | ACTIVE | TSSOP | PW | 14 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | 2700MT -ADJ | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM2700LD-ADJ/NOPB | WSON | NHE | 14 | 1000 | 178.0 | 12.4 | 4.3 | 4.3 | 1.3 | 8.0 | 12.0 | Q1 |
| LM2700MTX-ADJ/NOPB | TSSOP | PW | 14 | 2500 | 330.0 | 12.4 | 6.95 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM2700LD-ADJ/NOPB | WSON | NHE | 14 | 1000 | 208.0 | 191.0 | 35.0 |
| LM2700MTX-ADJ/NOPB | TSSOP | PW | 14 | 2500 | 367.0 | 367.0 | 35.0 |

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

## TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| LM2700MT-ADJ | PW | TSSOP | 14 | 94 | 495 | 8 | 2514.6 | 4.06 |
| LM2700MT-ADJ | PW | TSSOP | 14 | 94 | 495 | 8 | 2514.6 | 4.06 |
| LM2700MT-ADJ/NOPB | PW | TSSOP | 14 | 94 | 495 | 8 | 2514.6 | 4.06 |

PW (R−PDSO−G14)                                    PLASTIC SMALL OUTLINE

0,65    ◄─►   ◄─►  $\frac{0,30}{0,19}$     ⊕  0,10  Ⓜ

14                    8

△D   $\frac{4,50}{4,30}$    $\frac{6,60}{6,20}$

0,15 NOM

Gage Plane

1                    7

$\frac{5,10}{4,90}$                0°−8°            0,25

△C                                              $\frac{0,75}{0,50}$

1,20 MAX        $\frac{0,15}{0,05}$        Seating Plane

▱ 0,10

4040064−3/G  02/11

NOTES:   A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
      △C  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
      △D  Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.  Falls within JEDEC MO−153

# NHE0014A



(3)

(2.8)

(2.2)

(14X 0.5)

(14X 0.25)

(12X 0.5)

**RECOMMENDED LAND PATTERN**
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS

PIN 1 INDEX AREA

4±0.1

4±0.1

B

A

C

0.8 MAX

(0.2)

PIN 1 ID

3±0.1

12X 0.5

2.2±0.1

14X 0.5±0.1

14X 0.25±0.05

⊕ 0.1Ⓜ C AⓈ BⓈ

2X 3
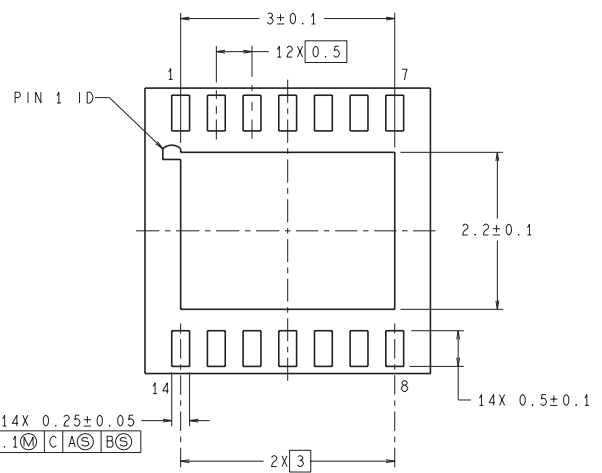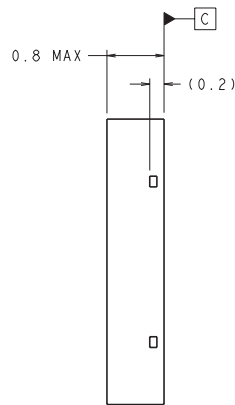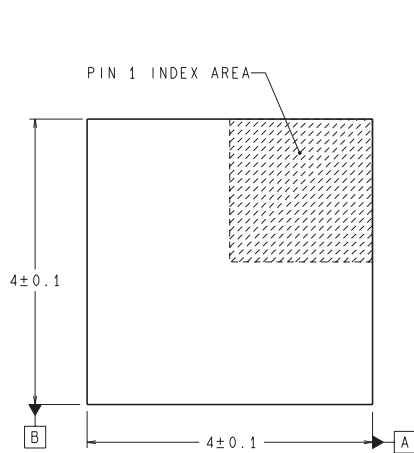
LDA14A (REV A)

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