LM317L 100mA Adjustable Floating Voltage Regulator

1 Features

- Output voltage range (V_O):
  - Adjustable 1.25V to 37V (for new chip)
  - Adjustable 1.25V to 32V (for legacy chip)
- Output current: Up to 100mA
- Accuracy:
  - Input regulation typically 0.01% per input voltage change
  - Output regulation typically 0.5%
- Ripple rejection typically:
  - 80 dB at 120Hz
  - 65 dB at 100kHz
- For higher output current requirements, see LM317M (500mA) and LM317 (1.5A)

2 Applications

- Electronic points of sale
- Medical, health, and fitness applications
- Printers
- Appliances and white goods
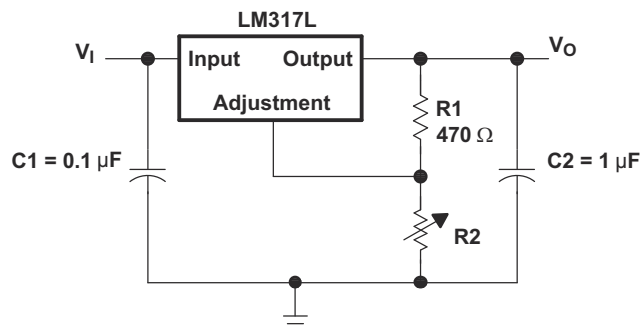- TV

3 Description

The LM317L is an adjustable, 3-terminal, positive-voltage regulator capable of supplying up to 100 mA over an output-voltage range of 1.25V to 37V. The device is exceptionally easy to use and requires only two external resistors to set the output voltage.

For the legacy chip, the LM317LC series is characterized for the junction temperature range of 0°C to +125°C and the LM317LI device is characterized for the operating junction temperature range of –40°C to +125°C. For the new chip, the both LM317LC and LM317LI series are characterized for the junction temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
LM317L	D (SOIC, 8)	4.9mm × 6mm
	LP (TO-92, 3)	4.8mm × 3.68mm
	PK (SOT-89, 3)	4.5mm × 4.095mm
	PW (TSSOP, 8)	3mm × 6.4mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
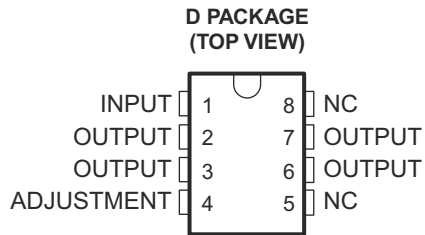(2) The package size (length × width) is a nominal value and includes pins, where applicable.
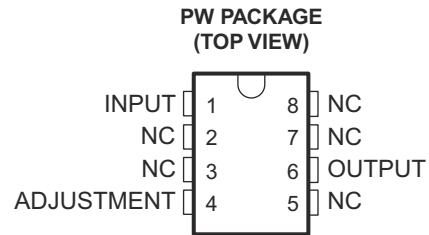

Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

D PACKAGE
(TOP VIEW)

INPUT	1	8	NC
OUTPUT	2	7	OUTPUT
OUTPUT	3	6	OUTPUT
ADJUSTMENT	4	5	NC

NC – No internal connection
OUTPUT terminals are all internally connected.

PW PACKAGE
(TOP VIEW)

INPUT	1	8	NC
NC	2	7	NC
NC	3	6	OUTPUT
ADJUSTMENT	4	5	NC

NC – No internal connection

PK PACKAGE
(TOP VIEW)

3 INPUT
2 OUTPUT
1 ADUSTMENT

LP PACKAGE
(TOP VIEW)

1 INPUT
2 OUTPUT
3 ADUSTMENT
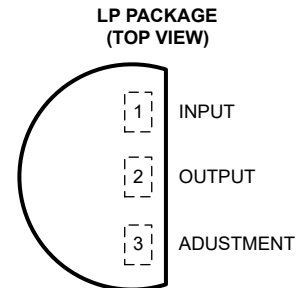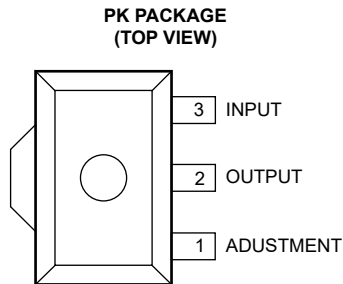
Table 4-1. Pin Functions

NAME	D	PW	LP	PK	TYPE[1]	DESCRIPTION
ADJUSTMENT	4	4	3	1	I	Output feedback voltage
INPUT	1	1	1	3	I	Input supply voltage
NC	5, 8	2, 3, 5, 7, 8	—	—	—	No connect. Recommended to ground pins for improved thermal performance but not required.
OUTPUT	2, 3, 6, 7	6	2	2	O	Regulated output voltage

(1)   I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage	Legacy chip		35	V
		New chip		40	
T_J	Operating virtual-junction temperature			150	°C
T_{stg}	Storage temperature	Legacy chip	−65	150	°C
		New chip	−55	150	

(1)   Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	Legacy chip	±3000	V
			New chip	±2000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]		±2000	

(1)   JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V_O	Output voltage		Legacy chip	1.25	32	V
			New chip	1.25	37	
$V_I - V_O$	Input-to-output voltage differential		Legacy chip	2.5	32	V
			New chip	2.5	37	
I_O	Output current			2.5	100	mA
T_J	Operating virtual-junction temperature	LM317LC	Legacy chip	0	125	°C
			New chip	−40	125	
		LM317LI	Legacy and new chip	−40	125	

5.4 Thermal Information

THERMAL METRIC[1]		LM317L							UNIT
		D 8 PINS		LP 3 PINS		PK 3 PINS		PW 8 PINS	
		Legacy Chip[2]	New Chip	Legacy Chip[2]	New Chip	Legacy Chip[2]	New Chip	Legacy Chip[2]	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.1	96.5	139.5	156.7	51.5	44	149.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		48.6		80.6		86.9		
$R_{\theta JB}$	Junction-to-board thermal resistance		34.8				8.5		
Ψ_{JT}	Junction-to-top characterization parameter		5.9		24.7		4.5		
Ψ_{JB}	Junction-to-board characterization parameter		34.2		135.8		8.5		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance						6.9		

(1)   For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2)   Legacy chip only $R_{\theta JA}$ values reported.

5.5 Electrical Characteristics

Unless otherwise noted, specifications over recommended operating virtual-junction temperature range, $V_I - V_O$ = 5V and I_O = 40mA, P ≤ rated dissipation, measured with a 0.1μF capacitor across the input and a 1μF capacitor across the output.

PARAMETER	TEST CONDITIONS[1]			MIN	TYP	MAX	UNIT
Line regulation	$V_I - V_O$ = 5V to 35V	T_J = 25°C	Legacy and new chip		0.01	0.02	%/V
		I_O = 2.5mA to 100mA	Legacy and new chip		0.02	0.05	
Ripple rejection	V_O = 10V, f = 120Hz		Legacy and new chip		65		dB
	V_O = 10V, 10μF capacitor between ADJUSTMENT and ground		Legacy and new chip	66	80		
Output voltage regulation	$V_I - V_O$ = 5V to 35V, T_J = 25°C, I_O = 2.5mA to 100mA	V_O ≤ 5V	Legacy and new chip		25		mV
		V_O ≥ 5V	Legacy and new chip		5		mV/V
	$V_I - V_O$ = 5V to 35V, I_O = 2.5mA to 100mA	V_O ≤ 5V	Legacy and new chip		50		mV
		V_O ≥ 5V	Legacy and new chip		10		mV/V
Output voltage change with temperature	T_J = 0°C to 125°C		Legacy and new chip		10		mV/V
Output voltage long-term drift	After 1000 hours at T_J = 125°C and $V_I - V_O$ = 35V		Legacy and new chip		3	10	mV/V
Output noise voltage	f = 10Hz to 10kHz, T_J = 25°C		Legacy and new chip		30		μV/V
Minimum output current to maintain regulation	$V_I - V_O$ = 35V		Legacy chip		1.5	2.5	mA
			New chip		3.5	5	
Peak output current	3V ≤ $V_I - V_O$ ≤ 13V		Legacy and new chip	100	200		mA
	$V_I - V_O$ = 35V		Legacy chip	100	200		
			New chip	25	50	150	
ADJUSTMENT current			Legacy and new chip		50	100	μA
Change in ADJUSTMENT current	$V_I - V_O$ = 5V, I_O = 40 mA		Legacy and new chip		0.2	5	μA
Reference voltage (output to ADJUSTMENT)	$V_I - V_O$ = 5V, I_O = 40 mA			1.2	1.25	1.3	V

(1) For all tests unless otherwise noted, power dissipation ≤ 1.4W in PK, D, and PW packages and ≤ 0.625W for LP package. Pulse-testing techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

5.6 Typical Characteristics

Unless otherwise noted, specifications over recommended operating virtual-junction temperature range, $V_I - V_O = 5V$ and $I_O = 40mA$, $P \leq$ rated dissipation.
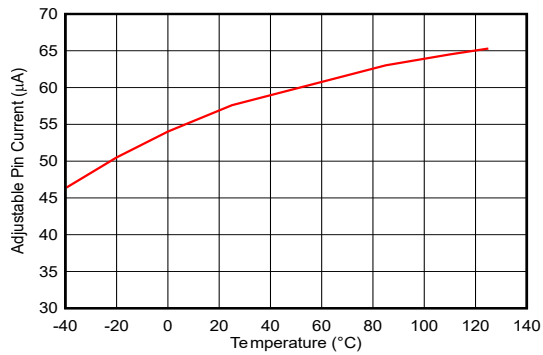

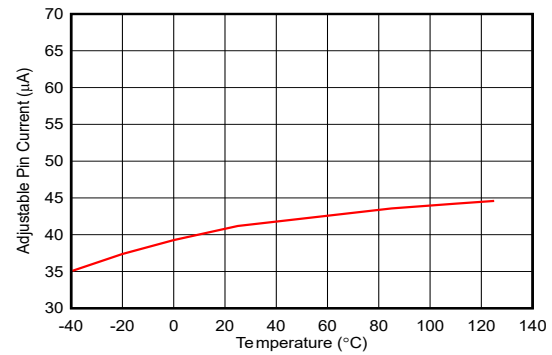**Figure 5-1. Change in Adjustment Current Over Temperature (Legacy Chip)**

Figure 5-2. Change in Adjustment Current Over Temperature (New Chip)

Product Folder Links: *LM317L*

6 Detailed Description

6.1 Overview

The LM317L is a 100mA linear regulator with high voltage tolerance up to 37V. The device has a feedback voltage that is relative to the output instead of ground. This ungrounded design allows the LM317L device to have superior line and load regulation. This design also allows the LM317L device to be used as a current source or current sink using a single resistor. Any output voltage from 1.25V to 32V can be obtained by using two resistors. The bias current of the device, up to 2.5mA, flows to the output; this current must be used by the load or the feedback resistors. The power dissipation is the product of pass transistor voltage and current, which is calculated as shown in Equation 1.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{1}$$

The application heat sink must be able to absorb the power calculated in Equation 1.

In addition to higher performance than fixed regulators, this regulator offers full overload protection, available only in integrated circuits. Included on the chip are current-limiting and thermal-overload protection. All overload-protection circuitry remains fully functional even when ADJUSTMENT is disconnected. Normally, no capacitors are needed unless the device is situated far from the input filter capacitors, in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. ADJUSTMENT can be bypassed to achieve very high ripple rejection, which is difficult to achieve with standard three-terminal regulators.

In addition to replacing fixed regulators, the LM317L regulator is useful in a wide variety of other applications. Because the regulator is floating and observes only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded. The primary application is that of a programmable output regulator, but by connecting a fixed resistor between ADJUSTMENT and OUTPUT, this device can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping ADJUSTMENT to ground, programming the output to 1.25V, where most loads draw little current.

The LM317LC is characterized for operation over the virtual junction temperature range of 0°C to 125°C. The LM317LI is characterized for operation over the virtual junction temperature range of –40°C to 125°C.

6.2 Functional Block Diagram

Product Folder Links: *LM317L*
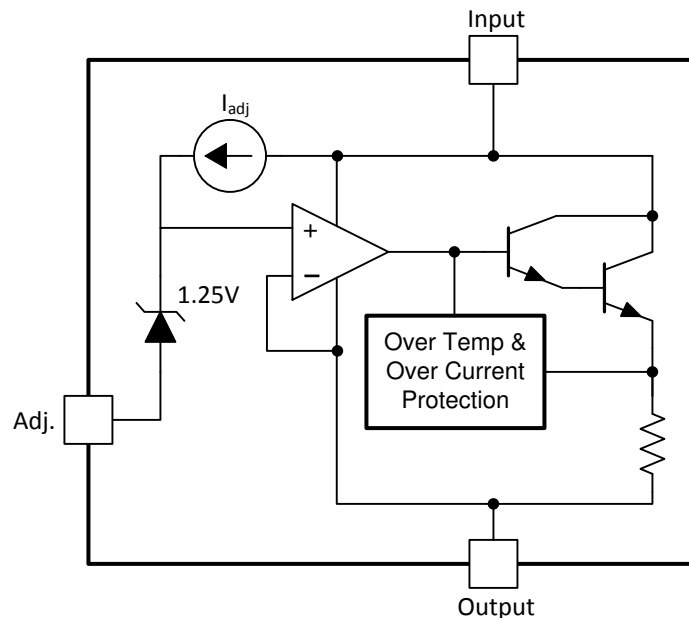
6.3 Feature Description

6.3.1 NPN Darlington Output Drive

The NPN Darlington output topology provides naturally low output impedance and an output capacitor is optional. To support maximum current and lowest temperature, a 2.5V headroom is recommended ($V_I – V_O$).

6.3.2 Overload Block

Overcurrent and overtemperature shutdown protects the device against overload or damage from operating in excessive heat.

6.3.3 Programmable Feedback

An op amp with a 1.25V offset input at the ADJUST pin provides easy output voltage or current (not both) programming. For current regulation applications, use a single resistor whose resistance value is 1.25V / I_{OUT} and power rating is greater than $(1.25V)^2$ / R. For voltage regulation applications, two resistors set the output voltage. See the *Typical Application* section for a schematic and the resistor formula.

6.4 Device Functional Modes

6.4.1 Normal operation

The device OUTPUT pin sources current necessary to make the OUTPUT pin 1.25V greater than the ADJUST terminal to provide output regulation.

6.4.2 Operation With Low Input Voltage

The device requires up to a 2.5V headroom ($V_I – V_O$) to operate in regulation. With less headroom, the device can drop out and the OUTPUT voltage is the INPUT voltage minus the dropout voltage.

6.4.3 Operation at Light Loads

The device passes the bias current to the OUTPUT pin. The load or feedback must consume this minimum current for regulation or the output can be too high.

6.4.4 Operation In Self Protection

When an overload occurs, the device shuts down the Darlington NPN output stage or reduces the output current to prevent device damage. The device automatically restarts when the over current is removed. The output can be reduced or cycle thermal shutdown on and off until the overload is removed.

Product Folder Links: *LM317L*

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The two output resistors are the only components required to adjust V_{OUT}.

7.2 Typical Application
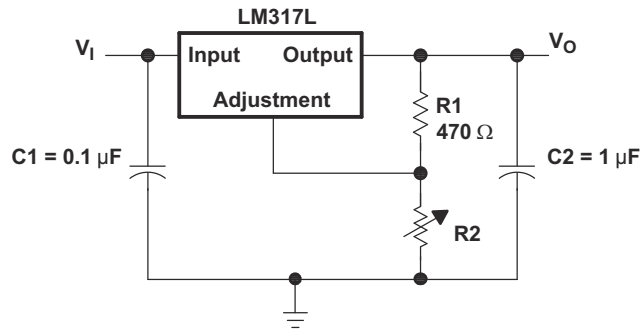
Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

1. Use an input bypass capacitor if the regulator is far from the filter capacitors.
2. For this design example, use the parameters listed in Table 7-1.
3. Using an output capacitor improves transient response, but is optional.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	(Output voltage + 2.5V) to 32V
Output voltage	$V_{REF} \times (1 + R_2 / R_1) + I_{ADJ} \times R_2$

7.2.2 Detailed Design Procedure

7.2.2.1 Input Capacitor

An input capacitor is not required, but is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1µF ceramic or 1µF tantalum provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.

7.2.2.2 Output Capacitor

An output capacitor improves transient response, but is not needed for stability.

7.2.2.3 Feedback Resistors

The feedback resistor sets the output voltage using Equation 2.

$$V_{REF} \times (1 + R_2 / R_1) + I_{ADJ} \times R_2 \tag{2}$$

Product Folder Links: *LM317L*

7.2.2.4 Adjustment Terminal Capacitor

The optional adjustment pin capacitor improves ripple rejection by preventing the amplification of the ripple. When this capacitor is used and V_{OUT} > 6V, a protection diode from adjust to output is recommended.

7.2.2.5 Design Options and Parameters

Common linear regulator designs are concerned with the following parameters:
- Input voltage range
- Input capacitor range
- Output voltage
- Output current rating
- Output capacitor range
- Input short protection
- Stability
- Ripple rejection

7.2.2.6 Output Voltage

V_O is calculated as shown in Equation 3.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right) + (I_{ADJ} \times R_2)$$

(3)

Because I_{ADJ} typically is 50µA, this parameter is negligible in most applications.

7.2.2.7 Ripple Rejection

C_{ADJ} is used to improve ripple rejection. This capacitor prevents amplification of the ripple when the output voltage is adjusted higher. If C_{ADJ} is used, include protection diodes to prevent ADJ from reverse-biasing when VOUT collapses quickly.

7.2.2.8 Input Short Protection

If the input is shorted to ground during a fault condition, protection diodes provide measures to prevent the possibility of external capacitors discharging through low-impedance paths in the device. By providing low-impedance discharge paths for C_3 and C_2, respectively, a protection diode across the input to the output and a protection diode across ADJ to the output prevent the capacitors from discharging into the output of the regulator.

7.2.3 Application Curve
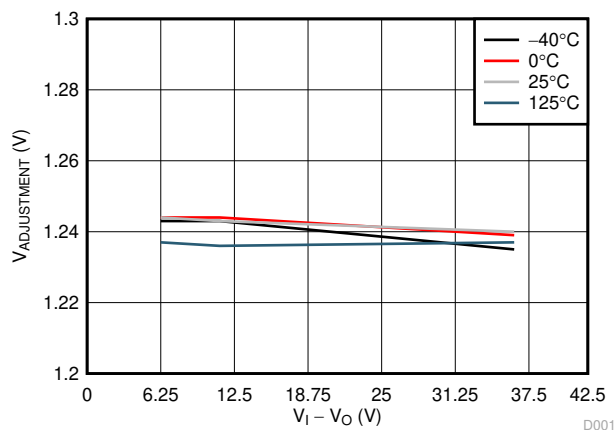
Figure 7-2. Adjustment Voltage Relative to Output Over Temperature (Legacy Chip)

7.3 System Examples

7.3.1 Regulator Circuit With Improved Ripple Rejection

C2 helps stabilize the voltage at the adjustment pin, which helps reject noise. Diode D1 exists to discharge C2 in case the output is shorted to ground.
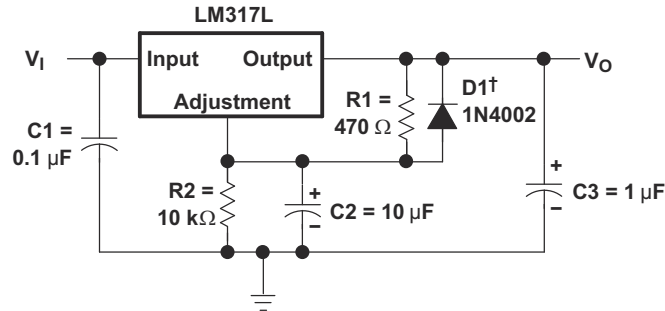
Figure 7-3. Regulator Circuit With Improved Ripple Rejection

7.3.2 0V to 30V Regulator Circuit

In the 0V to 30V regulator circuit application, the output voltage is determined by Equation 4.
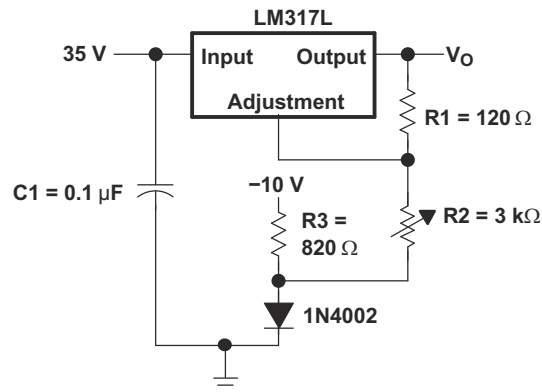
$$V_{OUT} = V_{REF}\left(1 + \frac{R_2 + R_3}{R_1}\right) - 10\,V$$

(4)

Figure 7-4. 0V to 30V Regulator Circuit

7.3.3 Precision Current-Limiter Circuit

This application limits the output current to the I_{LIMIT} shown in Figure 7-5.
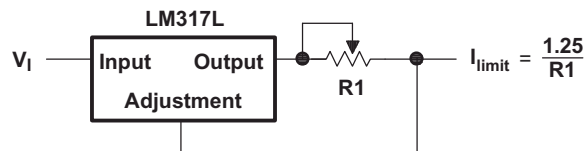
Figure 7-5. Precision Current-Limiter Circuit

7.3.4 Tracking Preregulator Circuit

The tracking preregulator circuit application keeps a constant voltage across the second LM317L in the circuit.
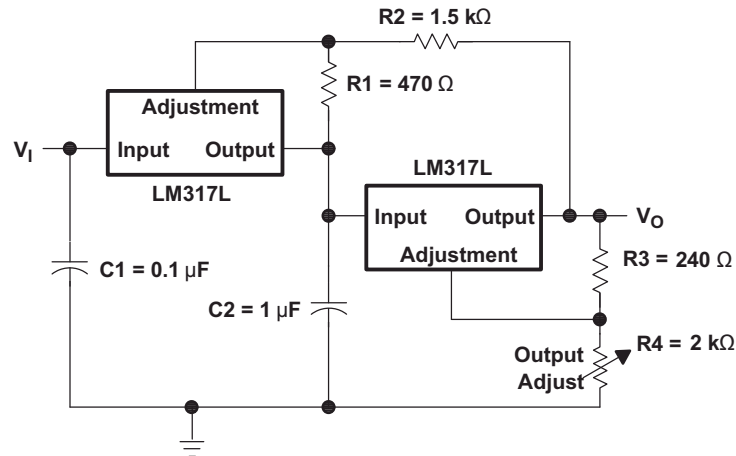
Figure 7-6. Tracking Preregulator Circuit

7.3.5 Slow-Turn On 15V Regulator Circuit

The capacitor C1, in combination with the PNP transistor, helps the circuit to slowly start supplying voltage. In the beginning, the capacitor is not charged. Therefore, output voltage starts at 1.9V, as determined by Equation 5. As the capacitor voltage rises, V_{OUT} rises at the same rate. When the output voltage reaches the value determined by R1 and R2, the PNP is turned off.

$$V_{C1} + V_{BE} + 1.25V = 0V + 0.65V + 1.25V = 1.9V \qquad (5)$$
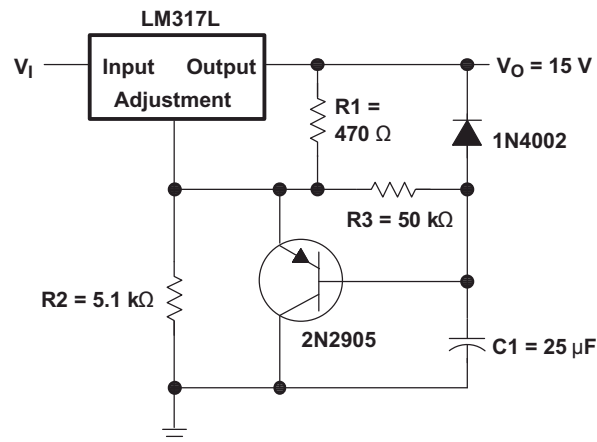
Figure 7-7. Slow-Turn On of the 15V Regulator Circuit

Product Folder Links: *LM317L*

7.3.6 50mA Constant-Current, Battery-Charger Circuit

The current-limit operation mode can be used to trickle charge a battery at a fixed current as determined by Equation 6. V_I must be greater than V_{BAT} + 3.75V.

$$I_{CHG} = 1.25V \div 24\Omega \tag{6}$$

$$(1.25V\ [V_{REF}] + 2.5V\ [\text{headroom}]) \tag{7}$$
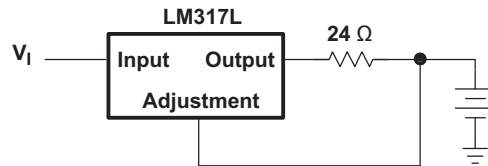
Figure 7-8. 50mA Constant-Current, Battery-Charger Circuit

7.3.7 Current-Limited 6V Charger

As the charge current increases, the voltage at the bottom resistor increases until the NPN starts sinking current from the adjustment pin. The voltage at the adjustment pin drops, and consequently the output voltage decreases until the NPN stops conducting.
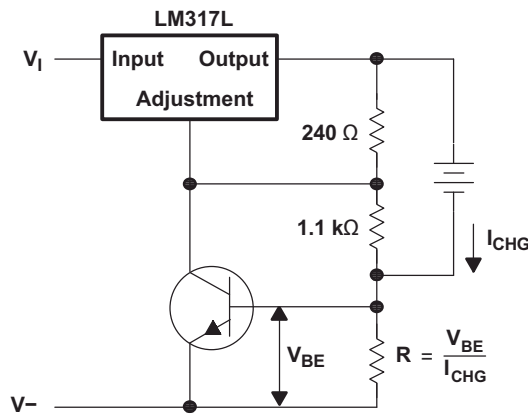
Figure 7-9. Current-Limited 6V Charger

Product Folder Links: *LM317L*

7.3.8 High-Current Adjustable Regulator

This application allows higher currents at V_{OUT} than the LM317L can provide, while still keeping the output voltage at levels determined by the adjustment-pin resistor divider of the LM317L.
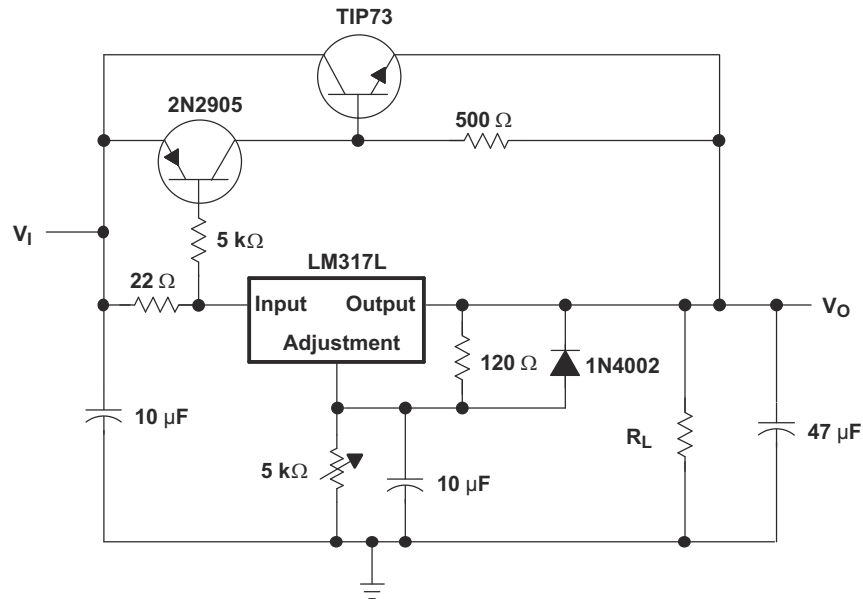
Figure 7-10. High-Current Adjustable Regulator

7.4 Power Supply Recommendations

The LM317L is designed to operate from an input voltage supply range between 2.5V to 32V greater than the output voltage. If the device is more than six inches from the input filter capacitors, an input bypass capacitor, 0.1µF or greater, of any type is needed for stability.

7.5 Layout

7.5.1 Layout Guidelines

- Bypass the input pin to ground with a bypass capacitor.
- The optimum placement is closest to the V_{IN} of the device and the GND of the system. Care must be taken to minimize the loop area formed by the bypass capacitor connection, the INPUT pin, and the GND pin of the system.
- For operation at a full-rated load, use wide trace lengths to eliminate IR drop and heat dissipation.

7.5.2 Layout Example
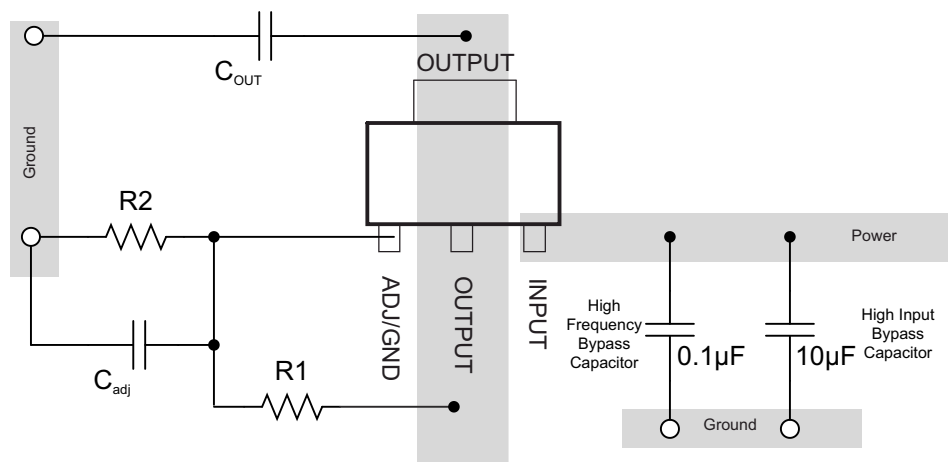
Figure 7-11. Layout Diagram

7.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Section 5.4* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D \tag{8}$$

$$T_J = T_T + \psi_{JT} \times P_D \tag{9}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D \tag{10}$$

where:

- T_B is the PCB surface temperature measured 1mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

Device Nomenclature

PRODUCT[1]	V_{OUT}
LM317L**xyyyz**	**x** is the operating temperature range designator. **yyy** is the package designator. **z** is the package quantity designator. Devices ship with either the legacy chip (CSO: SHE) or the new chip (CSO: TID). The reel packaging label provides CSO information to distinguish which chip is used. Device performance for new and legacy chips is denoted throughout the data sheet.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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8.5 Electrostatic Discharge Caution

![ESD Warning Symbol] This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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