LM3248 2.7 MHz, 2.5A Adjustable Boost-Buck DC/DC Converter with Boost and Active Current Assist and Analog Bypass (ACB)

Check for Samples: LM3248

FEATURES

- **Output Voltage V_{OUT} Adjustable from 0.4V to 4.0V (typ.)**
- **Input Voltage Range V_{IN} from 2.7V to 5.5V**
- **Boost-Buck and Buck (Boost-Bypass) Operating Modes with Seamless Transition**
- **2.5A Load Current Capability**
- **High Conversion Efficiency (> 90% typ.)**
- **High-Efficiency PFM/PWM Modes with Seamless Transition**
- **Very Fast Transient Response: 10 µs**
- **ACB Reduces Inductor Size Requirements**
- **Dither to aid RX Band Noise Compliance**

APPLICATIONS

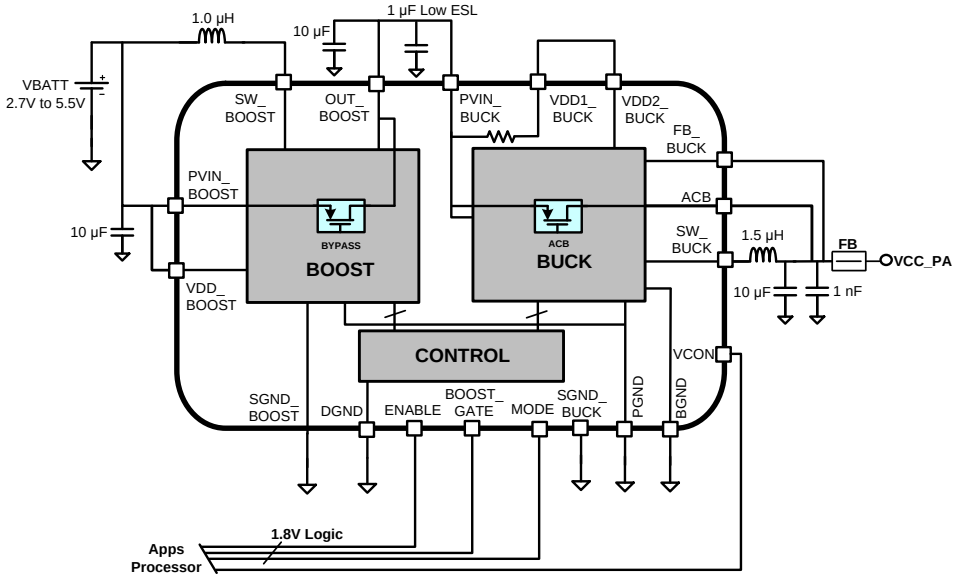
- **Multi-mode 2G/3G/4G and 3GPP/LTE Smart-phones and Tablets**
- **Hand-Held Radios**
- **RF Mobile Devices**

DESCRIPTION

The LM3248 is a PWM/PFM Boost-Buck DC/DC converter that provides efficient utilization of battery power over a wide voltage range. The device architecture is suitable for advanced RF front-end systems that demand dynamic voltage and current to support converged power amplifier architectures operating in 2G/3G/4G and 3GPP/LTE modes. For example, the LM3248 is designed to produce higher output voltages while maintaining PFM mode as required by some new reduced-power CMOS PAs. The extremely fast Boost-Buck function reduces RF PA overhead power dissipation, extending battery talk time. The device will operate at input voltage V_{IN} range of 2.7V to 5.5V and an adjustable output voltage V_{OUT} range of 0.4V to 4.0V at a maximum current load of 2.5A.

The LM3248 is available in a 30-bump, lead-free thin DSBGA package.

Typical Application Diagram



DESCRIPTION (CONTINUED)

The LM3248 utilizes step-up (Boost) and variable output step-down (Buck) DC/DC converters. Combining a cascaded Boost and Buck converter in a single package is ideal for powering the latest multimode/multi-standard RF power amplifiers. The Boost converter provides the RF power subsystem the capability to operate at lower battery voltages as well as to maintain increased PA linearity and transmit power margins over a wider battery voltage supply range.

The Buck has a unique **A**ctive **C**urrent assist and analog **B**ypass (ACB) feature to minimize inductor size without any loss of output regulation for the entire battery voltage and RF output power range, until dropout. ACB provides a parallel current path, when needed, to limit the maximum inductor current while still driving a 2.5A load. The LM3248 may also be configured as a Buck-only converter with a boost bypass feature to enable highest efficiency operation with minimal dropout voltage when the Boost is not needed.

The LM3248 automatically and seamlessly transitions between Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM) modes for high-efficiency operation with both full and light load conditions.

Connection Diagram

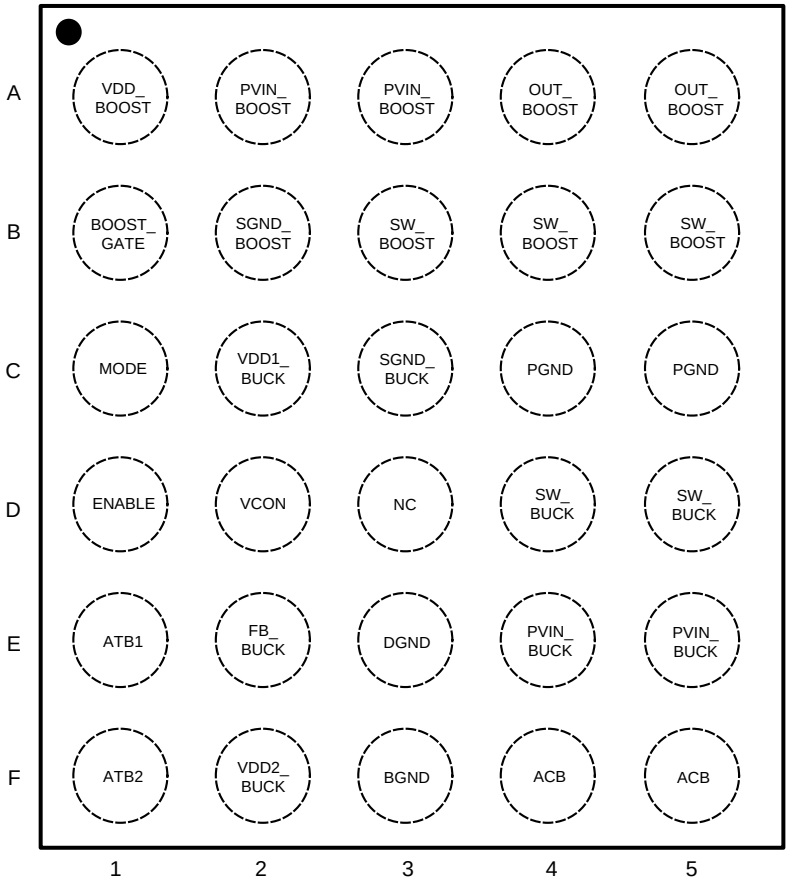


Figure 1. 30-Bump Thin DSBGA Package (0.4 mm pitch)
(Top View, bumps down)

Pin Descriptions

Pin #	Name	I/O	Description
A1	VDD_BOOST	-	Power supply voltage input for Boost Analog blocks. Connected to V_{BATT} supply.
A2	PVIN_BOOST	-	Power supply voltage input for Boost Bypass FET.
A3			
A4	OUT_BOOST	O	Boost converter output. When Boost and Buck are active, OUT_BOOST must be externally connected to PVIN_BUCK. A 10 µF capacitor must be placed between this node and GND. Internally connected to BUCK voltage input and feedback to inverting input of Boost error amplifier.
A5			
B1	BOOST_GATE	I	Digital input. A Low-to-High transition wakes up the boost converter and positions it to a high level in preparation for a possible VCON change.
B2	SGND_BOOST	-	Analog Ground for the Boost Analog blocks.
B3	SW_BOOST	I/O	Boost converter switch node. When Boost and Buck are active, SW_BOOST is typically connected to V_{BATT} supply through external power inductor.
B4			
B5			
C1	MODE	I	Digital input. Low = 3G/4G (PWM/PFM) operation; High = 2G (PWM only) operation.
C2	VDD1_BUCK		Power supply voltage input for Buck Analog PWM blocks. Internally connected to PVIN_BUCK when used with Boost. If Buck-only mode is used then must be directly connected to V_{BATT} supply.
C3	SGND_BUCK	-	Analog Ground for the Buck Analog Blocks.
C4	PGND	-	Power Ground for output FETs.
C5			
D1	ENABLE	I	Input. Chip enable. Setting ENABLE = High biases up the Buck and initiates VCON regulation by the Buck.
D2	VCON	I	Analog voltage control input which controls Buck output voltage.
D3	NC	-	No connect; leave this pin floating.
D4	SW_BUCK	O	Buck converter switch node for external filter inductor connection.
D5			
E1	ATB1	-	Test pin. Connect to SGND or System Ground.
E2	FB_BUCK	-	Feedback input to inverting input of error amplifier. Connect Buck output voltage directly to this node.
E3	DGND	-	Ground for Boost, Buck, and RFFE digital blocks.
E4	PVIN_BUCK	-	Power supply input for Buck PFET and ACB FET. A 10 µF capacitor must be placed between this node and PGND. Must be externally connected to OUT_BOOST.
E5			
F1	ATB2	-	Test pin. Connect to SGND or System Ground.
F2	VDD2_BUCK	-	Power supply voltage input for Buck Analog PWM blocks. Internally connected to PVIN_BUCK when used with Boost.
F3	BGND	-	Ground for ACB bypass circuit.
F4	ACB	-	Active Current assist and Bypass output. Connected to the Buck converter output filter capacitor.
F5			

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS (1) (2)

VBATT pins to GND (PVIN_BOOST, VDD_BOOST, SW_BOOST, PVIN_BUCK, VDD1_BUCK, VDD2_BUCK, SW_BUCK, ACB, SGND_BOOST, SGND_BUCK, BGND, PGND)	−0.2V to +6.0V
BOOST_GATE, MODE, ENABLE, OUT_BOOST, FB_BUCK, VCON	(GND −0.2V to P_{VIN_BOOST} +0.2V)
Junction Temperature ($T_{J\text{-}MAX}$)	+150°C
Storage Temperature Range	−65°C to +150°C
Continuous Power Dissipation (3)	Internally Limited
Maximum Lead Temperature (Soldering, 10 sec)	+260°C
ESD Rating (4) Human Body Model	2 kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins. The LM3248 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller, and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.5V.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J < 130°C (typ.).
(4) The Human Body Model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7)

RECOMMENDED OPERATING CONDITIONS (1)

Input Voltage Range V_{BATT}	2.7V to 5.5V
Boost Output, Buck Input Range	2.7V to 5.5V
Recommended Load Current	0A to 2.5A
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range	−30°C to +90°C

(1) All voltages are with respect to the potential at the GND pins. The LM3248 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller, and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.5V.

THERMAL PROPERTIES

Junction-to-Ambient Thermal Resistance (θ_{JA}) (1) 30-bump DSBGA	38°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7 and is board dependent.

ELECTRICAL CHARACTERISTICS (BOOST)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ +90°C). Unless otherwise noted, all specifications apply with V_{BATT} = 3.0V and Buck in IDLE state.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LIM-BOOST,PFET}$	PFET valley current limit	Open Loop (1), VCON = 1.44V, V_{OUT_BUCK} = 3.6V		4.1		A
$F_{OSC-Boost}$	Boost internal oscillator frequency	2G/3G/4G mode, PWM mode, average		2.7		MHz

(1) Current limit is built-in, fixed, and not adjustable.

SYSTEM CHARACTERISTICS (BOOST)

The following spec table entries are specified by design and verifications providing the component values in the Typical Application Diagram are used: L = 1.0 µH (TOKO 1276AS-H-1R0N); C_{IN} = 10 µF (Murata GRM155R61A106M); and C_{OUT} = 1µF (Taiyo Yuden LWK107B7105KA-T) + 10 µF (Murata GRM155R61A106M). **These parameters are not verified by production testing.**(1) (The Boost stage output voltage equation is given in (2).) Min and Max values are specified over the ambient temperature range T_A = −30°C ≤ T_A ≤ 90°C. Unless otherwise noted, typical values are specified at V_{BATT} = 3.0V, Buck in IDLE, and T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT_BOOST}	Boost output voltage	Boost Bypass mode	2.7		5.5	V
		VCON = 1.60V , MODE = LOW (3G/4G), Load = 100 mA (2)		4.45		
		VCON = 1.46V , MODE = HIGH (2G), Load = 100 mA (2)		4.65		
$V_{GOTOBOOST}$	Boost turn-on threshold voltage	MODE = LOW; BOOST_GATE = HIGH; SW_BOOST = switching; VCON = (V_{BATT} - $V_{GOTOBOOST}$)/2.5	–50	0	37	mV
		MODE = HIGH; BOOST_GATE = HIGH; SW_BOOST = switching; VCON = (V_{BATT} - $V_{GOTOBOOST}$)/2.5		125		
$T_{ENABLE\ to\ BOOST\_GATE}$	Minimum time from ENABLE = HIGH (and remains steady) to BOOST_GATE rising edge	Initially in Idle State: Boost in 0% duty cycle (bypass)	25			µs
$T_{BOOST\_GATE\_Active}$	Minimum time to assert BOOST_GATE signal before next TTI slot boundary	BOOST_GATE signal must remain HIGH during this interval	45			
$I_{IN-BOOST-MAX}$	Max input current averaged across a 2G burst (RMS)	V_{BATT} = 2.7V, V_{OUT_BOOST} = 4.2V PA active during GSM burst (2)	3.5			A
$Duty\ Cycle_{MAX-BOOST}$	PWM maximum duty cycle	$I_{OUT-BOOST}$ < 1 mA		70		%
$V_{LINE-TR}$	Line transient response	V_{BATT} = 3.4V to 3.7V, ΔV = ±300 mV, T_R =T_F = 10 µs, V_{OUT_BUCK} = 3.7V, R_{LOAD_BUCK} = 4Ω, MODE = 3G/4G (2)		150		mVpp
$V_{LOAD-TR}$	Load transient response	V_{BATT} = 2.7V, I_{OUT_BUCK} = 10 mA to 850 mA, I_{OUT}, T_R = T_F = 10 µs V_{OUT_BUCK} = 3.7V, MODE = 3G/4G (2)		600		
$V_{BOOST-RIPPLE}$	Boost ripple voltage at worst-case conditions	V_{BATT} = 2.7V, V_{BOOST} = 3.4V, I_{OUT} = 2A, 2G mode (Sufficient overhead between V_{BOOST} and V_{OUT})		100		mVpp

(1) Parameter is specified by design, characterization testing, or statistical analysis. Typical numbers are not verified by production testing, but do represent the most likely norm.
(2) $V_{OUT-BOOST}$ = VCON * 2.5 + [≈ 450 mV(3G/4G) or ≈ 950 mV(2G)].

ELECTRICAL CHARACTERISTICS (BUCK)

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A \le +90°C$). Unless otherwise noted, all specifications apply with $V_{BATT} = 3.8V$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{FB,MIN}$	Feedback voltage at low setting	VCON = 0.16V, MODE = HIGH (1) (2)	**0.35**	0.4	**0.45**	V
$V_{FB,MAX}$	Feedback voltage at high setting	VCON = 1.6V, MODE = HIGH, V_{BATT} = 5.0V (1) (2)	**3.88**	4.0	**4.12**	
$I_{LIM,PFET,Steady State}$	Positive steady state peak current limit	V_{OUT} = 1.5V (3)	**1.34**	1.45	**1.65**	A
$I_{P-ACB,2G}$	Positive Active Current assist Bypass current limit	VCON = 0.6V, VACB = 2.8V (3)	**1.40**	1.70	**2.0**	
$I_{LIM,NFET}$	NFET Switch negative peak current limit	VCON = 1.0V (3)		−1.50	**−1.31**	
I_{SHDN}	Shutdown supply current I_{BATT}	ENABLE = LOW (4)		0.02	**4**	µA
I_{Q_PFM}	DC bias current from V_{BATT}	ENABLE = HIGH		260	**350**	
I_{Q_PWM}		ENABLE = HIGH		1010	**1100**	
F_{OSC}	Internal oscillator frequency	2G/3G/4G mode, PWM mode, average	**2.484**	2.7	**2.916**	MHz

(1) The parameters in the electrical characteristics table are tested under open loop conditions at V_{BATT} = 3.8V unless otherwise specified. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.
(2) $V_{OUT-BOOST}$ = VCON * 2.5 + [≈ 450 mV(3G/4G) or ≈ 950 mV(2G)].
(3) Current limit is built-in, fixed, and not adjustable.
(4) Shutdown current includes leakage current of PFET.

SYSTEM CHARACTERISTICS (BUCK)

The following spec table entries are specified by design and verification providing the component values in the Typical Application Diagram are used: L = 1.5 µH (TOKO 1285AS-H-1R5N); C_{IN} = 10 µF (Murata GRM155R61A106A); and C_{OUT} = 10 µF + 4.7 µF (Murata GRM155R61A106A, GRM155R61A475MEAA) + 4 x 1.0 µF (Murata GRM033R60J105M). **These parameters are not verified by production testing.**(1) Min and Max values are specified over the ambient temperature range T_A = −30°C ≤ T_A ≤ +90°C. Typical values are specified at V_{BATT} = 3.8V and T_A = 25°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{Warm-Up}$	Time Delay required after BOOST_GATE = HIGH (before VCON can change)	ENABLE = High	30			µs
$T_{RESPONSE}$	Time for V_{OUT} to rise from 0V to 3.4V (90% or 3.06V)	V_{BATT} = 3.8V, R_{LOAD} = 68Ω, VCON = 0V to 1.36V			15	µs
	Time for V_{OUT} to fall from 3.4V to 0V (10% or 0.34V)	V_{BATT} = 3.8V, R_{LOAD} = 68Ω, VCON = 1.36V to 0V				
	Time for V_{OUT} to rise from 0.8V to 3.3V (90% or 3.05V)	V_{BATT} = 3.8V, R_{LOAD} = 20Ω, VCON = 0.32V to 1.32V			10	
	Time for V_{OUT} to fall from 3.3V to 0.8V (10% or 1.05V)	V_{BATT} = 3.8V, R_{LOAD} = 20Ω, VCON = 1.32 to 0.32V				
	Time for V_{OUT} to rise from 1.4V to 3.4V (90% or 3.2V)	V_{BATT} = 3.8V, R_{LOAD} = 6.8Ω, VCON = 0.56V to 1.36V			10	
	Time for V_{OUT} to fall from 3.4V to 1.4V (10% or 1.6V)	V_{BATT} = 3.8V, R_{LOAD} = 6.8Ω, VCON = 1.36V to 0.56V				
	Time for V_{OUT} to rise from 1.8V to 2.8V (93% or 2.73V)	V_{BATT} = 3.8V, R_{LOAD} = 2.2Ω, VCON = 0.72V to 1.12V MODE = 2G			15	
	Time for V_{OUT} to fall from 2.8V to 1.8V (7% or 1.87V)	V_{BATT} = 3.8V, R_{LOAD} = 2.2Ω VCON = 1.12V to 0.72V MODE = 2G				
$I_{LIM,PFET,Transient}$	Positive transient peak current limit	V_{OUT} = 1.5V (2)		1.9	2.1	A
$I_{OUT\_MAX,\ PWM}$	Maximum load current in PWM mode	V_{BATT} ≥ 2.88V, VCON = 1.48V (V_{OUT} = 3.7V), PWM mode, switcher plus ACB current	2.0			A
		V_{BATT} ≥ 3.0V, VCON = 1.48V (V_{OUT} = 3.7V), PWM mode, switcher plus ACB current	2.3			
		VCON = 1.2V (V_{OUT} = 3.0V), PWM mode, switcher plus ACB current	2.5			
I_{OUT_PFM}	Load current to enter into PFM mode at high duty cycle (D > 0.85 AND Boost in Bypass)	V_{BATT}/V_{OUT} = 3.6/3.3V, 4.2/4.0V, BOOST_GATE = LOW	35			mA
$I_{OUT\_MAX,\ PFM}$	Maximum load current to enter into PFM mode	D < 0.85 or SW_BOOST = switching		85		mA
$I_{OUT,PU}$	Maximum output transient pullup current limit	PWM mode (2), switcher plus ACB current	3.0			A
I_{OUT,PD_PWM}	PWM maximum output transient pulldown current limit				−3.0	
V_{OUT_ACC}	V_{OUT} accuracy over output voltage range	V_{OUT} = 0.6V to 3.6V (3)	−3		+3	%

(1) Parameter is specified by design, characterization testing, or statistical analysis. Typical numbers are not verified by production testing, but do represent the most likely norm.
(2) Current limit is built-in, fixed, and not adjustable.
(3) Accuracy limits are ±3% or ±50 mV, whichever is larger.

SYSTEM CHARACTERISTICS (BUCK) (continued)

The following spec table entries are specified by design and verification providing the component values in the Typical Application Diagram are used: L = 1.5 µH (TOKO 1285AS-H-1R5N); C_{IN} = 10 µF (Murata GRM155R61A106A); and C_{OUT} = 10 µF + 4.7 µF (Murata GRM155R61A106A, GRM155R61A475MEAA) + 4 x 1.0 µF (Murata GRM033R60J105M). **These parameters are not verified by production testing.**(1) Min and Max values are specified over the ambient temperature range T_A = −30°C ≤ T_A ≤ +90°C. Typical values are specified at V_{BATT} = 3.8V and T_A = 25°C unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT_RIPPLE}	Ripple voltage at no pulse skipping condition	V_{OUT} = 0.4V to 3.6V, R_{OUT} = 2.2Ω, 2G mode (4)		4	10	mVpp
	Ripple voltage at pulse skipping condition	V_{BATT} = 4.2V to dropout, V_{OUT} = 3.6V, R_{OUT} = 2.2Ω, 2G mode (4)		14	20	
	PFM ripple voltage	V_{OUT} = 1.0V, I_{OUT} = 40 mA (4)		9	15	
$V_{LINE-TR}$	Line transient response	V_{BATT} = 3.6V to 4.2V, T_R = T_F = 10 µs, V_{OUT} = 1.0V, I_{OUT} = 600 mA		70		mVpk
$V_{LOAD-TR}$	Load transient response	V_{OUT} = 3.0V, T_R = T_F = 10 µs, I_{OUT} = 0A to 1.2A, 2G mode		150		
F_{SW_PFM}	Minimum PFM frequency	V_{BATT} = 3.2V, V_{OUT} = 1.0V, I_{OUT} = 10 mA		100		kHz

(4) Ripple voltage should be measured at C_{OUT} node on a well-designed PC board, using suggested inductor and capacitors. Ripple voltage is defined as the maximum peak-to-peak output voltage variation measured over a 100 µs period.

SYSTEM CHARACTERISTICS (BOOST-BUCK)

See SYSTEM CHARACTERISTICS (BOOST) and SYSTEM CHARACTERISTICS (BUCK) for test conditions.

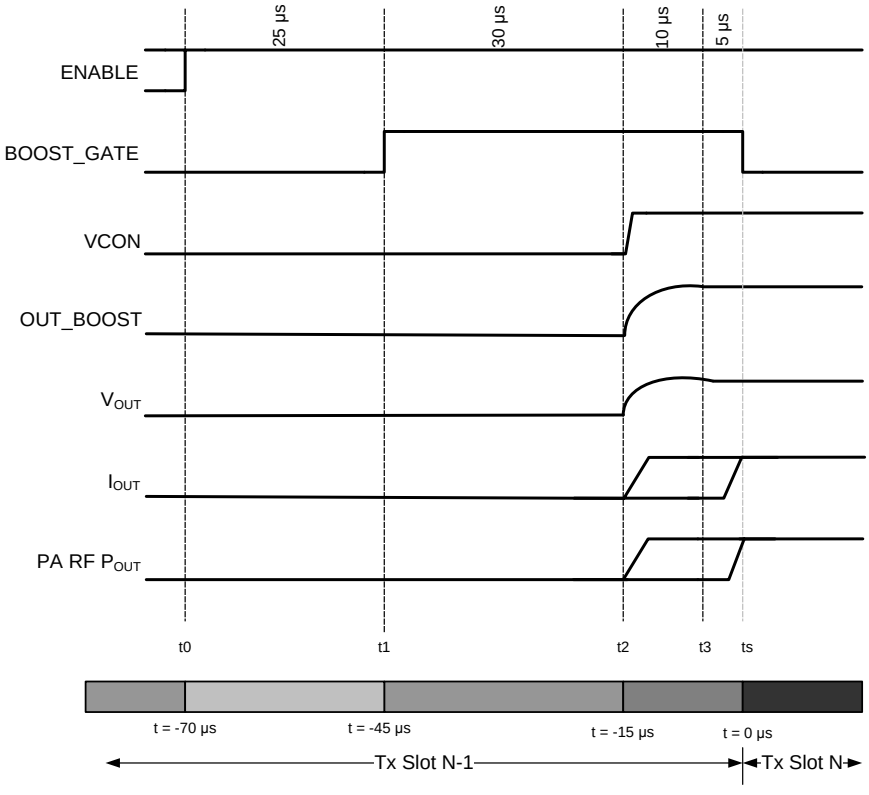
Symbol	Parameter	Condition	Min	Typ	Max	Units
η	Boost-Buck Efficiency	V_{BATT} = 4.0V, V_{OUT} = 3.4V, I_{OUT} = 2A (2G, PWM mode)		86		%
		V_{BATT} = 4.0V, V_{OUT} = 2.5V, I_{OUT} = 800 mA (2G, PWM mode)		89		
		V_{BATT} = 4.0V, V_{OUT} = 3.0V, I_{OUT} = 400 mA (2G, PWM mode)		93		
		V_{BATT} = 3.4V, V_{OUT} = 4.0V, I_{OUT} = 850 mA (3G/4G, PWM mode)		90		
		V_{BATT} = 3.4V, V_{OUT} = 3.0V, I_{OUT} = 500 mA (3G/4G, PWM mode)		94		
		V_{BATT} = 3.4V, V_{OUT} = 2.5V, I_{OUT} = 70 mA (3G/4G, PFM mode)		90		
		V_{BATT} = 3.4V, V_{OUT} = 0.9V, I_{OUT} = 200 mA (3G/4G, PWM mode)		86		
		V_{BATT} = 3.6V, V_{OUT} = 3.3V, I_{OUT} = 20 mA (3G/4G PFM mode)		92		
		V_{BATT} = 3.4V, V_{OUT} = 0.6V, I_{OUT} = 20 mA (3G/4G, PFM mode)		78		
$T_{RESPONSE}$	Time for V_{OUT} to rise from 0.4V to 4.0V (93% or 3.75V)	V_{BATT} = 2.7, 3.2V. R_{LOAD} = 11.4Ω, VCON = 0.16V to 1.6V; T_{rise} = T_{fall} = 1 µs MODE = 2G (HIGH)			15	µs
	Time for V_{OUT} to fall from 4.0V to 0.4V (7% or 0.65V)	V_{BATT} = 2.7, 3.2V. R_{LOAD} = 11.4Ω, VCON = 1.6V to 0.16V; T_{rise} = T_{fall} = 1 µs MODE = 2G (HIGH)				

ELECTRICAL CHARACTERISTICS (CONTROL INTERFACE)

Limits in standard typeface are for T_A = 25°C. Limits in **boldface** type apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ +90°C). Unless otherwise noted, all specifications apply with V_{BATT} = 2.7V to 5.5V.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input high level threshold BOOST_GATE, MODE, ENABLE		**1.35**			V
V_{IL}	Input low level threshold BOOST_GATE, MODE, ENABLE				**0.50**	
I_{IN}	MODE, ENABLE, BOOST_GATE Pins - HIGH Input Current	VDD_BOOST = VDD2_BUCK = PVIN_BOOST = 3.8V SW_BOOST = OUT_BOOST = VDD1_BUCK = PVIN_BUCK = NO CONNECT 1) ENABLE = 1.8V, all remaining pins = GND 2) MODE = 1.8V, all remaining pins = GND 3) BOOST_GATE = 1.8V, all remaining pins = GND	–1	0	1	µA
	MODE, ENABLE, BOOST_GATE Pins - LOW Input Current	VDD_BOOST = VDD2_BUCK = PVIN_BOOST= 3.8V SW_BOOST = OUT_BOOST = VDD1_BUCK = PVIN_BUCK = NO CONNECT 1) ENABLE = 0V, all remaining pins = 1.8V 2) MODE = ENABLE = 0V, all remaining pins = 1.8V 3) BOOST_GATE = ENABLE = 0V, all remaining pins = 1.8V				

STARTUP TIMING



t0 ENABLE must transition HIGH min. 25 µs before BOOST_GATE is brought HIGH.

t1 BOOST_GATE must transition HIGH min. 45 µs before slot boundary. LM3248 Auto-Boost cycle begins.

t2 VCON signal change must start min. 15 µs before slot boundary. V_{OUT} transition follows VCON change. OUT_BOOST tracks at V_{OUT} + 450 mV / 950 mV (3G4G/2G).

t3 V_{OUT} settles to within 90% of final value.

ts Slot Boundary. LM3248 Boost cycle ends. New boost output target selected. Start of next TTI power control.

Note: the BOOST_GATE minimum duration is shown. To minimize boost circuit current drain, the BOOST_GATE falling edge should occur as soon after this minimum time as possible and before the start of the next Tx slot.

Figure 2. Startup + Optional Boost Timing Sequence

TYPICAL CHARACTERISTICS

For all Efficiency vs Load Current graphs, L1=1276AS-H-1R0N, L3=1285AS-H-1R5N.

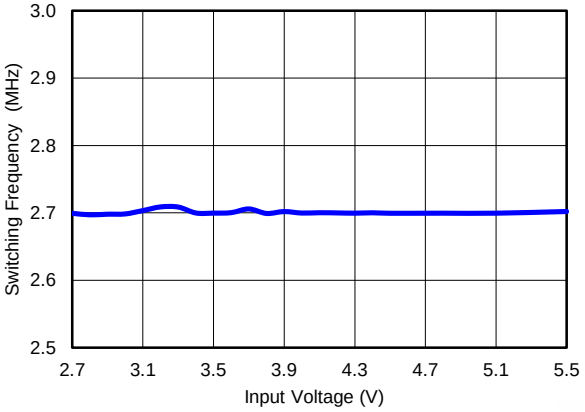
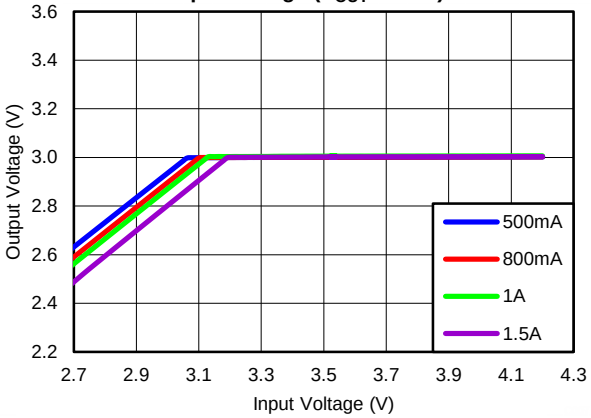


Figure 3.



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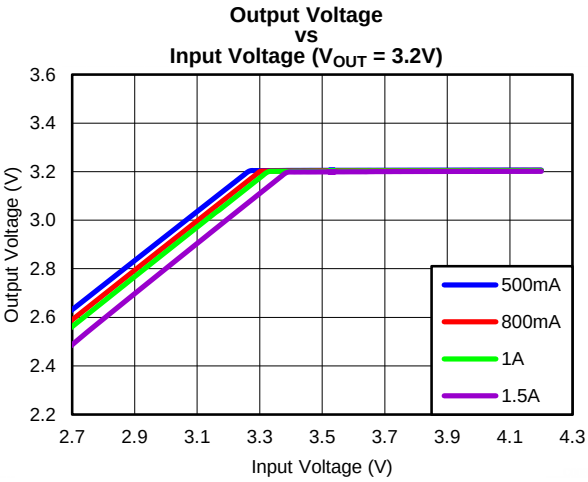
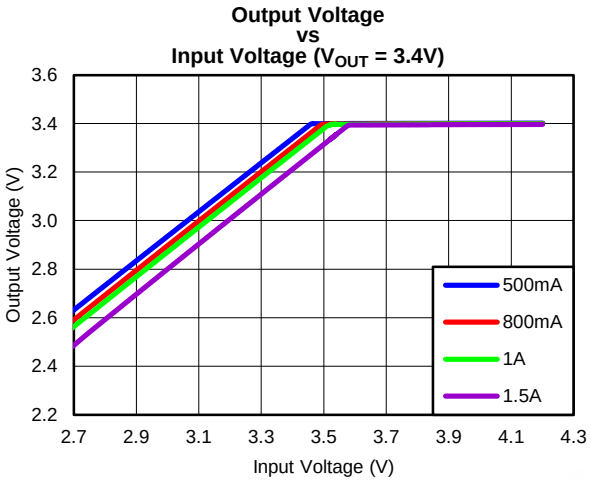


Figure 5.



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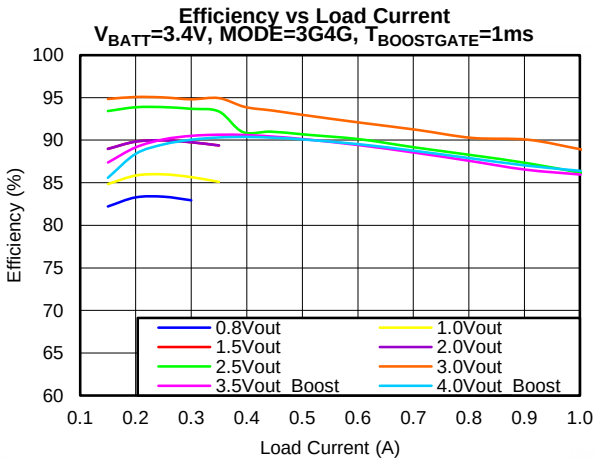

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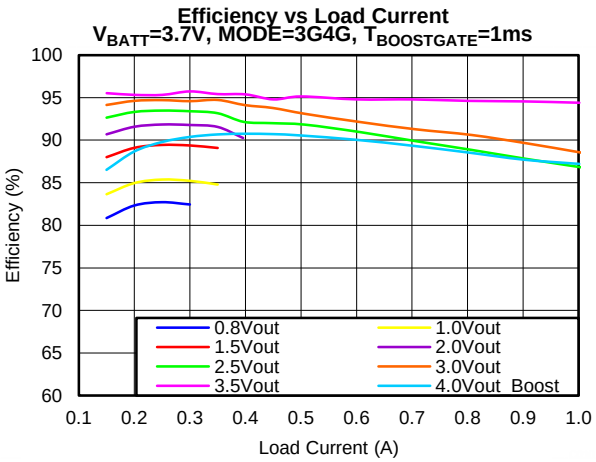
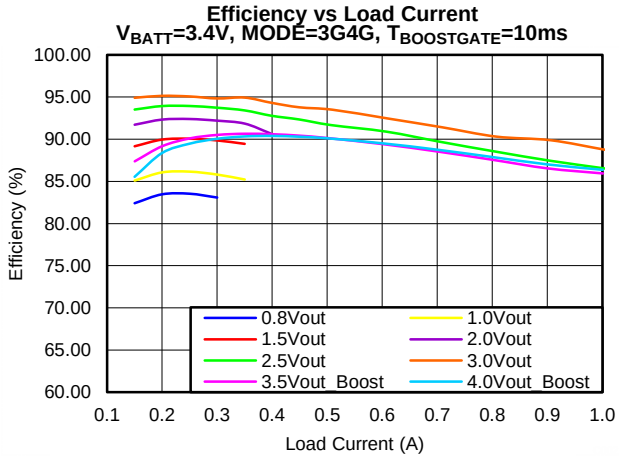


Figure 8.

TYPICAL CHARACTERISTICS (continued)

For all Efficiency vs Load Current graphs, L1=1276AS-H-1R0N, L3=1285AS-H-1R5N.



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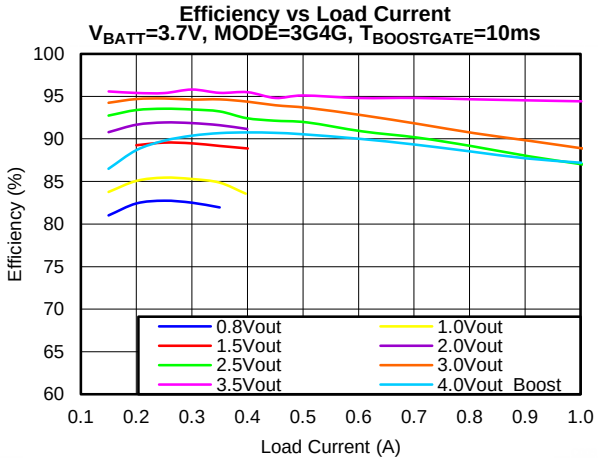

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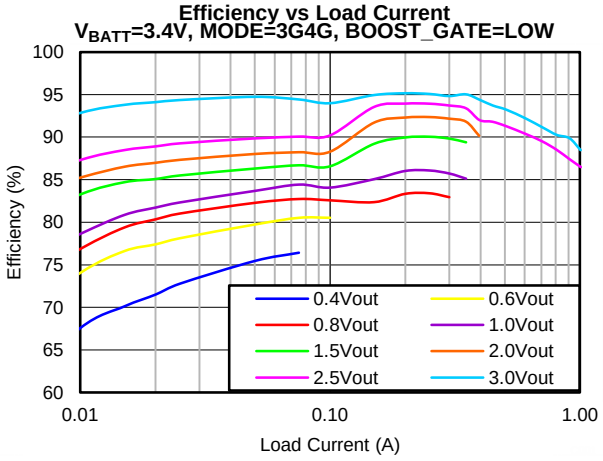

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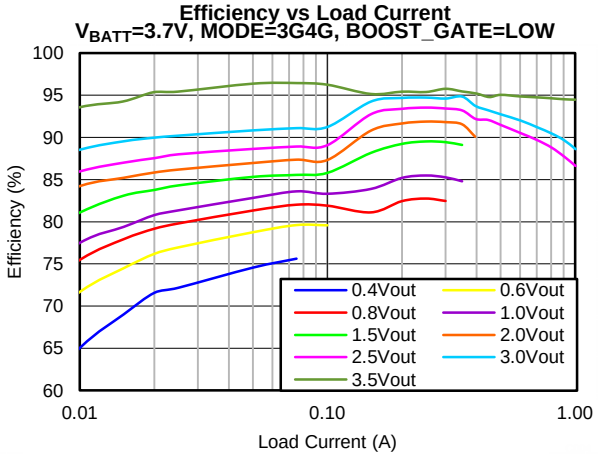

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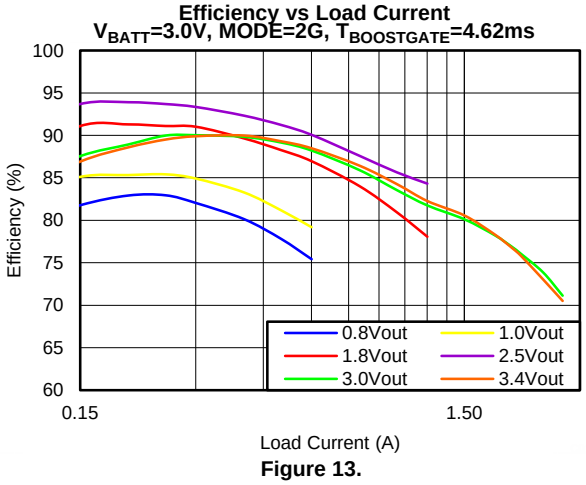


Figure 13.

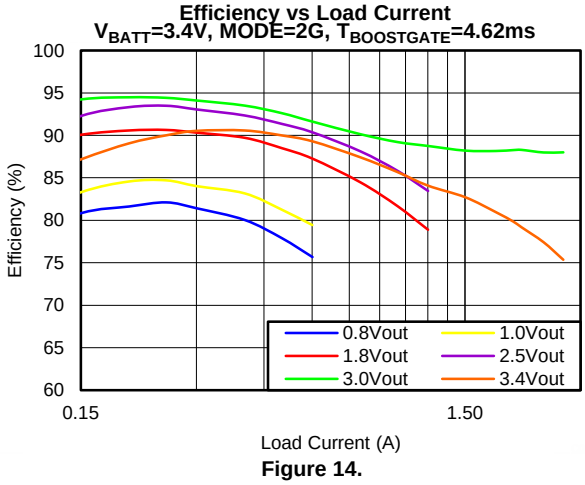


Figure 14.

TYPICAL CHARACTERISTICS (continued)

For all Efficiency vs Load Current graphs, L1=1276AS-H-1R0N, L3=1285AS-H-1R5N.

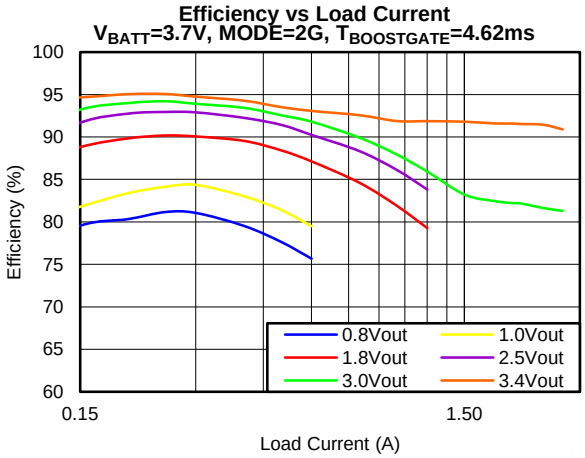


Figure 15.

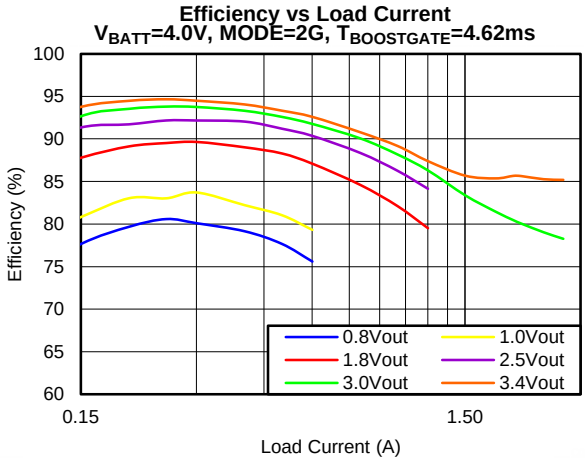


Figure 16.

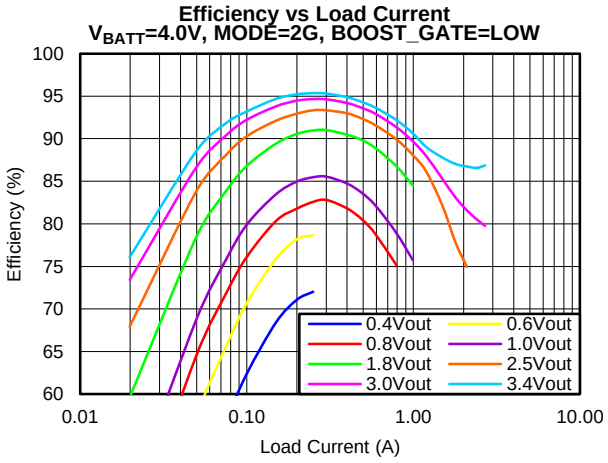


Figure 17.

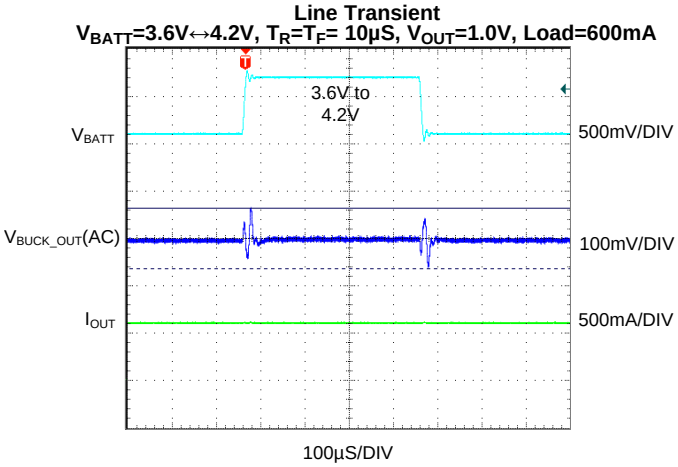


Figure 18.

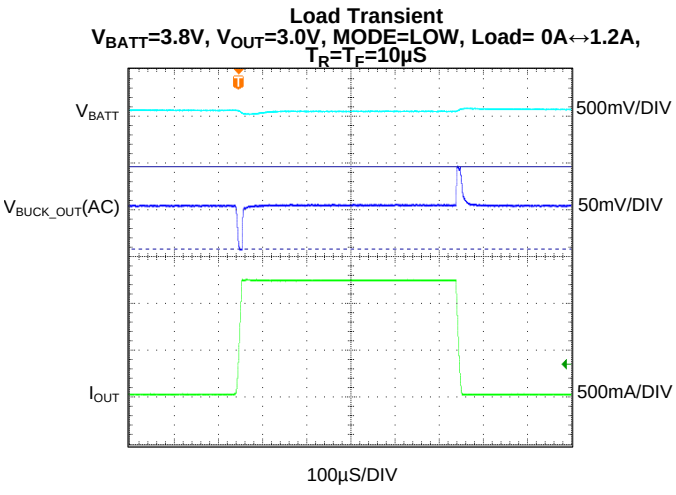


Figure 19.

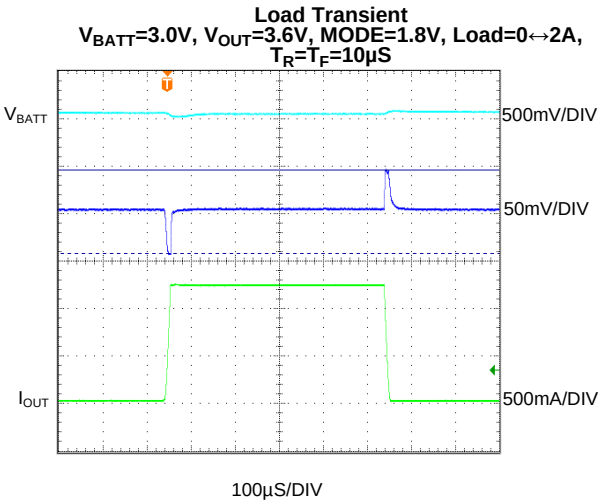


Figure 20.

TYPICAL CHARACTERISTICS (continued)

For all Efficiency vs Load Current graphs, L1=1276AS-H-1R0N, L3=1285AS-H-1R5N.

Startup in Auto-Boost Mode
V_{BATT}=2.7V, Load=200 mA, MODE=2G, V_{OUT}=0.4↔4V, T_R=T_F=10µS

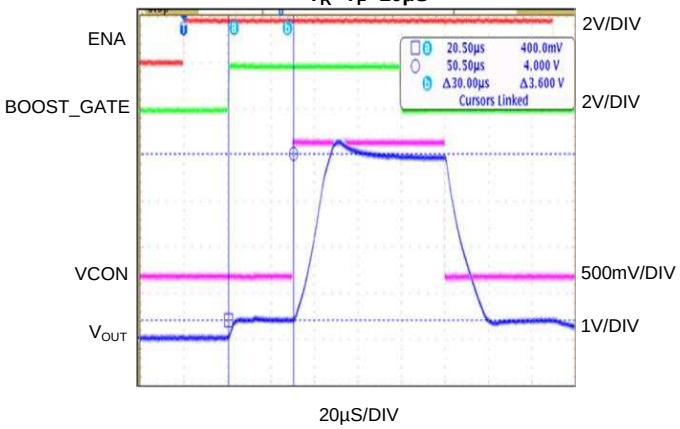


Figure 21.

Timed Output Current Limit into Short Circuit
V_{BATT}=4.3V, V_{OUT}=2.5V, Load=6.8Ω/Short to GND

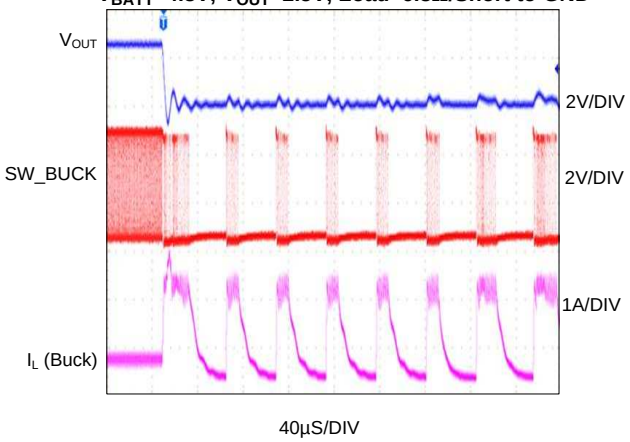


Figure 22.

VCON Transient with Boost Active
V_{BATT}=3.2V, MODE=2G, V_{OUT}= 0.4↔4 V, Load=11.4Ω

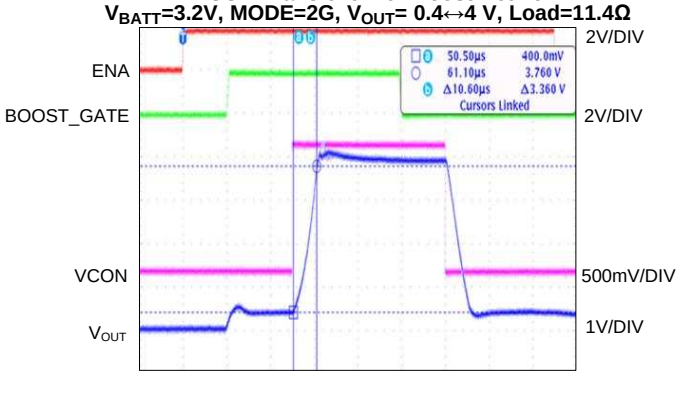


Figure 23.

VCON Transient Response
V_{BATT}=3.8V, V_{OUT}= 0.8V↔3.3V, MODE=LOW
BOOST_GATE=LOW, Load=20Ω, T_R=T_F=10µS

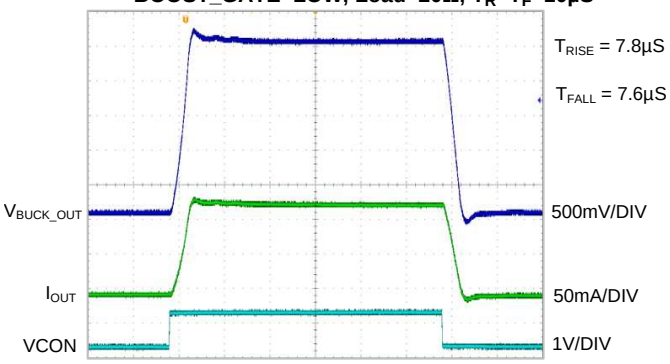


Figure 24.

VCON Transient Response
V_{BATT}=3.8V, V_{OUT}= 1.4V↔3.4V, MODE=LOW
BOOST_GATE=LOW, Load=6.8Ω, T_R=T_F=10µS

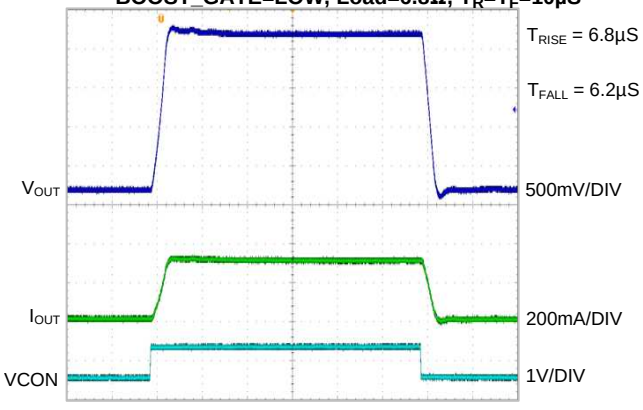


Figure 25.

VCON Transient Response
V_{BATT}=3.8V, V_{OUT}=1.0V, MODE=LOW
BOOST_GATE=LOW, Load=0A↔60mA, T_R=T_F=10µS

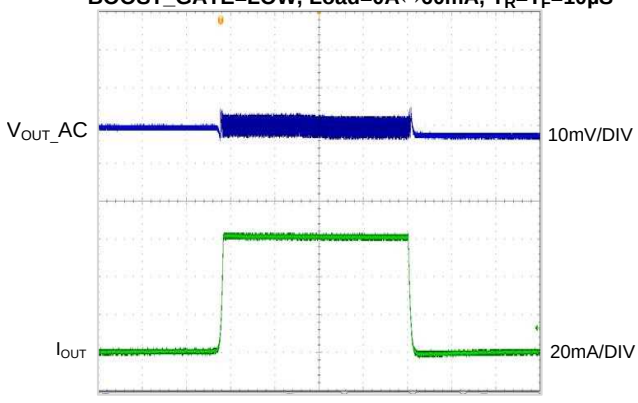


Figure 26.

FUNCTIONAL DESCRIPTION

The LM3248 is a high-efficiency boost-buck DC/DC converter used in mobile phones and other battery-powered RF devices to improve overall system efficiency by tailoring RF PA stage supply rail voltages to RF output power levels. The LM3248 optimizes efficiency over a wide range of power levels when using Li polymer battery cells operating as low as 2.7V.

The LM3248 architecture is comprised of a step-up (boost) DC/DC switching converter followed by a step-down (buck) DC/DC switching converter. This cascaded boost-buck architecture allows the device to support output voltages that are either above or below the input battery voltage, while simultaneously providing excellent output transient and noise performance. See Figure 27 for more details. The LM3248 minimizes 3G/4G/4G-LTE Advanced current consumption in User Equipment (UE) transmit power distribution environments and, in addition, supports higher power 2G functionality.

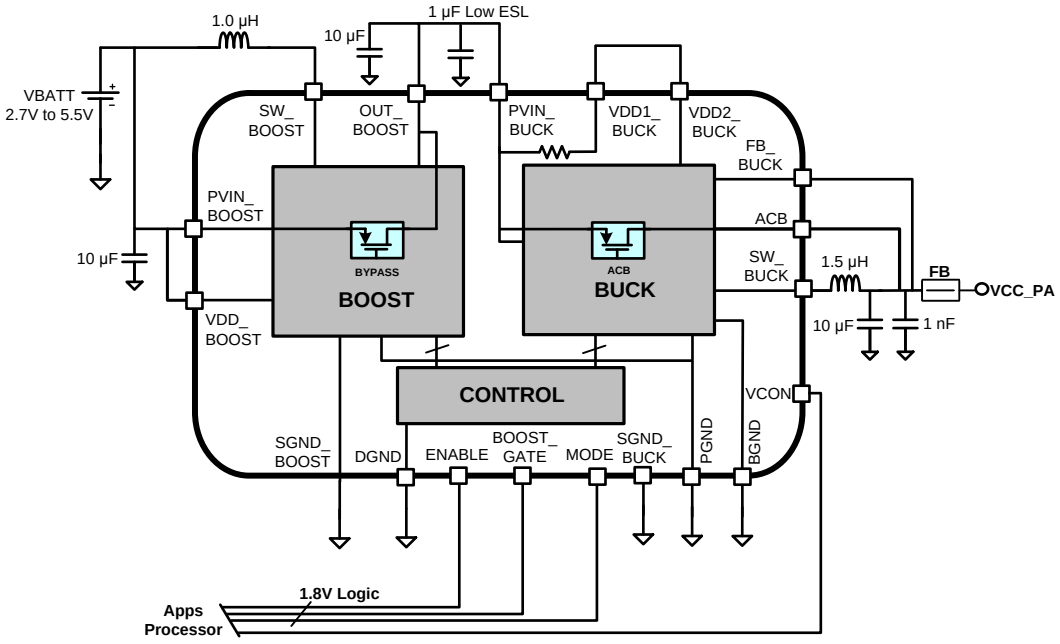


Figure 27. Typical Application: Boost-Buck

Boost Converter

The Boost DC/DC converter enables the LM3248 to support output voltages that are either above or below the input battery voltage. The Boost converter can be operated in either Boost or Boost-Bypass (Buck Only) modes. Both modes of operation require the device to be enabled (ENABLE) and either 2G or 3G/4G mode (MODE) to be selected. Boost mode automatically engages the boost circuit when needed and requires an additional digital control signal, BOOST_GATE. The Buck output settles to new VCON levels approximately 45 µs after BOOST_GATE transitions from LOW to HIGH (see Figure 2).

The Boost converter output (OUT_BOOST) is externally (and internally) connected to the Buck input (PVIN_BUCK) supply voltage. The Boost converter enables increased PA efficiency and higher linearity at higher Tx power settings when the battery voltage is lower than normally required. A unique synchronization scheme allows the Boost and Buck voltage transitions to occur with minimal time-critical programming. The LM3248 should be operated in Boost-Bypass mode (Buck-Only, BOOST_GATE=LOW) when it is known that the Buck output voltage will be lower than the battery voltage, such as at low transmit RF power levels. This practice reduces unnecessary battery drain caused by boost bias circuits and improves efficiency.

When Boost operation is selected (BOOST_GATE=HIGH), the LM3248 monitors the input voltage and compares it with the VCON output control voltage setting. The Boost circuit is activated on the rising edge of BOOST_GATE when V_{BOOST}, the target boost output voltage, is greater than the input or battery voltage (V_{BATT}) to achieve the desired output voltage level, according to the equations:

$$V_{BOOST} = VCON * 2.5 + 0\ mV\ [V_{BOOST} > V_{BATT}]\ (3G\ or\ 4G\ mode)$$
or
$$V_{BOOST} = VCON * 2.5 + 125\ mV\ [V_{BOOST} > V_{BATT}]\ (2G\ mode)$$

Once in Boost mode, the Boost voltage automatically adjusts according to the following equations:

$$V_{BOOST} = VCON * 2.5 + 450\ mV\ [V_{BOOST} > V_{BATT}]\ (3G\ or\ 4G\ mode)$$
or
$$V_{BOOST} = VCON * 2.5 + 950\ mV\ [V_{BOOST} > V_{BATT}]\ (2G\ mode)$$

In Boost mode, internal circuitry will automatically engage the large bypass switch to prevent the Boost output from ever falling below the battery voltage, V_{BATT}, by more than a few hundred millivolts (200 mV typ.) when Boost-Bypass conditions are not met. This functionality is described below.

When operating in Boost mode, the BOOST_GATE signal should be toggled between HIGH and LOW logic levels at a rate synchronous with the Transmission Time Interval (TTI) frame, per the Startup Timing requirements given in Figure 2. This provides sufficient setup time for the Boost bias circuits to activate before the new (possibly higher) Buck output level is updated, ensuring a smooth transition between levels.

Note that V_{BOOST} programmed output levels are determined by the VCON command voltage; not by the Buck DC/DC converter output voltage, V_{CC_PA}. This is necessary to minimize Boost output voltage tracking delay times.

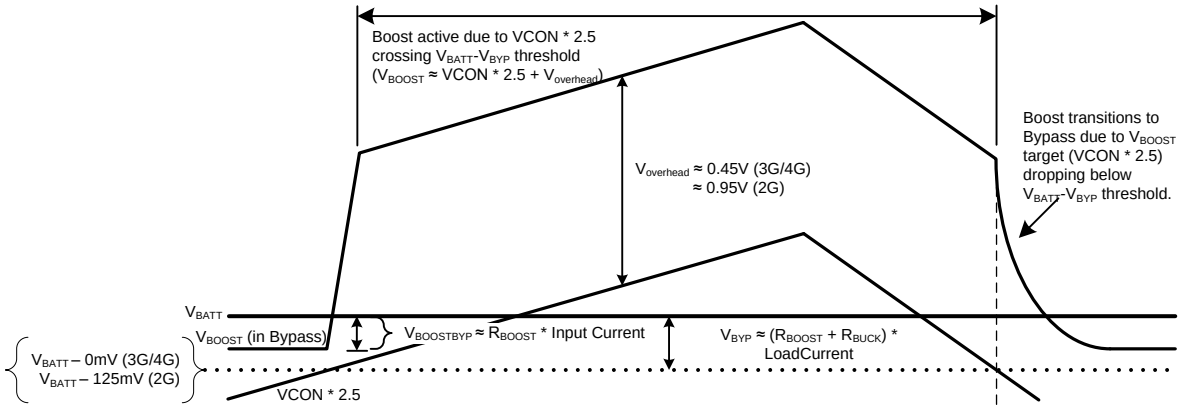


Figure 28. Boost Operation showing VCON-V_{BATT} Relationship

Boost-Bypass Function

The LM3248 provides a bypass function with very low dropout resistance when the Boost stage is not needed to support the output voltage requirements. The Boost circuit automatically enters Boost-Bypass mode when BOOST_GATE is high and the VCON voltage is approximately less than VCON(max), as shown below:

$$VCON(max) = \frac{[V_{BATT} - 0\ mV]}{2.5}\ (3G\ or\ 4G\ mode)$$

$$VCON(max) = \frac{[V_{BATT} - 125\ mV]}{2.5}\ (2G\ mode)$$

In Boost-Bypass mode, the low resistance (75 mΩ typ.) bypass circuit effectively connects the PVIN_BOOST and OUT_BOOST pins in parallel with the boost inductor and boost output power transistor. The Boost-Bypass circuit is active at all times when BOOST_GATE=LOW. When Boost-Bypass is active, the minimum total dropout resistance of the path between the PVIN_BOOST and OUT_BOOST pins is 60 mΩ (typ.). The Boost-Bypass mode of operation is valid for $2.7V < V_{BATT} < 5.5V$.

Buck Converter

The Buck converter output voltage, V_{CC_PA}, is directly proportional to the VCON control voltage, which level is determined by the applications processor, BBIC or RFIC RF output Power Amplifier control algorithm. The user can dynamically program the Buck output voltage from 0.4V to 4.0V (typ.) by adjusting the VCON voltage setting, per the equation: $V_{CC\_PA} = VCON * 2.5$.

The LM3248 has been designed to make rapid, smooth V_{CC_PA} output transitions required by fast 3G/4G and 2G burst ramp profiles.

The current consumption of RF Power Amplifier modules (RF PAs) typically increases with supply voltage. Accordingly, DC/DC converter output power requirements increase as the RF PA module V_{CC_PA} voltages increase. Two operating methods, Pulse Width Modulation (PWM) and Pulse Frequency Modulation (PFM), are used to optimize system efficiency over a range of PA power levels. When the LM3248 is not needed, the device can be set to shutdown mode (ENABLE = LOW) to minimize battery current drain. Current overload protection and thermal overload shutdown are also provided.

2G vs. 3G/4G Modes

The MODE pin enables selection of either constant PWM (2G) or automatic PWM/PFM (3G/4G) operation.

To maintain higher efficiency at light loads, the 3G/4G mode setting is used. When in Boost-Bypass, and average inductor current drops below 45 to 90 mA (typ.), PFM operation is active. The switching frequency is reduced to improve efficiency. Conversely, the LM3248 transitions back to PWM operation from PFM when the average inductor current increases to values above 90 to 160 mA (typ.). Automatic transition into PWM operation also occurs if the output voltage falls more than 25 mV due to a load current increase.

Active Current and Analog Bypass (ACB)

Fast transient 2G power bursts require high current levels to be sourced or sunk from the LM3248 Buck DC/DC converter. The **A**ctive **C**urrent assist and analog **B**ypass (ACB) feature, built into the Buck DC/DC converter, enables smooth waveform transitions with load currents as high as 2.5A using smaller footprint inductors and meets all of the transient requirements when supplying V_{CC_PA} voltages for the latest multi-mode RF Power Amplifier modules. The ACB circuit provides an additional current path when the load current exceeds 1.4A (typ.) or as the switcher approaches dropout. Similarly, the ACB circuit enables the LM3248 to respond with faster output voltage transition times by providing extra output current on rising and falling output edges. The LM3248 handles bypass events by sensing input voltage, output voltage, and load current conditions, and then automatically and seamlessly transitioning the converter into analog bypass, while maintaining output voltage regulation and low output voltage ripple. Full bypass (100% duty cycle) will occur if the total dropout resistance in bypass mode (≈ 50 mΩ) is insufficient to regulate the output voltage.

Shutdown

When the LM3248 ENABLE = LOW, the Buck and Boost DC/DC converters and control circuits are programmed into an OFF (Shutdown) state and the output power switches are placed in a tri-state condition. The Shutdown state reduces system current consumption to less than 4 µA.

Output Current Protection

The Buck DC/DC converter and the ACB circuit each have output current protection. The Buck converter includes a steady-state current limit which monitors load currents and enables the ACB circuit. During transient over-current conditions the peak current limit detector turns off the PFET switch within the current PWM cycle and initiates the timed output current limit.

Timed Output Current Limit

If the output load current rises above the $I_{LIM,PFET,Transient}$ threshold continuously for more than 11 µs, and the output voltage falls below 0.3V (typ.), the LM3248 Buck DC/DC converter switch node (SW_BUCK pin) is put into a high-impedance state, and the ACB circuit is disabled. The power switch then remains disabled for a period of 35 µs to force the inductor current to ramp down. If the short circuit condition continues, the cycle will repeat.

Thermal Overload Protection

The LM3248 IC has thermal overload protection that disables the device, protecting it from short-term misuse and overload conditions. If the junction temperature exceeds 150°C (typ.), all of the power functions will be turned off. Normal operation resumes after the temperature drops below 130°C (typ.), and the LM3248 will attempt to return to the operating state before the over-temperature condition occurred. Prolonged operation in thermal overload condition may damage the device and is therefore not recommended.

Digital Control Signals

The BOOST_GATE, MODE and ENABLE pins are 1.8V logic-level inputs for controlling the LM3248. A logic LOW level applied to the ENABLE pin puts the LM3248 into a Shutdown state, where minimum current is drawn from the battery. The MODE pin allows the user to select whether PWM (2G) or PWM/PFM (3G/4G) operation is allowed. The BOOST_GATE pin enables the Boost DC/DC converter circuitry and related functionality.

Manufacturing Considerations

Use of the DSBGA package requires specialized board layout, precision mounting, and careful re-flow techniques, as detailed in Texas Instruments Application Note AN-1112 (SNVA009). Please refer to the section *Surface Mount Assembly Considerations.* For best results in assembly, local alignment fiducial markers on the PC board should be used to facilitate placement of the device.

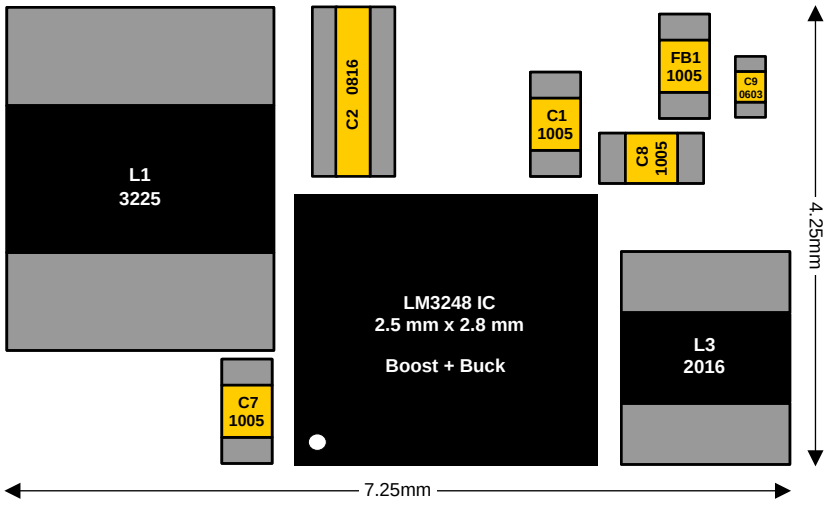
The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that would otherwise form if the solder-mask and pad overlap, which would hold the device off the surface of the board and interfere with mounting. See Application Note AN-1112 (SNVA009) for specific instructions how to do this.

The 30-bump(5x6) DSBGA package used for the LM3248 has the following Non-Solder Mask Defined (NSMD) mounting specifications:

- Solder ball diameter: 0.265 mm
- Copper pad size: 0.225 mm ± 0.02 mm
- Solder mask opening: 0.325 ± 0.02 mm

The trace to each pad should enter the pad with a 90°entry angle to prevent debris from being caught in deep corners. Symmetry is important to ensure the solder bumps re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1-A5, C4, C5, E4, E5, F4 and F5 since PVIN_BOOST, OUT_BOOST, PGND, PVIN_BUCK and ACB may be connected to large copper planes and inadequate thermal reliefs can result in inadequate re-flow of these bumps.

Typical Solution Size



APPLICATION INFORMATION

Recommended External Components

Inductor Selection

The LM3248 was designed to work with 1.0 µH and 1.5 µH buck inductors. The largest current magnitudes encountered with the LM3248 are in 2G mode (that is, 2.5A for 2G vs. <1A for 3G/4G). Because of the low duty cycles encountered with 2G transmission bursts, the maximum RMS current encountered is much less than the peak.

Suitable inductors are typically rated for maximum current with two different numbers:

1. ΔL/L = 30% (or similar) which means the current level that causes a 30% drop in the inductance value (due to core saturation), and
2. ΔT = 40°C (or similar) which means the current level that causes a 40°C rise in the inductor's temperature.

Because of the “peaky” nature of 2G current waveforms (low duty cycle, high peak-to-average ratio), the “ΔL/L=30%” (or similar) current limit will typically be reached long before the “ΔT=40°C” (or similar) current value. This means that selection of the inductor is saturation-limited.

Another way of saying this is that the inductor core saturation is proportional to the peak current value, while the temperature rise is due to the RMS current value. As a result, candidate inductors which may appear too small for the application when looking at the “ΔT=40°C” (or similar) current specification, may be sufficiently sized, as long as the “ΔL/L = 30%” (or similar) current value is less than the peak current required for the application.

If the “ΔL/L = 30%” (or similar) current value is not specified, or it is not clear whether the max current rating for the part refers to either one of these rules of measure, this information should be requested from the supplier.

The LM3248 automatically manages the inductor peak and RMS current (or steady-state current peak) through the SW_BUCK pin. The SW_BUCK pin has two positive current limits. The first is the 1.45A typical (or 1.65A maximum) overcurrent protection which sets the upper steady-state inductor peak current (as detailed in the ELECTRICAL CHARACTERISTICS (BUCK) parameter "$I_{LIM,PFET,SteadyState}$"). It is the dominant factor limiting currents from surpassing the buck inductor I_{SAT} specification. The second is an over-limit current protection "$I_{LIM,PFET,Transient}$" found in the SYSTEM CHARACTERISTICS (BUCK) table. It limits the maximum peak inductor current during large signal transients (i.e., < 20 µs) to 1.9A typical (2.1A maximum). When selecting the buck output inductor, the user should insure that a minimum of 0.3 µH is maintained when peak currents reach the $I_{LIM,PFET,Transient}$ current limit.

The **ACB** circuit automatically adjusts its output current to keep the steady-state inductor current below the $I_{LIM,PFET,Steady\ State}$ current limit. The inductor RMS current will always be less than this value during the transmit burst, thus keeping the inductor within its thermal operating limits.

For good efficiency, the inductor's resistance should be less than 0.15Ω. Low DCR inductors (< 0.15Ω) are recommended. Table 1 suggests some inductors and their suppliers. The slightly larger inductors listed in Table 1 were observed to enhance efficiency 1 to 2% under some V_{IN}/V_{OUT}/Load conditions.

Table 1. Suggested Inductors and Their Suppliers

Boost Inductor 1.0 µH, 3225, 3.0A, 60 mΩ				
Model	**Vendor**	**Dimensions (mm)**	**I_{SAT} (–30%) (A)**	**DCR (mΩ)**
1276AS-H-1R0N	TOKO	3.2 x 2.5 x 1.0	3.9	48
CIG32W1R0MNE	Samsung	3.2 x 2.5 x 1.0	3.0	60
1277AS-H-1R0M	TOKO	3.2 x 2.5 x 1.2	4.6	37
Buck Inductor 1.5 µH, 2016 or 2520, 2.2A, 150 mΩ				
Model	**Vendor**	**Dimensions (mm)**	**I_{SAT} (–30%) (A)**	**DCR (mΩ)**
1285AS-H-1R5N	TOKO	2.0 x 1.6 x 1.0	2.2	120
LQM2MPN1R5MG	Murata	2.0 x 1.6 x 1.0	2.0	110
MAKK2016T1R5M	Taiyo-Yuden	2.0 x 1.6 x 1.0	1.9	115
VLS201610MT-1R5N	TDK	2.0 x 1.6 x 1.0	1.4	151
1239AS-H-1R5N	TOKO	2.5 x 2.0 x 1.2	3.3	60

Capacitor Selection

The LM3248 is designed to use ceramic capacitors for input and output decoupling. Use a 10 µF capacitor for the input and approximately 10 µF actual total output capacitance. Capacitor types such as X5R and X7R are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 2 lists suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered while selecting the voltage rating and case size of the capacitor. Smaller 0402 (1005) case size capacitors are recommended for filtering. Use of multiple 2.2 µF or 1 µF capacitors can also be considered. For RF Power Amplifier applications, split the output capacitor between DC-DC converter and RF Power Amplifiers: 10 µF (COUT1) + 4.7 µF (COUT2) + 3 x 1.0 µF (COUT3) is recommended. The optimum capacitance split is application dependent, and for stability the actual total capacitance (taking into account effects of capacitor DC bias, temperature de-rating, aging and other capacitor tolerances) should target 10 µF with 2.5V DC bias (measured at 0.5 VRMS). Place all the output capacitors very close to the respective device. A high-frequency capacitor (3300 pF) is highly recommended to be placed next to COUT1.

Table 2. Suggested Capacitors and Their Suppliers

Capacitance	Model	Dimensions (mm)	Vendor
10 µF 6.3V X5R	CL05A106MQ5NUNC	1.0 x 0.5	Samsung
4.7 µF 10V X5R	GRM155R61A475M	1.0 x 0.5	Murata
1 µF 10V X5R	LWK107BJ105MV	0.8 x 1.6	Taiyo Yuden
1 µF 10V X5R	CL03A105MP3NSNC	0.61 x 0.3	Samsung
0.22 µF 6.3V X5R	C0603X5R0J224M	0.61 x 0.3	TDK
0.01 µF 6.3V X5R	C0603X5R0J103K	0.61 x 0.3	TDK
1000 pF 25V X7R	GRM033R71E102KA01D	0.61 x 0.3	Murata
100 pF 25V X7R	GRM033R71E101KA01D	0.61 x 0.3	Murata
3300 pF 6.3V X5R	C0402X5R0J332K020BC	0.41 x 0.2	TDK

PCB LAYOUT CONSIDERATIONS

Overview

PC board layout is critical to successfully designing a DC-DC converter into a product. A properly planned board layout optimizes the performance of a DC-DC converter and minimizes effects on surrounding circuitry while also addressing manufacturing issues that can have adverse impacts on board quality and final product yield.

PCB

Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. Erroneous signals could be sent to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance of the converter.

Energy Efficiency

Minimize resistive losses by using wide traces between the power components and doubling up traces on multiple layers when possible.

EMI

By its very nature, any switching converter generates electrical noise. The circuit board designer's challenge is to minimize, contain, or attenuate such switcher-generated noise. A high-frequency switching converter, such as the LM3248, switches Ampere-level currents within nanoseconds, and the traces interconnecting the associated components can act as radiating antennas. The following guidelines are offered to help to ensure that EMI is maintained within tolerable levels.

To help minimize radiated noise:

- Place the LM3248 DC-DC converter, its input capacitor, and output filter inductor and capacitor close together, and make the interconnecting traces as short as possible.
- Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the internal PFET of the LM3248 and the inductor, to the output filter capacitor, then back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the internal synchronous NFET of the LM3248 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- Make the current loop area(s) as small as possible. Interleave doubled traces with ground planes or return paths, where possible, to further minimize trace inductances.

To help minimize conducted noise in the ground-plane:

- Reduce the amount of switching current that circulates through the ground plane by connecting the ground bumps of the LM3248 and the boost output/buck input filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this copper fill to the system ground-plane by multiple vias. The multiple vias help to minimize ground bounce at the LM3248 by giving it a low-impedance ground connection.

To help minimize coupling to the DC-DC converter's own voltage feedback trace:

- Route noise sensitive traces, such as the voltage feedback path (FB_BUCK), as directly as possible from the switcher FB_BUCK pad to the VOUT pad of the output capacitor, but keep them away from noisy traces between the power components.

To help minimize noise coupled back into power supplies:

- **Use a star connection to route from the V_{BATT} power source to the LM3248 PVIN_BOOST pins and to the PA device VBATT pins.**
- Include sufficient decoupling capacitance, for both low and high frequency, at the PA V_{BATT} connections.
- Route traces for minimum inductance (short, wide connections) between supply pins and bypass capacitor(s).
- Route traces to minimize inductance between bypass capacitors and the ground plane.
- Utilize necessary power supply trace inductance(s) to reduce coupling between function blocks.
- Inserting a ferrite bead in series with the V_{BATT} power supply trace may offer a favorable tradeoff between board area and additional shunt bypass capacitors, by attenuating noise that might otherwise propagate through the supply connections.

4. LM3248 RF Evaluation Board

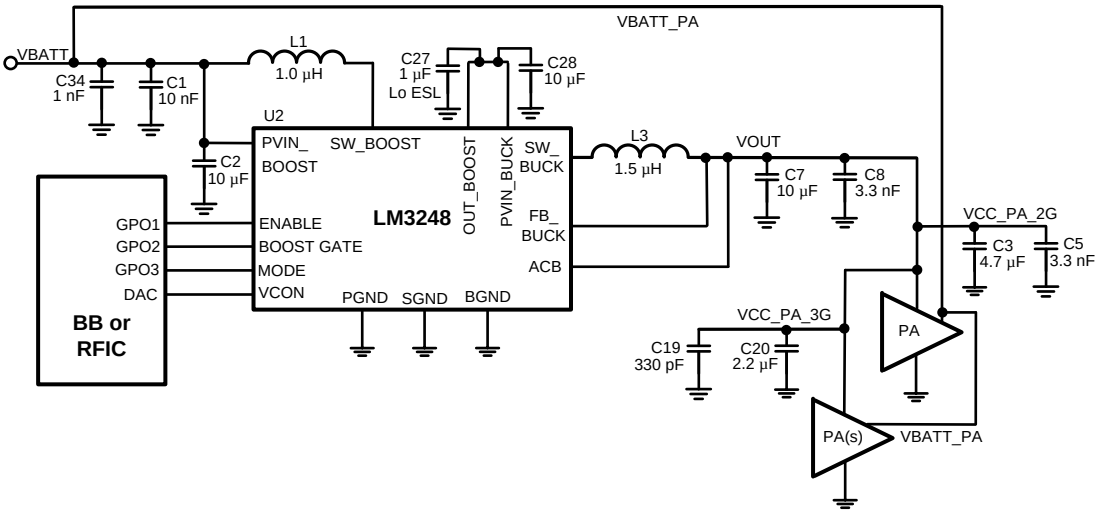


Figure 29. Simplified LM3248 RF Evaluation Board Schematic

LM3248 PCB Placement Considerations

1. Input Capacitor C2 should be placed closer to LM3248 than C1.
2. Optional to add a 1 nF (C34) capacitor on the input of LM3248 for high frequency filtering.
3. Bulk Output Capacitor C7 should be placed closer to LM3248 than C8.
4. Connect GND terminals of C7, C8 and C34 directly to System RF GND layer of phone board.
5. Connect GND terminals of boost output C27 and buck input C28 capacitors to copper PGND island on the component side. This island is then tied to the system ground layer through several vias.
6. Connect bumps SGND_BOOST(B2), SGND_BUCK(C3), DGND(E3), and BGND (F3) directly to system ground layer.
7. Small high-frequency filtering capacitors (e.g., C34) work better when they are connected to system ground instead of the PGND island. These capacitors should be 0201 (0603 metric) or 01005 (0402 metric) case size for minimum footprint and best high frequency characteristics.

RF Evaluation Board Layout Overview

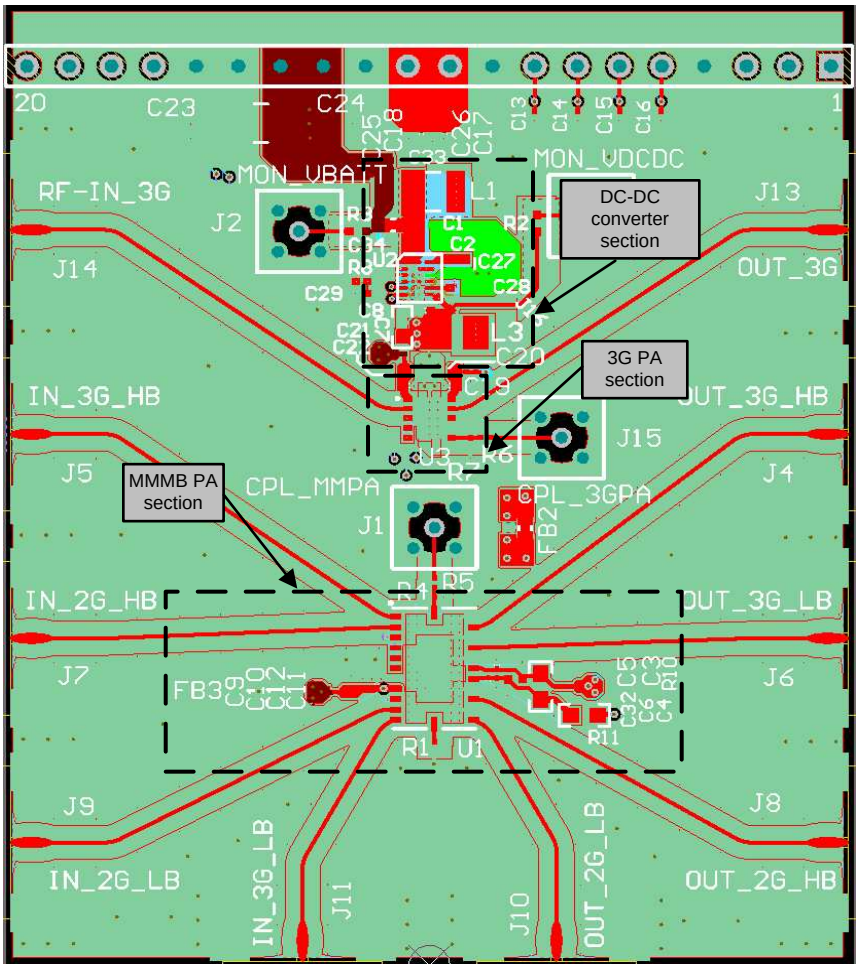


Figure 30. Top View of RF Evaluation Board

The LM3248 RF Evaluation board consists of the LM3248 DC/DC converter and two RF Power Amplifier stages – a standard 3x3 mm footprint “3G PA” and a Multi-Mode MultiBand (“MMMB PA”) 2G+3G/4G Power Amplifier. These circuits are outlined in Figure 30.

Layout Recommendations

Multi-Layer Chip-Capacitors (MLCC), rather than Tantalum, should be used in the LM3248 DC/DC converter, in order to minimize ESR effects.

One of the most important details is routing the power feed in a way that does not induce noise between the PA and DC/DC converter circuits that are connected to the common power feed. The “star connection” previously mentioned is illustrated below in Figure 31. The key is to route the power connections from the V_{BATT} power source to the PA and DC/DC converters separately, so that there is no shared current path – they only join at the power source. If this is not possible, due to other constraints, it is wise to design in pads for ferrite beads in series with the V_{BATT} connection to the device, at least in prototype layouts, so that additional filtering is available when performance is validated (see Figure 32).

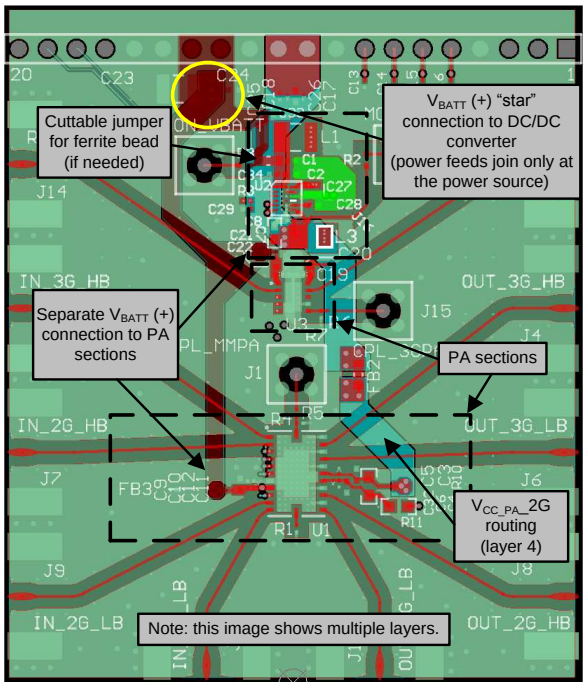


Figure 31. LM3248 V_{BATT} Star Connection and V_{CC_PA} Routing

Critical Boost Output/Buck Input Capacitors

The most critical placement and connections are the boost output/buck input filter capacitors, C27 and C28, which should be located as close as possible to the U2 LM3248 device OUT_BOOST/PVIN_BUCK and PGND pads. These two capacitors decouple the fastest (highest di/dt) switching currents in the power supply. By minimizing the connection length (inductance) between these capacitor and the LM3248 device pads, the user minimizes the noise that may propagate back into the V_{BATT} power bus. The best method to connect these components to the LM3248 is short, direct connecting traces from the capacitor pads to the device pads on the same layer (vias are resistive+inductive and impede the fast switching current flow). This is illustrated in Figure 32, below, with arrows indicating the fast circulating current flows. Note the copper PGND island, which joins the major current-carrying bypass capacitor GND terminals, C2, C27, and C28.

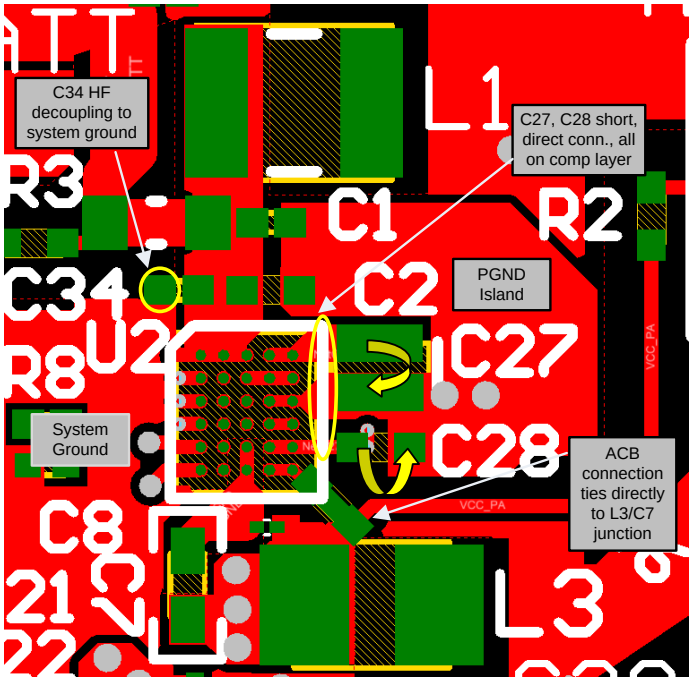


Figure 32. LM3248 Decoupling Cap Placement (Top View, Component Layer)

The V_{BATT} supply currents replenish the main decoupling caps mounted to the PGND island through the system ground by way of several vias, so that the fast switching currents are confined to the component layer. This technique reduces ground-plane noise by reducing the amount of switching current that circulates through the system ground plane. An additional high-frequency decoupling capacitor (C34, 1 nF, 0201 case size) is recommended between the main power (V_{BATT}) feed and the system ground (not to PGND) to return any common mode switching currents that appear on these surfaces.

The Active Current Assist and Bypass (ACB) trace should be kept short and routed directly from ACB pin to the junction of output inductor L3 and output capacitor C7 (see Figure 32).

Minimizing Switching Noise

Next, the boost and buck inductors, L1 and L3, should be placed so that routing will minimize exposure of the "noisy" end of each of these components to surrounding circuitry that ties directly to the SW_BUCK and SW_BOOST pins. Specifically, the FB_BUCK feedback sense connection should be routed away from the SW_BUCK (or SW_BOOST) nodes. Ideally, make a short, direct connection from the FB_BUCK pin to the junction of the output capacitor, C7, and buck output inductor, L3. This trace is a voltage sense connection and does not carry significant current (trace width is not critical). If this connection must be routed under either L1 or L3 inductors, there should be a ground layer between this trace and the noisy end of the inductor(s) to provide shielding. Connect output capacitors C7 and C8 directly to the system ground (not to the PGND copper island). In this example, C7 and C8 are routed to the Layer 3 system ground through multiple vias (see Figure 32 and Figure 33), which is acceptable, since they do not carry extremely fast (high di/dt) switching currents.

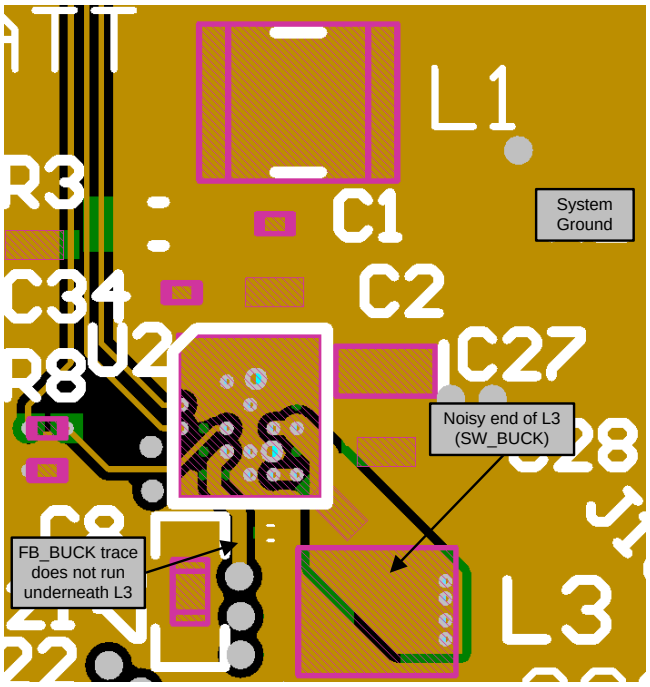


Figure 33. LM3248 Buck Feedback and Inductor L3 Routing for Low Noise (Layer 3 shown with Layer 1 Component Overlay)

The SW_BOOST routing to L1 is shown in Figure 34. Note the noisy end of inductor L1 does not cross sensitive the FB_BUCK trace, but is routed away from it.

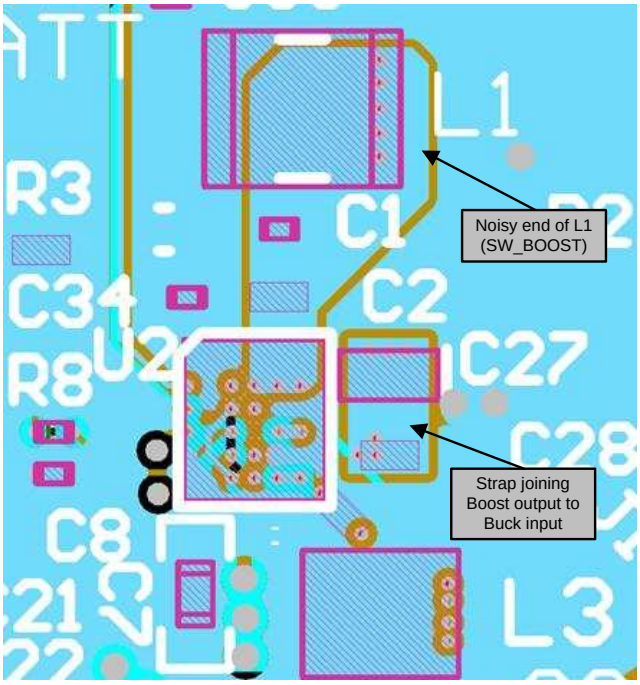


Figure 34. LM3248 Inductor L1 Routing for Low Noise (Layer 2 shown with Layer 1 Component Overlay)

REVISION HISTORY

Changes from Original (August 2013) to Revision A **Page**

- Changed Product Brief for Full Datasheet; 2 figures: Boost/Buck Output Voltage Timing Diagram and Boost Operation showing VCON-V_{BATT} Relationship 25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3248TME/NOPB	ACTIVE	DSBGA	YFQ	30	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 90	3248	Samples
LM3248TMX/NOPB	ACTIVE	DSBGA	YFQ	30	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 90	3248	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

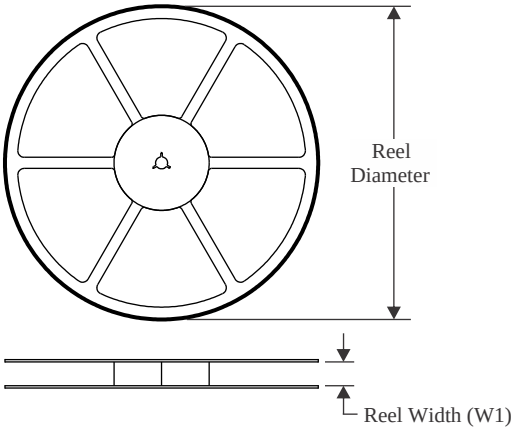
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

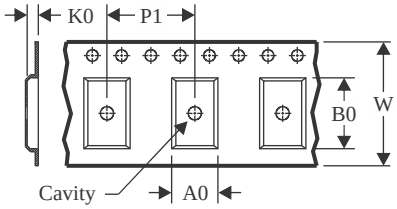
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

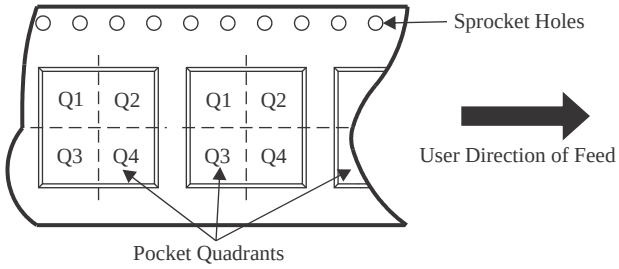


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

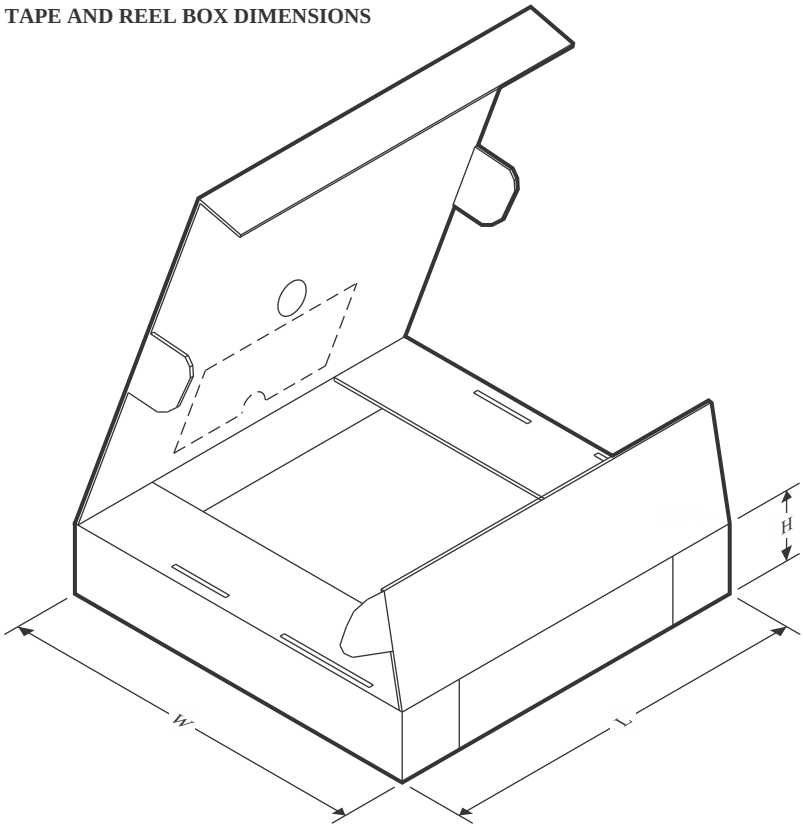
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3248TME/NOPB	DSBGA	YFQ	30	250	178.0	8.4	2.67	2.95	0.76	4.0	8.0	Q1
LM3248TMX/NOPB	DSBGA	YFQ	30	3000	178.0	8.4	2.67	2.95	0.76	4.0	8.0	Q1

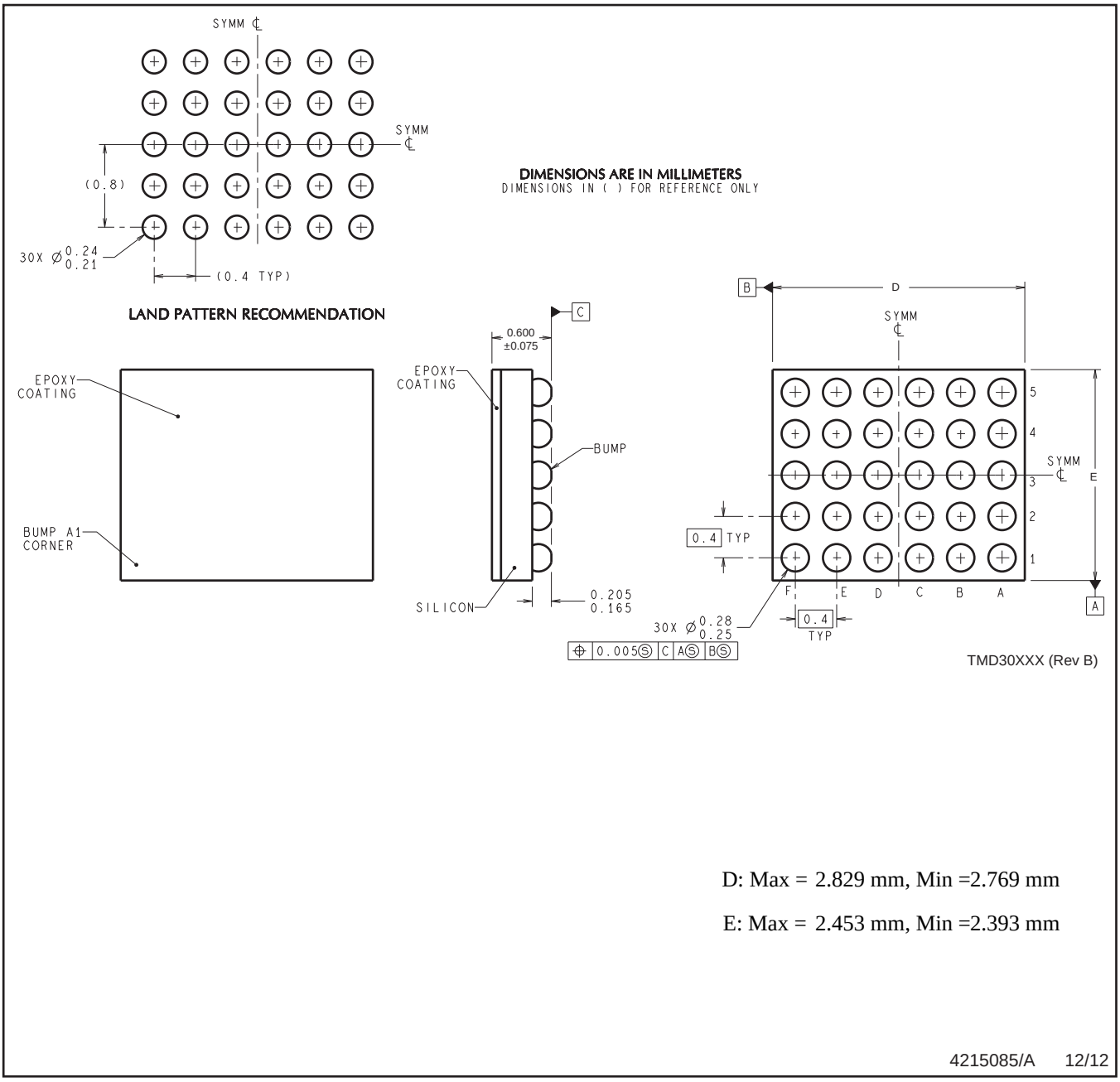
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3248TME/NOPB	DSBGA	YFQ	30	250	208.0	191.0	35.0
LM3248TMX/NOPB	DSBGA	YFQ	30	3000	208.0	191.0	35.0

YFQ0030



D: Max = 2.829 mm, Min =2.769 mm

E: Max = 2.453 mm, Min =2.393 mm

4215085/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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