

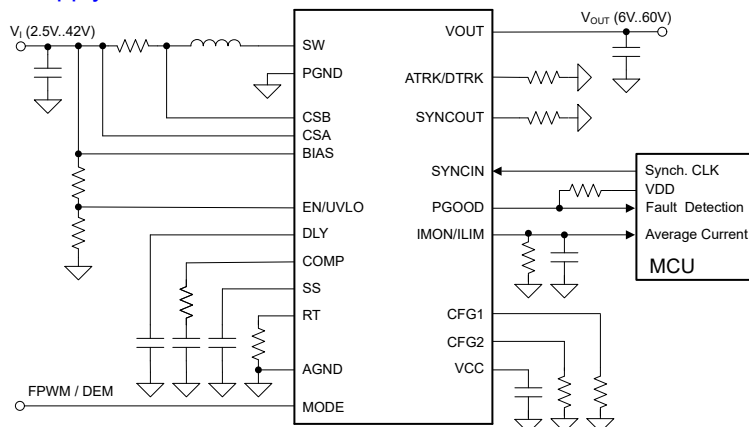
LMG5126 Wide-Input, 2.5MHz, Boost Converter

1 Features

- Input voltage 6.5V to 42V
 - Minimum 2.5V for $V_{BIAS} \geq 6.5V$ or $V_{OUT} \geq 6V$
- Output Voltage 6V to 60V
 - 2% accuracy, internal feedback resistors
 - Bypass operation for $V_I > V_{OUT}$
 - Boot refresh out of audio >20kHz
 - Dynamic output voltage tracking
 - Digital PWM tracking (DTRK)
 - Analog tracking (ATRK)
 - Over voltage protection (65V, 50V, 35V, 25V)
- Low shutdown I_{SD} of 50 μ A typ. (200 μ A max.)
- Low operating I_Q of 1.1mA typ. (2.5mA max.)
- Stacking with interleaved multiphase operation
 - Up to 4-devices without external clock
- Switching frequency from 300kHz to 2.5MHz
 - Synchronization to external clock (SYNCIN)
 - Spread Spectrum (DRSS)
- Dynamically selectable switching modes (FPWM, Diode emulation)
- Current sense resistor or DCR sensing
- Average inductor current monitor
- Average input current limit
- Selectable current limit (30mV or 60mV)
- Selectable delay time (DLY)
- Power good indicator
- Programmable V_I undervoltage lockout (UVLO)
- Lead-less RLF-22 package with wettable flanks

2 Applications

- High-end audio power supply



Typical Application

- Voltage stabilizer module
- Start-stop application

3 Description

The LMG5126 is a stackable multiphase synchronous boost converter. The device provides a regulated output voltage for lower or equal input voltage also supporting V_I to V_{OUT} bypass mode to save power. Up to 4 devices can be stacked with or without external clock.

V_{OUT} can be dynamically programmed using the digital or analog ATRK/DTRK function. V_I can be as low as 2.5V after startup as the internal VCC supply is automatically switched from V_{BIAS} to V_{OUT} for $V_{BIAS} < 6.5V$. The fixed switching frequency is set between 300kHz and 2.5MHz via a resistor on the RT-pin or the SYNCIN clock. The switching modes FPWM or Diode emulation can be changed during operation.

The implemented protections peak current limit, average input current limit, average inductor current monitor, over- and undervoltage protection or the thermal shutdown protect the device and the application.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LMG5126	22-pin VQFN-FCRLF	6mm x 4.5mm

- (1) For all available packages, see Section 10.
- (2) The package size (length x width) is a nominal value and includes pins, where applicable.



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4 Pin Configuration and Functions

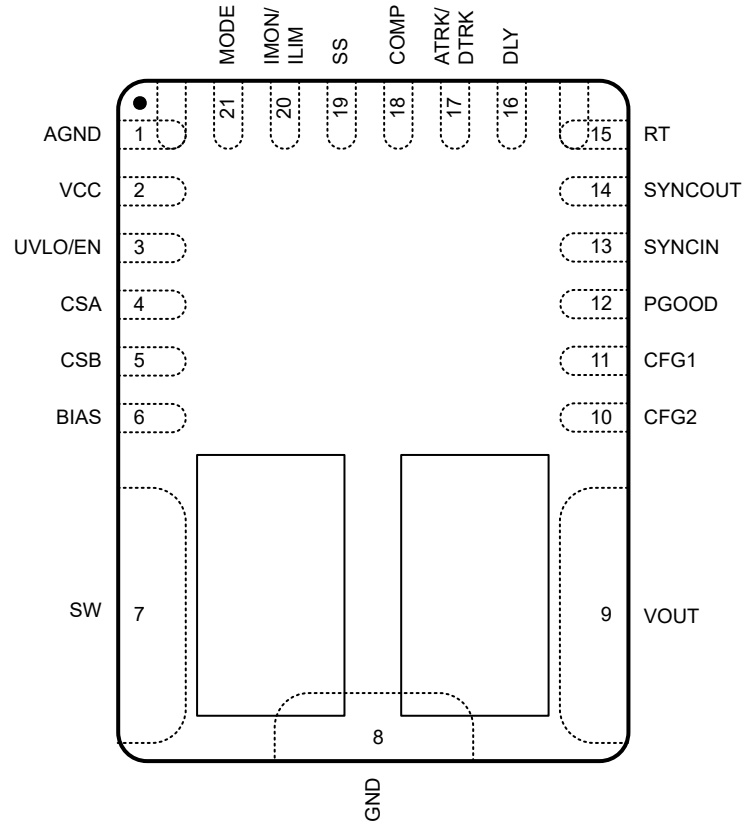


Figure 4-1. LMG5126 pin out (top view)

Table 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
AGND	1	G	Analog ground pin. Connect to the analog ground plane through a wide and short path.
VCC	2	P	Output of the internal VCC regulator and supply voltage input of the internal FET drivers. Connect a 4.7µF capacitor between the pin and GND.
UVLO/EN	3	I	Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. If greater than $V_{UVLO-RISING}$, the device is enabled.
CSA	4	I	Current sense amplifier input. The pin operates as the positive input pin. Input to the internal undervoltage lockout for the input voltage.
CSB	5	I	Current sense amplifier input. The pin operates as the negative input pin.
BIAS	6	P	Supply voltage input to the VCC regulator. Connect a 1µF local BIAS capacitor from the pin to ground.
SW	7	P	Switching node connection.
GND	8	G	Power ground connection pin for low-side FET.
VOUT	9	P	Output voltage pin. An internal feedback resistor voltage divider is connected from the pin to AGND.
CFG2	10	I	Device configuration pin. Sets if the device is configured as single, primary or secondary device using the internal or external clock and the PGOOD configuration.
CFG1	11	I	Device configuration pin. Sets the Spread Spectrum mode, 120% peak current limit latch off, sense voltage and gate drive strength.

Table 4-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
PGOOD	12	O	Power-good indicator with open-drain output stage. The pin is pulled low when the output voltage is less than the undervoltage threshold or greater than the overvoltage threshold based on the CFG2-pin setting. It is also pulled low indicating faults. The pin can be left floating if not used.
SYNCIN	13	I	External clock synchronization pin. Input for an external clock that overrides the free-running internal oscillator. Connect the SYNCIN pin to ground when it is not used.
SYNCOUT	14	O	Clock output and OVP as well as ATRK current configuration pin. SYNCOUT provides a phase shifted clock output, set by the CFG2.pin. A resistor is connected to this pin to select the LMG5126 OVP level and enable the 20µA ATRK current.
RT	15	O	Switching frequency setting pin. The switching frequency is programmed by a single resistor between the pin and AGND. Switching frequency is dynamically programmable during operation.
DLY	16	O	Average input current limit delay setting pin. A capacitor from DLY to AGND sets the delay from when V _{IMON} reaches 1V until the average input current limit is enabled.
ATRK/DTRK	17	I	Output regulation target programming pin. The output voltage regulation target can be programmed by connecting the pin through a resistor to AGND, or by controlling the pin voltage directly with a voltage in the recommended operating range of the pin from 0.2V to 2.0V. A digital PWM signal between 8% to 80% duty cycle sets the output voltage regulation in the recommended operating range.
COMP	18	O	Output of the internal transconductance error amplifier. Connect the loop compensation components between the pin and AGND.
SS	19	O	Soft-start time programming pin. An external capacitor and an internal current source set the ramp rate of the internal error amplifier reference during soft start. The device forces diode emulation during soft-start time.
IMON/ILIM	20	O	Input current monitor and average input current limit setting pin. Sources a current proportional to the differential current sense voltage. A resistor is connected from this pin to AGND.
MODE	21	I	Operation mode selection pin selecting DEM or FPWM.
EP	22	G	Exposed pad of the package. The Exposed pad must be connected to AGND and soldered to a large ground plane to reduce thermal resistance.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

ADVANCE INFORMATION

5 Specifications

Product Preview Samples

Note

The current devices marked XSE5126 have the following limitations. The next silicon sampling early Q2 2025 resolves the limitations:

Diode Emulation Mode (DEM) does not work at light load.

- Boot refreshing does not function as intended in DEM operation. Boot undervoltage event initiates low-side FET switching, but boot switch blocks boot capacitor charging. Repeated boot undervoltage trigger may cause V_{OUT} runaway. Boot refreshing does not operate in DEM therefore device cannot turn on the high-side switch at light load.
- DEM can only be used (activated) for loads high enough so boot refresh is not needed (usually for $I_{OUT} > 50\text{mA}$).
- It is recommended to keep the device in FPWM operation mode (MODE-pin = high).

High-side FET is not turning on for low inductor peak currents

- For inductor peak currents between 1A and about 5A (V_{OUT} dependant) the high side FET does not turn on causing higher losses.
- It is recommended to connect the BIAS-pin to 5V. This narrows down the peak current range where the high-side FET does not turn on.
- For efficiency measurements, it is recommended to connect the BIAS-pin to $\geq 5\text{V}$ (e.g. V_I).
 - For $V_I = 12\text{V}$ and $V_{OUT} = 24\text{V}$ a load $> 1\text{A}$ is recommended to get valid efficiency measurements.
 - For $V_I = 12\text{V}$ and $V_{OUT} = 48\text{V}$ a load $> 0.5\text{A}$ is recommended to get valid efficiency measurements.

Automatic BIAS supply switchover BIAS-pin to VOUT-pin is disabled.

- As a result BIAS-pin voltage must be $> 4.5\text{V}$.

Do not trigger thermal shutdown. Limit device temperature to 150°C max.

- The device can get damaged when thermal shutdown is triggered and a constant current load is applied. The device stops switching at thermal shutdown causing V_{OUT} to collapse to V_I . The around 2.5V reverse conduction threshold of the high-side FET then generates significant losses as the load is still applied. The high-side FET rapidly heats up and can get damaged.
- It is recommended to evaluate the device with assembled top-side heat sink only.

Do not trigger ICL latch feature as the device behaves as described for thermal shutdown.

When V_I is close to V_{OUT} (e.g. Bypass-Mode) a timing violation inside the device can happen.

- When the device operates at min t_{ON} a timing violation can cause the low-side FET to turn on but not off for one cycle. This results in cross conduction for one cycle.
- It is recommended to avoid min t_{ON} operation. The min. t_{ON} time should be $> 150\text{ns}$.

5.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise specified)⁽¹⁾

		MIN	MAX	UNIT
Input ⁽²⁾	BIAS to AGND	-0.3	50	V
	UVLO/EN to AGND	-0.3	BIAS + 0.3	
	CSA to AGND	-0.3	50	
	CSA to CSB	-0.3	0.3	
	VOUT to AGND	-0.3	75	
	SW to AGND	-5	75	
	SW to AGND (10ns)	-15		
	CFG1, CFG2, SYNCIN, ATRK/DTRK, DLY, MODE,	-0.3	5.5	
	RT to AGND	-0.3	2.5	
	GND to AGND	-0.3	0.3	
	GND to AGND (10ns)	-2	2	
Output ⁽²⁾	VCC to AGND	-0.3	5.8 ⁽³⁾	V
	PGOOD, SYNCOUT, SS, COMP, IMON/ILIM to AGND	-0.3	5.5	
Operating junction temperature, T _J ⁽⁴⁾		-40	150	°C
Storage temperature, T _{STG}		-55	150	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) It is not allowed to apply an external voltage directly to COMP, SS, RT pins.
- (3) Operating lifetime is derated when the pin voltage is greater than 5.5V.
- (4) High junction temperatures degrade operating lifetimes. Operating lifetime is derated for junction temperatures greater than 125°C.

5.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V	
		Charged-device model (CDM), per AEC Q100-011	All pins		±500
			Corner pins		±750

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over the recommended operating junction temperature range (unless otherwise specified)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _I	Boost Input Voltage (when BIAS ≥ 6.5V or V _{OUT} ≥ 6V)	2.5		42	V
V _{OUT}	Boost Output Voltage	6		60	V
V _{BIAS}	BIAS Input Voltage	6.5		42	V
V _{UVLO/EN}	UVLO/EN Input Voltage	0		42	V
V _{MODE}	MODE Input Voltage	0		5.25	V
V _{CSA, V_{CSB}}	Current Sense Input Voltage	2.5		42	V
V _{ATRK}	ATRK Input Voltage	0.2		2	V
V _{DTRK}	DTRK Input Voltage	0		5.25	V
V _{DLY}	DLY Voltage	0		5.25	V
V _{PGOOD}	PGOOD Voltage	0		5.25	V
V _{IMON/ILIM}	IMON/ILIM Voltage	0		5.25	V
V _{SYNCIN}	Synchronization Pulse Input Voltage	0		5.25	V
f _{SW}	Switching Frequency Range	300		2500 ⁽²⁾	kHz
f _{SYNCIN}	Synchronization Pulse Frequency Range	300		2500 ⁽²⁾	kHz
f _{DTRK}	DTRK Frequency Range	100		2200	kHz
T _J	Operating Junction Temperature	-40		150 ⁽³⁾	°C

- (1) *Operating Ratings* are conditions under the device is intended to be functional. For specifications and test conditions, see [Section 5.5](#)
- (2) Maximum switching frequency is programmed by R_{RT}. The device supports up to 2200kHz switching.
- (3) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMG5126	UNIT
		VQFN-FCRLF	
		22 PINS	
R _{qJA}	Junction-to-ambient thermal resistance	29.1	°C/W
R _{qJC(top)}	Junction-to-case (top) thermal resistance	1.0	°C/W
R _{qJB}	Junction-to-board thermal resistance	5.0	°C/W
γ _{JT}	Junction-to-top characterization parameter	3.7	°C/W
γ _{JB}	Junction-to-board characterization parameter	5.0	°C/W
R _{qJC(bot)}	Junction-to-case (bottom) thermal resistance	4.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application note](#).

5.5 Electrical Characteristics

Typical values correspond to T_J = 25 °C. Minimum and maximum limits apply over T_J = -40 °C to 150 °C. Unless otherwise stated, V_I = V_{BIAS} = 12 V, V_{OUT} = 24 V, f_{SW} = 400 kHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT (BIAS, VCC)					
I _{SD}	V _I current in shutdown state (BIAS connected to V _I). Current into BIAS, CSA, CSB, SW.	V _{UVLO/EN} = 0V, V _{OUT} = 12V, T _J = -40°C to 85°C	50	200	μA
I _{SD_BIAS}	BIAS-pin current in shutdown state.	V _{UVLO/EN} = 0V, V _{OUT} = 12V, T _J = -40°C to 85°C	2	5	μA
I _{SD_VOUT}	V _{OUT} -pin current in shutdown state.	V _{UVLO/EN} = 0V, V _{OUT} = 12V, T _J = -40°C to 85°C	0.001	0.5	μA
I _{Q_BIAS_FPWM}	BIAS-pin quiescent current in active state, FPWM-Mode, internal clock (not-switching, RT and IMON current is excluded).	V _{UVLO/EN} = 2.0V, CFG1 = level 10, CFG2 = level 1, V _{ATRK} = 0.8V, no load, T _J = -40°C to 125°C	1.1	2.5	mA

Typical values correspond to $T_J = 25\text{ }^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$. Unless otherwise stated, $V_I = V_{BIAS} = 12\text{ V}$, $V_{OUT} = 24\text{ V}$, $f_{SW} = 400\text{ kHz}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{Q_BIAS_DEM}$	BIAS-pin quiescent current in active state, DEM-Mode, internal clock (not-switching, RT and IMON current is excluded).	$V_{UVLO/EN} = 2.0\text{V}$, CFG1 = level 10, CFG2 = level 1, $V_{ATRK} = 0.8\text{V}$, no load, $T_J = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$		1.2	2	mA
$I_{Q_VOUT_FPWM}$	VOUT-pin quiescent current in active state, FPWM-Mode, internal clock (not-switching).	$V_{UVLO/EN} = 2.0\text{V}$, CFG1 = level 10, CFG2 = level 1, $V_{ATRK} = 0.8\text{V}$, no load, $T_J = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$		250	750	μA
$I_{Q_BIAS_BYP}$	BIAS-pin current in bypass state (RT and IMON current is excluded).	$V_{UVLO/EN} = 2.0\text{V}$, CFG1 = level 10, CFG2 = level 1, $V_{OUT} = 12\text{V}$, $T_J = -40\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$		1.5	8.5	mA
I_{BIAS}	BIAS-pin bias current when VCC is supplied by BIAS, FPWM-Mode (not-switching, RT and IMON current is excluded).	$V_{BIAS} = 12\text{V}$, $I_{VCC} = 100\text{mA}$		100	110	mA
I_{VOUT}	VOUT-pin bias current when VCC is supplied by VOUT, FPWM-Mode (not-switching).	$V_{BIAS} = 3.3\text{V}$, $I_{VCC} = 100\text{mA}$		100	110	mA
VCC REGULATORY (VCC)						
V_{BIAS_RISING}	Threshold to switch VCC supply from VOUT-pin to BIAS-pin	V_{BIAS} rising	6.0	6.25	6.5	V
$V_{BIAS_FALLING}$	Threshold to switch VCC supply from BIAS-pin to VOUT-pin	V_{BIAS} falling	5.6	5.9	6.2	V
V_{BIAS_HYS}	VCC supply threshold hysteresis		250	350		mV
V_{VCC_REG1}	VCC regulation	No load	5.1	5.3	5.5	V
V_{VCC_REG2}	VCC regulation during dropout	$V_{BIAS} = 5.9\text{V}$, $I_{VCC} = 100\text{mA}$	4.5	5.2		V
$V_{VCC_UVLO_RISING}$	VCC UVLO threshold	VCC rising	4.1	4.2	4.3	V
$V_{VCC_UVLO_FALLING}$	VCC UVLO threshold	VCC falling	3.8	3.9	4.0	V
$V_{VCC_UVLO_HYS}$	VCC UVLO threshold hysteresis	VCC falling		300		mV
I_{VCC_CL}	VCC sourcing current limit	$V_{VCC} = 4\text{V}$	100			mA
ENABLE (EN/UVLO)						
V_{EN_RISING}	Enable threshold	EN rising	0.50	0.55	0.6	V
$V_{EN_FALLING}$	Enable threshold	EN falling	0.40	0.45	0.50	V
V_{EN_HYS}	Enable hysteresis	EN falling		100		mV
R_{EN}	EN pull-down resistance	$V_{EN} = 0.2\text{V}$	30	37	50	k Ω
V_{UVLO_RISING}	UVLO threshold	UVLO rising	1.05	1.1	1.15	V
$V_{UVLO_FALLING}$	UVLO threshold	UVLO falling	1.025	1.075	1.125	V
V_{UVLO_HYS}	UVLO hysteresis	UVLO falling		25		mV
CONFIGURATION (CFG1, CFG2, SYNCOUT)						
R_{CFGx_1}	CFGx level 1 resistance			0	0.1	k Ω
R_{CFGx_2}	CFGx level 2 resistance		0.48	0.51	0.54	k Ω
R_{CFGx_3}	CFGx level 3 resistance		1	1.15	1.3	k Ω
R_{CFGx_4}	CFGx level 4 resistance		1.81	1.9	2.00	k Ω
R_{CFGx_5}	CFGx level 5 resistance		2.57	2.7	2.84	k Ω
R_{CFGx_6}	CFGx level 6 resistance		3.61	3.8	3.99	k Ω
R_{CFGx_7}	CFGx level 7 resistance		4.85	5.1	5.36	k Ω
R_{CFGx_8}	CFGx level 8 resistance		6.18	6.5	6.83	k Ω

Typical values correspond to $T_J = 25\text{ }^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$. Unless otherwise stated, $V_I = V_{BIAS} = 12\text{ V}$, $V_{OUT} = 24\text{ V}$, $f_{SW} = 400\text{ kHz}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
R _{CFGx_9}	CFGx level 9 resistance		7.89	8.3	8.72	kΩ	
R _{CFGx_10}	CFGx level 10 resistance		9.98	10.5	11.03	kΩ	
R _{CFGx_11}	CFGx level 11 resistance		12.64	13.3	13.97	kΩ	
R _{CFGx_12}	CFGx level 12 resistance		15.39	16.2	17.01	kΩ	
R _{CFGx_13}	CFGx level 13 resistance		19.48	20.5	21.53	kΩ	
R _{CFGx_14}	CFGx level 14 resistance		23.66	24.9	26.15	kΩ	
R _{CFGx_15}	CFGx level 15 resistance		28.60	30.1	31.61	kΩ	
R _{CFGx_16}	CFGx level 16 resistance		34.68	36.5	100	kΩ	
R _{SYNCOUt_1}	SYNCOUt level 1 resistance		0	24.9	26.15	kΩ	
R _{SYNCOUt_2}	SYNCOUt level 2 resistance		29.94	31.5	33.09	kΩ	
R _{SYNCOUt_3}	SYNCOUt level 3 resistance		37.92	39.9	41.91	kΩ	
R _{SYNCOUt_4}	SYNCOUt level 4 resistance		46.17	48.6	51.03	kΩ	
R _{SYNCOUt_5}	SYNCOUt level 5 resistance		58.44	61.5	64.59	kΩ	
R _{SYNCOUt_6}	SYNCOUt level 6 resistance		70.98	75	78.45	kΩ	
R _{SYNCOUt_7}	SYNCOUt level 7 resistance		85.8	90.9	94.83	kΩ	
R _{SYNCOUt_8}	SYNCOUt level 8 resistance		104.04	110	200	kΩ	
SWITCHING FREQUENCY							
V _{RT}	RT regulation		0.7	0.75	0.8	V	
f _{SW1}	Switching frequency	f _{SW} = 300kHz, RT = 104.4kΩ	255	300	345	kHz	
f _{SW2}	Switching frequency	f _{SW} = 2500kHz, RT = 12kΩ	2250	2500	2750	kHz	
t _{ON-MIN}	Minimum controllable on-time	f _{SW} = 2200kHz	14	20	50	ns	
t _{OFF-MIN}	Minimum forced off-time	f _{SW} = 2200kHz	45	65	85	ns	
D _{MAX1}	Maximum duty cycle limit	f _{SW} = 300kHz	97%	98%	99%		
D _{MAX2}	Maximum duty cycle limit	f _{SW} = 2200kHz	81%	86%	91%		
SYNCHRONIZATION (SYNCIN, SYNCOUt)							
	SYNCIN frequency activity detection threshold	Spread Spectrum = off	0		50	kHz	
	SYNCIN activity detection cycles			3		cycles	
f _{SYNC}	Syncing frequency range from RT set frequency during synchronization.	single device	Frequency synchronized to ext. clock min. = 300kHz, max. = 2500kHz.		-50%	50%	
		multi device			-25%	25%	
V _{SYNCIN_H}	SYNCIN high level input voltage		SYNCIN rising		1.19	5.25	V
V _{SYNCIN_L}	SYNCIN low level input voltage		SYNCIN falling		-0.3	0.41	V
	Minimum SYNCIN pullup / pulldown pulse width				60		ns
VOUt PROGRAMMING (ATrk/DTrk)							

Typical values correspond to $T_J = 25\text{ }^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$. Unless otherwise stated, $V_I = V_{BIAS} = 12\text{ V}$, $V_{OUT} = 24\text{ V}$, $f_{SW} = 400\text{ kHz}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V_{OUT_REG}	V_{OUT} regulation with ATRK voltage	ATRK = 0.2V	5.88	6	6.12	V		
		ATRK = 0.4V	11.82	12	12.18	V		
		ATRK = 0.8V	23.64	24	24.36	V		
		ATRK = 1.6V	47.28	48	48.72	V		
		ATRK = 2V	59.10	60	60.90	V		
G_{DTRK}	Conversion ratio of DTRK duty cycle to V_{ATRK}	$f_{DTRK} = 100\text{kHz}, 2200\text{kHz}$		25		mV / %		
	DTRK duty cycle range		8%		80%			
V_{ATRK}	ATRK voltage for given DTRK duty cycle	$f_{DTRK} = 100\text{kHz}, \text{DC} = 8\%$	0.196	0.2	0.204	V		
		$f_{DTRK} = 100\text{kHz}, \text{DC} = 40\%$	0.99	1	1.01	V		
		$f_{DTRK} = 100\text{kHz}, \text{DC} = 80\%$	1.98	2	2.02	V		
		$f_{DTRK} = 440\text{kHz}, \text{DC} = 8\%$	0.196	0.2	0.204	V		
		$f_{DTRK} = 440\text{kHz}, \text{DC} = 40\%$	0.99	1	1.01	V		
		$f_{DTRK} = 440\text{kHz}, \text{DC} = 80\%$	1.98	2	2.02	V		
		$f_{DTRK} = 2200\text{kHz}, \text{DC} = 8\%$	0.19	0.2	0.21	V		
		$f_{DTRK} = 2200\text{kHz}, \text{DC} = 40\%$	0.98	1	1.02	V		
$f_{DTRK} = 2200\text{kHz}, \text{DC} = 80\%$	1.98	2	2.02	V				
I_{ATRK}	Source current when activated through resistor setting at SYNCOUT		19.8	20	20.2	μA		
V_{DTRK_H}	DTRK high level input voltage	DTRK rising	1.19		5.25	V		
V_{DTRK_L}	DTRK low level input voltage	DTRK falling	-0.3		0.41	V		
	Minimum DTRK pull-up / pull-down pulse width		25			ns		
SOFT START (SS)								
I_{SS}	Soft-start current		42.5	50	57.5	μA		
V_{SS_DONE}	Soft-start done threshold		2.15	2.2	2.25	V		
R_{SS}	SS pulldown switch R_{DSON}			30	70	Ω		
V_{SS_DIS}	SS discharge detection threshold		20	45	70	mV		
CURRENT SENSE (CSA, CSB)								
A_{CS}	Current sense amplifier gain			10		V/V		
V_{CLTH}	Positive peak current limit threshold	60mV sensing	Referenced to CS input		54	60	66	mV
		30mV sensing			24	30	36	mV
V_{NCLTH}	Negative peak current limit threshold	60mV and 30mV sensing	Referenced to CS input, FPWM mode		-33	-30	-27	mV
V_{ICL}	Input current limit	60mV sensing	Referenced to CS input		65	72	80	mV
		30mV sensing			32.4	36	39.6	mV
	Peak current limit trip delay			50			ns	
V_{ZCD}	ZCD threshold (CSA–CSB)		CS input falling, DEM		0	1	2	mV
V_{ZCD_BYP}	ZCD threshold in bypass mode (CSA–CSB).				-3	-1.5	0	mV
V_{SLOPE}	Peak slope compensation amplitude		Referenced to CS input, $f_{SW} = 300\text{kHz}$		40	48	55	mV
I_{CSA}	CSA current		Device in Standby state, $V_I = V_{BIAS} = V_{OUT} = 12\text{V}$			150	170	μA
I_{CSB}	CSB current						1.2	μA
CURRENT MONITOR / LIMITER WITH DELAY (IMON/ILIM)								
G_{IMON}	Transconductance Gain		0.283	0.333	0.383	$\mu\text{A}/\text{mV}$		
I_{OFFSET}	Offset current		3	4	5	μA		

Typical values correspond to $T_J = 25\text{ }^\circ\text{C}$. Minimum and maximum limits apply over $T_J = -40\text{ }^\circ\text{C}$ to $150\text{ }^\circ\text{C}$. Unless otherwise stated, $V_I = V_{BIAS} = 12\text{ V}$, $V_{OUT} = 24\text{ V}$, $f_{SW} = 400\text{ kHz}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{ILIM}	ILIM regulation target		0.93	1	1.07	V	
V_{ILIM_th}	ILIM activation threshold			1		V	
V_{ILIM_reset}	DLY reset threshold	ILIM falling, referenced to V_{ILIM}	87%	90%	93%		
I_{DLY}	DLY sourcing/sinking current			5		μA	
$V_{DLY_peak_rise}$		V_{DLY} rising		2.6		V	
$V_{DLY_peak_fall}$		V_{DLY} falling		2.4		V	
V_{DLY_valley}				0.2		V	
OPERATION MODES							
V_{MODE_H}	MODE-pin high level	FPWM		1.19	5.25	V	
V_{MODE_L}	MODE-pin low level	DEM		-0.3	0.41	V	
OVER / UNDER VOLTAGE MONITOR							
V_{OVP-H}	Overvoltage threshold rising		V_{OUT} rising (referenced to error amplifier reference)	108%	110%	112%	
V_{OVP-L}	Overvoltage threshold falling		V_{OUT} falling (referenced to error amplifier reference)	101%	103%	105%	
V_{OVP_max-H}	Max. overvoltage threshold rising	25V setting	V_{OUT} rising (referenced to error amplifier reference)	23	24	25	V
		35V setting		33	34	35	V
		50V setting		48	49	50	V
		65V setting		63	64	65	V
V_{OVP_max-L}	Max. overvoltage threshold falling	25V setting	V_{OUT} falling (referenced to error amplifier reference)	22	23	24	V
		35V setting		32	33	34	V
		50V setting		47	48	49	V
		65V setting		62	63	64	V
V_{UVP-H}	Undervoltage threshold rising		V_{OUT} rising (referenced to error amplifier reference)	91%	93%	95%	
V_{UVP-L}	Undervoltage threshold falling		V_{OUT} falling (referenced to error amplifier reference)	88%	90%	92%	
PGOOD							
R_{PGOOD}	PGOOD pull-down switch R_{DSON}		1mA sinking		90	180	Ω
	Minimum BIAS for valid PGOOD			2		V	
THERMAL SHUTDOWN (TSD)							
$T_{TSD-RISING}$	Thermal shutdown threshold		Temperature rising		175		$^\circ\text{C}$
$T_{TSD-HYS}$	Thermal shutdown hysteresis				15		$^\circ\text{C}$
TIMINGS							
$STANDBY_{timer}$	STANDBY timer			130	150	170	μs

5.6 Timing Requirements

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
OVERALL DEVICE FEATURES						
	Minimum time low EN toggle	the time measured from EN toggle from high to low and low to high	1			μs

6 Detailed Description

6.1 Overview

The LMG5126 is a wide input range boost converter using integrated GaN FETs. The device provides a regulated output voltage if the input voltage is equal or lower than the adjusted output voltage. The resistor-to-digital (R2D) interface offers the user a simple and robust selection of all the device functionality.

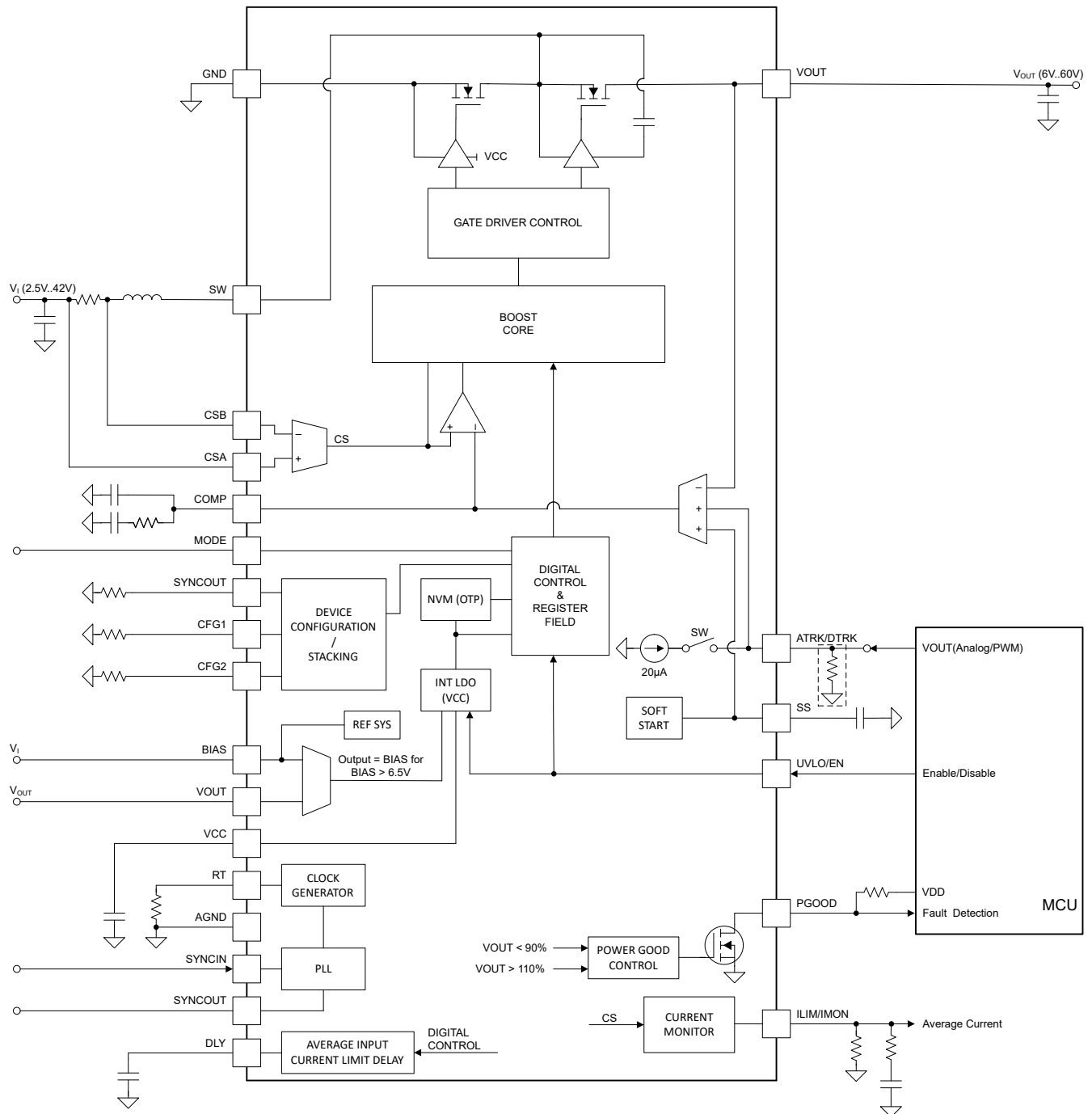
The operation modes DEM (Diode Emulation Mode) and FPWM (Forced Pulse Width Modulation) are on-the-fly pin-selectable during operation. The peak current mode control operates with fixed switching frequency set by the RT-pin. Through the activation of the dual random spread spectrum operation, EMI mitigation is achievable at any time of the design process.

The integrated average current monitor can help monitor or limit input current. The output voltage can be dynamically adjusted during operation (dynamic voltage scaling and envelope tracking). The adjustment is either possible by changing the analog reference voltage of the ATRK/DTRK-pin or the adjustment can be done directly with a PWM input signal on the ATRK/DTRK-pin.

The internal wide input LDOs provide a robust supply of the device functionality under different input and output voltage conditions. Due to the high drive capability and the automatic and headroom depended voltages selection, the power losses are kept at a minimum. The separate BIAS-pin can be connected to the input, output, or an external supply to further reduce power losses in the device. At all times, the internal supply voltage is monitored to avoid undefined failure handling.

The devices built-in protection features provide a safe operation under different fault conditions. There is a V_I undervoltage lockout protection to avoid brownout situations. Because the input UVLO threshold and hysteresis can be configured through an external feedback divider, the brownout is avoided under the different designs. The device has an output overvoltage protection. The selectable hiccup overcurrent protection avoids excessive short circuit currents by using the internal cycle-by-cycle peak current protection. Due to the integrated thermal shutdown, the device is protected against thermal damage caused by an overload condition. All output-related fault events are monitored and indicated at the open-drain PGOOD-pin of the device.

6.2 Functional Block Diagram



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6.3 Feature Description

6.3.1 Device Configuration

The CFG1-pin defines the Clock Dithering, the 120% input current limit protection (I_{CL_latch}) and max. Overvoltage Protection behavior (OVP_{max_latch}), the sense voltage and the gate driver strength. The levels shown in [Table 6-1](#) are selected by the specified resistors in [Section 5](#).

Device Clock Dithering, I_{CL_latch} & OVP_{max_latch} , Sense Voltage and Gate Drive Strength

- **Spread Spectrum:** Enables dual random spread spectrum (DRSS) clock dithering or disables clock dithering.
- **I_{CL_latch} & OVP_{max_latch} :** When I_{CL_latch} is enabled and the peak current limit is exceeded by 20% the device goes to the Shutdown State (turns off and is latched). If I_{CL_latch} is disabled the device stays active and tries to limit the inductor current at peak current limit. When OVP_{max_latch} is enabled and V_{OUT} reached the max. set OVP level the device goes to the Shutdown state (turns off and is latched).
- **Sense Voltage:** The device peak current voltage ($V_{CSA - CSB}$) at the sense resistor can be set to 30mV or 60mV.
- **Gate Drive Strength:** The internal GaN FET gate driver strength can be set to weak (slower switch node rising/falling) or strong (faster switch node rising/falling). For highest performance (efficiency), the strong setting can be used, while for lowest EMI or not optimized PCB layout the weak setting is the better choice.
- **SYNCIN:** Defines if the clock syncing function at the SYNCIN-pin is active (on) or disabled (off). The device is only syncing to an external clock applied to the SYNCIN-pin when SYNCIN is active.
- **Clock Dithering:** In case the internal oscillator is used the clock dithering is set according to the CFG1-pin setting Clock Dithering Mode. When an external clock is used the clock dithering function is disabled ignoring the CFG1-pin setting.

Table 6-1. CFG1-pin Settings

Level	Spread Spectrum	I_{CL_latch} & OVP_{max_latch}	Sense Voltage	Gate Drive Strength
1	on	on	30mV	weak
2	on	on	60mV	weak
3	on	on	30mV	strong
4	on	on	60mV	strong
5	on	off	30mV	weak
6	on	off	60mV	weak
7	on	off	30mV	strong
8	on	off	60mV	strong
9	off	on	30mV	weak
10	off	on	60mV	weak
11	off	on	30mV	strong
12	off	on	60mV	strong
13	off	off	30mV	weak
14	off	off	60mV	weak
15	off	off	30mV	strong
16	off	off	60mV	strong

The CFG2-pin defines both the power good pin OVP behavior and if the device uses the internal clock generator or an external clock applied at the SYNCIN-pin. Additionally, the CFG2-pin configures if the device is used as a single device or part of a multi device configuration, the SYNCIN and SYNCOUT-pin is enabled/disabled accordingly. During clock synchronization the clock dither function is disabled. The levels shown in [Table 6-2](#) are selected by the specified resistors in [Section 5](#).

PGOOD_{OVP_enable}, Single / Multichip, SYNCIN, SYNCOUT and Clock Dithering

- **PGOOD_{OVP_enable}:** When PGOOD_{OVP_enable} is enabled the PGOOD-pin is pulled low for V_{OUT} above OVP (Over Voltage Protection) or below the UV (Under Voltage) threshold. If PGOOD_{OVP_enable} is disabled the PGOOD-pin is only pulled low when V_{OUT} is below UV (Under Voltage) threshold.
- **Single or Multichip:** Defines if the device is used stand-alone (single) using the internal oscillator or an external clock. When SYNCIN is on the clock signal applied at SYNCIN is used. In case no clock is applied or the clock is stopped the device switches to the internal oscillator.
- **Primary:** Device is used as primary device acting as a controller in a multi device configuration using the internal oscillator when no clock is applied at SYNCIN-pin. At the SYNCOUT-pin a phase shifted clock (90°, 120° or 180°) is generated for the next device.
- **Secondary:** Device is used as secondary device syncing the clock to the SYNCIN-pin signal. At the SYNCOUT-pin a phase shifted clock (90° or 120°) can be generated for the next device.

Table 6-2. CFG2-pin Settings

Level	PGOOD _{OVP_enable}	Single / Multichip	SYNCIN	SYNCOUT	Clock Dithering
1	on	Single int. clock	off	off	CFG1-pin
2	on	Single ext. clock	on	off	off
3	on	Primary	on	90°	off
4	on	Primary	on	120°	off
5	on	Primary	on	180°	off
6	on	Secondary	on	off	off
7	on	Secondary	on	90°	off
8	on	Secondary	on	120°	off
9	off	Single int. clock	off	off	CFG1-pin
10	off	Single ext. clock	on	off	off
11	off	Primary	on	90°	off
12	off	Primary	on	120°	off
13	off	Primary	on	180°	off
14	off	Secondary	on	off	off
15	off	Secondary	on	90°	off
16	off	Secondary	on	120°	off

The SYNCOUT-pin is used at startup to define the V_{OUT} Over Voltage Protection level (OVP_{max}) and the 20µA ATRK-pin current. When V_{OUT} is programmed by resistor the 20µA ATRK-pin current must be on, for voltage tracking current must be off. The levels shown in [Table 6-3](#) are selected by the specified resistors in [Section 5](#).

OVP, Spread Spectrum, Peak Current Limit Latch, Power Good Pin Behavior

- **OVP_{max}:** Sets the V_{OUT} max. overvoltage protection level to 25V, 35V, 50V or 65V.
- **20µA ATRK-pin current:** Enables and disables the 20µA ATRK-pin current.

Table 6-3. SYNCOUT-pin Settings

Level	OVP _{max}	20µA ATRK-pin current
1	25V	on
2	25V	off
3	35V	on
4	35V	off
5	50V	on
6	50V	off
7	65V	on

Table 6-3. SYNCOUT-pin Settings (continued)

Level	OVP _{max}	20µA ATRK-pin current
8	65V	off

6.3.2 Switching Frequency and Synchronization (SYNCIN)

The switching frequency of 300kHz to 2.5MHz is set by the RT resistor connected between the RT-pin and AGND. The RT resistor must be selected between 12kΩ and 100kΩ according to [Figure 6-1](#). If configured to use an external clock the device can synchronize the switching frequency to an external clock applied at the SYNCIN-pin. For single device configuration within ±50% of the set frequency by the RT-pin, in multi device configuration within ±25%. The internal clock is synchronized at the rising edge of the external clock signal applied at the SYNCIN-pin. The CFG1-pin Spread Spectrum setting is ignored during frequency synchronization and clock dithering is disabled.

The device always starts with the internal clock and starts synchronizing to an applied external clock during the START PHASE and the ACTIVE state (see). The device synchronizes to the external clock as soon as the clock is applied and switches back to the internal clock in case the external clock stops.

$$F_{SW} = \frac{1}{\frac{R_{RT} \times s}{31.5 \text{ G}\Omega} + 18 \text{ ns}} \quad (1)$$

$$R_{RT} = \left(\frac{1}{F_{SW}} - 18 \text{ ns} \right) \times 31.5 \frac{\text{G}\Omega}{\text{s}} \quad (2)$$

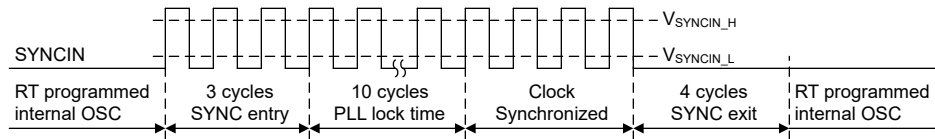


Figure 6-1. Clock Synchronization

6.3.3 Dual Random Spread Spectrum (DRSS)

The device provides a digital spread spectrum, which reduces the EMI of the power supply over a wide frequency range. This function can be enabled by the CFG1-pin. When the spread spectrum is enabled, the internal modulator dithers the internal clock. When the device is configured to use an external clock applied at the SYNCIN-pin, the internal spread spectrum is disabled. DRSS combines a low frequency triangular modulation profile with a high frequency cycle-by-cycle random modulation profile. The low frequency triangular modulation improves performance in lower radio frequency bands (for example AM band), while the high frequency random modulation improves performance in higher radio frequency bands (for example FM band). In addition, the frequency of the triangular modulation is further modulated randomly to reduce the likelihood of any audible tones. To minimize output voltage ripple caused by spread spectrum, duty cycle is modified on a cycle-by-cycle basis to maintain a nearly constant duty cycle when dithering is enabled.

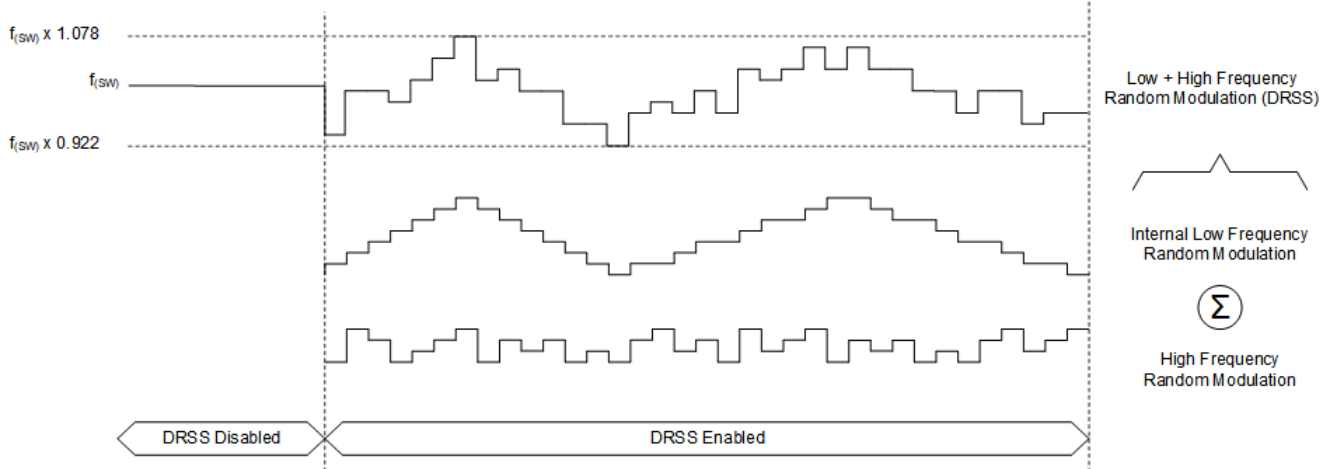


Figure 6-2. Dual Random Spread Spectrum

6.3.4 Operation Modes (BYPASS, DEM, FPWM)

The device supports bypass mode, forced PWM (FPWM) and diode emulation mode (DEM) operation. The mode can be changed on the fly and is set by the MODE-pin. Bypass mode is automatically activated for $V_{OUT} < V_I$. In multi-device stacked operation all devices must use the same mode.

The device operation mode is set to DEM for $V_{MODE} < 0.4V$ and to FPWM for $V_{MODE} > 1.2V$.

Table 6-4. Mode-pin Settings

Operation Mode	MODE-pin
DEM	$V_{MODE} < 0.4V$
FPWM	$V_{MODE} > 1.2V$

Details about the different operation modes are described in table Table 6-5.

Table 6-5. Operation Modes

Operation Mode	Description
BYPASS	V_I is connected to V_{OUT} (no regulation) while current flow from V_{OUT} to V_I is prevented for DEM selection and limited to V_{NCLTH} for FPWM selection.
DEM	Current flow from V_{OUT} to V_I is prevented. The SW-pin voltage is monitored during the high-side on time and the high-side switch is turned off when the voltage falls below the zero current detection threshold V_{ZCD} . This improves light load efficiency.
FPWM	Converter keeps switching also for light load with fixed frequency in continuous conduction mode (CCM) for best light load transient response.

The device enters and exits Bypass mode when the conditions in table Table 6-6 are met.

Table 6-6. Bypass Mode Entry, Exit

Operation Mode	Bypass	Conditions
DEM / FPWM	Entry	$V_{OUT} < V_I - 100mV$ and $V_{COMP} < V_{COMP-MIN} + 100mV$
DEM	Exit	$V_{COMP} > V_{COMP-MIN} + 100mV$ $((V_{CSP1} - V_{CSN1}) < V_{ZCD_BYP} (V_{CSP2} - V_{CSN2}) < V_{ZCD_BYP})$
FPWM	Exit	$V_{COMP} > V_{COMP-MIN} + 100mV$ $((V_{CSP1} - V_{CSN1}) < V_{NCLTH} (V_{CSP2} - V_{CSN2}) < V_{NCLTH})$

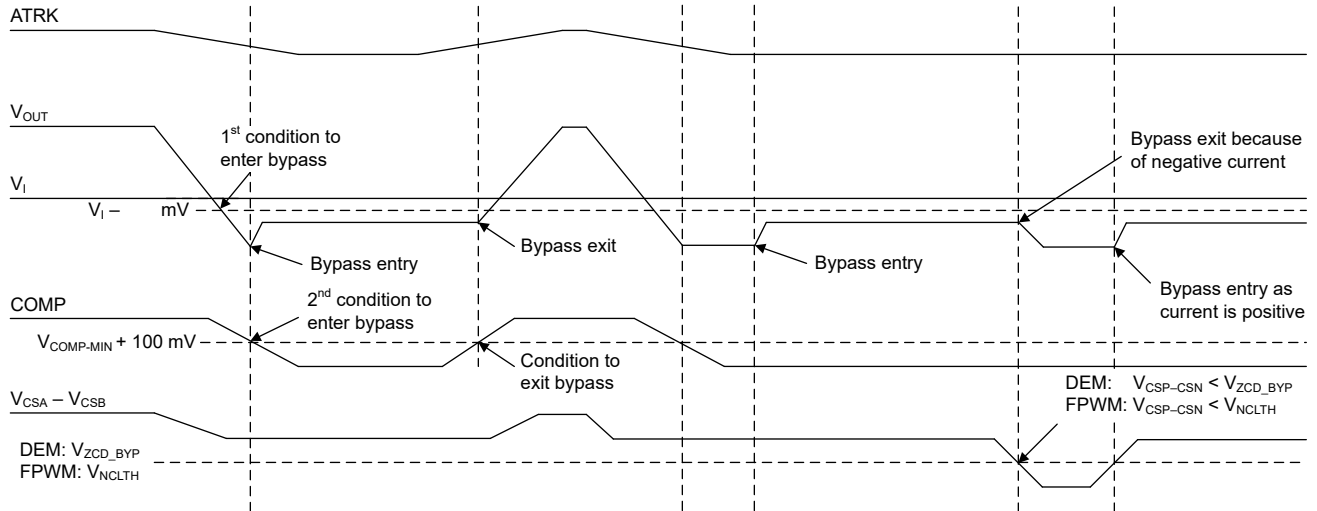


Figure 6-3. Bypass Mode Entry, Exit

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6.4 Device Functional Modes

The different operation modes are shown in the [Functional State Diagram](#).

- (1) : Does not include BOOT, READ CONFIGURATION, THERMAL SHUTDOWN, VCC CHECK, and FAULT LATCH state.
- (2) : GND for $V_{BIAS} > 1.7\text{ V}$, HIZ for $V_{BIAS} < 1.7\text{ V}$.
- (3) : Bypass = active is generated by $V_{OUT} < (V_1 + 100\text{ mV})$ & $COMP < COMP_SKIP_TH$ while bypass = inactive is generated by $COMP > COMP_SKIP_TH$
- (4) : ATRK/DTRK function (resistor, analog, digital) is detected during STANDBY state and latched at the transition to the START state.
- (5) .SYNCOUT = LOW for single device configuration.

|| : logic OR
& : logic AND
! : logic NOT
TSD : Thermal Shutdown
①②③ : Priority

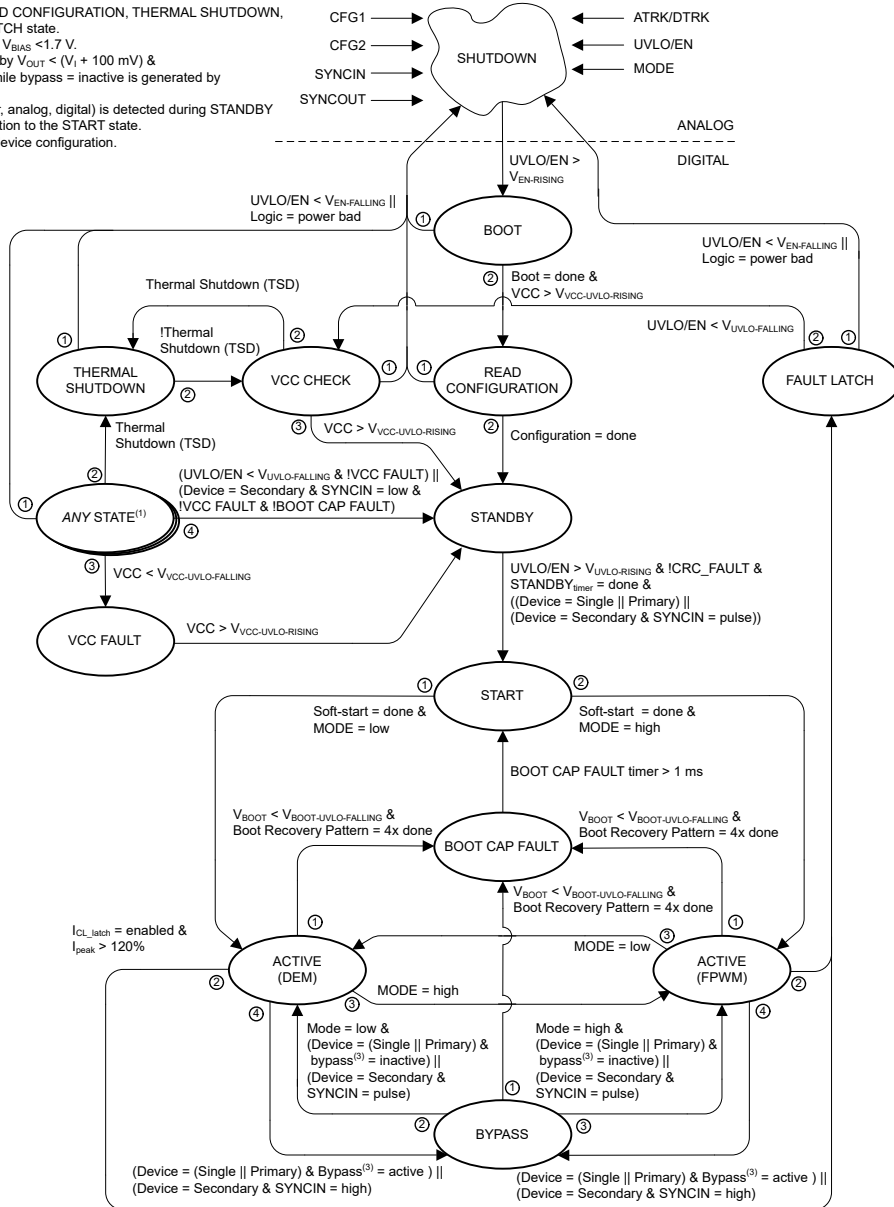
THERMAL SHUTDOWN	
Output stage	= OFF
VCC	= OFF
CFGx	= OFF
PGOOD	= GND
STANDBY _{timer}	= RESET
SYNCOUT	= LOW

VCC CHECK	
Output stage	= OFF
VCC	= ON
CFGx	= OFF
PGOOD	= GND
SYNCOUT	= LOW

VCC FAULT	
Output stage	= ON
VCC	= ON
PGOOD	= GND
Operation Mode	= no switching
STANDBY _{timer}	= ON
SYNCOUT	= LOW

BOOT CAP FAULT	
Output stage	= ON
VCC	= ON
PGOOD	= GND
Operation Mode	= no switching
BOOT CAP FAULT timer	= start
SYNCOUT	= LOW

BYPASS	
Output stage	= ON
VCC	= ON
PGOOD	= HIZ
Operation Mode	= BYPASS
SYNCOUT	= HIGH ⁽⁵⁾



SHUTDOWN	
Output stage	= OFF
VCC	= OFF
CFGx/SYNCOUT	= RESET
PGOOD	= GND ⁽²⁾
SYNCOUT	= HIZ

BOOT	
Read OTP	= ON
Output stage	= OFF
VCC	= ON
CFGx	= OFF
PGOOD	= GND
SYNCOUT	= LOW

READ CONFIGURATION	
Read OTP	= OFF
Output stage	= OFF
VCC	= ON
CFGx/SYNCOUT	= READ
PGOOD	= GND
STANDBY _{timer}	= RESET
SYNCOUT	= current

FAULT LATCH	
Output stage	= OFF
VCC	= OFF
PGOOD	= GND
STANDBY _{timer}	= RESET
SYNCOUT	= LOW

STANDBY	
Output stage	= ON
VCC	= ON
CFGx	= OFF
PGOOD	= GND
Operation Mode	= no switching
ATRK/DTRK Mode	= detect ⁽⁴⁾
STANDBY _{timer}	= ON
SYNCOUT	= LOW

START	
Output stage	= ON
VCC	= ON
CFGx	= OFF
PGOOD	= GND
Operation Mode	= DEM
ATRK/DTRK Mode	= latched ⁽⁴⁾
SYNCOUT	= pulse ⁽⁵⁾

ACTIVE	
Output stage	= ON
VCC	= ON
PGOOD	= HIZ
Operation Mode	= DEM/FPWM
ATRK/DTRK Mode	= latched ⁽⁴⁾
SYNCOUT	= pulse ⁽⁵⁾

Figure 6-4. Functional State Diagram

6.4.1 Shutdown State

The device shuts down for UVLO/EN pin = low consuming 2µA from the BIAS pin and 48µA from the pins connected to V_1 . In shutdown, COMP, SS, and PGOOD are grounded. The VCC regulator is disabled.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The device integrates several optional features to meet system design requirements, including input UVLO, programmable soft-start time, clock synchronization, spread spectrum, Average input current regulation, inductor current monitoring, 5V compatible BIAS pin for enhanced thermal capability, cold crank support, synchronization and dynamic output voltage tracking.

7.1.1 Feedback Compensation

The open-loop response of a boost regulator is defined as the product of modulator transfer function and feedback transfer function. When plotted on a dB scale, the open loop gain is shown as the sum of modulator gain and feedback gain. The modulator transfer function of a current mode boost regulator including a power stage transfer function with an embedded current loop can be simplified as one pole, one zero, and one right-half-plane zero (RHPZ) system.

Modulator transfer function is defined as follows:

$$\frac{\hat{v}_{out}}{\hat{v}_{comp}} = A_M \times \frac{\left(1 + \frac{s}{\omega_{Z_ESR}}\right)\left(1 - \frac{s}{\omega_{RHPZ}}\right)}{1 + \frac{s}{\omega_{P_LF}}} \quad (3)$$

where

- Modulator DC gain $A_M = \frac{R_{out} \times D'}{2 \times A_{cs} \times R_{cs_eq}}$
- Load pole $\omega_{P_LF} = \frac{2}{R_{out} \times C_{out}}$
- ESR zero $\omega_{Z_ESR} = \frac{1}{R_{ESR} \times C_{out}}$
- RHPZ $\omega_{RHPZ} = \frac{R_{out} \times D'^2}{L_{m_eq}}$
- The equivalent load resistance $R_{out} = \frac{v_{out}^2}{P_{out_total}}$
- The equivalent inductance $L_{m_eq} = \frac{L_m}{N_p}$
- The equivalent current sense resistor $R_{cs_eq} = \frac{R_{cs}}{N_p}$
- N_p is the number of the phases.

If the equivalent series resistance (ESR) of C_{out} (R_{ESR}) is small enough and the RHPZ frequency is far away from the target crossover frequency, the modulator transfer function can be further simplified to a one pole system and the voltage loop can be closed with only two loop compensation components, R_{COMP} and C_{COMP} , leaving a single pole response at the crossover frequency. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

As shown in [Figure 7-1](#), a g_m amplifier is utilized as the output voltage error amplifier. The feedback transfer function includes the feedback resistor divider gain and loop compensation of the error amplifier. R_{COMP} , C_{COMP} , and C_{HF} configure the error amplifier gain and phase characteristics, create a pole at origin, a low frequency zero and a high frequency pole.

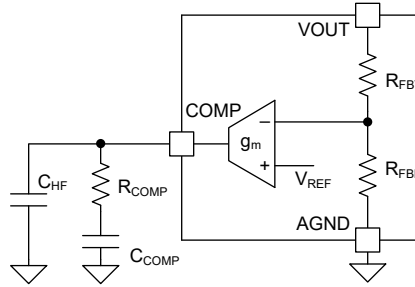


Figure 7-1. Type II g_m amplifier compensation

Feedback transfer function is defined as follows:

$$-\frac{\hat{v}_{\text{comp}}}{\hat{v}_{\text{out}}} = \frac{A_{VM} \times \omega_{Z_EA}}{s} \times \frac{1 + \frac{s}{\omega_{Z_EA}}}{1 + \frac{s}{\omega_{P_EA}}} \quad (4)$$

where

- The middle-band voltage gain $A_{VM} = K_{FB} \times g_m \times R_{COMP}$
- The feedback resistor divider gain $K_{FB} = \frac{R_{FBB}}{R_{FBT} + R_{FBB}}$. $K_{FB} = \frac{1}{30}$ for the internal feedback resistor divider.
- Low frequency zero $\omega_{Z_EA} = \frac{1}{R_{COMP} \times C_{COMP}}$
- High frequency pole $\omega_{P_EA} \approx \frac{1}{R_{COMP} \times C_{HF}}$

The pole at the origin minimizes the output steady state error. Place the low frequency zero to cancel the load pole of the modulator. The high frequency pole can be used to cancel the zero created by the output capacitor ESR or to decrease noise susceptibility of the error amplifier. By placing the low frequency zero an order of magnitude less than the crossover frequency, the maximum amount of phase boost can be achieved at the crossover frequency. The high frequency pole should be placed beyond the crossover frequency since the addition of C_{HF} adds a pole in the feedback transfer function.

The crossover frequency (open loop bandwidth) is usually limited to one fifth of the RHPZ frequency.

For higher crossover frequency, R_{COMP} can be increased, while proportionally decreasing C_{COMP} . Conversely, decreasing R_{COMP} while proportionally increasing C_{COMP} , results in lower bandwidth while keeping the same zero frequency in the feedback transfer function.

7.2 Typical Application

7.2.1 Application

A typical application example is a single-phase boost converter as shown in [Figure 7-2](#). This converter is designed for Class-H audio amplifier. The output voltage is adjustable up to 60V.

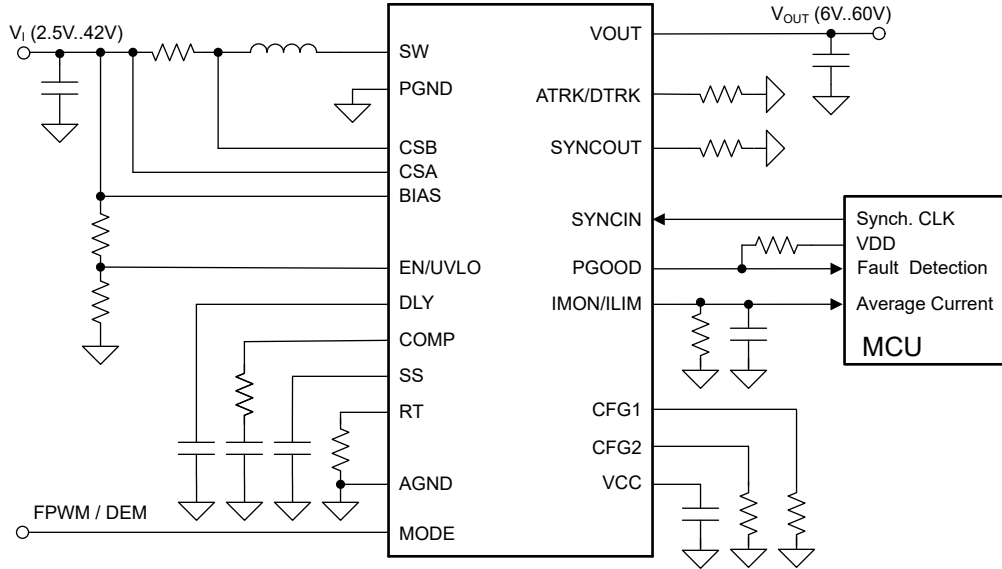


Figure 7-2. Schematic of single-phase Boost Converter

7.2.2 Design Requirements

Table 7-1. Design Parameters

PARAMETER	VALUE
Minimum input voltage V_{in_min}	9V
Typical input voltage V_{in_typ}	12
Maximum input voltage V_{in_max}	18V
Output voltage V_{out}	24V
Maximum output power	350W

7.2.3 Detailed Design Procedure

7.2.3.1 Determining the Duty Cycle

In CCM, The duty cycle is defined as:

$$D = \frac{V_{out} - V_{in}}{V_{out}} \quad (5)$$

$$D' = 1 - D \quad (6)$$

In this application The max duty cycle can be found as:

$$D_{max} = \frac{V_{out} - V_{in_min}}{V_{out_max}} = 0.625 \quad (7)$$

7.2.3.2 Timing Resistor R_T

Generally, higher switching frequency (f_{sw}) leads to smaller size and higher losses. Operation around 400kHz is a reasonable compromise considering size, efficiency and EMI. The value of R_T for 400kHz switching frequency is calculated as follows:

$$R_T = \left(\frac{1}{f_{sw}} - 18ns \right) \times 31.5 \frac{\Omega}{ns} = 78.2k\Omega \quad (8)$$

A standard value of 78.7kΩ is chosen for R_T.

7.2.3.3 V_{out} Programming

For fixed output voltage, V_{OUT} can be programmed by connecting a resistor to ATRK/DTRK and turn on precise internal 20μA current source.

$$R_{\text{ATRK}} = \frac{V_{\text{out_max}}}{6\text{V}} \times 10\text{k}\Omega = 100\text{k}\Omega \quad (9)$$

For class-H audio application, V_{out} can be adjusted to optimize the efficiency. Analog tracking or digital tracking can be applied with ATRK/DTRK.

For analog tracking, apply a voltage to ATRK/DTRK to program V_{out}. The voltage can be found as:

$$V_{\text{ATRK_max}} = \frac{V_{\text{out_max}}}{30} = 2\text{V} \quad (10)$$

$$V_{\text{ATRK_min}} = \frac{V_{\text{out_min}}}{30} = 0.8\text{V} \quad (11)$$

The output voltage can also be programmed by digital PWM signal (DTRK). The duty cycle D_{TRK} can be found as:

$$D_{\text{TRK}} = \frac{V_{\text{out_max}}}{0.75\text{V}} \times 100\% = 80\% \quad (12)$$

$$D_{\text{TRK_min}} = \frac{V_{\text{out_min}}}{0.75\text{V}} \times 100\% = 32\% \quad (13)$$

Make sure the DTRK frequency is between 100kHz and 2200kHz.

A two stage RC filter with offset can be utilized to convert a digital PWM signal to analog voltage as shown in Figure 7-3.

The two stage RC filter is used to filter the PWM signal into a smooth analog voltage. The two stage RC filter is selected considering voltage ripple and rise time on ATRK/DTRK.

Pullup resistor (R_{PU}) and pulldown resistor (R_{PD}) are utilized to add an offset voltage to ATRK/DTRK so that 100% PWM duty cycle sets the output voltage to V_{out_max} and 0% PWM duty cycle sets the output voltage to V_{out_min}.

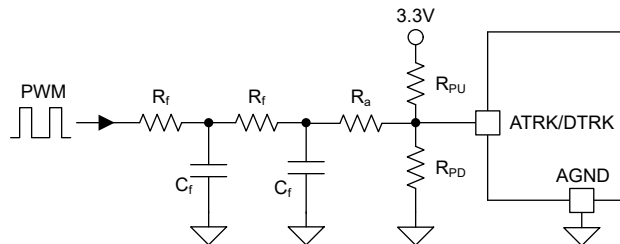


Figure 7-3. Two Stage RC Filter to ATRK/DTRK

7.2.3.4 Inductor Selection L_m

Three main parameters are considered when selecting the inductance value: inductor current ripple ratio (RR), falling slope of the inductor current and the RHPZ frequency of the control loop.

- The inductor current ripple ratio is selected to balance the winding loss and core loss of the inductor. As the ripple current increases the core loss increases and the copper loss decreases.
- The falling slope of the inductor current should be small enough to prevent sub-harmonic oscillation. A larger inductance value results in a smaller falling slope of the inductor current.

- The RHPZ should be placed at high frequency, allowing a higher crossover frequency of the control loop. As the inductance value decrease the RHPZ frequency increases.

According to peak current mode control theory, the slope of the slope compensation ramp must be greater than half of the sensed inductor current falling slope to prevent subharmonic oscillation at high duty cycle, that is:

$$V_{\text{slope}} \times f_{\text{sw}} > \frac{V_{\text{out_max}} - V_{\text{in_min}}}{2 \times L_m} \times R_{\text{cs}} \quad (14)$$

where

- V_{slope} is a 48mV peak (at 100% duty cycle) slope compensation ramp at the input of the current sense amplifier.

The lower limit of the inductance can be found as:

$$L_m > \frac{V_{\text{out_max}} - V_{\text{in_min}}}{2 \times V_{\text{slope}} \times f_{\text{sw}}} \times R_{\text{cs}} \quad (15)$$

It can be estimated $R_{\text{cs}}=1.5\text{m}\Omega$, it can be found:

$$L_m > 1.9\mu\text{H} \quad (16)$$

The RHPZ frequency can be found as:

$$\omega_{\text{RHPZ}} = \frac{R_{\text{out}} \times D^2}{L_{m_eq}} \quad (17)$$

The crossover frequency should be lower than 1/5 of RHPZ frequency :

$$f_c < \frac{1}{5} \times \frac{\omega_{\text{RHPZ}}}{2\pi} \quad (18)$$

Assume a crossover frequency of 1kHz is desired, the upper limit of the inductance can be found as:

$$L_m < 7.4\mu\text{H} \quad (19)$$

The inductor ripple current is typically set between 30% and 70% of the full load current, known as a good compromise between core loss and winding loss of the inductor.

Per phase input current can be calculated as:

$$I_{\text{in_vinmax}} = \frac{P_{\text{out}}}{V_{\text{in_max}}} = 19.44\text{A} \quad (20)$$

In continuous conduction mode (CCM) operation, the maximum ripple ratio occurs at a duty cycle of 33%. The input voltage that result in a maximum ripple ratio can be found as:

$$V_{\text{in_RRmax}} = V_{\text{out_max}} \times (1 - 0.33) = 40\text{V} \quad (21)$$

Thus, the maximum input voltage $V_{\text{in_max}}$ should be used to calculate the maximum ripple ratio.

For this example, a ripple ratio of 0.4, 40% of the input current was chosen. Knowing the switching frequency and the typical output voltage, the inductor value can be calculated as follows:

$$L_m = \frac{V_{\text{in_max}}}{I_{\text{in}} \times \text{RR}} \times \frac{1}{f_{\text{sw}}} \times \left(1 - \frac{V_{\text{in_max}}}{V_{\text{out_max}}}\right) = \frac{18\text{V}}{19.44\text{A} \times 0.4} \times \frac{1}{400\text{kHz}} \times 0.7 = 4\mu\text{H} \quad (22)$$

The closest standard value of 3.3 μH was chosen for L_m .

The inductor ripple current at typical input voltage can be calculated as:

$$I_{pp} = \frac{V_{in_typ}}{L_m} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in_typ}}{V_{out}}\right) = 4.5A \quad (23)$$

If a ferrite core inductor is selected, make sure the inductor will not saturate at peak current limit. The inductance of a ferrite core inductor is almost constant until saturation. Ferrite core has low core loss with a big size.

For powder core inductor, the inductance decreases slowly with increased DC current. This will lead to higher ripple current at high inductor current. For this example, the inductance drops to 70% at peak current limit compared to 0A. The current ripple at peak current limit can be found as:

$$I_{pp_bias} = \frac{V_{in_typ}}{0.7 \times L_m} \times \frac{1}{f_{sw}} \times \left(1 - \frac{V_{in_typ}}{V_{out}}\right) = 6.5A \quad (24)$$

7.2.3.5 Output Capacitor C_{out}

The output capacitors smooth the output voltage ripple and provide a source of charge during load transient conditions.

Ripple current rating of output capacitor must be carefully selected. In boost regulator, the output is supplied by discontinuous current and the ripple current requirement is usually high. In practice, the ripple current requirement can be dramatically reduced by placing high-quality ceramic capacitors earlier than the bulk aluminum capacitors close to the power switches.

The output voltage ripple is dominated by ESR of the output capacitors. Paralleling output capacitor is a good choice to minimize effective ESR and split the output ripple current into capacitors.

The single phase boost output RMS ripple current can be expressed as:

$$I_{1p_rms} \approx I_{out} \times \sqrt{\frac{D}{D'}} \quad (25)$$

The output RMS current is reduced with interleaving as shown in Figure 7-4. Dual phase interleaved boost output RMS ripple current can be expressed as:

$$I_{out_2p_rms} \approx \begin{cases} \frac{I_{out}}{\sqrt{2}} \times \sqrt{\frac{D \times (1-2D)}{D'}}, & D < 0.5 \\ \frac{I_{out}}{\sqrt{2}} \times \sqrt{\frac{2D-1}{D'}}, & D \geq 0.5 \end{cases} \quad (26)$$

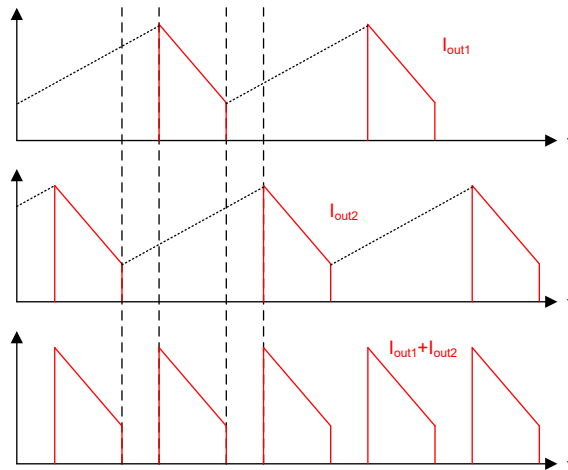


Figure 7-4. Normalized Output Capacitor RMS Ripple Current

Decoupling capacitors are critical for minimized voltage spike of the MOSFETs. This is also important from EMI view. Quite a few 0603/100nF ceramic capacitors are placed close to the MOSFETs following "vertical loop" concept. Refer to [Improve High-Current DC/DC Regulator EMI Performance for Free With Optimized Power Stage Layout application brief](#) for more details.

A few 10µF ceramic capacitors are also necessary to reduce the output voltage ripple and split the output ripple current.

Typically, aluminum capacitors are required for high capacitance. In this example, four 150µF aluminum capacitors are selected.

The output transient response is closely related to the bandwidth of the loop gain and the output capacitance. According to [How to Determine Bandwidth from the Transient-response Measurement technical article](#), the overshoot or undershoot V_p can be estimated as:

$$V_p = \frac{\Delta I_{tran}}{2\pi \times f_c \times C_{out}} \quad (27)$$

where ΔI_{tran} is the transient load current step.

Please be aware that [Equation 27](#) is valid only if the converter is always operating in CCM or FPWM during load step. If the converter enters DCM or pulsing skip mode at light load, the overshoot is worse.

Due to the inherent path from input to output, unlimited inrush current can flow when the input voltage rises quickly and charges the output capacitor. The slew rate of input voltage rising must be controlled by a hot-swap or by starting the input power supply softly for the inrush current not to damage the inductor, sense resistor or high-side MOSFET.

7.2.4 Application Curves

7.2.4.1 Efficiency

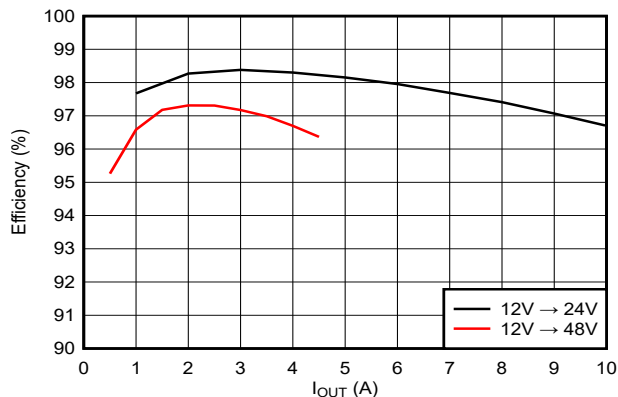


Figure 7-5. Efficiency vs Output Current, $V_{in} = 12V$, $V_{out} = 24V, 48V$

7.3 Power Supply Recommendations

The LMG5126 is designed to operate over a wide input voltage range. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. In addition, the input supply must be capable of delivering the required input current to the fully loaded regulator. Use [Equation 28](#) to estimate the average input current.

$$I_I = \frac{P_O}{V_I \eta} \quad (28)$$

where

- η the efficiency.

One way to get a value for the efficiency is the data from the efficiency graphs in [Section 7.2.4.1](#) in the worst case operation mode. For most applications, the boost operation is the region of highest input current.

If the device is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse effect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at V_I each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. One way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. An EMI input filter is often used in front of the converter power stage. Unless carefully designed, it can lead to instability as well as some of the previously mentioned affects.

7.4 Layout

7.4.1 Layout Guidelines

The performance of switching converters heavily depends on the quality of the PCB layout. Poor PCB design can cause among others converter instability, load regulation problems, noise or EMI issues. Thermal relieved connections in the power path for VCC should not be used as they add significant inductance.

- Place the VCC and BIAS capacitors close to the corresponding device pins and connect them with short and wide traces to minimize inductance as they carry high peak currents.
- Place CSA and CSB filter resistors and capacitors close to the corresponding device pins to minimize noise coupling between the filter and the device. Route the traces to the sense resistor R_{CS} , which is placed close to the inductor, as differential pair and surrounded by ground to avoid noise coupling. Use Kelvin connections to the sense resistor.
- Place the compensation network R_{COMP} and C_{COMP} as well as the frequency setting resistor R_{RT} close to the corresponding device pins and connect them with short traces to avoid noise coupling. Connect the analog ground pin AGND to these components.
- Place the ATRK resistor R_{ATRK} (when used) close to the ATRK pin and connect it to AGND.
- The layout of following components is not so critical:
 - Soft-Start capacitor C_{SS}
 - DLY capacitor C_{DLY}
 - ILIM/IMON resistor and capacitor R_{ILIM} and C_{ILIM}
 - CFG1, CFG2 and SYNCOUT resistors
 - UVLO/EN resistors
- Place the filter V_{OUT} capacitors (small size ceramic) close to the VOUT-pin. Use short and wide traces to minimize the power stage loop C_{OUT} to VOUT connection to avoid high voltage spikes.
- Connect the PGND-pin connection with short and wide traces to the V_{OUT} and V_I capacitors ground to minimize inductance causing high voltage spikes.
- It is recommended to connect the AGND and PGND pin directly to the exposed pad (EP) to form a star connection at the device.
- Connect the device exposed pad (EP) with several vias to a ground plane to conduct heat away.
- Separate power and signal traces and use a ground plane to provide noise shielding.

To spread the heat generated by the converter and the inductor, the inductor should be placed away from the converter. However the longer the trace between the inductor and the converter the higher the EMI and noise emissions. For highest efficiency the inductor should be connected by wide and short traces to minimize resistive losses.

7.4.2 Layout Example

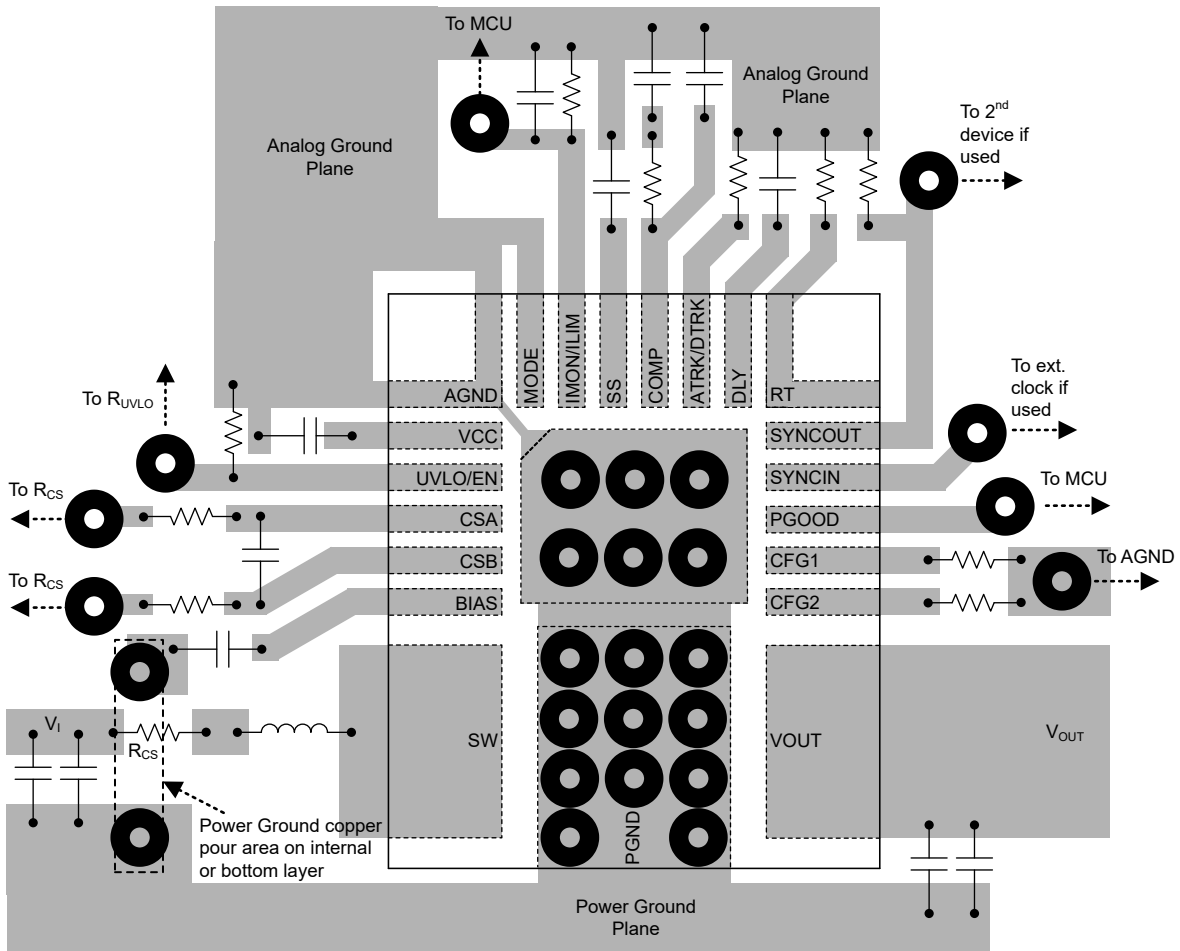


Figure 7-6. Layout Example

ADVANCE INFORMATION

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial APL Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Package Option Addendum

Packaging Information

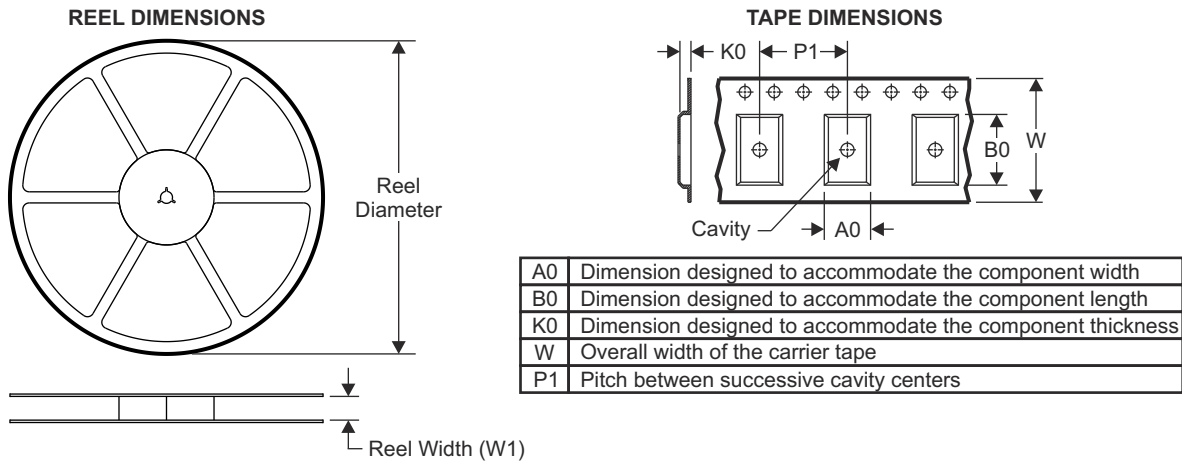
Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽¹⁾	Lead/Ball Finish ⁽⁵⁾	MSL Peak Temp ⁽²⁾	Op Temp (°C)	Device Marking ^{(3) (4)}
XLMG5126VBT T	PREVIEW	VQFN-FCRLF	VBT	22	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	XSE5126

- (1) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details. **TBD:** The Pb-Free/Green conversion plan has not been defined. **Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above. Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (2) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (3) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (4) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (5) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

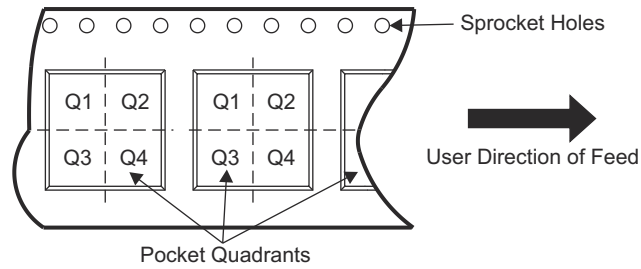
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10.2 Tape and Reel Information



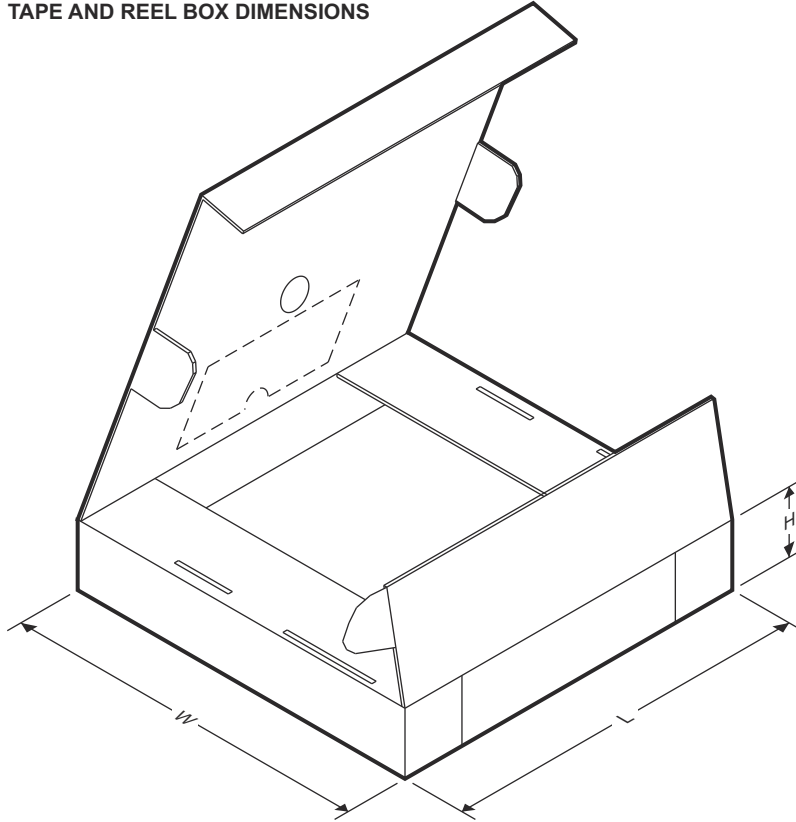
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XLMG5126VBTT	VQFN-FCRLF	VBTT	22	250	330	12.0	5.3	6.3	1.2	8	12	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XLMG5126VBTT	VQFN-FCRLF	VBT	22	250	340	338	22

ADVANCE INFORMATION

10.3 Mechanical Data

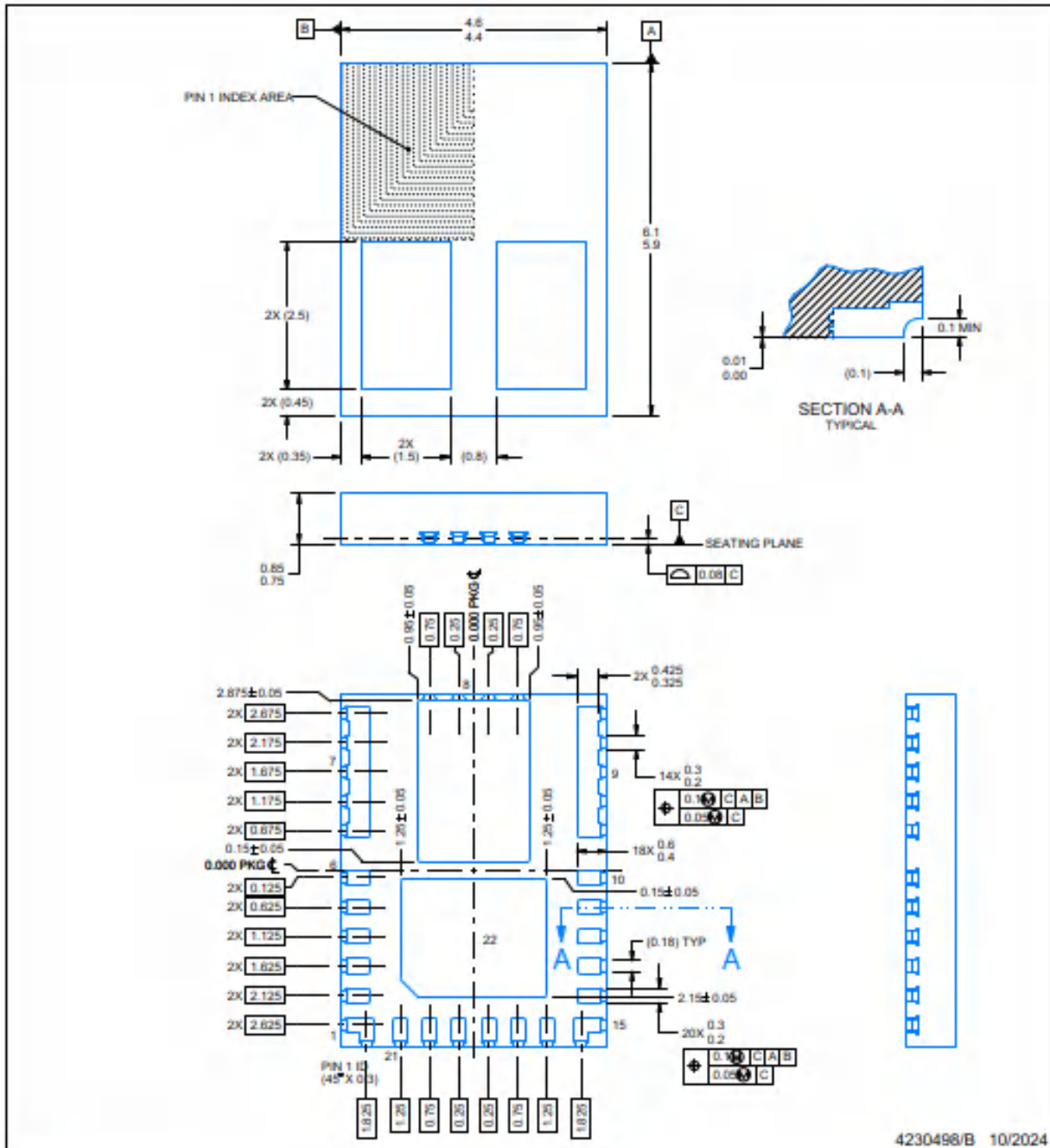
VBT0022A



PACKAGE OUTLINE

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

4230498/B 10/2024

ADVANCE INFORMATION

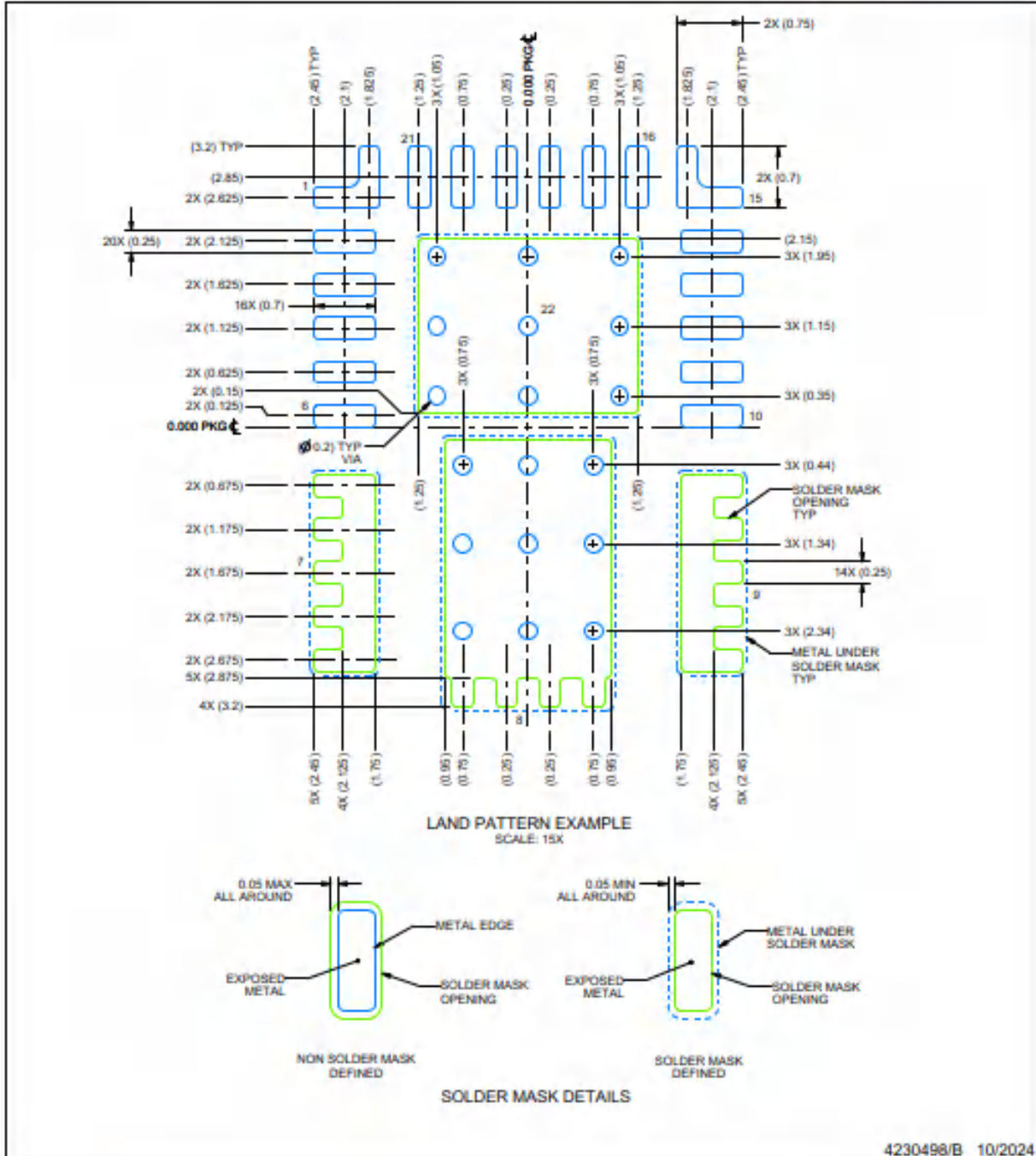
EXAMPLE BOARD LAYOUT

VBT0022A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

ADVANCE INFORMATION



NOTES: (continued)

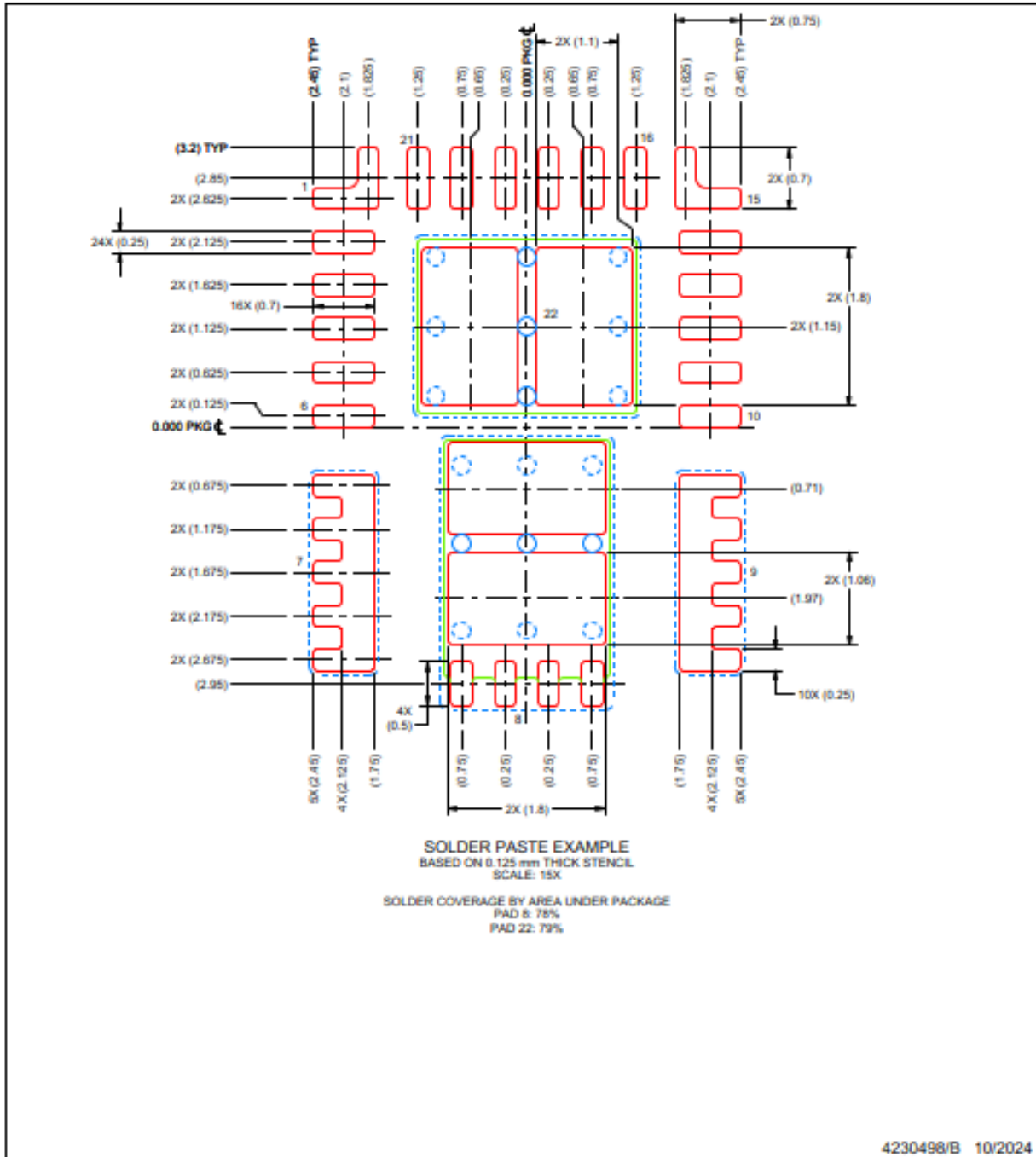
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VBT0022A

VQFN-FCRLF - 0.85 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

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