LMK3H0102 Reference-Less 2-Differential or 5-Single-Ended Output PCIe Gen 1-6 Compliant Programmable BAW Clock Generator

1 Features

- Integrated BAW resonator, no need for external reference
- Flexible frequency generation:
  - Two channel dividers: up to three unique output frequencies from 2.5MHz to 400MHz
  - LVCMOS outputs supported up to 200MHz: 1.8V, 2.5V, or 3.3V
  - Combination of AC-LVDS, DC-LVDS, LP-HCSL, and LVCMOS on OUT0 and OUT1 pins
  - Additional LVCMOS output for generation of up to 5 LVCMOS clocks
- Total output frequency stability: ±25ppm
- 2 functional modes: I^2C or preprogrammed OTP
  - Fully configurable I^2C address
- Ambient temperature: –40°C to 85°C
- PCIe Gen 1 to Gen 6 compliant: Common Clock with or without SSC, SRNS, and SRIS
- Very low PCIe jitter with SSC:
  - PCIe Gen 3 Common Clock jitter: 135.3fs maximum (PCIe limit is 1ps)
  - PCIe Gen 4 Common Clock jitter: 135.3fs maximum (PCIe limit is 500fs)
  - PCIe Gen 5 Common Clock jitter: 57.5fs maximum (PCIe limit is 150fs)
  - PCIe Gen 6 Common Clock jitter: 34.5fs maximum (PCIe limit is 100fs)
- Programmable SSC modulation depth
  - Preprogrammed: –0.1%, –0.25%, –0.3%, and –0.5% down spread
  - Register programmable: –0.1% to –3% down spread or ±0.05% to ±1.5% center spread
- 1.8V to 3.3V supply voltage
- Internal LDOs with –93.1dBc PSNR at 500kHz switching noise for LP-HCSL outputs
- Start-up time: <1.5ms
- Output-to-output skew: <50ps
- Fail-safe digital input pins

2 Applications

- PCIe Gen 1 to Gen 6 clock generation
- Server Motherboard
- NIC, SmartNIC
- Hardware Accelerator
- Multifunction Printer
- PCIe SSD
- Add-In Card, PCIe Expansion Card

3 Description

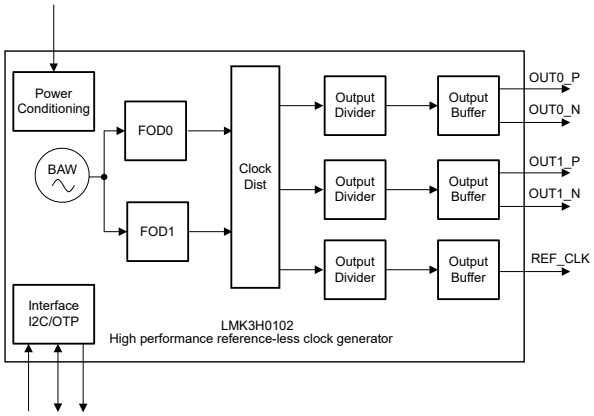
The LMK3H0102 is a 2-output PCIe Gen 1 to Gen 6 compliant reference-less clock generator with Spread Spectrum Clocking (SSC) support. The part is based on TI proprietary Bulk Acoustic Wave (BAW) technology and provides ±25ppm clock outputs without any crystal or external clock reference. The device can provide two SSC clocks, two non-SSC clocks, or one SSC clock and one non-SSC clock at the same time. The device meets the full PCIe compliance from Gen 1 to Gen 6, including Common Clock with or without SSC, Separate Reference No Spread (SRNS), and Separate Reference Independent Spread (SRIS).

The device can be easily configured through either GPIO pins or I^2C interface. An external DC/DC can be used to power the device. Refer to *Power Supply Recommendations* for detailed guidelines on power supply filtering and sourcing from DC/DC.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMK3H0102	RER (TQFN, 16)	3.0mm × 3.0mm

(1) For all available packages, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

Table of Contents

4 Pin Configuration and Functions

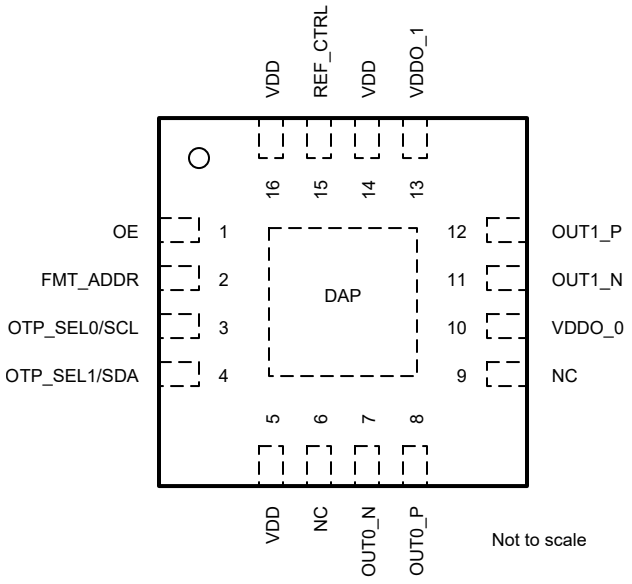


Figure 4-1. LMK3H0102 16-Pin TQFN Top View

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
OUT0_P, OUT0_N	8, 7	O	Clock output 0. Supports LP-HCSL (85 Ω or 100 Ω), LVDS or 1.8-V/2.5-V/3.3-V LVCMOS.
OUT1_P, OUT1_N	12, 11	O	Clock output 1. Supports LP-HCSL (85 Ω or 100 Ω), LVDS or 1.8-V/2.5-V/3.3-V LVCMOS.
REF_CTRL (REF_CLK)	15	I/O	Multifunctional pin. At power up, the state of this pin is latched to select the functionality of Pin 2, Pin 3 and Pin 4. Pull low or leave floating for I2C mode or high for OTP mode prior to power-up. After power-up, this pin can be programmed as an additional LVCMOS output (REF_CLK), active-high CLK_READY signal, or disabled. See REF_CTRL Operation for more details. This pin has an 880-kΩ internal pulldown resistor.
OE	1	I	Output Enable. Active low. 2-state logic input pin. This pin has a 75-kΩ internal pulldown resistor. This pin can control either OUT0 alone or OUT0 and OUT1. See Output Enable for more details. • Low/Floating: OUT0 and OUT1 enabled • High: OUT0 and OUT1 disabled
FMT_ADDR	2	I	Multifunctional pin. Functionality is determined by REF_CTRL (pin 15) at power up. See OTP Mode and I2C Mode for more details. This pin has an 880-kΩ internal pulldown resistor. • I2C Mode: This pin can select the I2C address, function as the output enable for OUT1, or have no function. • OTP Mode: This pin can set the output format, function as the output enable for OUT1, or have no function.

Table 4-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OTP_SEL0/SCL, OTP_SEL1/SDA	3, 4	I, I/O	Multifunctional pin. Functionality is determined by REF_CTRL (pin 15) at power up. See OTP Mode and I2C Mode for details. These pins have 880-kΩ internal pulldown resistors. • I2C Mode: These pins are the I2C clock and data connections. • OTP Mode: These pins select the OTP page.
VDD	5, 14, 16	P	1.8-V, 2.5-V or 3.3-V device power supply. A 0.1-µF capacitor must be placed as close to each of the pins as possible. For LMK3H0102V18, only provide 1.8 V to this pin.
VDDO_0, VDDO_1	10, 13	P	1.8-V, 2.5-V or 3.3-V OUT0 and OUT1 power supply. If VDD is 1.8 V or 2.5 V, the VDDO pins must be the same voltage as VDD. A 0.1-µF capacitor must be placed as close to each of the pins as possible.
NC	6, 9	N/A	No connect. Pins can be connected to GND, VDD, or otherwise tied to any potential within the Supply Voltage range stated in the *Absolute Maximum Ratings*.
DAP	17	G	GND

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD}	Device supply voltage	–0.3	3.9	V
V_{DDO}	Output supply voltage	–0.3	3.9	V
V_{IN}	Logic input voltage (V_{DD} = V_{DDO} = -0.3 to 3.9 V)	–0.3	3.9	V
V_{OUT}	Voltage applied to OUTx_P and OUTx_N pins (when outputs are high or low)	–0.3	V_{DDO_x} + 0.3	V
	Voltage applied to OUTx_P and OUTx_N pins (when outputs are LVCMOS tri-state)	–0.3	1.89	V
	Voltage applied to OUTx_P and OUTx_N pins (when outputs are LP-HCSL or LVDS tri-state)	–0.3	1.5	V
T_J	Junction temperature		105	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

		MIN	NOM	MAX	UNIT
V_{DD}	Device supply voltage	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
V_{DDO}	Output supply voltage	1.71	1.8	1.89	V
		2.375	2.5	2.625	V
		3.135	3.3	3.465	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		105	°C
t_{ramp}	Power supply ramp time. V_{DD} = 1.8 V	0.05		5	ms
t_{ramp}	Power supply ramp time. V_{DD} = 2.5 V or 3.3 V	0.05		5	ms

5.4 Thermal Information

THERMAL METRIC(1)		LMK3H0102 RER (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	69.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W

THERMAL METRIC(1)		LMK3H0102 RER (QFN) 16 PINS	UNIT
Ψ_{JB}	Junction-to-board characterization parameter	38.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY STABILITY						
Δf_{total}	Total frequency stability	All factors included: temperature variation, 10-year aging, solder shift, hysteresis and initial frequency accuracy	–25		25	ppm
LP-HCSL CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		400	MHz
V_{min}	Output low voltage (undershoot included)		–60		25	mV
$V_{overshoot}$	Overshoot voltage. V_{max} - V_{OH}				150	mV
$V_{OH,2.5/3.3}$	Output high voltage. VDD = 2.5 V or 3.3 V	code = 0	594	625	656	mV
		code = 1	614	647	679	mV
		code = 2	635	668	702	mV
		code = 3	656	690	725	mV
		code = 4	676	712	747	mV
		code = 5	697	733	770	mV
		code = 6 (default)	717	755	793	mV
		code = 7	738	777	816	mV
		code = 8	758	798	838	mV
		code = 9	779	820	861	mV
		code = 10	800	842	884	mV
		code = 11	820	863	907	mV
		code = 12	841	885	929	mV
		code = 13	861	907	952	mV
		code = 14	882	928	975	mV
		code = 15	903	950	998	mV

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH,1.8}$	Output high voltage. VDD = 1.8 V	code = 0	563	625	688	mV
		code = 1	582	647	712	mV
		code = 2	601	668	735	mV
		code = 3	621	690	759	mV
		code = 4	641	712	783	mV
		code = 5	660	733	806	mV
		code = 6 (default)	680	755	831	mV
		code = 7	699	777	855	mV
		code = 8	718	798	878	mV
		code = 9	738	820	902	mV
		code = 10	758	842	926	mV
		code = 11	777	863	949	mV
		code = 12	797	885	974	mV
		code = 13	816	907	998	mV
		code = 14	835	928	1021	mV
		code = 15	855	950	1045	mV
Z_{diff}	LP-HCSL static differential impedance		80.75	85	91.25	Ω
			95	100	105	Ω
dV/dt	Output slew rate (rising and falling edge)	Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 0[1]	2.1		3.1	V/ns
		Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 0	2.3		3.5	V/ns
		Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 1	2		3.2	V/ns
		Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 2	1.7		2.8	V/ns
		Measured from –150 mV to +150 mV on the differential waveform, centered on the zero crossing point. OUTx_SLEW_RATE = 3	1.4		2.7	V/ns
ΔdV/dt	Rising edge rate to falling edge rate matching	See[1]			3	%
ODC	Output duty cycle	See[1]	49.9		50.3	%
		f_{out} ≤ 325 MHz	48.8		50.8	%
		325 MHz < f_{out} ≤ 400 MHz	48.6		51.8	%
t_{skew}	Output to output skew	Same FOD, LP-HCSL output			50	ps
V_{cross}	Absolute crossing point voltage	See[1]	280		480	mV
ΔV_{cross}	Variation of V_{cross} over all clock edges	See[1]			30	mV
$\|V_{RB}\|$	Absolute value of ring back voltage	See[1]	100			mV
t_{stable}	Time before V_{RB} is allowed	See[1]	500			ps
$J_{cycle-to-cycle}$	Cycle to cycle jitter, Common Clock no SSC	See[1]			150	ps

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{cycle-to-cycle}$	Cycle to cycle jitter, Common Clock, -0.5% SSC	See(1)			150	ps
t_{period_abs}	Absolute period including jitter and SSC	See(1)	9.949	10	10.101	ns
$t_{period\_avg\_CC}$	Average clock period accuracy, Common Clock	See(1)	–100		2600	ppm
$t_{period\_avg\_SRIS}$	Average clock period accuracy, SRIS	See(1)	–100		1600	ppm
LVDS CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		400	MHz
$\|V_{OD}\|$	Steady-state magnitude of the differential output voltage $\|V_{OUTP} - V_{OUTN}\|$	100 Ω external termination	250	350	450	mV
$\Delta V_{pp-diff}$	Change in differential output voltage swing between complementary output states	100 Ω external termination			50	mV
V_{OS}	Output offset voltage (common mode voltage)	V_{DDO} = 3.3 V, 100 Ω external termination	1.12	1.2	1.365	V
		V_{DDO} = 2.5 V, 100 Ω external termination	1.1	1.2	1.345	V
		V_{DDO} = 1.8 V, 100 Ω external termination	0.8		0.97	V
ΔV_{OS}	Change in V_{OS} between complementary output states				50	mV
I_{SA}, I_{SB}	Short-circuit current. Magnitude of current with the generator output terminals short-circuited to the generator circuit common		–24		24	mA
I_{SAB}	Short-circuit current. Magnitude of current with generator output terminals short-circuited to each other		–12		12	mA
t_R, t_F	20% to 80% differential rise/fall time	PADCAP_CHx = 0	195		315	ps
		PADCAP_CHx = 1	250		440	ps
		PADCAP_CHx = 2	270		610	ps
		PADCAP_CHx = 3	280		800	ps
t_{skew}	Output to output skew	Same FOD, LVDS output			50	ps
ODC	Output duty cycle		49		51.1	%
LVCMOS CLOCK OUTPUT CHARACTERISTICS						
f_{out}	Output frequency		2.5		200	MHz
dV/dt	Output slew rate	V_{DDO} = 3.3 V ± 5%, measured from 20% to 80%, 4.7 pF load	2.6		4.7	V/ns
		V_{DDO} = 2.5 V ± 5%, measured from 20% to 80%, 4.7 pF load	2.6		3.7	V/ns
		V_{DDO} = 1.8 V ± 5%, measured from 20% to 80%, 4.7 pF load	1.5		3.2	V/ns
V_{OH}	Output high voltage	I_{OH} = –15 mA at 3.3 V	0.8 x V_{DDO}		V_{DDO}	V
		I_{OH} = –12 mA at 2.5 V				
		I_{OH} = –8 mA at 1.8 V				
V_{OL}	Output low voltage	I_{OL} = 15 mA at 3.3 V			0.4	V
		I_{OL} = 12 mA at 2.5 V				
		I_{OL} = 8 mA at 1.8 V				
I_{leak}	Output leakage current	Output tri-stated. V_{DD} = V_{DDO} = 3.465 V	–5	0	5	µA
R_{out}	Output impedance			17		Ω
ODC	Output duty cycle	f_{out} ≤ 156.25 MHz	45		55	%
		f_{out} > 156.25 MHz	40		60	%
t_{skew}	Output-to-output skew	Same FOD, LVCMOS output			50	ps

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{load}	Maximum load capacitance				15	pF
LVCMOS REFCLK CHARATERISTICS						
f_{out}	Output frequency	See(2)	12.5(3)		200	MHz
dV/dt	Output slew rate	V_{DDO} = 3.3 V ± 5%, measured from 20% to 80%, 4.7 pF load(2)	2.6		6.7	V/ns
		V_{DDO} = 2.5 V ± 5%, measured from 20% to 80%, 4.7 pF load(2) (4)	1.8		4.5	V/ns
		V_{DDO} = 1.8 V ± 5%, measured from 20% to 80%, 4.7 pF load(2) (4)	1		3.2	V/ns
I_{leak}	Output leakage current	Output tri-stated. V_{DD} = V_{DDO} = 3.465 V(2) (4)	–5		5	µA
R_{out}	Output impedance			17		Ω
ODC	Output duty cycle	f_{out} ≤ 156.25 MHz(2)	45		55	%
ODC	Output duty cycle	f_{out} > 156.25 MHz(2)	40		60	%
C_{load}	Maximum load capacitance	See(2)			15	pF
RJ	Random jitter	12 kHz to 20 MHz integrated jitter at 50 MHz(2)			0.5	ps
SSC CHARACTERISTICS						
f_{out}	Output frequency range that supports SSC (any output format)		2.5		200	MHz
f_{SSC}	SSC modulation frequency		30	31.5	33	kHz
$f_{SSC-deviation}$	SSC deviation (modulation depth)	Down spread (programmable)	–3		–0.1	%
		Center spread (programmable)	±0.05		±1.5	%
$f_{SSC-deviation-accuracy}$	SSC deviation accuracy	f_{out} ≤ 100 MHz, down spread	0		0.01	%
		100 MHz < f_{out} ≤ 200 MHz, down spread	0		0.05	%
		f_{out} ≤ 100 MHz, center spread	0		0.01	%
		100 MHz < f_{out} ≤ 200 MHz, center spread	0		0.05	%
df/dt	max SSC frequency slew rate	0 < $f_{SSC-deviation}$ ≤ –0.5%			1250	ppm/µs
JITTER CHARACTERISTICS						
$J_{PCIe1-cc-SSC\_off}$	PCIe Gen 1 Common Clock jitter, SSC is off (jitter limit = 86 ps)	SSC disabled on both outputs			0.8	ps
$J_{PCIe1-cc-SSC\_on}$	PCIe Gen 1 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 86 ps)	SSC enabled on both outputs			1.4	ps
$J_{PCIe2-cc-SSC\_off}$	PCIe Gen 2 Common Clock jitter, SSC is off (jitter limit = 3 ps)	SSC disabled on both outputs		0.2	0.3	ps
$J_{PCIe2-cc-SSC\_on}$	PCIe Gen 2 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 3 ps)	SSC enabled on both outputs		0.3	0.5	ps
$J_{PCIe2-SRNS}$	PCIe Gen 2 SRNS jitter	SSC disabled on both outputs		0.2	0.3	ps
$J_{PCIe2-SRIS}$	PCIe Gen 2 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		0.3	0.5	ps
$J_{PCIe3-cc-SSC\_off}$	PCIe Gen 3 Common Clock jitter, SSC is off (jitter limit = 1 ps)	SSC disabled on both outputs		42.8	84.2	fs
$J_{PCIe3-cc-SSC\_on}$	PCIe Gen 3 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 1 ps)	SSC enabled on both outputs		63.1	135.3	fs
$J_{PCIe3-SRNS}$	PCIe Gen 3 SRNS jitter	SSC disabled on both outputs		48.8	97.5	fs
$J_{PCIe3-SRIS}$	PCIe Gen 3 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		194.1	418.5	fs
$J_{PCIe4-cc-SSC\_off}$	PCIe Gen 4 Common Clock jitter, SSC is off (jitter limit = 500 fs)	SSC disabled on both outputs		42.8	84.2	fs

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$J_{PCIe4\text{-}cc\text{-}SSC\_on}$	PCIe Gen 4 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 500 fs)	SSC enabled on both outputs		63.1	135.3	fs
$J_{PCIe4\text{-}SRNS}$	PCIe Gen 4 SRNS jitter	SSC disabled on both outputs		48.8	97.5	fs
$J_{PCIe4\text{-}SRIS}$	PCIe Gen 4 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		98.5	205.4	fs
$J_{PCIe5\text{-}cc\text{-}SSC\_off}$	PCIe Gen 5 Common Clock jitter, SSC is off (jitter limit = 150 fs)	SSC disabled on both outputs		17.8	35.6	fs
$J_{PCIe5\text{-}cc\text{-}SSC\_on}$	PCIe Gen 5 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 150 fs)	SSC enabled on both outputs		26.4	57.5	fs
$J_{PCIe5\text{-}SRNS}$	PCIe Gen 5 SRNS jitter	SSC disabled on both outputs		19.8	39	fs
$J_{PCIe5\text{-}SRIS}$	PCIe Gen 5 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		30.2	63.9	fs
$J_{PCIe6\text{-}cc\text{-}SSC\_off}$	PCIe Gen 6 Common Clock jitter, SSC is off (jitter limit = 100 fs)	SSC disabled on both outputs		11	22	fs
$J_{PCIe6\text{-}cc\text{-}SSC\_on}$	PCIe Gen 6 Common Clock jitter, –0.5% ≤ SSC < 0% (jitter limit = 100 fs)	SSC enabled on both outputs		16	34.5	fs
$J_{PCIe6\text{-}SRNS}$	PCIe Gen 6 SRNS jitter	SSC disabled on both outputs		14.8	27.9	fs
$J_{PCIe6\text{-}SRIS}$	PCIe Gen 6 SRIS jitter, –0.3% ≤ SSC < 0%	SSC enabled on both outputs		22.2	45.9	fs
RJ_{RMS}	12 kHz to 20 MHz RMS jitter	f_{out} = 156.25MHz		105	144	fs
TIMING CHARACTERISTICS						
$t_{startup}$	Start-up time	V_{DD} = 2.5 V or 3.3 V. Time elapsed from all V_{DD} pins reach 2.1 V until first output clock rising edge. Output clock is always within specification			1	ms
		V_{DD} = 1.8 V. Time elapsed from all V_{DD} pins reach 1.6 V until first output clock rising edge. Output clock is always within specification			1.5	ms
t_{OE}	Output enable time.	After CLOCK_READY status is '1', time elapsed between OE assertion and first output clock rising edge. Output is not tristated when disabled.			7	output clock cycles
t_{OD}	Output disable time.	Time elapsed between OE deassertion and last output clock falling edge.			7	output clock cycles
POWER CONSUMPTION CHARACTERISTICS						
I_{DD}	Core supply current, not including output drivers	One FOD enabled, 100 MHz ≤ f_{FOD} ≤ 200 MHz		57.5	79.9	mA
		One FOD enabled, 200 MHz < f_{FOD} ≤ 400 MHz		67	90.7	mA
		Two FODs enabled, 100 MHz ≤ f_{FOD} ≤ 200 MHz		81.1	105.8	mA
		Two FODs enabled, 200 MHz < f_{FOD} ≤ 400 MHz		97.8	125.8	mA

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DDO}	Output supply current, per output channel	LP-HCSL. f_{out} ≤ 100 MHz		10.1	10.8	mA
		LP-HCSL. 100 MHz < f_{out} ≤ 200 MHz		13.2	14.1	mA
		LP-HCSL. 200 MHz < f_{out} ≤ 300 MHz		13.7	15.1	mA
		LP-HCSL. 300 MHz < f_{out} ≤ 400 MHz		14.4	16.4	mA
		LVDS. f_{out} ≤ 100 MHz		6	8	mA
		LVDS. 100 MHz < f_{out} ≤ 200 MHz		6.8	9.2	mA
		LVDS. 200 MHz < f_{out} ≤ 300 MHz		7.6	10.2	mA
		LVDS. 300 MHz < f_{out} ≤ 400 MHz		8.4	11.3	mA
		1.8 V LVCMOS. f_{out} = 50 MHz		4.2	5	mA
		1.8 V LVCMOS. f_{out} = 200 MHz		11.7	13.4	mA
		2.5 V LVCMOS. f_{out} = 50 MHz		5.6	6.4	mA
		2.5 V LVCMOS. f_{out} = 200 MHz		15.3	17.3	mA
		3.3 V LVCMOS. f_{out} = 50 MHz		6.8	7.7	mA
		3.3 V LVCMOS. f_{out} = 200 MHz		19.2	21.7	mA
I_{DDREF}	REFCLK supply current	1.8 V LVCMOS. f_{out} = 50 MHz		3.4	3.9	mA
		1.8 V LVCMOS. f_{out} = 200 MHz		9.5	11.7	mA
		2.5 V LVCMOS. f_{out} = 50 MHz		4.7	5.3	mA
		2.5 V LVCMOS. f_{out} = 200 MHz		12.8	15.8	mA
		3.3 V LVCMOS. f_{out} = 50 MHz		5.9	6.6	mA
		3.3 V LVCMOS. f_{out} = 200 MHz		16.6	20.2	mA
PSNR CHARACTERISTICS						
$PSNR_{LVCMOS}$	Power Supply Noise Rejection for LVCMOS outputs(4)	10 kHz		–76.7	–61.2	dBc
		50 kHz		–80.9	–60.9	dBc
		100 kHz		–81.8	–60	dBc
		500 kHz		–84.3	–64.9	dBc
		1 MHz		–97.6	–82.1	dBc
		5 MHz		–104.3	–83.1	dBc
		10 MHz		–108.7	–94.2	dBc
$PSNR_{LVDS}$	Power Supply Noise Rejection for LVDS outputs(4)	10 kHz		–79.5	–74.5	dBc
		50 kHz		–83.5	–77	dBc
		100 kHz		–83	–75.3	dBc
		500 kHz		–88.3	–83.1	dBc
		1 MHz		–123.4	–106.6	dBc
		5 MHz		–115	–92.3	dBc
		10 MHz		–123.7	–108.9	dBc
$PSNR_{LP-HCSL}$	Power Supply Noise Rejection for LP-HCSL outputs(4)	10 kHz		–80.1	–74.5	dBc
		50 kHz		–84.7	–76.7	dBc
		100 kHz		–84.6	–73.7	dBc
		500 kHz		–93.1	-82.9	dBc
		1 MHz		–124.6	–106.8	dBc
		5 MHz		–114.3	–92.9	dBc
		10 MHz		–123	–109.2	dBc
2-STATE LOGIC INPUT CHARACTERISTICS						
$V_{IH-Pin2}$	Input high voltage for Pin 2		0.7 × V_{DD}		V_{DD} + 0.3	V

V_{DD} = V_{DDO} = 1.8 V, 2.5 V or 3.3 V ± 5%, T_A = $T_{A,min}$ to $T_{A,max}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL-Pin2}$	Input low voltage for Pin 2		GND – 0.3		0.3 × V_{DD}	V
$V_{IH-Pin1}$	Input high voltage for Pin 1		1.15		V_{DD} + 0.3	V
$V_{IL-Pin1}$	Input low voltage for Pin 1		–0.3		0.65	V
$V_{IH-Pin3,4}$	Input voltage high for OTP_SEL[1:0]		0.7 × V_{DD}		V_{DD} + 0.3	V
$V_{IL-Pin3,4}$	Input voltage low for OTP_SEL[1:0]		GND - 0.3		0.8	V
$V_{IH-Pin15}$	Input voltage high for Pin 15		0.65 × V_{DD}		V_{DD} + 0.3	V
$V_{IL-Pin15}$	Input voltage low for Pin 15		–0.3		0.4	V
$R_{ext-up/down-Pin1,2}$	Recommended external pullup or pulldown resistor for Pin 1, 2		0	1	10	kΩ
$R_{ext-up/down-Pin3,4,15}$	Recommended external pullup or pulldown resistor for Pin 3, 4, 15		0	10	60	kΩ
t_R/t_F	OE signal rise or fall time				10	ns
C_{in}	Input capacitance				3	pF

(1) PCIe test load, 15 dB loss at 4 GHz, f_{out} = 100 MHz, Z_{diff} = 100 Ω
(2) Tested with 10 kΩ external pullup or pulldown resistor
(3) REFCLK can be /2, /4, /8 from either FOD0 or FOD1. Both FODs support 100 to 400 MHz.
(4) All power supply pins are tied together. 0.1 µF capacitor placed close to each power supply pin. Apply 50 mVpp ripple and measure the spur level at the clock output

5.6 I2C Interface Specification

All timing requirements referred to V_{IH-min} and V_{IL-max}. Chip V_{DD} = I^2C V_{DD}.

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
V_{IL}	Input low voltage		–0.3	0.3 × V_{DD}	–0.3	0.3 × V_{DD}	V
V_{IH}	Input high voltage		0.7 × V_{DD}	V_{DD} + 0.3	0.7 × V_{DD}	V_{DD} + 0.3	V
V_{hys}	Hysteresis of Schmitt trigger input				0.05 × V_{DD}		V
V_{OL1}	Low level output voltage 1	At 3 mA sink current. V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	Low level output voltage 2	At 2 mA sink current. V_{DD} ≤ 2 V			0	0.2 x V_{DD}	V
I_{OL}	Low level output current	V_{OL} = 0.4 V	3		3		mA
		V_{OL} = 0.6 V			6		mA
t_{OF}	Output fall time from VIHmin to VILmax			250	20 × (V_{DD} / 5.5 V)	250	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter				0	50	ns
I_i	Input current each I/O pin	0.1 × V_{DD} < V_{IN} < 0.9 × V_{DDmax}	–10	10	–10	10	µA
C_i	Capacitance for each I/O pin			10		10	pF
f_{SCL}	SCL clock frequency		0	100	0	400	kHz
t_{HD-STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4		0.6		µs
tlow	Low period of the SCL clock		4.7		1.3		µs

All timing requirements referred to V_{IH-min} and V_{IL-max}. Chip V_{DD} = I^2C V_{DD}.

PARAMETER		TEST CONDITIONS	STANDARD MODE		FAST MODE		UNIT
			MIN	MAX	MIN	MAX	
thigh	High period of the SCL clock		4		0.6		µs
t_{SU-STA}	Set-up time for a repeated START condition		4.7		0.6		µs
t_{HD-DAT}	Data hold time	I^2C bus devices	0		0		µs
t_{SU-DAT}	Data set-up time		0.25		0.1		µs
t_R	Rise time of both SDA and SCL signals (1)			300	20	300	ns
t_F	Fall time of both SDA and SCL signals (1)			300	20 × (V_{DD} / 5.5 V)	300	ns
t_{SU-STO}	Set-up time for STOP condition		4		0.6		µs
t_{BUF}	Bus free time between a STOP and START condition		4.7		1.3		µs
C_B	Capacitive load for each bus line			400		400	pF
t_{VD-DAT}	Data valid time			3.45		0.9	µs
t_{VD-ACK}	Data valid acknowledge time			3.45		0.9	µs
V_{NL}	Noise margin at the low level	For each connected device, including hysteresis	0.1 x V_{DD}		0.1 × V_{DD}		V
V_{NH}	Noise margin at the high level	For each connected device, including hysteresis	0.2 x V_{DD}		0.2 × V_{DD}		V

6 Parameter Measurement Information

6.1 Output Format Configurations

This section describes the characterization test setup of each output format option in the LMK3H0102.

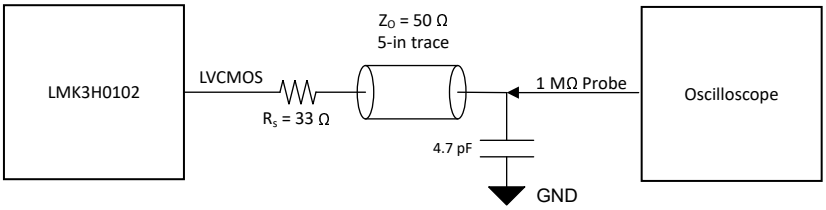


Figure 6-1. LVCMOS Output Configuration During Device Test

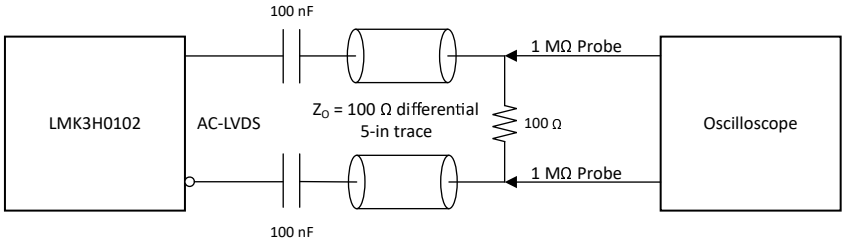


Figure 6-2. AC-LVDS Output Configuration During Device Test

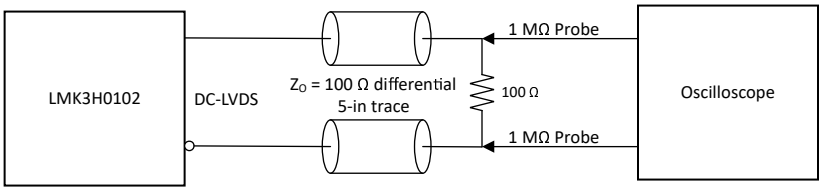


Figure 6-3. DC-LVDS Output Configuration During Device Test

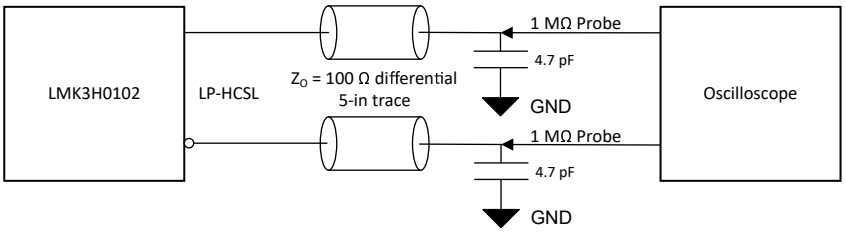


Figure 6-4. LP-HCSL Output Configuration During Non-PCIe Device Test

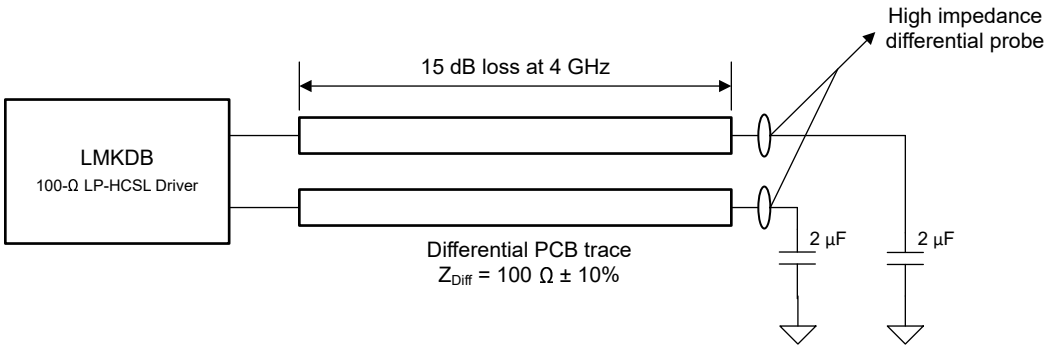


Figure 6-5. LP-HCSL Output Configuration During PCIe Device Test

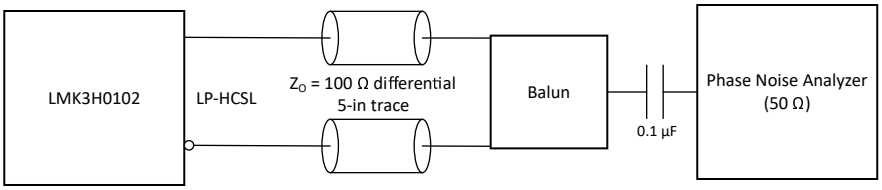


Figure 6-6. PCIe Test Configuration Using Phase Noise Analyzer

6.2 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions, causing confusion when reading data sheets or communicating with other engineers. This section addresses the measurement and description of a differential signal so that the reader is able to understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, the signal only exists in reference to the differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 6-7 shows the two different definitions side-by-side for inputs and Figure 6-8 shows the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

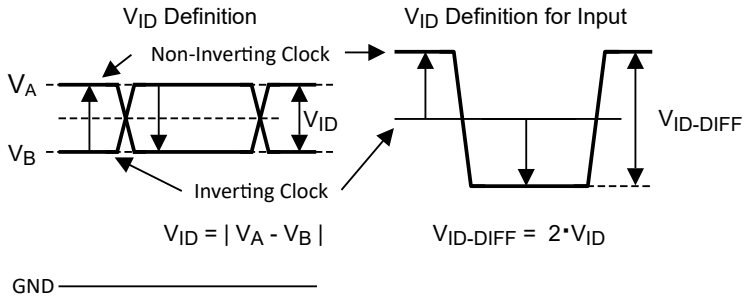


Figure 6-7. Two Different Definitions for Differential Input Signals

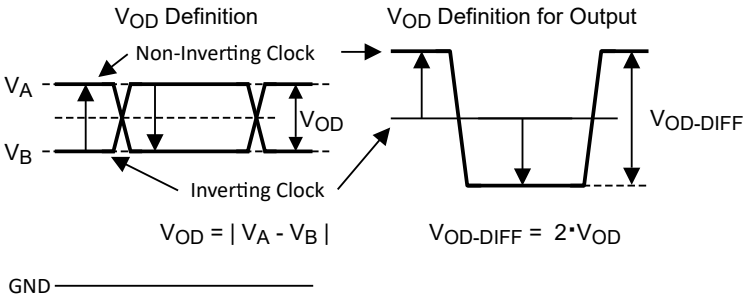


Figure 6-8. Two Different Definitions for Differential Output Signals

7 Detailed Description

7.1 Overview

The LMK3H0102 is a dual-channel clock generator primarily used for PCIe Gen 1 to Gen 6 clock generation, either with or without Spread Spectrum Clocking (SSC). The device has an integrated Bulk Acoustic Wave (BAW) resonator and does not require any external crystal or clock reference. The device has four selectable pages of memory, referred to as OTP pages. The collection of these pages in memory is referred to as the EFUSE.

The default output configuration is two 100-MHz clocks, each with a 100-Ω LP-HCSL output format, both disabled at startup. The LMK3H0102 supports 100-Ω LP-HCSL, 85-Ω LP-HCSL, LVDS and 1.8-V, 2.5-V, or 3.3-V LVCMOS output formats, as well as programmable output frequencies up to 200 MHz for single-ended outputs and 400 MHz for differential outputs. The LMK3H0102V33 is the part number for the default configuration with a 3.3 V supply voltage. The LMK3H0102V18 is the part number for the default configuration with a 1.8 V supply voltage. Custom configuration part numbers are LMK3H0102Axxx, where xxx denotes the custom configuration number.

The LMK3H0102 supports two functional modes determined by the REF_CTRL pin at power-up: One-Time Programming (OTP) mode or I^2C mode.

1. In OTP mode, one out of four OTP pages is selected by pins OTP_SEL0 and OTP_SEL1. The default output frequency across all OTP pages is 100 MHz.
2. In I^2C mode, the LMK3H0102 is configured by modifying the active registers. If a configuration other than the default operation is desired, the registers must be written every time at start-up.

Refer to *Pin Configuration and Functions* for the detailed descriptions of the device pins.

The LMK3H0102 has flexible SSC configurations, including:

1. SSC disabled on both outputs
2. SSC enabled on both outputs
3. SSC enabled on a single output

The SSC specifications and jitter performance are fully compliant to PCIe Gen 1 to Gen 6. Refer to *Spread-Spectrum Clocking* for SSC and jitter performance details.

7.2 Functional Block Diagram

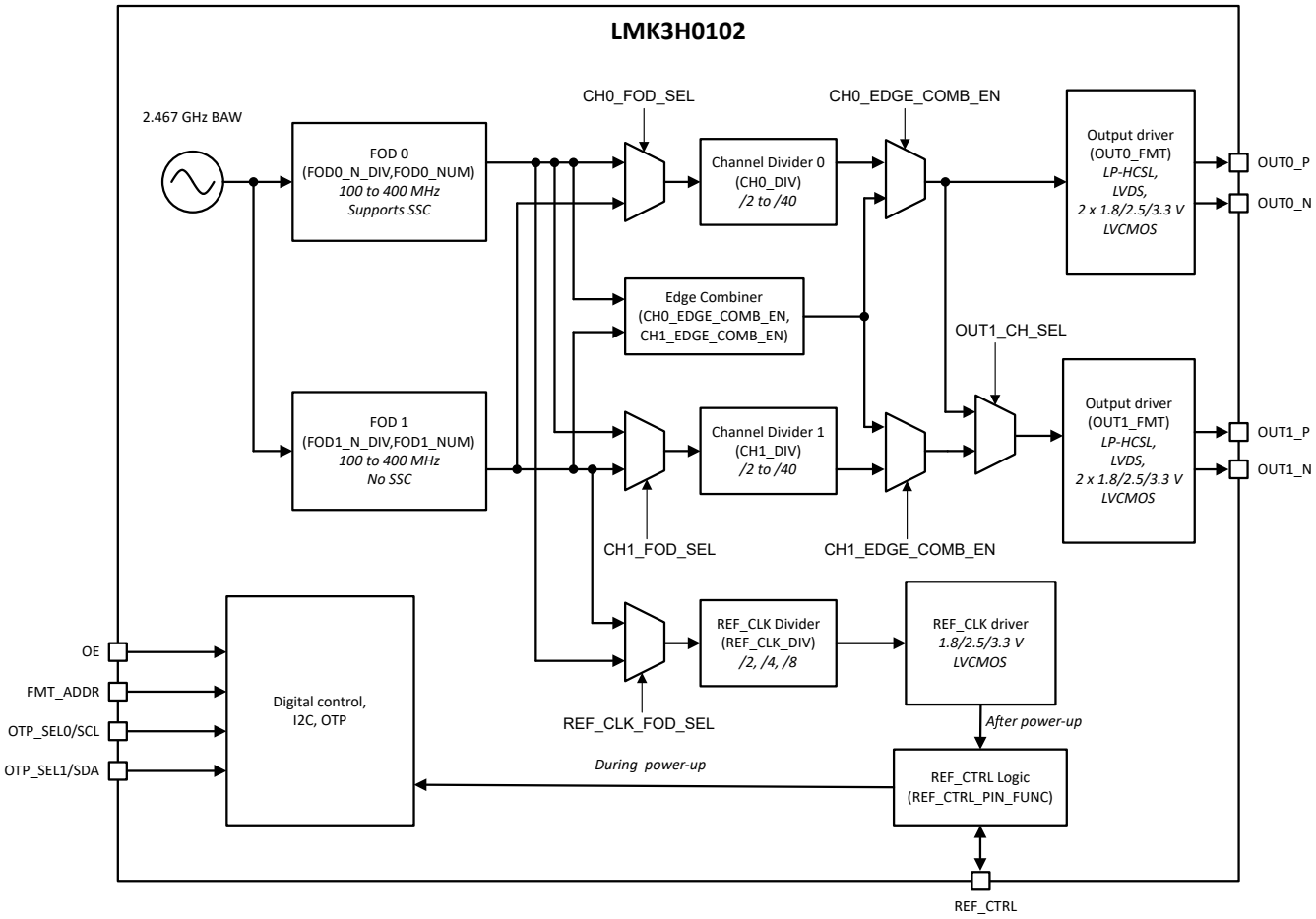


Figure 7-1. LMK3H0102 Functional Block Diagram

7.3 Feature Description

7.3.1 Device Block-Level Description

The LMK3H0102 is a reference-less clock generator with an integrated BAW oscillator. The BAW frequency, nominally 2467MHz, is divided down by two fractional output dividers (FODs), each of which is capable of generating frequencies between 100MHz and 400MHz. Each FOD can be routed to one of two channel dividers, which divides the FOD frequency down to generate frequencies from 2.5MHz to 200MHz. For generating frequencies above 200MHz, the edge combiner, which utilizes both FODs, must be used. In this case, the channel divider is bypassed, resulting in generated frequencies from 200MHz to 400MHz. An additional LVCMOS clock, with a voltage corresponding with VDD, can be optionally generated on the REF_CTRL pin.

7.3.2 Device Configuration Control

Figure 7-2 shows the relationships between device states, the configuration pins, device initialization, and device operational modes. OTP mode is entered when the REF_CTRL pin is pulled high at start-up. I^2C mode is entered when the REF_CTRL pin is pulled low at start-up. In OTP mode, the state of the OTP_SEL0/SCL and OTP_SEL1/SDA pins determines the OTP page that is loaded into the active registers. The device is one-time programmable, meaning that the register settings stored into the internal EFUSE can not be changed. The device can be transitioned from OTP to I^2C mode, or reciprocally, by changing the state of the REF_CTRL pin, then triggering a device power cycle by pulling VDD low, then high again. In OTP mode, a change in the level of the OTP_SEL0 or OTP_SEL1 pins, followed by pulling the REF_CTRL pin high, dynamically changes the active

OTP page. The time between the first OTP_SEL pin change and pulling REF_CTRL high must be less than 350 µs, otherwise the device enters I2C Mode.

In I^2C mode, the state of the FMT_ADDR pin can determine the I^2C address of the device, with the OTP_SEL0/SCL and OTP_SEL1/SDA pins re-purposed as I^2C clock and data pins, respectively. In I^2C mode, the host can update the active device registers. If using a configuration different than the programmed configuration, the registers must be written after each power cycle.

The device can be placed into a low power state by setting the PDN bit (R10[1]) to '1'. Clearing the PDN bit takes the device out of the low power state. If DEV_IDLE_STATE_SEL bit (R10[4]) is a '0' and the outputs are disabled, the device enters the low power state. Entering the low power state is required for changing the frequency of the FOD used by Channel 0, changing the SSC configuration, and changing the output format. TI recommends performing register writes within this low power state. Set the OTP_AUTOLOAD_DIS (R10[2]) bit to a '1' to prevent automatic loading of OTP Page 0 prior to setting PDN to '0'.

There are two fields that determine the state of the device when coming out of the low power state. PIN_RESAMPLE_DIS (R10[3]) controls whether or not the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and REF_CTRL pins are resampled when exiting the low power state. If the pins are resampled, the device can be transitioned into OTP mode if the REF_CTRL pin is pulled high. Set this bit to a '1' to disable this functionality. OTP_AUTOLOAD_DIS controls whether or not the contents of OTP Page 0 are loaded into the device registers when exiting the low power state. If OTP_AUTOLOAD_DIS bit is a '1' and PIN_RESAMPLE_DIS is a '1', then the register contents do not change. If OTP_AUTOLOAD_DIS bit is a '0' and PIN_RESAMPLE_DIS is a '1', then the contents of OTP Page 0 are loaded to the registers. If PIN_RESAMPLE_DIS is a '0' and REF_CTRL is pulled high, then the device enters OTP Mode. In this case, OTP_SEL0/SCL and OTP_SEL1/SDA control the OTP page loaded into the device registers.

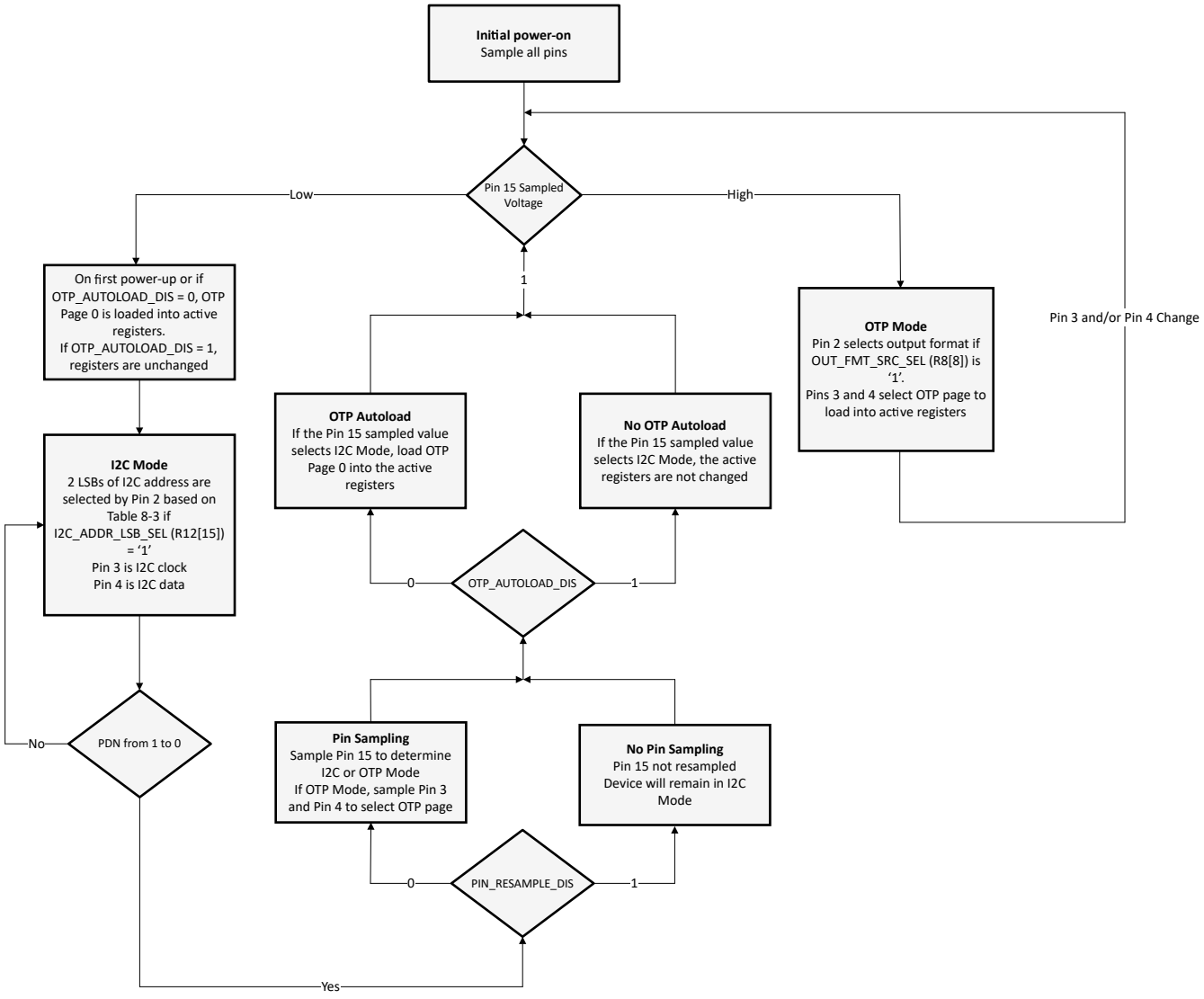


Figure 7-2. LMK3H0102 Device Mode Diagram

In I^2C Mode, the device registers are from the contents of OTP Page 0. In OTP mode, these values come from one of the four OTP pages, selectable based on the state of the OTP_SELx pins on start-up. Figure 7-3 shows interface and control blocks within the LMK3H0102, with the arrows referring to read and write access from the different embedded memories.

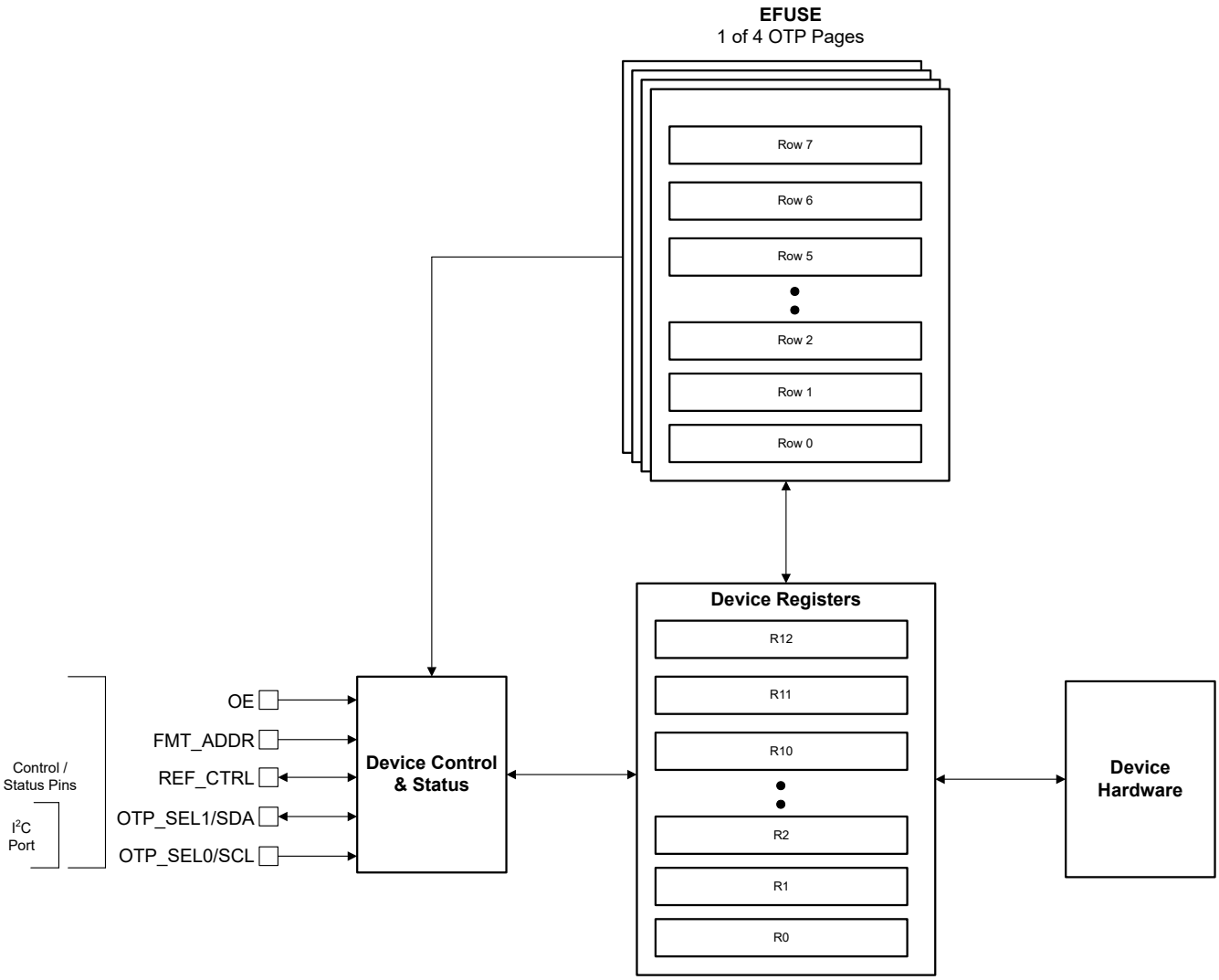


Figure 7-3. LMK3H0102 Interface and Control Blocks

7.3.3 OTP Mode

In this mode, the configuration pins allow for selection of one of four one-time programmable (OTP) pages, as well as output format selection. I^2C is not enabled in this mode, as the I^2C pins are repurposed for OTP page selection. Table 7-1 shows the OTP page selected based on the state of the OTP_SEL0 and OTP_SEL1 pins.

Table 7-1. OTP Page Selection in OTP Mode

OTP_SEL1 Pin	OTP_SEL0 Pin	OTP Page
Low	Low	0
Low	High	1
High	Low	2
High	High	3

The EFUSE of the devices is permanently programmed and has OTP_BURNT(R0[0]) = 1. If a new configuration is desired, the configuration must be loaded through I^2C on each start-up. Contact TI for creation of a custom OTP configuration.

The following fields can be unique between the four OTP pages. All other register settings are shared between the OTP pages:

- SSC_EN: Enable or disable SSC.
- OE_0: Enable or disable OUT0.
- OE_1: Enable or disable OUT1.
- OP_TYPE_CH0: OUT0 output format type, see *Output Format Types*.
- OP_TYPE_CH1: OUT1 output format type, see *Output Format Types*.
- SSC_SETTING: SSC modulation type, see *Spread Spectrum Clocking*.

When OTP_SEL1 or OTP_SEL0 pin state changes, the device automatically goes through a power cycle and reloads the new OTP page. The time elapsed from when pins 3 and 4 change to a stable state in the new OTP is no more than 1.5ms.

7.3.4 I²C Mode

In this mode, I²C is enabled and the SCA and SDL pins function as the I²C clock and I²C data pins, respectively. Table 7-2 shows the four default I²C addresses selectable by the FMT_ADDR pin. The 5 MSBs of the I²C address are set in the upper five bits of I2C_ADDR (R12[14:8]).

If I2C_ADDR_LSB_SEL (R12[15]) = 0, then the FMT_ADDR pin is ignored, and the I²C address is solely determined by I2C_ADDR. If using the FMT_ADDR pin for I²C LSB selection, then the pin must not be configured for individual output enable control.

Table 7-2. I²C Address Selection

REF_CTRL PIN (1)	FMT_ADDR PIN	I²C ADDRESS (2)
High	X	N/A (I2C disabled)
Low	0	0x68 / 0xD0
Low	1	0x69 / 0xD2
Low	Tied to SDA	0x6A / 0xD4
Low	Tied to SCL	0x6B / 0xD8

(1) This is the state of the REF_CTRL pin at power-up, not the live pin state.
(2) The 0xD0, 0xD2, 0xD4, and 0xD8 addresses are with the R/W bit included set to '0'.

When changing the registers of the device, first set PDN to '1', write to the device registers, then set PDN to '0'.Figure 7-4 shows this process.

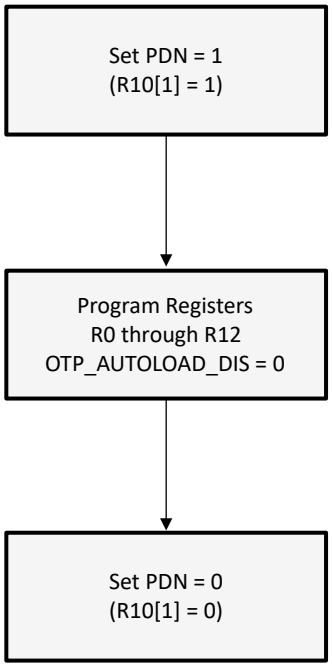


Figure 7-4. LMK3H0102 Programming Sequence

7.4 Device Functional Modes

7.4.1 Fail-Safe Inputs

The LMK3H0102 digital input pins are designed to support fail-safe input operation, with the exception of the REF_CTRL pin. This feature allows the user to drive the digital inputs before VDD is applied without damaging the device. Refer to *Section 5.1* for more information on the maximum input voltages supported by the device.

7.4.2 Fractional Output Dividers

The LMK3H0102 contains two fractional output dividers. If all outputs are able to be generated by a single FOD, TI recommends disabling FOD1 to conserve power and improve performance. If no output channels select FOD1, then FOD1 is disabled.

7.4.2.1 FOD Operation

The internal BAW resonator is divided down by one or two Fractional Output Dividers (FODs). FOD0 has an SSC generator and FOD1 does not have an SSC generator. If both OUT0 and OUT1 must be SSC clocks, the two clocks must be sourced by FOD0. If one SSC clock and one non-SSC clock are required at the same time, then FOD0 is enabled for the SSC clock and FOD1 is enabled for the non-SSC clock. If neither output clock requires SSC, then either FOD can be used.

Note

TI recommends that FOD0 be used as the default FOD if only one FOD is needed for an application. If both FODs are in use, TI recommends using FOD0 with OUT0 and FOD1 with OUT1.

The maximum frequency that can be generated at the clock outputs by a single FOD is 200 MHz, as the minimum channel divider value is a divide by two. To generate a greater than 200 MHz output, the edge combiner is used, bypassing the channel dividers. This requires that both FODs are enabled and have the same integer divider and fractional numerator values, and the same gain calibration values. When one of the outputs exceeds 200 MHz, the other output can only select the shared FOD frequency divided by one of the channel divider values, or be the FOD frequency. Below 200 MHz, the two FODs can be configured independently so that OUT0 and OUT1 can have different frequencies. TI recommends sourcing from a single FOD whenever possible to make sure that OUT0 and OUT1 have a deterministic phase relationship.

The FODs in the LMK3H0102 can be configured to accommodate various output frequencies through I2C programming, or in the absence of programming, the one-time programmed (OTP) settings. The FODs can be configured by setting the integer (FODx_N_DIV) and fractional (FODx_NUM) divide values. Table 7-3 shows the register locations for these fields for each FOD.

Table 7-3. FOD Integer and Numerator Divide Locations

Field	Register
FOD0_N_DIV	R0[9:3]
FOD0_NUM[23:16]	R1[15:8]
FOD0_NUM[15:0]	R2[15:0]
FOD1_N_DIV	R3[15:9]
FOD1_NUM[23:16]	R6[12:5]
FOD1_NUM[15:0]	R8[15:0]

An example of how to set the integer and numerator divide values is shown in Equation 1 and Equation 2.

$$FODx\_N\_DIV = floor(F_{BAW}/F_{FOD}) \quad (1)$$

where:

- FODx_N_DIV: Integer portion of the FOD divide value (7 bits, 6 to 24)
- F_{BAW}: BAW frequency, 2467 MHz plus offset, described in further detail below
- F_{FOD}: Desired FOD frequency (100 MHz to 400 MHz)

$$FODx\_NUM = int(((F_{BAW}/F_{FOD}) - FODx\_N\_DIV) \times 2^{24}) \quad (2)$$

where FODx_NUM is the fractional portion of the FOD divide value (24 bits, that is 0 to 16777215).

The output frequency (F_{OUT}) is related to the FOD frequency as given in Equation 3, or is equal to the FOD frequency when the edge combiner is enabled. OUTDIV can be 2, 4, 6, 8, 10, 20, or 40.

$$F_{OUT} = F_{FOD}/OUTDIV \quad (3)$$

Use Equation 4 to calculate the actual value of the BAW frequency for a device. Users can find the value of BAWFREQ_OFFSET_FIXEDLUT by reading R238, which is a signed 16-bit value.

$$F_{BAW} = 2467\ MHz \times (1 + (BAWFREQ\_OFFSET\_FIXEDLUT \times 128E\text{-}9)) \quad (4)$$

7.4.2.2 Edge Combiner

Use the edge combiner to generate output frequencies greater than 200 MHz. To use the Edge Combiner, set CH0_EDGE_COMB_EN (R3[3]) or CH1_EDGE_COMB_EN (R3[7]) to '1'. When using the edge combiner, both FODs must operate at the same exact frequency (that is, the divide values must match). The device handles this by automatically loading the divider values from FOD0 into FOD1 when either CHx_EDGE_COMB_EN bit is set to a '1'. SSC on FOD0 is not supported when using the edge combiner, and must not be enabled. Either of the FODs can still generate the LVCMOS REF_CLK output.

For proper edge combiner operation, the following conditions must be true:

- The gain calibration codes for both FODs must be averaged. For example, if DTC1_GAIN_RT = 200, and DTC2_GAIN_RT = 220, then both of these fields must be written to 210. The gain calibration codes are in the protected register space. Unlock the protected registers using R12[7:0] = 0x5B, write only the averaged gain calibration codes, and then lock the protected registers by setting R12[7:0] = 0x00. See R146, R147, and R148 for more information.
- If the edge combiner is used for OUT1 **only**, CH0_FOD_SEL (R3[4]) must **always** be set to '0' (FOD0), regardless of the disable state of OUT0.

7.4.2.3 Digital State Machine

The digital state machine of the LMK3H0102 has a clock that originates from one of the FODs. The FOD selected by CH0_FOD_SEL (R3[4]) drives the input to the state machine clock divider. The total divide value is the DIG_CLK_N_DIV (R0[9:3]) field plus two. Set DIG_CLK_N_DIV such that the FOD frequency divided by the total state machine clock divide value is between 40 MHz and 50 MHz. The divider value used to set this clock is equal to the value stored in . As an example, if the frequency of FOD0 is 200 MHz, and CH0_FOD_SEL is a '0', then DIG_CLK_N_DIV must be set to '2', as 200 MHz divided by 4 is 50 MHz.

7.4.2.4 Spread-Spectrum Clocking

FOD0 supports spread-spectrum clocking (SSC). SSC can be used to reduce peak radiated emissions by modulating the output frequency. When SSC_EN (R4[0]) = '1', any outputs that are sourced from FOD0 have SSC. SSC_MOD_TYPE (R4[1]) selects between down-spread modulation (SSC_MOD_TYPE = 0) or center-spread modulation (SSC_MOD_TYPE = 1). The LMK3H0102 has four built-in down-spread SSC options, as well as a custom SSC option. SSC_CONFIG_SEL (R9[11:9]) selects between the custom or preconfigured options. The preconfigured options are optimized for a 200 MHz output from FOD0. Table 7-4 details the register settings for the preconfigured SSC options. The preconfigured SSC options are optimized for 200 MHz outputs from FOD0. If the edge combiner is used, then spread-spectrum clocking must be disabled.

Table 7-4. Predefined SSC Configurations

SSC_CONFIG_SEL	Down-spread SSC Depth
0x0	Custom, based on SSC_STEPS and SSC_STEP_SIZE
0x1	–0.10%
0x2	–0.25%
0x3	–0.30%
0x4	–0.50%
All other values	Reserved

If Custom SSC is selected, then SSC_STEPS (R4[14:2]) and SSC_STEP_SIZE (R5) must be configured to set the modulation depth. Use Equation 5 and Equation 6 to determine the SSC_STEPS (R4[14:2]) register settings, and use Equation 7 or Equation 8 to determine the SSC_STEP_SIZE (R5) settings. Equation 7 is for down-spread SSC and Equation 8 is for center-spread SSC.

$$\text{Down-spread: SSC\_STEPS} = \text{int}((F_{FOD0}/F_{MOD})/2) \quad (5)$$

$$\text{Center-spread: SSC\_STEPS} = \text{int}((F_{FOD0}/F_{MOD})/4) \quad (6)$$

where:

- F_{FOD0}: FOD0 Frequency
- F_{MOD}: Modulation frequency, use 31.5 kHz for PCIe applications

$$SSC\_STEP\_SIZE = floor((F\_BAW/F\_FOD0 * (1/(1 - SSC\_DEPTH)) - 1))/(SSC\_STEPS) * DEN) \quad (7)$$

$$SSC\_STEP\_SIZE = floor((F\_BAW/F\_FOD0 * (1/(1 - SSC\_DEPTH)) - 1/(1 + SSC\_DEPTH)))/(2 * SSC\_STEPS) * DEN) \quad (8)$$

where:

- SSC_STEP_SIZE: Numerator increment value per step for SSC
- F_{BAW}: BAW frequency, 2467 MHz. Note that the F_{BAW} value varies from device to device.
- SSC_DEPTH: Modulation depth, expressed as a positive value. If –0.5% depth is used, this value is 0.005
- SSC_STEPS: Result from Equation 5 for down-spread or Equation 6 for center-spread
- DEN: Fractional denominator, 2^{24}

If using a mix of SSC on one output and no SSC on a different output, there can be crosstalk between the two outputs. Contact TI to request measurement data for a specific configuration when configuring SSC on only a single output.

When modifying the SSC settings, do not set SSC_EN to a '1' until the other SSC settings have been configured. Perform the following steps for configuring the SSC:

1. Set PDN to a '1'.
2. Set OTP_AUTOLOAD_DIS to a '1'.
3. Modify SSC_MOD_TYPE, SSC_STEP_SIZE, and SSC_STEPS as necessary.
4. Set SSC_EN to a '1'.
5. Set PDN to a '0'.

7.4.2.5 Integer Boundary Spurs

When the decimal portion of the FOD divide value is near an integer boundary, integer boundary spurs can occur. In general, this "integer boundary" is when the decimal portion is between 0.9 and 1, or 0 and 0.1. For example, if the BAW frequency is 2467 MHz, and an output of 122.88 MHz, then the FOD must run at 245.76 MHz. 2467 MHz divided by 245.76 MHz is approximately 10.038. The decimal portion of the divide value is 0.038, which falls between 0 and 0.1, and thus means that generating a 122.88 MHz output can result in spurs in the 12 kHz to 20 MHz band on the output clock. In some cases, proper frequency planning can account for this by increasing the FOD frequency and the channel divider value. For any concerns about integer boundary spurs for a specific frequency plan, contact TI.

7.4.3 Output Behavior

7.4.3.1 Output Format Selection

This device supports LP-HCSL (both 85Ω and 100Ω internal termination), LVDS, and LVCMOS. For LVCMOS outputs,VDDO can be 1.8V, 2.5V or 3.3V if the VDD is 3.3V. Otherwise, the VDDO must be the same voltage as VDD. When OUT0 and OUT1 use different formats, DC-LVDS and differential LVCMOS are 180 degrees out of phase from all other formats.

Table 7-5. Output Format via Registers

OUT0_FMT / OUT1_FMT	Description
0x0	LP-HCSL 100Ω Termination
0x1	LP-HCSL 85Ω Termination
0x2	AC-coupled LVDS
0x3	DC-coupled LVDS
0x4	LVCMOS enabled on OUTx_P LVCMOS disabled on OUTx_N
0x5	LVCMOS disabled on OUTx_P LVCMOS enabled on OUTx_N
0x6	LVCMOS enabled on OUTx_P LVCMOS enabled on OUTx_N 180 degrees out of phase (1)
0x7	LVCMOS enabled on OUTx_P LVCMOS enabled on OUTx_N OUTx_P and OUTx_N in phase

(1) For best output performance, TI recommends using 180 degree out of phase LVCMOS if both OUTx_P and OUTx_N traces are required.

In OTP mode, the FMT_ADDR pin function can be determined by OUT_FMT_SRC_SEL (R9[8]). Table 7-6 describes the output format settings available using the OUT_FMT_SRC_SEL field. If using the FMT_ADDR pin for output format selection, the pin must not be configured for individual output enable.

Table 7-6. FMT_ADDR Output Format Options

OUT_FMT_SRC_SEL	FMT_ADDR Pin	Output Format
0	X	Set by OUT0_FMT (R6[2:0])/ OUT1_FMT (R7[4:2])
1	GND	LP-HCSL 100Ω Termination
1	VDD	LP-HCSL 85Ω Termination

7.4.3.1.1 Output Format Types

Figure 7-5 through Figure 7-8 display how to connect the LMK3H0102 outputs based on the output format selected.

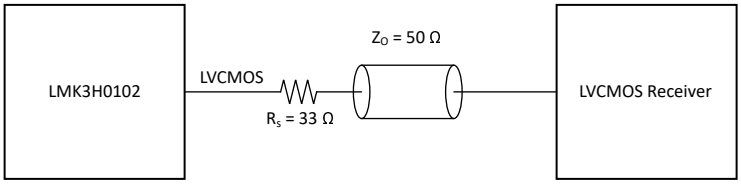


Figure 7-5. Interfacing LMK3H0102 LVCMOS Output With an LVCMOS Receiver

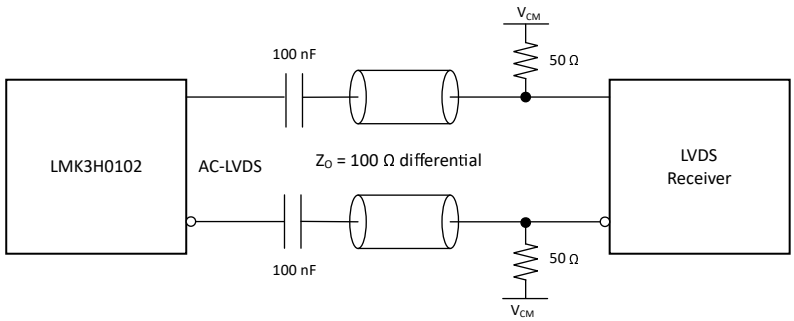


Figure 7-6. Interfacing LMK3H0102 LVCMOS Output With an AC-LVDS Receiver

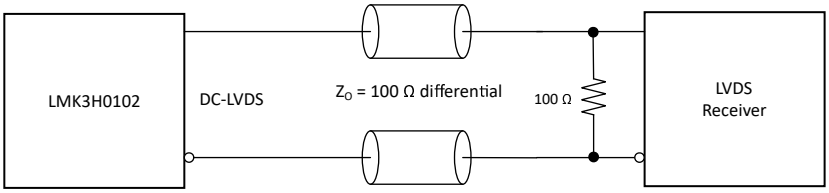


Figure 7-7. Interfacing LMK3H0102 LVCMOS Output With a DC-LVDS Receiver

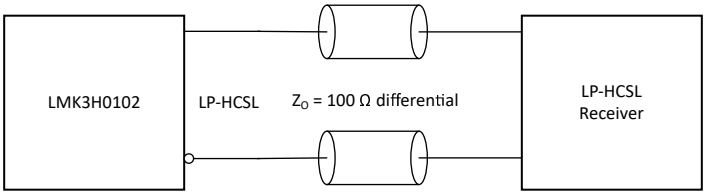


Figure 7-8. Interfacing LMK3H0102 LVCMOS Output With an LP-HCSL Receiver

7.4.3.1.1.1 LP-HCSL Termination

For LP-HCSL outputs, the LMK3H0102 uses internal 50-Ω termination resistors for the termination to GND. External termination resistors are not required.

7.4.3.2 Output Slew Rate Control

For all LVDS and LP-HCSL outputs, the slew rate can be configured. OUT0_SLEW_RATE (R6[4:3]) and OUT1_SLEW_RATE (R7[6:5]) can be used to slow down output slew rate to reduce EMI for OUT0 and OUT1, respectively. Table 7-7 shows the slew rate options available.

Table 7-7. Slew Rate Settings

OUT0_SLEW_RATE OUT1_SLEW_RATE	Slew Rate
0x0	Between 2.3 and 3.5 V/ns
0x1	Between 2.0 and 3.2 V/ns
0x2	Between 1.7 and 2.8 V/ns
0x3	Between 1.4 and 2.7 V/ns

7.4.3.3 REF_CTRL Operation

At start-up, the REF_CTRL pin selects I^2C mode when low, and OTP mode when high. After start-up, REF_CTRL can be programmed to output an LVCMOS REF_CLK, which is derived from either FOD0 or FOD1 followed by an integer divider (/2, /4, /8). Alternatively, this pin can be disabled, or function as a "clock ready" signal. REF_CTRL_PIN_FUNC (R7[14:13]) controls the function of the REF_CTRL pin. Table 7-8 shows these options.

Table 7-8. REF_CTRL Function after Startup

REF_CTRL_PIN_FUNC	REF_CTRL Function
0x0	Disabled, forced low
0x1	Disabled, tri-state
0x2	REF_CLK LVCMOS output
0x3	CLK_READY output

7.4.4 Output Enable

7.4.4.1 Output Enable Control

This device supports synchronous Output Enable (OE). Synchronous OE means there is no glitch on the outputs when OE signal is asserted or deasserted.

The following table shows the enabling and disabling outputs through pin configuration and I^2C. Note that the OE pin must be low **and** OE bit must be "1" for the output to be active. The output enable bits are OUT0_EN (R7[1]) and OUT1_EN (R7[8]).

Table 7-9. OE Functionality

OE Pin	OE Pin Polarity	Software Output Enable OUTx_EN	OUTx
High	Active low	0	Off
High	Active low	1	Off
Low	Active low	0	Off
Low	Active low	1	Running
High	Active high	0	Off
High	Active high	1	Running
Low	Active high	0	Off

Table 7-9. OE Functionality (continued)

OE Pin	OE Pin Polarity	Software Output Enable OUTx_EN	OUTx
Low	Active high	1	Off

7.4.4.2 Output Enable Polarity

OE pin polarity is programmable. When the OE pin is active low, the internal pulldown resistor is automatically enabled, and the internal pullup resistor is disabled. When the OE pin is active high, the internal pullup resistor is automatically enabled, and the internal pulldown resistor is disabled. By default, clock outputs are enabled when the OE pin is floating. The OE pin polarity is set by OE_PIN_POLARITY (R7[0]) as '1' for active-low (default), or '0' for active-high.

7.4.4.3 Individual Output Enable

The FMT_ADDR pin can be reconfigured as a second output enable pin. Set SEPARATE_OE_EN (R11[14]) to enable this functionality. This bit is OTP programmable. When FMT_ADDR is used as an output enable pin, the OE pin controls OUT0, and the FMT_ADDR pin controls OUT1. The OE_PIN_POLARITY (R7[0]) bit applies to the OE and FMT_ADDR pins in this case. If using the FMT_ADDR pin for individual output enable control, the pin must not be configured for I^2C LSB selection or output format selection.

7.4.4.4 Output Disable Behavior

When the outputs are disabled, the outputs can be either tri-state or set to the levels in Table 7-10, determined by OUT0_DISABLE_STATE (R3[5]) for OUT0 and OUT1_DISABLE_STATE (R3[6]) for OUT1.

Table 7-10. Output Disable Behavior

Output Format	OUTx_P	OUTx_N
LP-HCSL	LOW	LOW
AC-LVDS (1)	N/A	N/A
DC-LVDS (2)	HIGH	LOW
LVCMOS, P Only	LOW	LOW
LVCMOS, N Only	LOW	LOW
LVCMOS, Opposite Phase	HIGH	LOW
LVCMOS, In Phase	LOW	LOW

(1) DC-LVDS assumes that the outputs are DC terminated with 100Ohms.

7.4.5 Device Default Settings

Table 7-11 summarizes the default settings of the LMK3H0102V33 and LMK3H0102V18 at start-up for the four OTP pages. In I^2C mode, the Page 0 settings are loaded. For a full list of every default register setting, see *Device Registers*.

Table 7-11. LMK3H0102 Start-up Settings

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
VDD supply voltage	3.3V (LMK3H0102V33) 1.8V (LMK3H0102V18)			
OUT0 Frequency	100MHz	100MHz	100MHz	100MHz
OUT0 Output Format	100Ω LP-HCSL in I2C mode. Set by Pin 2 in OTP mode: • Pin 2 = Low: 100Ω LP-HCSL • Pin 2 = High: 85Ω LP-HCSL	Set by Pin 2: • Pin 2 = Low: 100Ω LP-HCSL • Pin 2 = High: 85Ω LP-HCSL	Set by Pin 2: • Pin 2 = Low: 100Ω LP-HCSL • Pin 2 = High: 85Ω LP-HCSL	Set by Pin 2: • Pin 2 = Low: 100Ω LP-HCSL • Pin 2 = High: 85Ω LP-HCSL

Table 7-11. LMK3H0102 Start-up Settings (continued)

Parameter	OTP Page 0	OTP Page 1	OTP Page 2	OTP Page 3
OUT0 Enable	Enable	Enable	Enable	Enable
OUT0 Differential Slew Rate	2.3V/ns to 3.5V/ns	2.3V/ns to 3.5V/ns	2.3V/ns to 3.5V/ns	2.3V/ns to 3.5V/ns
OUT0 LP-HCSL Amplitude	755mV (typical)	755mV (typical)	755mV (typical)	755mV (typical)
OUT0_P/N Disable Behavior	Low/Low	Low/Low	Low/Low	Low/Low
OUT1 Frequency	100MHz	100MHz	100MHz	100MHz
OUT1 Output Format	100Ω LP-HCSL in I2C mode. Set by Pin 2 in OTP mode: • Pin 2 = Low: 100Ω LP-HCSL • Pin 2 = High: 85Ω LP-HCSL	Set by Pin 2: • Pin 2 = Low: 100Ω LP-HCSL • Pin 2 = High: 85Ω LP-HCSL	Set by Pin 2: • Pin 2 = Low: 100Ω LP-HCSL • Pin 2 = High: 85Ω LP-HCSL	Set by Pin 2: • Pin 2 = Low: 100Ω LP-HCSL • Pin 2 = High: 85Ω LP-HCSL
OUT1 Enable	Enable	Enable	Enable	Enable
OUT1 Differential Slew Rate	2.3V/ns to 3.5V/ns	2.3V/ns to 3.5V/ns	2.3V/ns to 3.5V/ns	2.3V/ns to 3.5V/ns
OUT1 LP-HCSL Amplitude	755mV (typical)	755mV (typical)	755mV (typical)	755mV (typical)
OUT1_P/N Disable Behavior	Low/Low	Low/Low	Low/Low	Low/Low
REF_CTRL Behavior	CLK_READY	CLK_READY	CLK_READY	CLK_READY
FOD0 Frequency	200MHz	200MHz	200MHz	200MHz
FOD1 Frequency	200MHz	200MHz	200MHz	200MHz
SSC Enable	Disable	Enable	Enable	Enable
SSC Modulation Type	N/A	Down-spread	Down-spread	Down-spread
SSC Modulation Depth	N/A	-0.1%	-0.3%	-0.5%
Pin 2 Function	I2C Address LSB Selection (I²C Mode Only Output Format Selection (OTP Mode Only)	I2C Address LSB Selection (I²C Mode Only Output Format Selection (OTP Mode Only)	I2C Address LSB Selection (I²C Mode Only Output Format Selection (OTP Mode Only)	I2C Address LSB Selection (I²C Mode Only Output Format Selection (OTP Mode Only)

7.5 Programming

The host (DSP, Microcontroller, FPGA, and so forth) configures and monitors the LMK3H0102 through the I²C port. The host reads and writes to a collection of control bits called the register set. The device blocks can be controlled and monitored through a specific grouping of bits located within the register space. In the absence of the host, the LMK3H0102 can be configured to operate in OTP mode from one of four of the on-chip OTP pages, stored in the internal EFUSE, depending on the state of REF_CTRL and OTP_SELx pins. The EFUSE is one-time programmed by TI, and is not rewritable. This means that the values of the registers that are automatically loaded from the EFUSE at power-up can not be customized. However, the values of the registers can be changed subsequently via the I²C register interface. Within the device registers, there are certain bits that have read/write access. Other bits are read-only (an attempt to write to a read only bit does not change the state of the bit). Certain device registers and bits are reserved meaning that the fields must not be changed from the default reset state.

7.5.1 I²C Serial Interface

The I²C port on the LMK3H0102 works as a peripheral device and supports both the 100-kHz standard mode and 400-kHz fast-mode operations. Fast mode imposes a glitch tolerance requirement on the control signals. Therefore, the input receivers ignore pulses of less than 50-ns duration. The I²C timing requirements are provided in the *I2C Interface Specification*. Figure 7-9 shows the timing diagram.

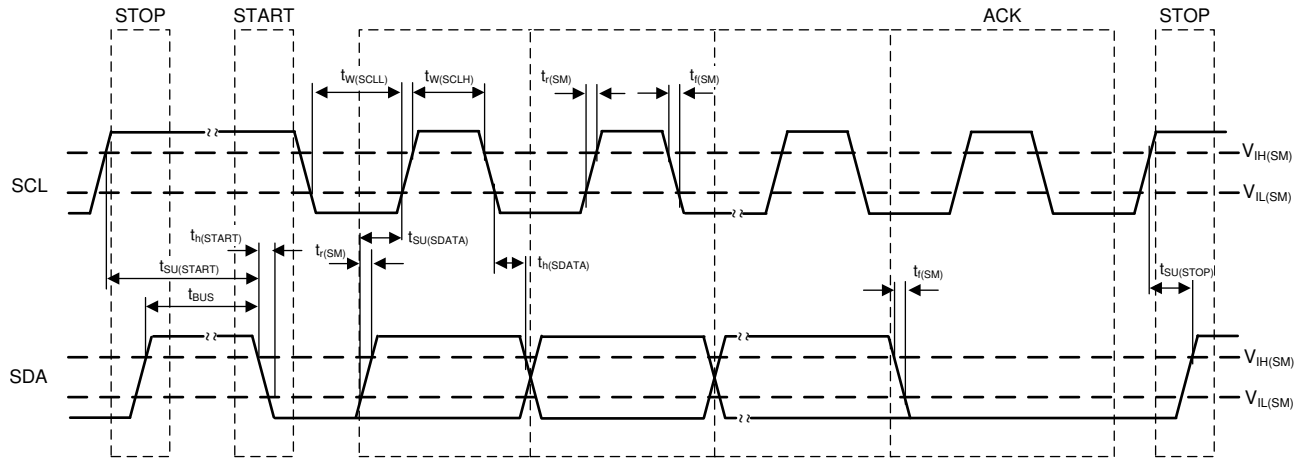


Figure 7-9. I²C Timing Diagram

The LMK3H0102 is accessed through a 7-bit peripheral address transmitted as part of an I²C packet. Only the device with a matching peripheral address responds to subsequent I²C commands. In I²C mode, the LMK3H0102 allows up to four unique peripheral devices to occupy the I2C bus based on the pin strapping of FMT_ADDR (tied to VDD, GND, SDA, or SCL). By default, the device peripheral address is 0b11010xx (the two LSBs are determined by the FMT_ADDR pin). The full address can be configured through I²C.

During the data transfer through the I²C interface, one clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. The start data transfer condition is characterized by a high-to-low transition on the SDA line while SCL is high. The stop data transfer condition is characterized by a low-to-high transition on the SDA line while SCL is high. The start and stop conditions are always initiated by the controller. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit and bytes are sent MSB first. The LMK3H0102 has an 8-bit register address, followed by a 16-bit data word.

The acknowledge bit (A) or non-acknowledge bit (A') is the 9th bit attached to any 8-bit data byte and is always generated by the receiver to inform the transmitter that the byte has been received (when A = 0) or not (when A' = 0). A = 0 is done by pulling the SDA line low during the 9th clock pulse and A' = 0 is done by leaving the SDA line high during the 9th clock pulse.

The I²C controller initiates the data transfer by asserting a start condition which initiates a response from all peripheral devices connected to the serial bus. Based on the 8-bit address byte sent by the controller over the SDA line (consisting of the 7-bit peripheral address (MSB first) and an R/W' bit), the device whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data transfer with the controller.

After the data transfer occurs, stop conditions are established. In write mode, the controller asserts a stop condition to end data transfer during the 10th clock pulse following the acknowledge bit for the last data byte from the peripheral. In read mode, the controller receives the last data byte from the peripheral but does not pull SDA low during the 9th clock pulse. This is known as a non-acknowledge bit. By receiving the non-acknowledge bit, the peripheral knows the data transfer is finished and enters the idle mode. The controller then takes the data line low during the low period before the 10th clock pulse, and high during the 10th clock pulse to assert a stop condition. Figure 7-10 and Figure 7-11 show the sequence for block writes and block reads using the LMK3H0102, respectively.

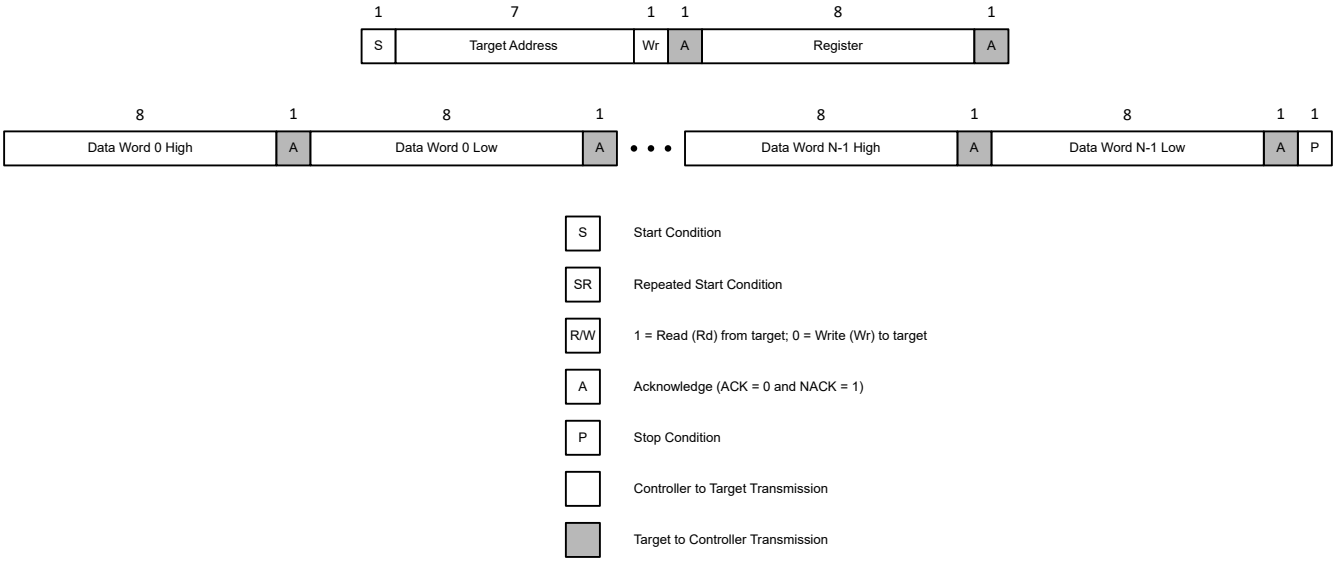


Figure 7-10. Generic Block Write Sequence

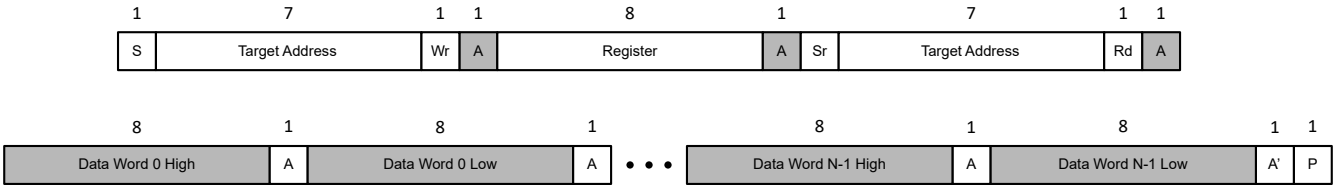


Figure 7-11. Generic Block Read Sequence

7.5.2 One-Time Programming Sequence

The upper register space includes all registers from R13 onward, as well as I2C_ADDR (R12[15:8]). Unlocking the upper register space is performed by writing 0x5B to UNLOCK_PROTECTED_REG (R12[7:0]), leaving I2C_ADDR unchanged. If using the edge combiner, performing the unlock first is required before modifying R146, R147, and R148.

There are six fields that can have different values depending on the EFUSE page loaded at device start-up.

- OUT0 Output Format
- OUT0 Enable
- OUT1 Output Format
- OUT1 Enable
- SSC Enable
- SSC Configuration (either preconfigured or custom)

All other fields retain the same value across all four EFUSE pages. For generating custom configurations, contact TI.

8 Device Registers

8.1 Register Maps

Table 8-1 lists the LMK3H0102 Device registers. All register offset address not listed in Table 8-1 can be considered as reserved locations and the register contents must not be modified.

Table 8-1. LMK3H0102 Registers

Address	Acronym	Section
0x0	R0	Go
0x1	R1	Go
0x2	R2	Go
0x3	R3	Go
0x4	R4	Go
0x5	R5	Go
0x6	R6	Go
0x7	R7	Go
0x8	R8	Go
0x9	R9	Go
0xA	R10	Go
0xB	R11	Go
0xC	R12	Go
0x92	R146	Go
0x93	R147	Go
0x94	R148	Go
0xEE	R238	Go

Complex bit access types are encoded to fit into small table cells. Table 8-2 shows the codes that are used for access types in this section.

Table 8-2. LMK3H0102 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
WL	W L	Write Locked, requires UNLOCK_PROTECTED_REG (R12[7:0]) = 0x5B to unlock and write successfully

8.1.1 R0 Register (Address = 0x0) [reset = 0x0861/0x0863]

R0 is shown in Table 8-3.

Return to the Summary Table.

Table 8-3. R0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	DIG_CLK_N_DIV	R/W	0x02	Digital State Machine clock rate. Derived from the FOD frequency sourced by the CH0_FOD_SEL multiplexer. The target for the frequency is 50MHz maximum. The actual divide value is the DIG_CLK_N_DIV value plus 2. This field is stored in the EFUSE.
9:3	FOD0_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD0 frequency. This field is stored in the EFUSE.
2:1	SUP_LVL_SEL	R/W	0x0 (V33) 0x1 (V18)	Operating voltage for core supply LDO. This field is factory programmed, and **must not** be overwritten with a different value than the programmed value. Supply voltage on VDD and VDDO pins **must not** exceed the selected voltage value + 10%. 0: 3.3V 1: 1.8V 2: 2.5V
0	OTP_BURNT	R/WL	0x1	Indicates that the EFUSE has been programmed. If this field is '1', the EFUSE is programmed.

8.1.2 R1 Register (Address = 0x1) [reset = 0x5599]

R1 is shown in Table 8-4.

Return to the Summary Table.

Table 8-4. R1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	FOD0_NUM[23:16]	R/W	0x55	High byte of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
7:0	ADC_CLK_N_DIV	R/W	0x99	ADC clock frequency in MHz, derived directly from BAW. Default is ceil(2467 / 16) - 2 = 0x9B. This field is stored in the EFUSE. TI does not recommend modifying the value of this field.

8.1.3 R2 Register (Address = 0x2) [reset = 0xC28F]

R2 is shown in Table 8-5.

Return to the Summary Table.

Table 8-5. R2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD0_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD0 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

8.1.4 R3 Register (Address = 0x3) [reset = 0x1801]

R3 is shown in Table 8-6.

Return to the Summary Table.

Table 8-6. R3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:9	FOD1_N_DIV	R/W	0x0C	Integer Ratio of BAW frequency to FOD1 frequency. This field is stored in the EFUSE.
8	CH1_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 1. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.

Table 8-6. R3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	CH1_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 1 or using the Edge Combiner as the input source for Output Driver 1. This field is stored in the EFUSE. 0h: Channel Divider 1 input 1h: Edge Combiner input
6	OUT1_DISABLE_STATE	R/W	0x0	When OUT1 is disabled, this bit selects whether the OUT1_P and OUT1_N pins are forced to GND or tri-state. This field is stored in the EFUSE. 0h: Forced to GND on disable. 1h: Tri-state on disable.
5	OUT0_DISABLE_STATE	R/W	0x0	When OUT0 is disabled, this bit selects whether the OUT0_P and OUT0_N pins are forced to GND or tri-state. This field is stored in the EFUSE. 0h: Forced to GND on disable. 1h: Tri-state on disable.
4	CH0_FOD_SEL	R/W	0x0	Selects the FOD to use as the input source for Channel Divider 0. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
3	CH0_EDGE_COMB_EN	R/W	0x0	Selects between using Channel Divider 0 or using the Edge Combiner as the input source for Output Driver 0. This field is stored in the EFUSE. 0h: Channel Divider 0 input 1h: Edge Combiner input
2:0	CH0_DIV	R/W	0x1	Divider value for Channel Divider 0. This field is stored in the EFUSE. 0h: Channel Divider disabled. Set CH0_DIV to '0' when using the edge combiner for OUT0. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40

8.1.5 R4 Register (Address = 0x4) [reset = 0x0000]

R4 is shown in Table 8-7.

Return to the Summary Table.

Table 8-7. R4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R	N/A	Reserved, do not write to this field.
14:2	SSC_STEPS	R/W	0x0000	Number of steps in each segment of the triangular profile for SSC. See Spread Spectrum Clocking for instructions to calculate this value. This field is stored in the EFUSE.
1	SSC_MOD_TYPE	R/W	0x0	Selects between down-spread or center-spread modulation for custom SSC configurations. This field is stored in the EFUSE. 0h: Down-spread modulation. 1h: Center-spread modulation.
0	SSC_EN	R/W	0x0	Enable SSC. This field is stored in the EFUSE. 0h: SSC Disabled. 1h: SSC Enabled.

8.1.6 R5 Register (Address = 0x5) [reset = 0x0000]

R5 is shown in Table 8-8.

Return to the Summary Table.

Table 8-8. R5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	SSC_STEP_SIZE	R/W	0x0000	Numerator increment value per step for SSC. See Spread Spectrum Clocking for instructions to calculate this value. This field is stored in the EFUSE.

8.1.7 R6 Register (Address = 0x6) [reset = 0x2AA0]

R6 is shown in Table 8-9.

Return to the Summary Table.

Table 8-9. R6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	CH1_DIV	R/W	0x0	Divider value for Channel Divider 1. This field is stored in the EFUSE. 0h: Channel Divider disabled. Set CH1_DIV to '0' when using the edge combiner for OUT1. 1h: FOD / 2 2h: FOD / 4 3h: FOD / 6 4h: FOD / 8 5h: FOD / 10 6h: FOD / 20 7h: FOD / 40
12:5	FOD1_NUM[23:16]	R/W	0x55	High byte of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.
4:3	OUT0_SLEW_RATE	R/W	0x3	Slew rate control for OUT0. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
2:0	OUT0_FMT	R/W	0x0	Selects the output format for OUT0. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.

8.1.8 R7 Register (Address = 0x7) [reset = 0x6503]

R7 is shown in Table 8-10.

Return to the Summary Table.

Table 8-10. R7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	N/A	0x0	Reserved, do not write to this field.

Table 8-10. R7 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:13	REF_CTRL_PIN_FUNC	R/W	0x1	Sets the function of the REF_CTRL pin. This field is stored in the EFUSE. 0h: REF_CTRL pin disabled, pulled to GND. 1h: REF_CTRL pin disabled, tri-state. 2h: REF_CTRL pin functions as an additional LVCMOS REF_CLK output. 3h: REF_CTRL pin functions as "clock ready" signal.
12:11	REF_CLK_DIV	R/W	0x0	REF_CLK output divisor value when REF_CTRL is used as REF_CLK. This field is stored in the EFUSE. 0h: REF_CLK disabled. 1h: FOD / 2. 2h: FOD / 4. 3h: FOD / 8.
10	Reserved	R/W	0x1	Reserved. Do not write any value other than '1' to this field.
9	REF_CLK_FOD_SEL	R/W	0x0	Select the FOD used to generate the REF_CLK output. This field is stored in the EFUSE. 0h: FOD0. 1h: FOD1.
8	OUT1_EN	R/W	0x0	Output Enable bit for OUT1. This field is stored in the EFUSE. 0h: OUT1 is disabled. 1h: OUT1 is enabled.
7	OUT1_CH_SEL	R/W	0x0	Selects the source for OUT1. If the Edge Combiner is enabled, then this bit is ignored. This field is stored in the EFUSE. 0h: OUT1 is sourced from Channel Divider 0 if CH0_EDGE_COMB_EN is a '0', or the Edge Combiner if CH0_EDGE_COMB_EN is a '1'. 1h: OUT1 is sourced from Channel Divider 1 if CH1_EDGE_COMB_EN is a '0', or the Edge Combiner if CH1_EDGE_COMB_EN is a '1'.
6:5	OUT1_SLEW_RATE	R/W	0x0	Slew rate control for OUT1. This field is stored in the EFUSE. Only applies to differential output formats. 0h: Between 2.3V/ns and 3.5V/ns. 1h: Between 2.0V/ns and 3.2V/ns. 2h: Between 1.7V/ns and 2.8V/ns. 3h: Between 1.4V/ns and 2.7V/ns.
4:2	OUT1_FMT	R/W	0x0	Selects the output format for OUT1. This field is stored in the EFUSE. 0h: LP-HCSL 100Ω Termination. 1h: LP-HCSL 85Ω Termination. 2h: AC-coupled LVDS. 3h: DC-coupled LVDS. 4h: LVCMOS, OUTx_P enabled, OUTx_N disabled. 5h: LVCMOS, OUTx_P disabled, OUTx_N enabled. 6h: LVCMOS, OUTx_P enabled, OUTx_N enabled, 180 degrees out of phase. 7h: LVCMOS, OUTx_P enabled, OUTx_N enabled, OUTx_P and OUTx_N in phase.
1	OUT0_EN	R/W	0x0	Output Enable bit for OUT0. This field is stored in the EFUSE. 0h: OUT0 is disabled. 1h: OUT0 is enabled.
0	OE_PIN_POLARITY	R/W	0x1	OE pin polarity selection. This bit does not affect the polarity of the OUTx_EN bits, only the OE pin. This field is stored in the EFUSE. 0h: OE is active high (OE tied to VDD enables outputs). 1h: OE is active low (OE tied to GND enables outputs).

8.1.9 R8 Register (Address = 0x8) [reset = 0xC28F]

R8 is shown in Table 8-11.

Return to the Summary Table.

Table 8-11. R8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FOD1_NUM[15:0]	R/W	0xC28F	Lower two bytes of the FOD1 fractional divide value. The value of this field changes from device to device. This field is stored in the EFUSE.

8.1.10 R9 Register (Address = 0x9) [reset = 0x3166]

R9 is shown in Table 8-12.

Return to the Summary Table.

Table 8-12. R9 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	OTP_ID	R/W	0x3	Configurable field for identifying the OTP configuration. Can be used in I2C mode as a 4-bit spare field. This field is stored in the EFUSE.
11:9	SSC_CONFIG_SEL	R/W	0x0	SSC modulation configuration. If center-spread modulation is desired, then custom SSC configuration is required. Four preconfigured down-spread modulation depths are also available. Any other modulation depths require custom SSC configuration. This field is stored in the EFUSE. The preconfigured SSC options are specifically for 100MHz clock outputs. For other output frequencies, TI recommends creating a custom SSC configuration. 0h: Custom SSC Configuration - see Spread Spectrum Clocking for details on creating a custom configuration. 1h: –0.10% preconfigured down-spread. 2h: –0.25% preconfigured down-spread. 3h: –0.30% preconfigured down-spread. 4h: –0.50% preconfigured down-spread. All other values: Reserved
8	OUT_FMT_SRC_SEL	R/W	0x1	Forces the FMT_ADDR pin to override the output format register settings in OTP Mode. When in I2C mode, the FMT_ADDR pin is never used for this purpose. This field is stored in the EFUSE. 0h: FMT_ADDR pin is ignored in OTP mode for output format selection. 1h: FMT_ADDR pin overrides the register settings in OTP mode.. The output format is LP-HCSL, and the termination resistor values are based on the FMT_ADDR pin state on start-up.

Table 8-12. R9 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:4	OUT1_LPHSCL_AMP_SEL	R/W	0x3	OUT1 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.
3:0	OUT0_LPHSCL_AMP_SEL	R/W	0x6	OUT0 output swing level when using LP-HCSL output format. This field is stored in the EFUSE. 0h: 625mV. 1h: 647mV. 2h: 668mV. 3h: 690mV. 4h: 712mV. 5h: 733mV. 6h: 755mV. 7h: 777mV. 8h: 798mV. 9h: 820mV. Ah: 842mV. Bh: 863mV. Ch: 885mV. Dh: 907mV. Eh: 928mV. Fh: 950mV.

8.1.11 R10 Register (Address = 0xA) [reset = 0x0010]

R10 is shown in Table 8-13.

Return to the Summary Table.

Table 8-13. R10 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14:11	PROD_REVID	R	N/A	Product revision identifier.
10	CLK_READY	R	N/A	CLK_READY status. The REF_CTRL pin mirrors this status signal when the pin functions as a "clock ready" signal.
9	Reserved	R	N/A	Reserved, do not write to this field.
8	RB_PIN_15	R	N/A	Readback of the REF_CTRL pin.
7	RB_PIN_4	R	N/A	Readback of the OTP_SEL1/SDA pin.

Table 8-13. R10 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	RB_PIN_3	R	N/A	Readback of the OTP_SEL0/SCL pin.
5	RB_PIN_2	R	N/A	Readback of the FMT_ADDR pin.
4	DEV_IDLE_STATE_SEL	R/W	0x1	This bit controls the behavior of the device when both outputs are disabled. Placing the device into a low-power state is not recommended for PCIe applications, as the time to re-enable the clocks is extended. This field is stored in the EFUSE. 0h: When both outputs are disabled, the outputs are muted, and the device is placed into a low-power state. 1h: When both outputs are disabled, the outputs are muted. The device does not enter a low-power state.
3	PIN_RESAMPLE_DIS	R/W	0x0	This bit controls the resampling of the device pins when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: Pin resampling is enabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are resampled. If FMT_ADDR is high, the device enters OTP Mode. 1h: Pin resampling is disabled. When exiting the low power mode, the FMT_ADDR, OTP_SEL0/SCL, OTP_SEL1/SDA, and FMT_ADDR pins are not resampled. The device remains in I2C Mode.
2	OTP_AUTOLOAD_DIS	R/W	0x0	This bit controls the behavior of the device when exiting the low power mode. Write this bit while in the low power mode. TI recommends keeping this bit as a '1' unless the functionality is explicitly desired. 0h: OTP autoload is enabled. When exiting the low power mode, the contents of OTP Page 0 are written to the device registers. 1h: OTP autoload is disabled. When exiting the low power mode, the contents of OTP Page 0 are not written to the device registers.
1	PDN	R/W	0x0	Writing a '1' to this bit puts the device into a low power state.
0	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.

8.1.12 R11 Register (Address = 0xB) [reset = 0x0000]

R11 is shown in Table 8-14.

Return to the Summary Table.

Table 8-14. R11 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	Reserved	R/W	0x0	Reserved. Only write '0' to this bit.
14	SEPARATE_OE_EN	R/W	0x0	This bit enables the separate output enable functionality of the device. If this bit is a '1', then OUT_FMT_SRC_SEL and I2C_ADDR_LSB_SEL must be set to '0'. This field is stored in the EFUSE. 0h: Pin 1 is the output enable for OUT0 and OUT1. 1h: Pin 1 is the output enable for OUT0, Pin 2 is the output enable for OUT1.
13:0	Reserved	R/W	0x0000	Reserved, do not write to this field.

8.1.13 R12 Register (Address = 0xC) [reset = 0x6800]

R12 is shown in Table 8-15.

Return to the Summary Table.

Table 8-15. R12 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	I2C_ADDR_LSB_SEL	R/WL	0x0	I2C peripheral address source. If this bit is a '1', SEPARATE_OE_EN must be '0'. This field is stored in the EFUSE. 0h: I2C peripheral address comes entirely from the I2C_ADDR field. 1h: The two lowest bits of the I2C peripheral address come from the FMT_ADDR pin, all other bits come from R12[14:10].
14:8	I2C_ADDR	R/WL	0x68	I2C peripheral address. After writing to this field, the device responds to the new I2C address. This field is stored in the EFUSE.
7:0	UNLOCK_PROTECTED_REG	R/W	0x00	This field locks all registers from R13 onward, in addition to R12[15:8]. Registers R13 onward are largely device calibration registers, and the contents modified if not described in this document. These registers can be read from normally regardless of the unlock status. 5Bh: Unlocks register writes for R12[15:8] and above. Any other value: R12[15:8] and above ignore all writes.

8.1.14 R146 Register (Address = 0x92) [reset = 0x0000]

R146 is shown in Table 8-16.

Return to the Summary Table.

Table 8-16. R146 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/WL	0x0	Reserved, do not write to this field.
12:5	DTC1_GAIN_RT	R/WL	0x00	Room temperature gain calibration code for FOD0. The value of this field varies from device to device. This must be averaged with DTC2_GAIN_RT when using the edge combiner. This field is stored in the EFUSE.
4:0	DTC1_GAIN_DELTA_CT	R/WL	0x00	Cold temperature gain calibration code for FOD0. The value of this field varies from device to device. This must be averaged with DTC2_GAIN_DELTA_CT when using the edge combiner. This field is stored in the EFUSE.

8.1.15 R147 Register (Address = 0x93) [reset = 0x0000]

R147 is shown in Table 8-17.

Return to the Summary Table.

Table 8-17. R147 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:11	Reserved	R/WL	0x00	Reserved, do not write to this field.
13:8	DTC2_GAIN_DELTA_CT	R/WL	0x00	Cold temperature gain calibration code for FOD1. The value of this field varies from device to device. This must be averaged with DTC1_GAIN_DELTA_CT when using the edge combiner. This field is stored in the EFUSE.
7:0	DTC1_GAIN_DELTA_HT	R/WL	0x00	Hot temperature gain calibration code for FOD0. The value of this field varies from device to device. This must be averaged with DTC2_GAIN_DELTA_HT when using the edge combiner. This field is stored in the EFUSE.

8.1.16 R148 Register (Address = 0x94) [reset = 0x0000]

R148 is shown in Table 8-18.

Return to the Summary Table.

Table 8-18. R148 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	Reserved	R/WL	0x0	Reserved, do not write to this field.

Table 8-18. R148 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13:8	DTC2_GAIN_DELTA_HT	R/WL	0x00	Hot temperature gain calibration code for FOD1. The value of this field varies from device to device. This must be averaged with DTC1_GAIN_DELTA_HT when using the edge combiner. This field is stored in the EFUSE.
7:0	DTC2_GAIN_RT	R/WL	0x00	Room temperature gain calibration code for FOD1. The value of this field varies from device to device. This must be averaged with DTC1_GAIN_RT when using the edge combiner. This field is stored in the EFUSE.

8.1.17 R238 Register (Address = 0xEE) [reset = 0x0000]

R246 is shown in Table 8-19.

Return to the Summary Table.

Table 8-19. R246 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	BAWFREQ_OFFSET_FIXEDLUT	R/WL	0x0000	Offset value from 2467MHz for the BAW frequency. Signed 16-bit integer value. This field is stored in the EFUSE. Each bit of this fields corresponds to 128ppm of frequency deviation. **This field varies from part to part.** This field is for calculation purposes only, the device does not use this register for any internal calculation. Do **NOT** write to this field.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The LMK3H0102 is a reference-less BAW-based clock generator that can be used to provide reference clocks for various applications, including PCIe reference clocking and 1Gb/10Gb Ethernet Switches.

9.2 Typical Applications

9.2.1 Application Block Diagram Examples

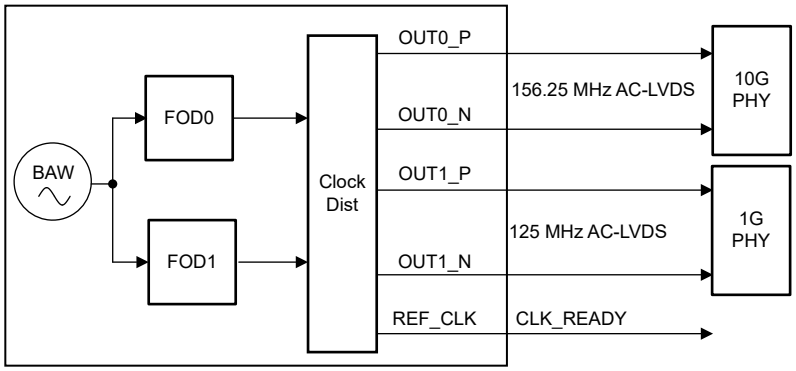


Figure 9-1. 1Gb/10 Gb Ethernet Switch

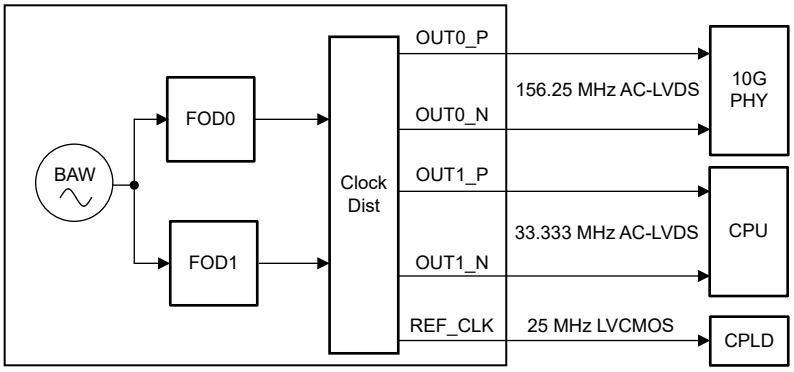


Figure 9-2. 10 Gb Ethernet Switch

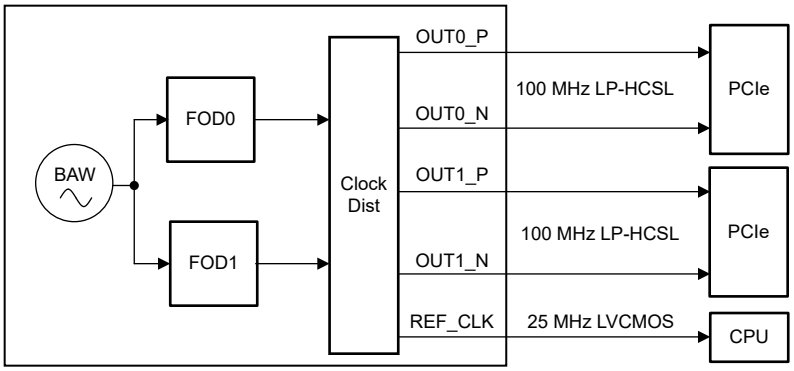


Figure 9-3. PCIe Applications

9.2.2 Design Requirements

Consider a typical PCIe application. In a system such as this, the clocks are expected to be available upon request without the need for any additional device-level programming. A typical output clock requirement in this application is two 100MHz LP-HCSL clocks. A 33MHz clock is added to show how to configure the REF_CLK output as well. The section below describes the detailed design procedure to generate the required output frequencies for the above PCIe scenario using the LMK3H0102.

9.2.3 Detailed Design Procedure

Design of all aspects of the LMK3H0102 is straightforward, and software support is available to assist in frequency planning and part programming. This design procedure gives a straightforward outline of the process.

1. Frequency Planning
   a. The first step of designing an LMK3H0102 configuration is to determine the FOD frequencies that are required to generate the required output frequencies. The process is as such:
      i. If the output frequencies are greater than 200MHz, the frequencies must both be the same, and can not use SSC. If the frequencies are different, or require SSC, then this frequency plan can not be supported by the device.
         - In the case of two identical frequencies greater than 200MHz, the edge combiner must be enabled, the FOD divider values must match, and REF_CLK, if used, can be sourced from either FOD.
      ii. If both output frequencies are the same, and have the same SSC settings (that is, both use SSC or both do not use SSC), only one FOD is required.
      iii. If both output frequencies are different, but have the same SSC settings, the outputs can share an FOD to conserve current. If both frequencies can be generated from dividing a single valid FOD frequency by the channel divider options, then the second FOD can be disabled. Otherwise, both FODs must be used. If both outputs require SSC, then this frequency plan can not be supported by the LMK3H0102 device.
      iv. If one output requires SSC and the other does not, then the SSC output must use FOD0 and the non-SSC output must use FOD1.
   b. If SSC is being used, determine whether or not a preconfigured down-spread modulation, a custom down-spread modulation, or a center-spread modulation is required for the application. If a custom configuration is required, follow the steps outlined in *Spread-Spectrum Clocking*.
   c. Set the digital clock divider such that the digital clock frequency is as close to 50MHz as possible.
   d. Determine the REF_CTRL pin functionality. If this is used as an additional LVCMOS reference clock, verify that the desired frequency can be generated based on the FOD0 and FOD1 frequencies, as the divider range for the REF_CLK output is /2, /4, or /8 only.
      i. Keep in mind that if SSC is used on FOD0, and the REF_CLK source is FOD0, this output now has SSC as well.
2. Setting the Output Formats

a. The output formats that are required are based upon the clock format needed in the system. For PCIe applications, this is most often a 100MHz LP-HCSL clock. The internal termination resistance value must be chosen such that the impedance matches the input impedance of the receiver. Note that the termination scheme is different for AC-LVDS and DC-LVDS - an AC-LVDS receiver requires an AC-LVDS output from the LMK3H0102.
b. For differential outputs, the slew rate is selectable, from the slowest range (1.4V/ns to 2.7V/ns) to the fastest range (2.3V/ns to 3.5V/ns).
c. For LP-HCSL outputs of either termination scheme, the amplitude is selectable between 625mV and 950mV.
d. For LVCMOS outputs, the P and N phases can be in phase, opposite, or individually enabled or disabled. This allows for the generation of up to five LVCMOS clocks between OUT0, OUT1, and the REF_CTRL pin.
    i. For LVCMOS outputs, the VDDO_x voltage MUST match the VDD voltage if VDD is 1.8V or 2.5V.

3. Output Enable Behavior
    a. The output enable pin is active low by default, with an internal pulldown resistor to GND. If this functionality is not desired, then OE_PIN_POLARITY can be set to '0' to change the behavior of the OE pin to active-high. If this is done, the internal pulldown is disabled, and an internal pullup to VDD is used.
    b. Determine whether or not both outputs being disabled means that the device enters low-power mode. While this is able to conserve current, low-power mode is not recommended for any applications where the clocks must turn back on quickly, such as PCIe clocking.

For the PCIe example, the following settings are required:

1. One FOD can be used to generate both LP-HCSL outputs. As such, FOD0 can be set to have an output frequency of 200MHz, with Channel Divider 0 set to divide by two. Alternatively, FOD0 can be set to 400MHz with a divider by four. Both configurations are valid. Both output drivers select Channel Divider 0, and are both set to LP-HCSL.
    a. DIG_CLK_N_DIV must be set to two to set the state machine clock properly. The state machine clock must be as close to 50MHz as possible without exceeding this frequency. Equation 9 shows the relationship between the digital state machine frequency, the frequency selected by the CH0_FOD_SEL multiplexer, and the DIG_CLK_N_DIV field. Write the DIG_CLK_N_DIV field only while the device is in the low power state.
2. FOD1 can be used to generate the 33MHz LVCMOS clock, as FOD0 can not support 33MHz in addition to 100MHz. The REF_CLK divider options are divides by two, four, or eight. While dividing by two does not yield any valid configurations, both 132MHz with a divide by four and 264MHz with a divide by 8 are valid options.

$$F_{DIG} = \frac{F_{CH0\_FOD\_SEL}}{2 + \text{DIG\_CLK\_N\_DIV}} \quad (9)$$

where F_{DIG} is the digital state machine clock frequency and $F_{CH0\_FOD\_SEL}$ is the frequency selected by the CHO_FOD_SEL multiplexer

9.2.4 Example: Changing Output Frequency

If the user wants to change the output from 100-MHz LP-HCSL on OUT0 and OUT1 to 24-MHz differential LVCMOS clocks on OUT0 and OUT1- with an additional LVCMOS clock on the REF_CTRL pin, the value of the BAWFREQ_OFFSET_FIXEDLUT field for this example is 0x3701. The steps for changing the frequency are as follows:

1. Determine the BAW frequency of the device. This is critical for all following calculations. From Equation 4, if BAWFREQ_OFFSET_FIXEDLUT is 0x3701, then the BAW frequency of this device is approximately 2471.446441856.
2. Determine the channel divider settings and required FOD frequency. If the output frequency is 24 MHz, and the range of the FODs is from 100 MHz to 400 MHz, then a channel divider value of at least 5 is required to generate the output. As there is not a divide by 5 option, and REF_CLK must also have a clock (see

CH0_DIV, CH1_DIV, and REF_CLK_DIV), a divide by 8 is required. From here, 24 MHz times 8 yields an FOD output frequency of 192 MHz. If OUT1 were a different frequency, then using FOD1 can be required if both frequencies can not be generated by dividing down from the same FOD frequency.

3. Set the FOD divide values. Use Equation 1 to calculate the integer divide value FOD0_N_DIV = floor(2471.446441856/192) = 12. From Equation 2, the numerator divide value FOD0_NUM = int(((2471.446441856/192) - 12) x 2^{24}) = 14631693
4. Write the desired settings to the device registers. This includes the divider settings listed above, as well as the output driver settings. Follow the procedure outlined in Figure 7-4:
   a. Set PDN = 1.
   b. Set FOD0_N_DIV = 12 and FOD0_NUM = 14631693.
   c. Set CH0_DIV, and REF_CLK_DIV to divide by 8 (by default, OUT1_CH_SEL is set to select Channel Divider 0).
   d. Set OUT0_FMT and OUT1_FMT to select Differential LVCMOS as the output format.
   e. Set REF_CTRL_PIN_FUNC to output REF_CLK.
   f. Set OTP_AUTOLOAD_DIS to 1 (disable the OTP Page 0 autoload feature).
   g. Set DIG_CLK_N_DIV = 2 to set the digital state machine clock to 48 MHz, based on Equation 9
   h. Set PDN = 0

The time required for the frequency change to take affect is typically on the order of 1 ms between issuing PDN = 0 and the output clocks starting at the desired frequency.

9.2.5 Crosstalk

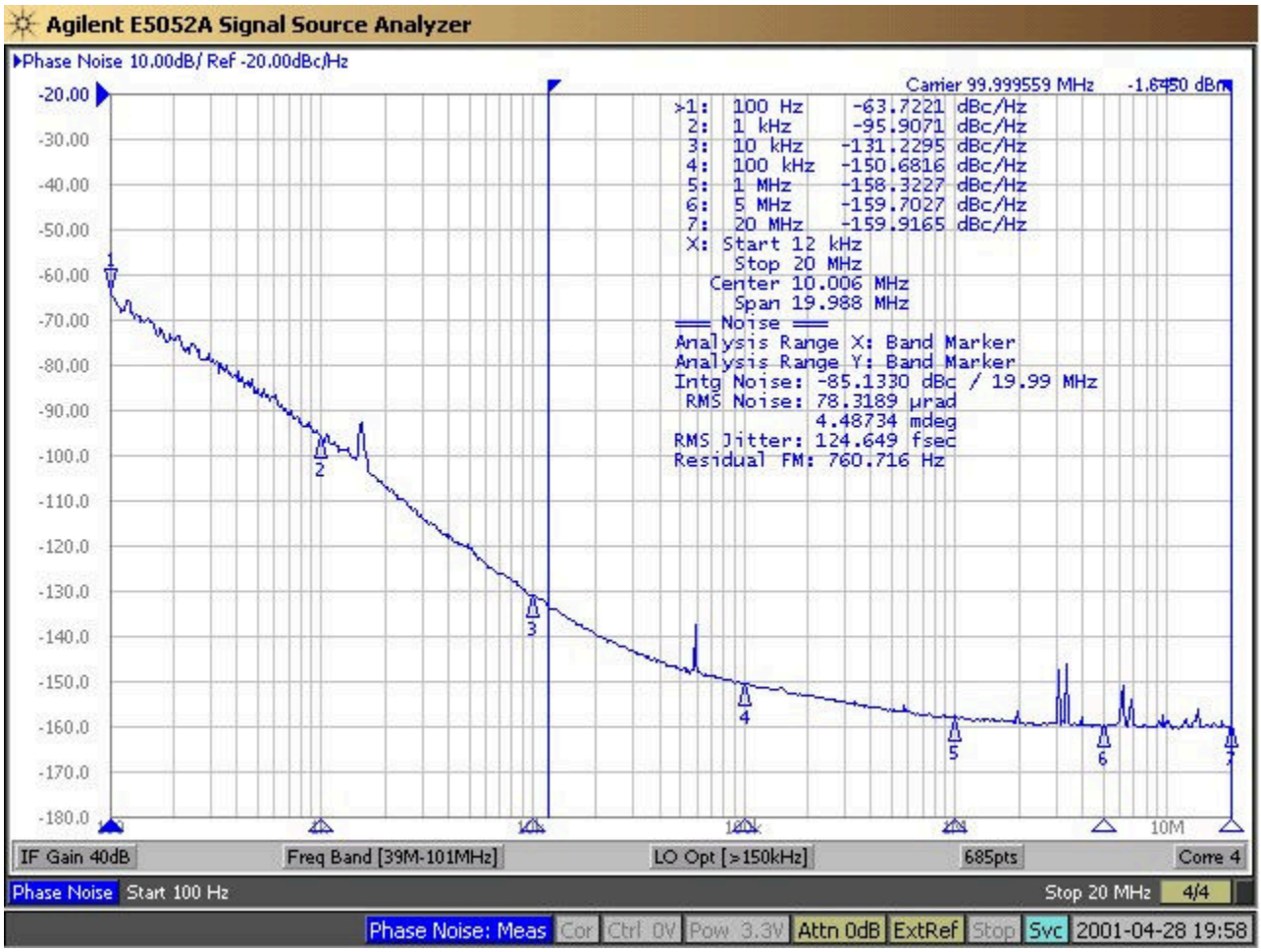
Performance degradation can occur in the LMK3H0102 due to crosstalk in the device when the outputs are operating at different frequencies. Table 9-1 displays the performance of the LMK3H0102 outputs for common LVCMOS frequencies. Contact TI for measurement of additional combinations for impact of crosstalk on output performance.

Table 9-1. LMK3H0102 LVCMOS Output Crosstalk (1)

FOD0 Frequency (MHz)	FOD1 Frequency (MHz)s	OUT0 Frequency (MHz) (2)	OUT1 Frequency (MHz) (2)	Typical OUT0 RMS Jitter (fs) (3)	Typical OUT1 RMS Jitter (fs) (3)
240	250	24	25	852	716
240	270	24	27	457	371
240	200	24	50	832	779
250	240	25	24	784	717
250	270	25	27	757	787
270	240	27	24	429	367
270	250	27	25	913	641
270	200	27	50	865	930
200	240	50	24	806	548
200	270	50	27	913	704

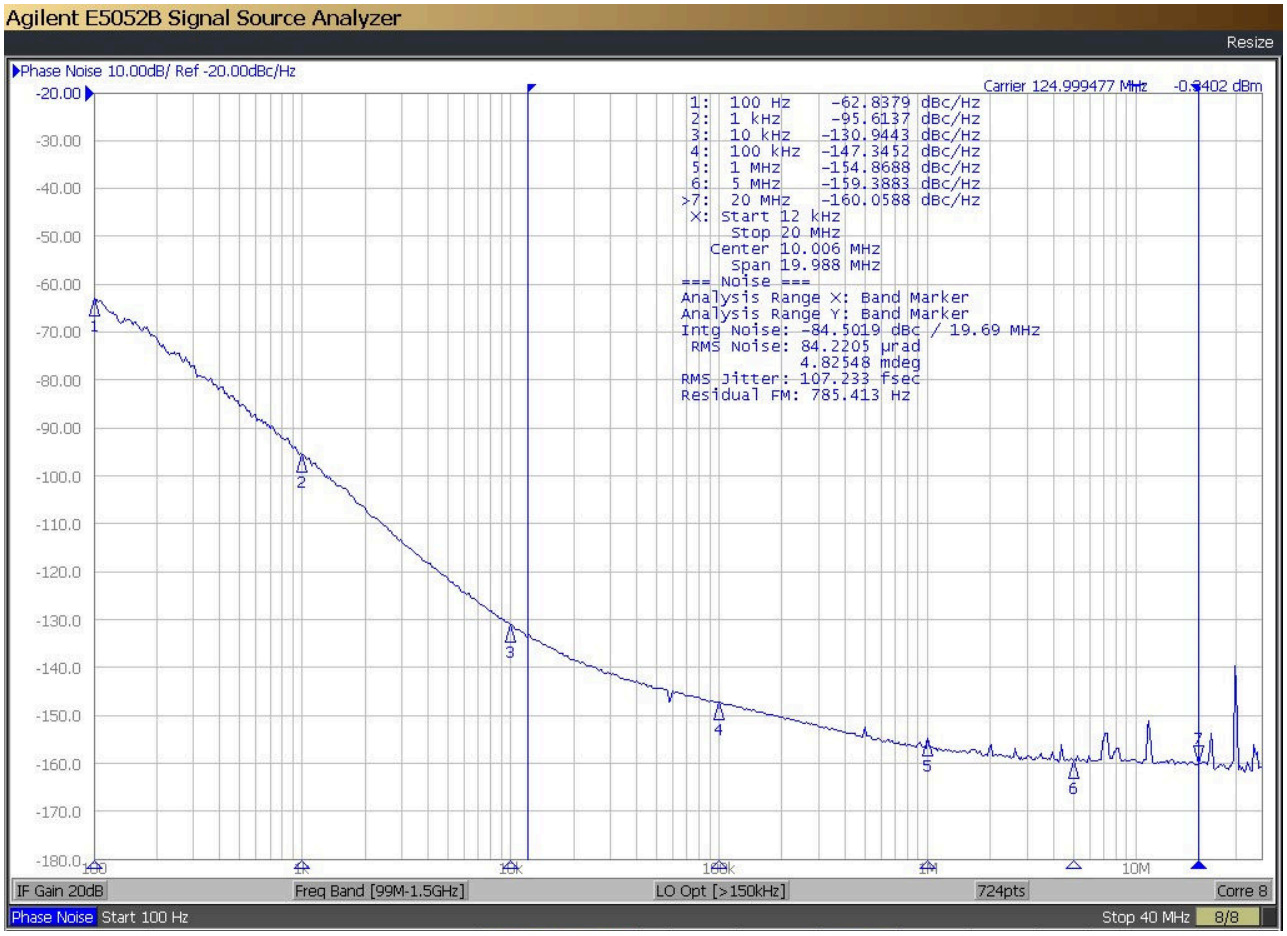
(1) Measured over 25°C to 105°C using differential LVCMOS output formats using VDD = VDDO_x = 3.3V, no SSC.
(2) OUT0 and OUT1 are generated using FOD0 and FOD1, respectively.
(3) RMS Jitter measured over the 12kHz to 5MHz integration bandwidth.

9.2.6 Application Curves



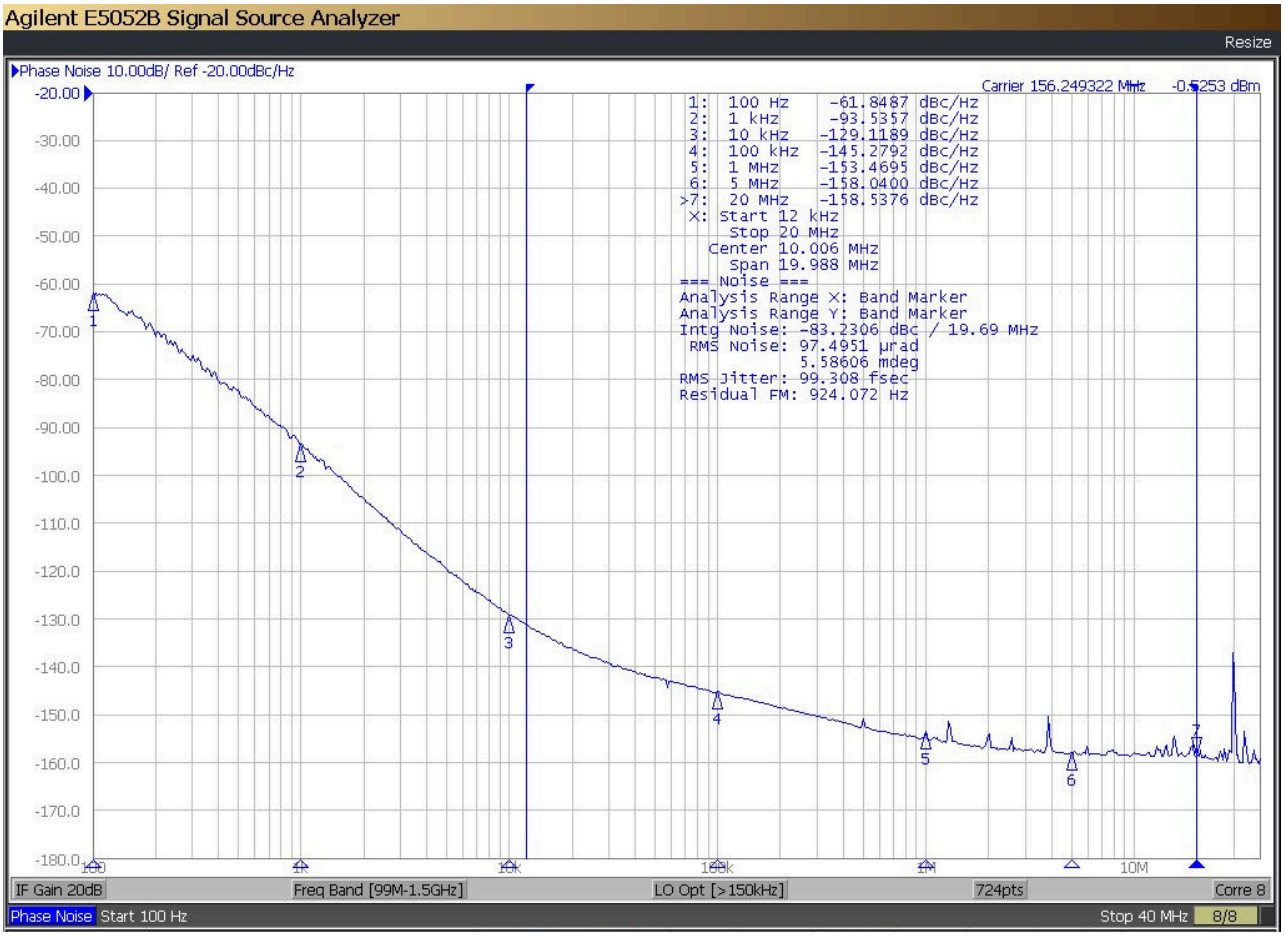
OUT0: 100 MHz LP-HCSL
OUT1: 100 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 125 fs

Figure 9-4. 100-MHz LP-HCSL Output for PCIe Application, Measured on OUT0



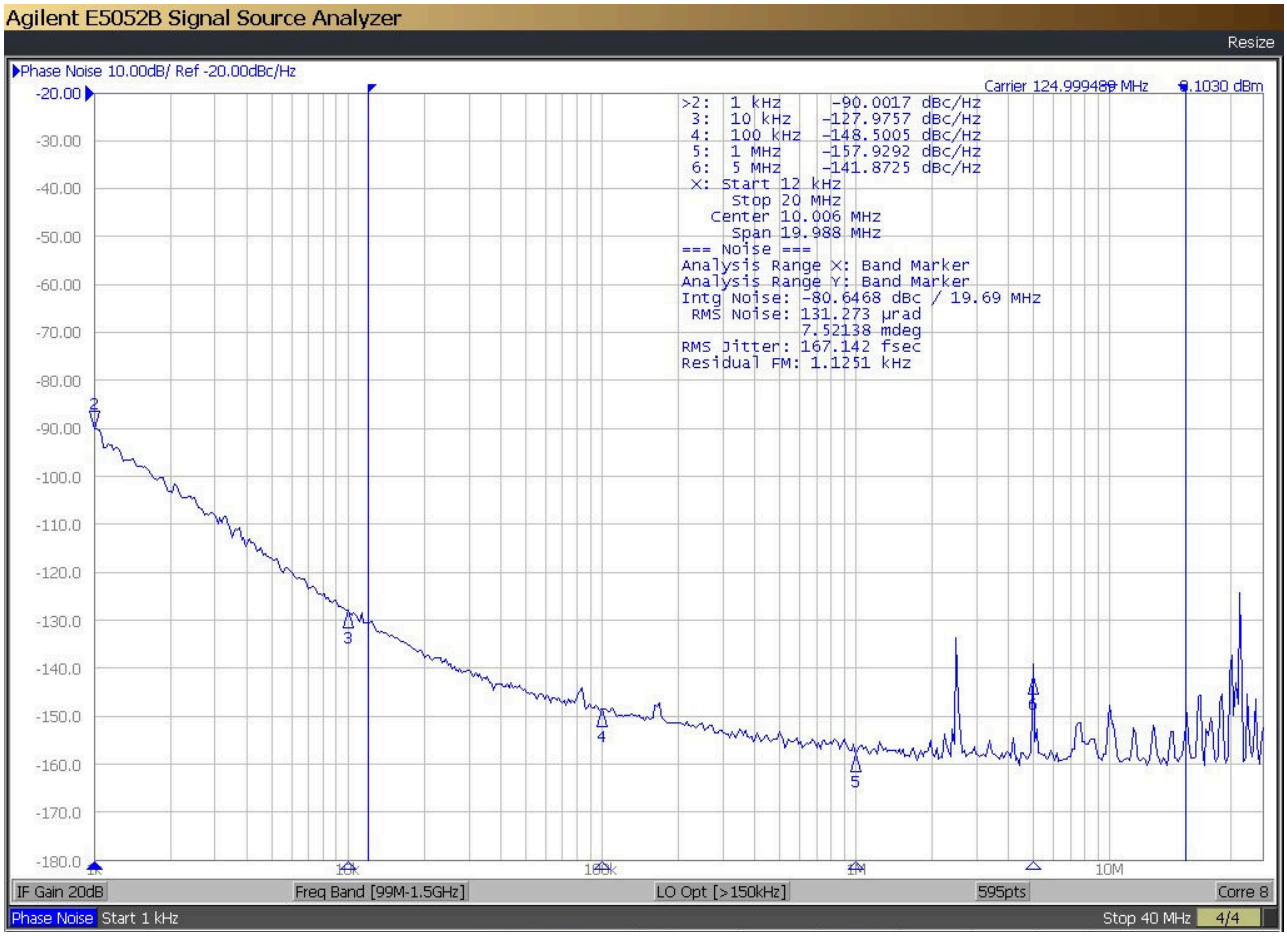
OUT0: 125 MHz LP-HCSL
OUT1: 125 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 107 fs

Figure 9-5. 125-MHz LP-HCSL Output, Measured on OUT0



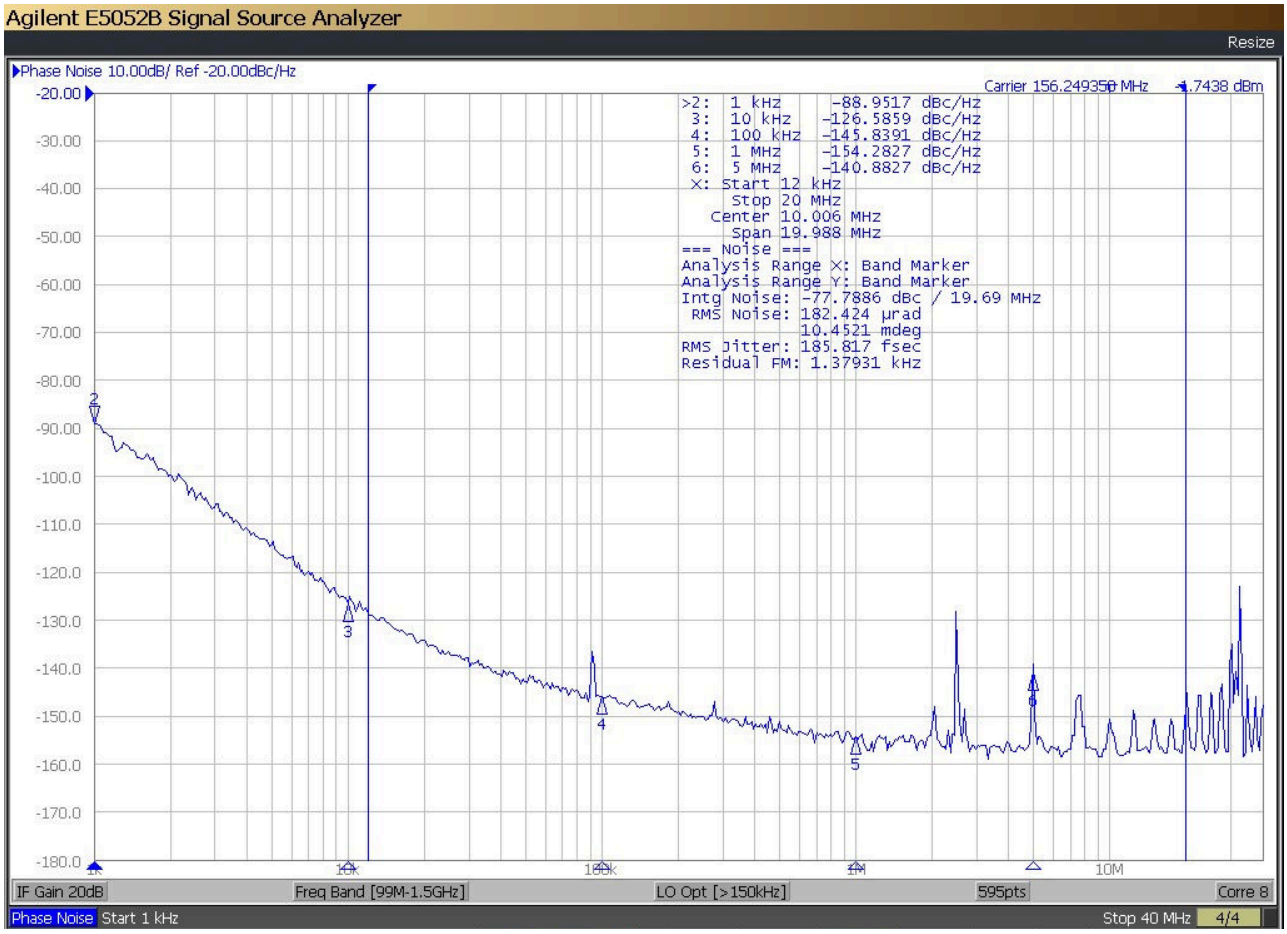
OUT0: 156.25 MHz LP-HCSL
OUT1: 156.25 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 99 fs

Figure 9-6. 156.25-MHz LP-HCSL Output, Measured on OUT0



OUT0: 125 MHz LP-HCSL
OUT1: 156.25 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 167 fs

Figure 9-7. 125-MHz LP-HCSL on OUT0 with 156.25-MHz LP-HCSL on OUT1



OUT0: 125 MHz LP-HCSL
OUT1: 156.25 MHz LP-HCSL
Temperature: 25 °C
12k – 20M RMS Jitter: 186 fs

Figure 9-8. 156.25-MHz LP-HCSL on OUT1 with 125 MHz-LP-HCSL on OUT0

9.3 Power Supply Recommendations

9.3.1 Power-Up Sequencing

The LMK3H0102 provides multiple power supply pins. Each power supply supports 1.8 V, 2.5 V, or 3.3 V. Internal low-dropout regulators (LDO) source the internal blocks and allow each pin to be supplied with individual supply voltages. The VDD pin supplies the control pins, the serial interface, and the REF_CTRL pin. Therefore, any pullup resistors must be connected to the same domain as VDD.

If an output is not used, connect the corresponding VDDO_x rail to VDD. If the VDD and VDDO_x rails are the same voltage, TI recommends connecting these together directly. If VDD and the VDDO_x rails differ, VDD must ramp first, with VDDO_x no more than 5 ms after.

9.3.2 Decoupling Power Supply Inputs

Do not tie VDD and VDDO pins to ground. Use a separate ferrite bead to isolate the VDD and the VDDO supplies. If OUT0 and OUT1 are different frequencies, a separate ferrite bead must be used for each VDDO supply. For each supply voltage pin, a 0.1-µF or 1-µF capacitor must be placed very close to the pin.

9.4 Layout

9.4.1 Layout Guidelines

For this example, follow these guidelines:

- Isolate outputs using a GND shield. Route all outputs as differential pairs.
- Isolate outputs to adjacent outputs when generating multiple frequencies.
- Avoid impedance jumps in the fan-in and fan-out areas when possible.
- Use five vias to connect the thermal pad to a solid GND plane. Full-through vias are preferred.
- Place decoupling capacitors with small capacitance values very close to the supply pins. Place the decoupling capacitors on the same layer or on the bottom layer directly underneath the device. Larger values can be placed more far away. Ferrite beads are recommended to isolate the different output supplies and the VDD supply.
- Use multiple vias to connect wide supply traces to the respective power planes.

9.4.2 Layout Example

Below are printed circuit board (PCB) layout examples that show the application of thermal design practices and a low-inductance ground connection between the device DAP and the PCB.

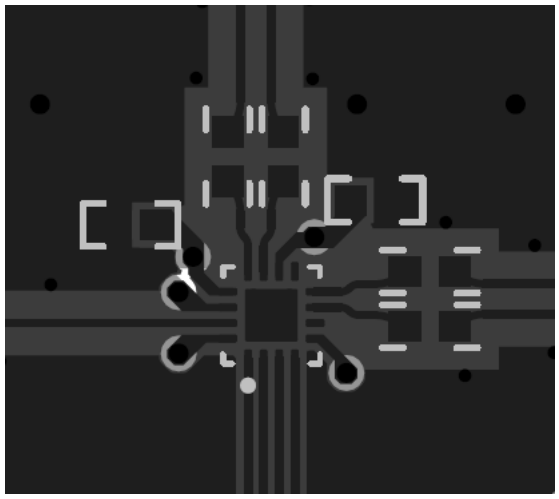


Figure 9-9. PCB Layout Example for LMK3H0102, Top Layer

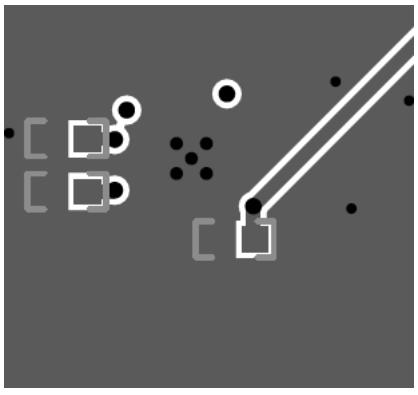


Figure 9-10. PCB Layout Example for LMK3H0102, Bottom Layer

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

For documentation related to the evaluation module, refer to the *LMK3H0102EVM* user's guide.

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2024) to Revision C (October 2024)	Page
• Changed data sheet status from Advanced Information to Production Data	1
• Updated the number formatting for tables, figures, and cross-references throughout the document	1

Changes from Revision A (December 2023) to Revision B (June 2024)	Page
• Updated the number formatting for tables, figures, and cross-references throughout the document	1

Changes from Revision * (November 2023) to Revision A (December 2023)	Page
• Updated the number formatting for tables, figures, and cross-references throughout the document	1

12 Mechanical, Packaging, and Orderable Information

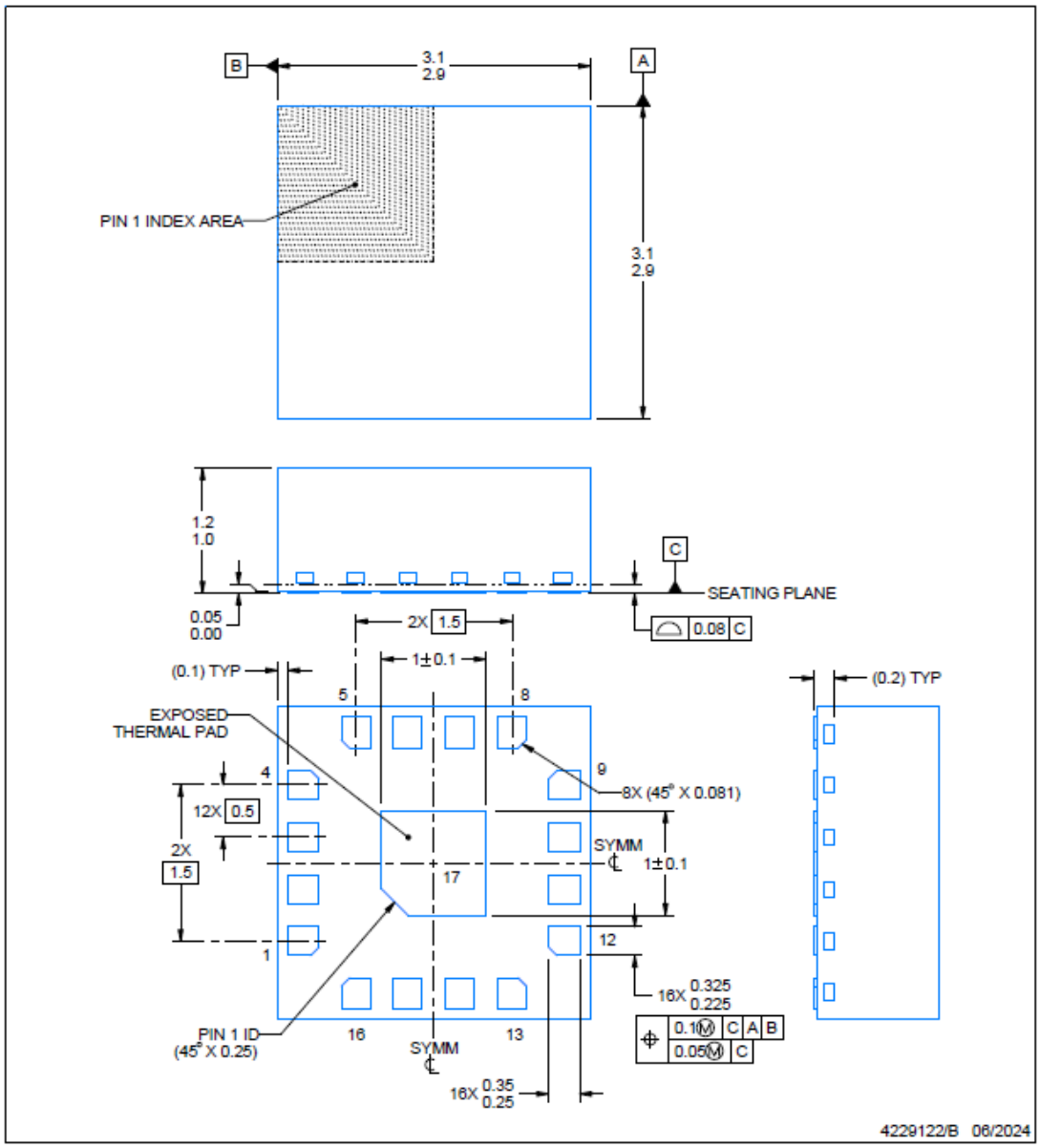
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RER0016A

TQFN - 1.2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



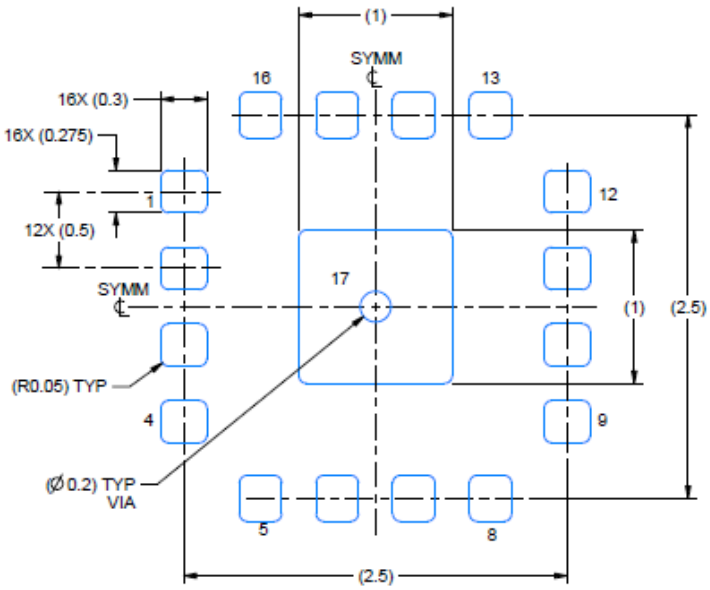
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

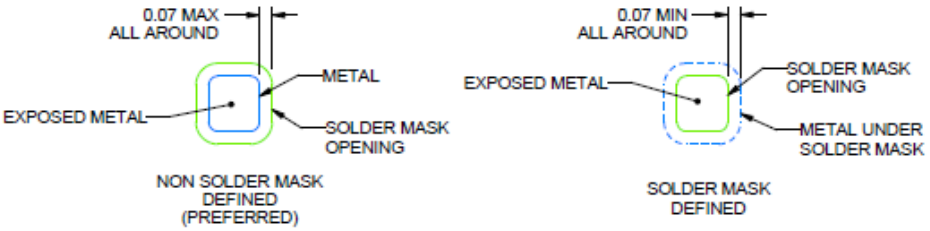
EXAMPLE BOARD LAYOUT

RER0016A — **TQFN - 1.2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

4229122/B 06/2024

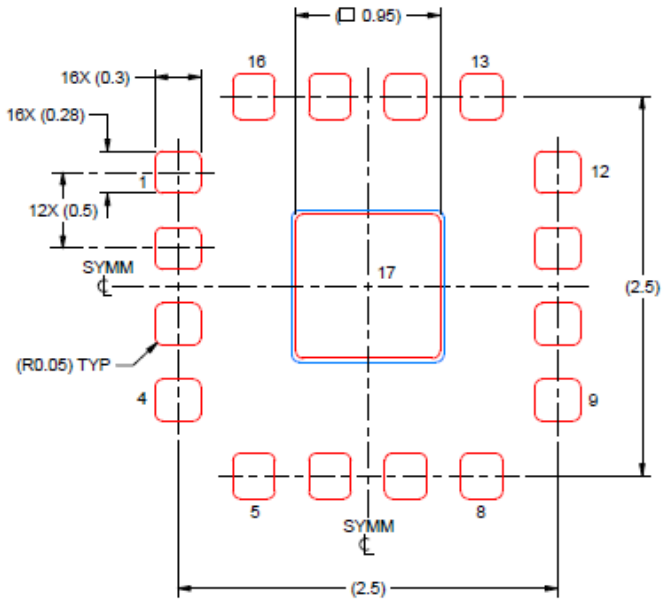
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RER0016A — **TQFN - 1.2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

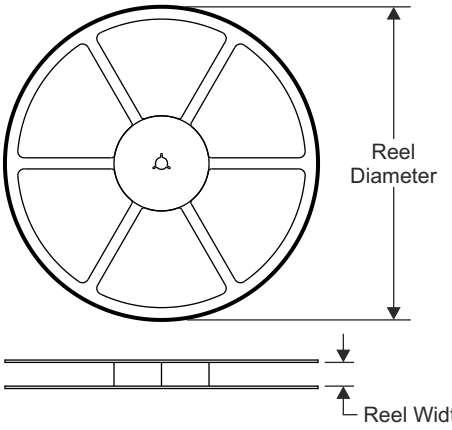
4229122/B 06/2024

NOTES: (continued)

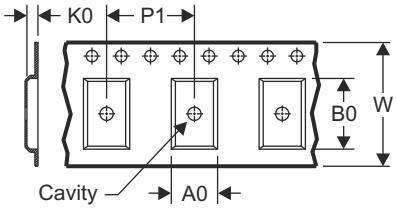
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

12.1 Tape and Reel Information

REEL DIMENSIONS

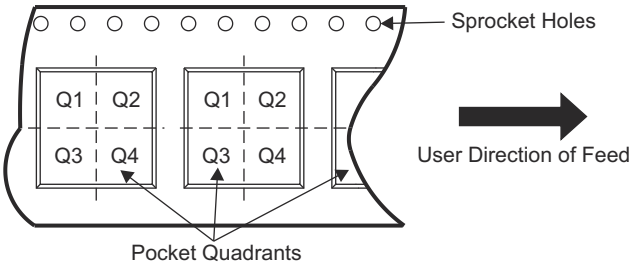


TAPE DIMENSIONS



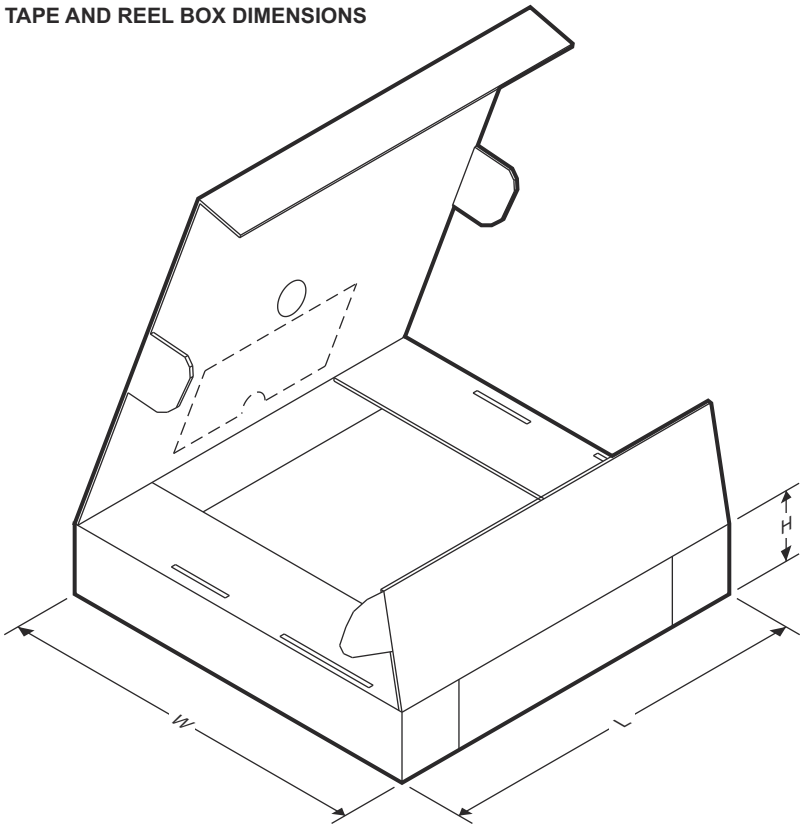
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK3H0102V33RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
LMK3H0102V18RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
LMK3H0102A001RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
LMK3H0102A006RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
LMK3H0102A014RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
LMK3H0102A015RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1
LMK3H0102A016RERR	TQFN	RER0016A	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK3H0102V33RERR	TQFN	RER0016A	16	3000	346	346	33
LMK3H0102V18RERR	TQFN	RER0016A	16	3000	346	346	33
LMK3H0102A001RERR	TQFN	RER0016A	16	3000	346	346	33
LMK3H0102A006RERR	TQFN	RER0016A	16	3000	346	346	33
LMK3H0102A014RERR	TQFN	RER0016A	16	3000	346	346	33
LMK3H0102A015RERR	TQFN	RER0016A	16	3000	346	346	33
LMK3H0102A016RERR	TQFN	RER0016A	16	3000	346	346	33

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