

LMX2522/LMX2532 PLLatinum™ Frequency Synthesizer System with Integrated VCOs

Check for Samples: [LMX2522](#), [LMX2532](#)

FEATURES

- **Small Size**
 - Small 5.0 mm x 5.0 mm x 0.75 mm 28-Pin WQFN Package
- **RF/GPS Synthesizer System**
 - Integrated RF VCO
 - Integrated GPS VCO
 - Integrated Loop Filter
 - Low Spurious, Low Phase Noise Fractional-N RF PLL Based on 11-bit Delta Sigma Modulator
 - 10 kHz Frequency Resolution
- **IF Synthesizer System**
 - Integer-N IF PLL
 - Programmable Charge Pump Current Levels
 - Programmable Frequencies
- **Supports Various Reference Oscillator Frequencies**
 - 19.20/19.68 MHz
- **Fast Lock Time: 500 μ s**
- **Low Current Consumption**
 - 17 mA at 2.8 V
- **2.7 V to 3.3 V Operation**
- **Digital Filtered Lock Detect Output**
- **Hardware and Software Power Down Control**

APPLICATIONS

- **Korean PCS CDMA Systems with GPS**
- **Korean Cellular CDMA Systems with GPS**

DESCRIPTION

LMX2522 and LMX2532 are highly integrated, high performance, low power frequency synthesizer systems optimized for Korean PCS (K-PCS) with GPS and Korean Cellular (K-Cellular) with GPS, CDMA (1xRTT, IS-95) mobile handsets. Using a proprietary digital phase locked loop technique, LMX2522 and LMX2532 generate very stable, low noise local oscillator signals for up and down conversion in wireless communications devices.

LMX2522 and LMX2532 include a RF voltage controlled oscillator (VCO), a GPS VCO, a loop filter, and a fractional-N RF PLL based on a delta sigma modulator. In concert these blocks form a closed loop RF and GPS synthesizer system. LMX2522 supports the Korean PCS band with GPS and LMX2532 supports the Korean Cellular band with GPS.

LMX2522 and LMX2532 include an Integer-N IF PLL also. For more flexible loop filter designs, the IF PLL includes a 4-level programmable charge pump. Together with an external VCO and loop filter, LMX2522 and LMX2532 make a complete closed loop IF synthesizer system.

Serial data is transferred to the device via a three-wire MICROWIRE interface (DATA, LE, CLK).

Operating supply voltage ranges from 2.7 V to 3.3 V. LMX2502 and LMX2512 feature low current consumption: 17 mA at 2.8 V.

LMX2522 and LMX2532 are available in a 28-pin WQFN package.



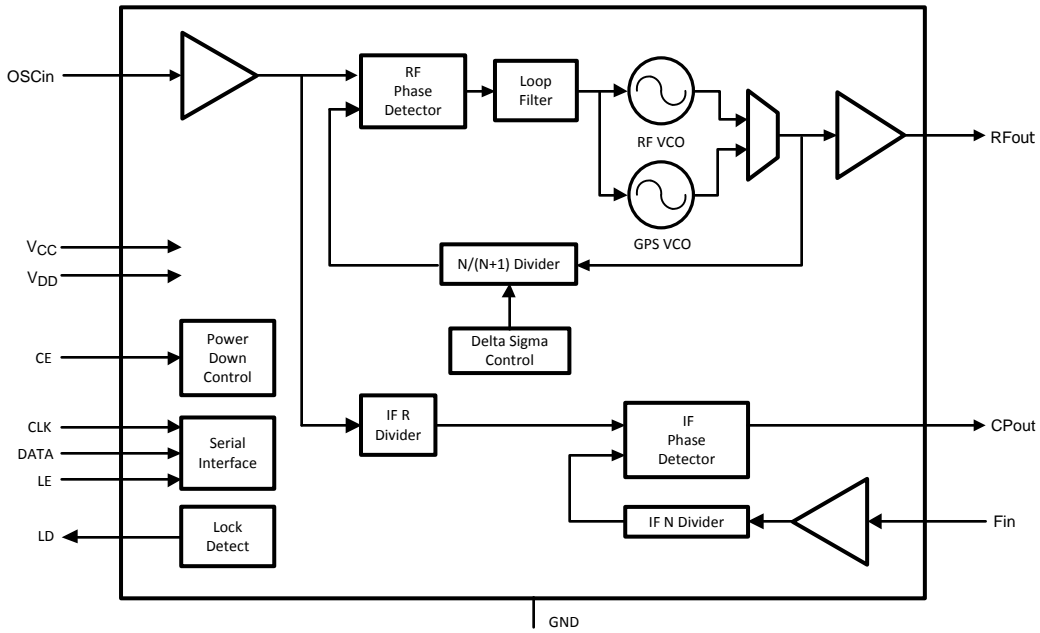
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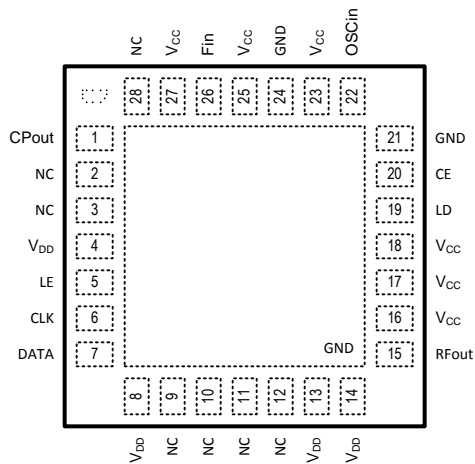
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Functional Block Diagram



Connection Diagram



NOTE: Analog ground connected through exposed die attached pad.

Figure 1. 28-Pin WQFN (NJB) Package

PIN DESCRIPTIONS

| Pin Number | Name | I/O | Description |
|------------|-------------------|-----|--|
| 1 | CPout | O | IF PLL charge pump output |
| 2 | NC | — | Do not connect to any node on printed circuit board. |
| 3 | NC | — | Do not connect to any node on printed circuit board. |
| 4 | V _{DD} | — | Supply voltage for IF analog circuitry |
| 5 | LE | I | MICROWIRE Latch Enable |
| 6 | CLK | I | MICROWIRE Clock |
| 7 | DATA | I | MICROWIRE Data |
| 8 | V _{DD} | — | Supply voltage for VCOs |
| 9 | NC | — | Do not connect to any node on printed circuit board. |
| 10 | NC | — | Do not connect to any node on printed circuit board. |
| 11 | NC | — | Do not connect to any node on printed circuit board. |
| 12 | NC | — | Do not connect to any node on printed circuit board. |
| 13 | V _{DD} | — | Supply voltage for VCOs |
| 14 | V _{DD} | — | Supply voltage for VCOs output buffer |
| 15 | RFout | O | Buffered VCO output |
| 16 | V _{CC} | — | Supply voltage for RF prescaler |
| 17 | V _{CC} | — | Supply voltage for charge pump |
| 18 | V _{CC} | — | Supply voltage for RF digital circuitry |
| 19 | LD | O | Lock Detect |
| 20 | CE | I | Chip Enable control pin |
| 21 | GND | — | Ground for digital circuitry |
| 22 | OSCI _n | I | Reference frequency input |
| 23 | V _{CC} | — | Supply voltage for reference input buffer |
| 24 | GND | — | Ground for digital circuitry |
| 25 | V _{CC} | — | Supply voltage for IF digital circuitry |
| 26 | Fin | I | IF buffer/prescaler input |
| 27 | V _{CC} | — | Supply voltage for IF buffer/prescaler |
| 28 | NC | — | Do not connect to any node on printed circuit board. |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾⁽³⁾

| Parameter | Symbol | Ratings | Units |
|---------------------------|------------------|----------------------|-------|
| Supply Voltage | V_{CC}, V_{DD} | -0.3 to 3.6 | V |
| Voltage on any pin to GND | V_I | -0.3 to $V_{DD}+0.3$ | V |
| | | -0.3 to $V_{CC}+0.3$ | V |
| Storage Temperature Range | T_{STG} | -65 to 150 | °C |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, refer to the Electrical Characteristics section. The ensured specifications apply only for the conditions listed.
- (2) This device is a high performance RF integrated circuit with an ESD rating < 2 kV and is ESD sensitive. Handling and assembly of this device should be done at ESD protected work stations.
- (3) GND = 0 V.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|-------------------------|------------------|-----|-----|-----|-------|
| Ambient Temperature | T_A | -30 | 25 | 85 | °C |
| Supply Voltage (to GND) | V_{CC}, V_{DD} | 2.7 | | 3.3 | V |

Electrical Characteristics

($V_{CC} = V_{DD} = 2.8$ V, $T_A = 25$ °C; unless otherwise noted.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------------------|---|---------------------------------------|-------|-----|----------|-----------|
| I_{CC} PARAMETERS | | | | | | |
| $I_{CC} + I_{DD}$ | Total Supply Current | OB_CRL [1:0] = 00 | | 17 | 19 | mA |
| $(I_{CC} + I_{DD})_{RF}$ | RF PLL Total Supply Current | OB_CRL [1:0] = 00 | | 16 | 18 | mA |
| I_{PD} | Power Down Current ⁽¹⁾ | CE = Low or RF_EN = 0 IF_EN = 0 | | | 20 | µA |
| REFERENCE OSCILLATOR | | | | | | |
| f_{OSCin} | Reference Oscillator Input Frequency ⁽²⁾ | 19.20 MHz and 19.68 MHz are supported | 19.20 | | 19.68 | MHz |
| V_{OSCin} | Reference Oscillator Input sensitivity | | | 0.2 | V_{CC} | V_{P-P} |

- (1) In power down mode, set DATA, CLK and LE pins to 0 V (GND).
- (2) The reference frequency must also be programmed using the OSC_FREQ control bit. For other reference frequencies, please contact Texas Instruments.

Electrical Characteristics (continued)
 $(V_{CC} = V_{DD} = 2.8\text{ V}, T_A = 25\text{ }^\circ\text{C}; \text{ unless otherwise noted.})$

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|----------------|--------------------------------|--------------------|------------------------|---------|---------|---------|---------------|
| RF VCO | | | | | | | |
| f_{RFout} | Frequency Range ⁽³⁾ | LMX2522LQ1635 | RF VCO | 1619.62 | | 1649.62 | MHz |
| | | LMX2532LQ0967 | | 954.42 | | 979.35 | MHz |
| | | LMX2532LQ1065 | | 1052.64 | | 1077.57 | MHz |
| P_{RFout} | RF Output Power | OB_CRL [1:0] = 11 | | -2 | 1 | 4 | dBm |
| | | OB_CRL [1:0] = 10 | | -5 | -2 | 1 | dBm |
| | | OB_CRL [1:0] = 01 | | -7 | -4 | -1 | dBm |
| | | OB_CRL [1:0] = 00 | | -9 | -6 | -3 | dBm |
| | Lock Time ⁽⁴⁾ | LMX2522LQ1635 | 30 MHz Band for RF PLL | | 500 | 800 | μs |
| | | LMX2532LQ0967 | 25 MHz Band for RF PLL | | 500 | 800 | μs |
| | | LMX2532LQ1065 | 25 MHz Band for RF PLL | | 500 | 800 | μs |
| | Reference Spurs | | | | | -75 | dBc |
| | RMS Phase Error | RF PLL in all band | | 1.3 | | | degrees |
| L(f) | Phase Noise | LMX2522LQ1635 | @100 kHz offset | | -113 | -112 | dBc/Hz |
| | | | @1.25 MHz offset | | -138 | -136 | dBc/Hz |
| | | LMX2532LQ0967 | @100 kHz offset | | -117 | -115 | dBc/Hz |
| | | | @900 kHz offset | | -139 | -138 | dBc/Hz |
| | | LMX2532LQ1065 | @100 kHz offset | | -117 | -115 | dBc/Hz |
| | | | @900kHz offset | | -139 | -138 | dBc/Hz |
| | 2nd Harmonic Suppression | | | | | -25 | dBc |
| | 3rd Harmonic Suppression | | | | | -20 | dBc |
| GPS VCO | | | | | | | |
| f_{RFout} | Operating Frequency | LMX2522LQ1635 | GPS VCO | | 1355.04 | | MHz |
| | | LMX2532LQ0967 | | | 1490.04 | | MHz |
| | | LMX2532LQ1065 | | | 1391.82 | | MHz |
| P_{RFout} | Output Power | OB_CRL [1:0] = 11 | | -2 | 1 | 4 | dBm |
| | | OB_CRL [1:0] = 10 | | -5 | -2 | 1 | dBm |
| | | OB_CRL [1:0] = 01 | | -7 | -4 | -1 | dBm |
| | | OB_CRL [1:0] = 00 | | -9 | -6 | -3 | dBm |
| | Lock Time ⁽⁴⁾ | | From RF to GPS PLL | | 600 | 800 | μs |
| | Reference Spurs | | | | | -75 | dBc |
| | RMS Phase Error | RF PLL in all band | | 1.3 | | | degrees |
| L(f) | Phase Noise | @100 kHz offset | | | -113 | -112 | dBc/Hz |
| | | @1.25 MHz offset | | | -138 | -136 | dBc/Hz |
| | 2nd Harmonic Suppression | | | | | -25 | dBc |
| | 3rd Harmonic Suppression | | | | | -20 | dBc |

(3) For other frequency ranges, please contact Texas Instruments.

(4) Lock time is defined as the time difference between the beginning of the frequency transition and the point at which the frequency remains within +/- 1 kHz of the final frequency.

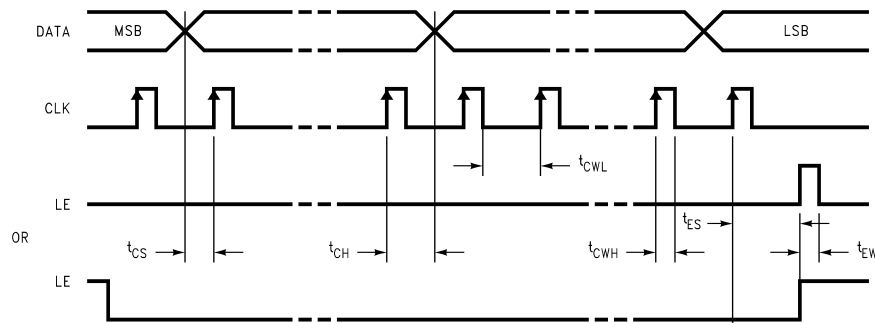
Electrical Characteristics (continued)

($V_{CC} = V_{DD} = 2.8\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$; unless otherwise noted.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|-----------------------------------|-------------------|--------------------------------------|-----|--------------|---------------|
| IF PLL | | | | | | |
| f_{Fin} | Operating Frequency (5) | LMX2522LQ1635 | IF_FREQ [1:0] = 10, Default Value | | 440.76 | MHz |
| | | LMX2532LQ0967 | IF_FREQ [1:0] = 00, Default Value | | 170.76 | MHz |
| | | LMX2532LQ1065 | IF_FREQ [1:0] = 01, Default Value | | 367.20 | MHz |
| P_{Fin} | IF Input Sensitivity | | -10 | | 0 | dBm |
| $f_{\Phi IF}$ | Phase Detector Frequency | | | 120 | | kHz |
| I_{CPout} | Charge Pump Current | IF_CUR [1:0] = 00 | | 100 | | μA |
| | | IF_CUR [1:0] = 01 | | 200 | | μA |
| | | IF_CUR [1:0] = 10 | | 300 | | μA |
| | | IF_CUR [1:0] = 11 | | 800 | | μA |
| DIGITAL INTERFACE (DATA, CLK, LE, LD, CE) | | | | | | |
| V_{IH} | High-Level Input Voltage | | $0.8 V_{DD}$ | | V_{DD} | V |
| | | | $0.8 V_{CC}$ | | V_{CC} | V |
| V_{IL} | Low-Level Input Voltage | | 0 | | $0.2 V_{DD}$ | V |
| | | | 0 | | $0.2 V_{CC}$ | V |
| I_{IH} | High-Level Input Current | | -10 | | 10 | μA |
| I_{IL} | Low-Level Input Current | | -10 | | 10 | μA |
| | Input Capacitance | | | 3 | | pF |
| V_{OH} | High-Level Output Voltage | | $0.9 V_{DD}$ | | | V |
| | | | $0.9 V_{CC}$ | | | V |
| V_{OL} | Low-Level Output Voltage | | | | $0.1 V_{DD}$ | V |
| | | | | | $0.1 V_{CC}$ | V |
| | Output Capacitance | | | | 5 | pF |
| MICROWIRE INTERFACE TIMING | | | | | | |
| t_{CS} | Data to Clock Set Up Time | | 50 | | | ns |
| t_{CH} | Data to Clock Hold Time | | 10 | | | ns |
| t_{CWH} | Clock Pulse Width High | | 50 | | | ns |
| t_{CWL} | Clock Pulse Width Low | | 50 | | | ns |
| t_{ES} | Clock to Latch Enable Set Up Time | | 50 | | | ns |
| t_{EW} | Latch Enable Pulse Width | | 50 | | | ns |

(5) Frequencies other than the default value can be programmed using Words R4 and R5. See [Programming Description](#) for details.

Serial Data Input Timing



FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

LMX2522/32 is a highly integrated frequency synthesizer system that generates LO signals for PCS, Cellular CDMA and GPS systems. These devices include all of the functional blocks of a PLL, RF VCO, prescaler, RF phase detector, and loop filter. The need for external components is limited to a few passive elements for matching the output impedance and bypass elements for power line stabilization.

In addition to the RF circuitry, the IC also includes IF frequency dividers, and an IF phase detector to complete the IF synthesis with an external VCO and loop filter. [Table 4](#) summarizes the counter values to generate the default IF frequencies.

Using a low spurious fractional-N synthesizer based on a delta sigma modulator, the circuit can support 10 kHz channel spacing for PCS, Cellular CDMA and GPS systems.

The fractional-N synthesizer enables faster lock time, which reduces power consumption and system set-up time. Additionally, the loop filter occupies a smaller area as opposed to the integer-N architecture. This allows the loop filter to be embedded into the circuit, minimizing the external noise coupling and total form factor. The delta sigma architecture delivers very low spurious, which can be a significant problem for other PLL solutions.

The circuit also supports commonly used reference frequencies of 19.20 MHz and 19.68 MHz.

FREQUENCY GENERATION

RF-PLL Section

The divide ratio can be calculated using the following equation:

LMX2522 – PCS CDMA:

$$f_{VCO} = \{8 \times RF_B + RF_A + (RF_FN / f_{OSC}) \times 10^4\} \times f_{OSC}$$

where

- (RF_A < RF_B)

LMX2532 – Cellular CDMA:

$$f_{VCO} = \{6 \times RF_B + RF_A + (RF_FN / f_{OSC}) \times 10^4\} \times f_{OSC}$$

where

- (RF_A < RF_B)
- f_{VCO} : Output frequency of voltage controlled oscillator (VCO)
- RF_B: Preset divide ratio of binary 4-bit programmable counter ($2 \leq RF_B \leq 15$)
- RF_A: Preset divide ratio of binary 3-bit swallow counter ($0 \leq RF_A \leq 7$ for LMX2522 or $0 \leq RF_A \leq 5$ for LMX2532)
- RF_FN: Preset numerator of binary 11-bit modulus counter ($0 \leq RF_FN < 1920$ for $f_{OSC} = 19.20$ MHz or $0 \leq RF_FN < 1968$ for $f_{OSC} = 19.68$ MHz)
- f_{OSC} : Reference oscillator frequency

GPS-PLL SECTION

The divide ratio can be calculated using the following equation:

LMX2522 – PCS CDMA:

$$f_{VCO} = \{6 \times RF_B + RF_A + (RF_FN / f_{OSC}) \times 10^4\} \times f_{OSC}$$

where

- (RF_A < RF_B)

LMX2532 – Cellular CDMA:

$$f_{VCO} = \{8 \times RF_B + RF_A + (RF_FN / f_{OSC}) \times 10^4\} \times f_{OSC}$$

where

- (RF_A < RF_B)
- f_{VCO}: Output frequency of voltage controlled oscillator (VCO)
- RF_B: Preset divide ratio of binary 4-bit programmable counter (2 ≤ RF_B ≤ 15)
- RF_A: Preset divide ratio of binary 3-bit swallow counter (0 ≤ RF_A ≤ 5 for LMX2522 or 0 ≤ RF_A ≤ 7 for LMX2532)
- RF_FN: Preset numerator of binary 11-bit modulus counter (0 ≤ RF_FN < 1920 for f_{OSC} = 19.20 MHz or 0 ≤ RF_FN < 1968 for f_{OSC} = 19.68 MHz)
- f_{OSC}: Reference oscillator frequency

PCS CDMA applications using the LMX2522, if the GPS frequency is 1355.04 MHz, [Table 1](#) provides the proper register settings:

Table 1. Settings for GPS (1355.04 MHz) in LMX2522 PCS CDMA application

| Reference Frequency | RF_B | RF_A | RF_FN |
|---------------------|------|------|-------|
| 19.20 MHz | 11 | 4 | 1104 |
| 19.68 MHz | 11 | 2 | 1680 |

Cellular CDMA applications using the LMX2532, in which the GPS frequency is 1490.04 MHz, then [Table 2](#) provides the proper register settings:

Table 2. Settings for GPS (1490.04 MHz) in LMX2532 Cellular CDMA application

| Reference Frequency | RF_B | RF_A | RF_FN |
|---------------------|------|------|-------|
| 19.20 MHz | 9 | 5 | 1164 |
| 19.68 MHz | 9 | 3 | 1404 |

Cellular CDMA applications using the LMX2532, in which the GPS frequency is 1391.82 MHz, then [Table 3](#) provides the proper register settings:

Table 3. Settings for GPS (1391.82 MHz) in LMX2532 Cellular CDMA application

| Reference Frequency | RF_B | RF_A | RF_FN |
|---------------------|------|------|-------|
| 19.20 MHz | 9 | 0 | 942 |
| 19.68 MHz | 8 | 6 | 1422 |

IF-PLL SECTION

$$f_{VCO} = \{16 \times IF_B + IF_A\} \times f_{OSC} / IF_R$$

where

- (IF_A < IF_B)
- f_{VCO} : Output frequency of the voltage controlled oscillator (VCO)
- IF_B: Preset divide ratio of the binary 9-bit programmable counter ($1 \leq IF_B \leq 511$)
- IF_A: Preset divide ratio of the binary 4-bit swallow counter ($0 \leq IF_A \leq 15$)
- f_{OSC} : Reference oscillator frequency
- IF_R: Preset divide ratio of the binary 9-bit programmable reference counter ($2 \leq IF_R \leq 511$)

From the above equation, the LMX2522/32 generates the fixed IF frequencies as summarized in [Table 4](#).

Table 4. IF Frequencies

| Device Type | f_{VCO} (MHz) | IF_B | IF_A | f_{OSC}/IF_R (kHz) |
|---------------|--------------------|------|------|--------------------------|
| LMX2522LQ1635 | 440.76 | 229 | 9 | 120 |
| LMX2532LQ0967 | 170.67 | 88 | 15 | 120 |
| LMX2532LQ1065 | 367.20 | 191 | 4 | 120 |

VCO FREQUENCY TUNING

The center frequency of the RF VCO is mainly determined by the resonant frequency of the tank circuit. This tank circuit is implemented on-chip and requires no external inductor. The LMX2522/32 actively tunes the tank circuit to the required frequency with the built-in tracking algorithm.

BANDWIDTH CONTROL AND FREQUENCY LOCK

During the frequency acquisition period, the loop bandwidth is significantly extended to achieve frequency lock. Once frequency lock occurs, the PLL will return to a steady state condition with the loop bandwidth set to its nominal value. The transition between acquisition and lock modes occurs seamlessly and extremely fast, thereby, meeting the stringent requirements associated with lock time and phase noise. Several controls (BW_DUR, BW_CRL and BW_EN) are used to optimize the lock time performance.

SPURIOUS REDUCTION

To improve the spurious performance of the device one of two types of spurious reduction schemes can be selected:

- A continuous optimization scheme, which tracks the environmental and voltage variations, giving the best spurious performance over changing conditions
- A one time optimization scheme, which sets the internal compensation values only when the PLL goes into a locked state.

The spurious reduction can also be disabled, but it is recommended that the continuous optimization mode be used for normal operation.

POWER DOWN MODE

The LMX2522 and LMX2532 include a power down mode to reduce the power consumption. The LMX2522/32 enters into the power down mode either by taking the CE pin LOW or by setting the power down bits in Register R1. Table 5 summarizes the power down function. If CE is set LOW, the circuit is powered down regardless of the register values. When CE is HIGH, the IF and RF circuitry are individually powered down by setting the register bits.

Table 5. Power Down Configuration⁽¹⁾

| CE Pin | RF_EN | IF_EN | RF Circuitry | IF Circuitry |
|--------|-------|-------|--------------|--------------|
| 0 | X | X | OFF | OFF |
| 1 | 0 | 0 | OFF | OFF |
| 1 | 0 | 1 | OFF | ON |
| 1 | 1 | 0 | ON | OFF |
| 1 | 1 | 1 | ON | ON |

(1) X = Don't care.

LOCK DETECT

The LD output can be used to indicate the lock status of the RF PLL. Bit 21 in Register R0 determines the signal that appears on the LD pin. When the RF PLL is not locked, the LD pin remains LOW. After obtaining phase lock, the LD pin will have a logical HIGH level. The output can also be programmed to be ground at all times.

Table 6. Lock Detect Modes

| LD Bit | Mode |
|--------|---------------|
| 0 | Disable (GND) |
| 1 | Enable |

Table 7. Lock Detect Logic Table⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾⁽⁵⁾

| RF PLL Section | LD Output |
|----------------|-----------|
| Locked | HIGH |
| Not Locked | LOW |

- (1) LD output becomes low when the phase error is larger than t_{W2} .
- (2) LD output becomes high when the phase error is less than t_{W1} for four or more consecutive cycles.
- (3) Phase Error is measured on leading edge. Only errors greater than t_{W1} and t_{W2} are labeled.
- (4) t_{W1} and t_{W2} are equal to 10 ns.
- (5) The lock detect comparison occurs with every 64th cycle of f_R and f_N .

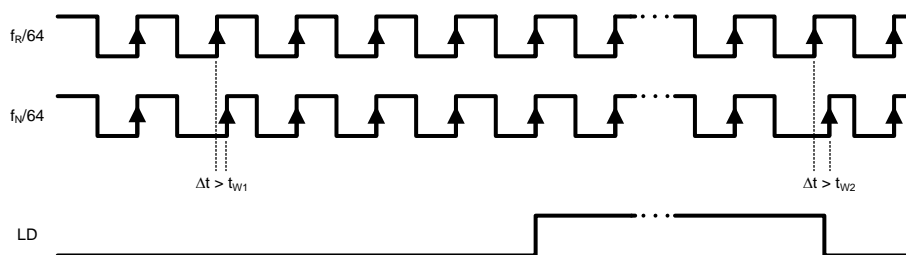


Figure 2. Lock Detect Timing Diagram Waveform

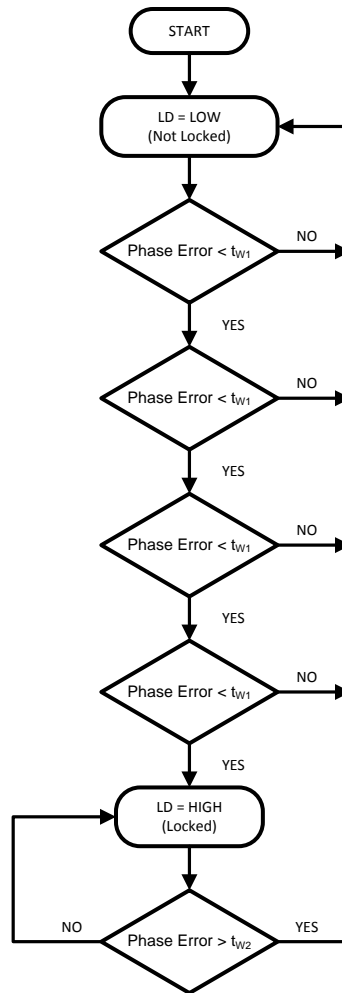


Figure 3. Lock Detect Flow Diagram

MICROWIRE INTERFACE

The programmable register set is accessed via the MICROWIRE serial interface. The interface comprises three signal pins: CLK, DATA, and LE. Serial data (DATA) is clocked into the 24-bit shift register on the rising edge of the clock (CLK). The last bits decode the internal control register address. When the Latch Enable (LE) transitions from LOW to HIGH, data stored in the shift registers is loaded into the corresponding control register.

Programming Description

CONTROL REGISTER CONTENT MAP

The serial interface has a 24-bit shift register to store the incoming data bits temporarily. The incoming Data is loaded into the shift register from MSB to LSB. The Data is shifted at the rising edge of the Clock signal. When the Latch Enable signal transitions from LOW to HIGH, the data stored in the shift register is transferred to the proper register depending on the address bit settings. The selection of the particular register is determined by the control bits indicated in boldface text.

At initial start-up, the MICROWIRE loading requires 4 default words (registers R3, loaded first, to R0, loaded last). After the device has been initially programmed, the RF VCO frequency can be changed using a single register (R0). If an IF frequency other than the default value for the device is desired the SPI_DEF bit should be set to 0, the desired values for IF_A, IF_B, and IF_R entered and words R6 to R0 should be sent.

The control register content map describes how the bits within each control register are allocated to the specific control functions.

Table 8. Complete Register Map

| Register | SHIFT REGISTER BIT LOCATION | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|-----------------------------|---------|--------------|----------|------------|----------|----|----|------------|------------|----|----------------|----|----|----|---|---|---|--------------|--------------|----------|---------------|----------|----------|----------|----------|----------|
| | MSB | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | LSB | | |
| R0 (Default) | SPI_DEF | RF_SE L | RF_LD | SPUR_CRL | RF_B [3:0] | | | | | RF_A [2:0] | | | | | | | | | | RF_FN [10:0] | | | | 0 | 0 | | |
| R1 (Default) | IF_FREQ [1:0] | | OSC_FREQ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SPUR_RDT [1:0] | 0 | 0 | 1 | 0 | 1 | | OB_CRL [1:0] | | RF_EN | IF_EN | 0 | 1 | | | |
| R2 (Default) | IF_CUR[1:0] | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | | |
| R3 (Default) | BW_DUR [1:0] | | BW_CRL [1:0] | | BW_EN | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | | VCO_CUR [1:0] | 0 | 1 | 1 | | |
| R4 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | | IF_A [3:0] | | | | | | | | | | | | | | 0 | 1 | 1 | 1 | |
| R5 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | | | | | | | | | | | | | 0 | 1 | 1 | 1 | 1 |
| R6 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | |

NOTE: **Bold** numbers represent the address bits.

R0 REGISTER

The R0 register address bits (R0 [1:0]) are “00”.

The SPI_DEF bit selects between using the default IF counter values and user programmable values. The use of the default counter values requires that only words R0 to R3 (registers R3, loaded first, to R0, loaded last) be sent after initial power up.

The RF_LD bit activates the lock detect output of the LD pin (pin 19). The lock detect mode shows the lock status of the RF PLL. The waveform of the lock detect mode is shown in [Figure 2](#), in the [Functional Description](#) section on **LOCK DETECT**.

The SPUR_CRL bit is set to 1 only in the GPS mode with the LMX2532LQ1065 when a 19.68 MHz reference oscillator is used.

The RF N counter consists of the 4-bit programmable counter (RF_B counter), the 3-bit swallow counter (RF_A counter) and the 11-bit delta sigma modulator (RF_FN counter). The equations for calculating the counter values are presented below.

Table 9. R0 REGISTER

| Register | SHIFT REGISTER BIT LOCATION | | | | | | | | | | | | | | | | | | | | MSB | | LSB | |
|---------------------|-----------------------------|--------|-------|----------|------------|------------|----|----|----|--------------|----|----|----|----|---|---|---|---|---|---|-----|---|---------------|---|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Data Field | | | | | | | | | | | | | | | | | | | | | | Address Field | |
| R0 (Default) | SPI_DEF | RF_SEL | RF_LD | SPUR_CRL | RF_B [3:0] | RF_A [2:0] | | | | RF_FN [10:0] | | | | | | 0 | 0 | | | | | | | |

| Name | Functions |
|--------------|---|
| SPI_DEF | Default Register Selection 0 = OFF (Use values set in R0 to R6) 1 = ON (Use default values set in R0 to R3) |
| RF_SEL | RF Select Configuration See Table 10 . RF_SEL Configuration below |
| RF_LD | RF Lock Detect 0 = Hard zero (GND) 1 = Lock detect |
| SPUR_CRL | Spur Control 1 = LMX2532LQ1065 in GPS mode with 19.68 MHz reference oscillator only 0 = All other options |
| RF_B [3:0] | RF_B Counter 4-bit programmable counter $2 \leq RF_B \leq 15$ |
| RF_A [2:0] | RF_A Counter 3-bit swallow counter $0 \leq RF_A \leq 7$ for LMX2522 $0 \leq RF_A \leq 5$ for LMX2532 |
| RF_FN [10:0] | RF Fractional Numerator Counter 11-bit programmable counter $0 \leq RF_FN < 1920$ for $f_{OSC} = 19.20$ MHz $0 \leq RF_FN < 1968$ for $f_{OSC} = 19.68$ MHz |

Table 10. RF_SEL Configuration

| Device Type | RF_SEL = 0 | RF_SEL = 1 |
|-------------|------------|------------|
| LMX2522 | GPS | K-PCS |
| LMX2532 | K-Cellular | GPS |

RF N Counter Setting:

| Counter Name | Symbol | Function |
|----------------------|--------|---|
| Modulus Counter | RF_FN | RF N Divider $N = \text{Prescaler} \times \text{RF_B} + \text{RF_A} + (\text{RF_FN} / f_{\text{OSC}}) 10^4$ |
| Programmable Counter | RF_B | |
| Swallow Counter | RF_A | |

Pulse Swallow Function:

$$f = \{\text{Prescaler} \times \text{RF_B} + \text{RF_A} + (\text{RF_FN} / f_{\text{OSC}}) \times 10^4\} \times f_{\text{OSC}} \text{ where } (\text{RF_A} < \text{RF_B})$$

where

- f_{VCO} : Output frequency of voltage controlled oscillator (VCO)

Prescaler Values:

| Device Type | RF Prescaler | GPS Prescaler |
|-------------|--------------|---------------|
| LMX2522 | 8 | 6 |
| LMX2532 | 6 | 8 |

- RF_B: Preset divide ratio of binary 4-bit programmable counter ($2 \leq \text{RF_B} \leq 15$)
- RF_A: Preset divide ratio of binary 3-bit swallow counter ($0 \leq \text{RF_A} \leq 7$ for prescaler of 8 or $0 \leq \text{RF_A} \leq 5$ for prescaler of 6)
- RF_FN: Preset numerator of binary 11-bit modulus counter ($0 \leq \text{RF_FN} < 1920$ for $f_{\text{OSC}} = 19.20 \text{ MHz}$; $0 \leq \text{RF_FN} < 1968$ for $f_{\text{OSC}} = 19.68 \text{ MHz}$)
- f_{OSC} : Reference oscillator frequency

NOTE: For the use of reference frequencies other than those specified, please contact Texas Instruments.

R1 REGISTER

The R1 register address bits (R1 [1:0]) are “01”.

The IF_FREQ bits selects the default IF frequency applicable to the specific CDMA system. For the LMX2522 the default IF frequency is 440.76 MHz, and for the LMX2532 the default IF frequencies are 367.20 MHz and 170.76 MHz, depending on variant.

Reference Frequency Selection bit (OSC_FREQ) selects either 19.20 MHz or 19.68 MHz for the reference oscillator frequency.

The internal spurious reduction scheme is controlled by the SPUR_RDT [1:0] bits. There are two different spur reduction schemes: a continuous tracking mode and a single optimization mode. The continuous tracking mode will adjust for variations in voltage and temperature. The single optimization mode fixes the internal compensation parameters only when the PLL goes into the locked state. The spur reduction can also be disabled, but it is recommended that the continuous mode be used for normal operation.

The OB_CRL [1:0] bits determine the power level of the RF output buffer. The power level is set according to the system requirement.

The two bits, RF_EN and IF_EN, logically select the active state of the RF/GPS synthesizer system and the IF PLL, respectively. The entire IC can be placed in a power down state by using the CE control pin (pin 20).

Table 11. R1 REGISTER

| Register | SHIFT REGISTER BIT LOCATION | | | | | | | | | | | | | | | | | | | | LSB | | | | |
|---------------------|-----------------------------|----------|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|--------------|-------|---------------|---|---|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | Data Field | | | | | | | | | | | | | | | | | | | | | | Address Field | | |
| R1 (Default) | IF_FREQ [1:0] | OSC_FREQ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | OB_CRL [1:0] | RF_EN | IF_EN | 0 | 1 |

| Name | Functions |
|----------------|--|
| IF_FREQ [1:0] | IF Frequency Selection 00 = 170.76 MHz (LMX2532LQ0967) 01 = 367.20 MHz (LMX2532LQ1065) 10 = 440.76 MHz (LMX2522LQ1635) |
| OSC_FREQ | Reference Frequency Selection 0 = 19.20 MHz 1 = 19.68 MHz |
| SPUR_RDT [1:0] | Spur Reduction Scheme 00 = No spur reduction 01 = Not Used 10 = Continuous tracking of variation (Recommended) 11 = One time optimization |
| OB_CRL [1:0] | RF Output Power Control 00 = Minimum Output Power 01 = 10 = 11 = Maximum Output Power |
| RF_EN | RF Enable 0 = RF Off 1 = RF On |
| IF_EN | IF Enable 0 = IF Off 1 = IF On |

R2 REGISTER

The R2 Register address bits (R2 [1:0]) are “10”.

The IF_CUR [1:0] bits program the IF charge pump current. Considering the external IF VCO and loop filter, the user can select the amount of IF charge pump current to be 100µA, 200µA, 300µA or 800µA.

Table 12. R2 REGISTER

| Register | MSB | SHIFT REGISTER BIT LOCATION | | | | | | | | | | | | | | | | | | | | LSB | | |
|---------------------|-------------|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|-----|---------------|---|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | Data Field | | | | | | | | | | | | | | | | | | | | | | Address Field | |
| R2 (Default) | IF_CUR[1:0] | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

| Name | Functions |
|--------------|---|
| IF_CUR [1:0] | IF Charge Pump Current 00 = 100 µA 01 = 200 µA 10 = 300 µA 11 = 800 µA |

R3 REGISTER

The R3 register address bits (R3 [2:0]) are “011”.

Register R3 contains the controls for the phase lock bandwidth controls (BW_DUR, BW_CRL and BW_EN). The duration of the digital controller portion of the bandwidth control is set by BW_DUR [1:0]. The minimum time set with 00 and increasing durations to the maximum value set with 11. BW_CRL [1:0] sets the phase offset criterion for the bandwidth controller. Once the phase offset between the reference clock and the divided VCO signal are within the set criterion, the bandwidth control stops. The maximum phase offset is set with 00 and decreases to the minimum value set with 11. BW_EN enables the bandwidth control in the locking state.

The VCO dynamic current is also controlled in register R3 with VCO_CUR [1:0]. The minimum value corresponds to 00 and increases to a maximum value set at 11.

Table 13. R3 REGISTER

| Register | SHIFT REGISTER BIT LOCATION | | | | | | | | | | | | | | | | | | | | LSB | | |
|---------------------|-----------------------------|--------------|-------|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---------------|---|---------------|---|---|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| | Data Field | | | | | | | | | | | | | | | | | | | | Address Field | | |
| R3 (Default) | BW_DUR [1:0] | BW_CRL [1:0] | BW_EN | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | VCO_CUR [1:0] | 0 | 1 | 1 | |

| Name | Functions |
|---------------|--|
| BW_DUR [1:0] | Bandwidth Duration 00 = Minimum value (Recommended) 01 = 10 = 11 = Maximum value |
| BW_CRL [1:0] | Bandwidth Control 00 = Maximum phase offset (Recommended) 01 = 10 = 11 = Minimum phase offset |
| BW_EN | Bandwidth Enable 0 = Disable 1 = Enable (Recommended) |
| VCO_CUR [1:0] | VCO Dynamic Current 00 = Minimum value 01 = 10 = 11 = Maximum value (Recommended) |

R4 REGISTER

The R4 register address bits (R3 [3:0]) are “0111”.

Register R4 is used to set the IF N counters if the default value is not desired. This register is only active if the SPI_DEF bit in register R0 is 0.

The IF N counter consists of the 9-bit programmable counter (IF_B counter) and the 4-bit swallow counter (IF_A counter). The equations for calculating the counter values are presented below.

Table 14. R4 REGISTER

| Register | SHIFT REGISTER BIT LOCATION | | | | | | | | | | | | | | | | | | | | MSB | LSB | |
|----------|-----------------------------|----|----|----|----|----|----|------------|----|----|----|------------|----|----|---|---|---------------|---|---|---|-----|-----|---|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | | | 3 |
| | Data Field | | | | | | | | | | | | | | | | Address Field | | | | | | |
| R4 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | IF_A [3:0] | | | | IF_B [8:0] | | | | 0 | 1 | 1 | 1 | | | | |

| Name | Functions |
|------------|---|
| IF_A [3:0] | IF A Counter 4-bit swallow counter 0 ≤ IF_A ≤ 15 |
| IF_B [8:0] | IF B Counter 9-bit programmable counter 1 ≤ IF_B ≤ 511 |

IF Frequency Setting:

$$f_{VCO} = \{16 \times IF_B + IF_A\} \times f_{OSC} / R \text{ where } (IF_A < IF_B)$$

where

- f_{VCO} : Output frequency of IF voltage controlled oscillator (IF VCO)
- IF_B: Preset divide ratio of binary 9-bit programmable counter (1 ≤ IF_B ≤ 511)
- IF_A: Preset divide ratio of binary 4-bit swallow counter (0 ≤ IF_A ≤ 15)
- IF_R: Preset divide ratio of binary 9-bit programmable reference counter (2 ≤ IF_R ≤ 511)
- f_{OSC} : Reference oscillator frequency

R5 REGISTER

The R5 register address bits (R5 [4:0]) are “01111”.

Register R5 is used to set the IF_R divider if the default value is not desired. This register is only active if the SPI_DEF bit in register R0 is 0.

Table 15. R5 REGISTER

| Register | MSB | SHIFT REGISTER BIT LOCATION | | | | | | | | | | | | | | | | | | | | LSB | | | |
|----------|------------|-----------------------------|----|----|----|----|----|----|----|----|------------|----|----|----|---|---------------|---|---|---|---|---|-----|---|---|--|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | Data Field | | | | | | | | | | | | | | | Address Field | | | | | | | | | |
| R5 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | IF_R [8:0] | | | | | 0 | 1 | 1 | 1 | 1 | | | | | |

| Name | Functions |
|------------|---|
| IF_R [8:0] | IF R Counter 9-bit programmable counter $2 \leq \text{IF_R} \leq 511$ |

R6 REGISTER

The R6 register address bits (R6 [5:0]) are “011111”.

Register R6 is used for internal testing of the device and is not intended for customer use. This register is only active if the SPI_DEF bit in register R0 is 0.

Table 16. R6 REGISTER

| Register | MSB | SHIFT REGISTER BIT LOCATION | | | | | | | | | | | | | | | | | | | | LSB | | | |
|----------|------------|-----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|---|---------------|---|---|---|---|---|-----|---|---|---|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | Data Field | | | | | | | | | | | | | | | Address Field | | | | | | | | | |
| R6 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

REVISION HISTORY

| Changes from Revision A (April 2013) to Revision B | Page |
|--|--------------------|
| • Changed layout of National Data Sheet to TI format | 19 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| LMX2522LQ1635/NOPB | ACTIVE | WQFN | NJB | 28 | 1000 | RoHS & Green | SN | Level-3-260C-168 HR | -30 to 85 | 25221635 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMX2522LQ1635/NOPB | WQFN | NJB | 28 | 1000 | 178.0 | 12.4 | 5.3 | 5.3 | 1.3 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMX2522LQ1635/NOPB | WQFN | NJB | 28 | 1000 | 208.0 | 191.0 | 35.0 |

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