LMZ22005 5-A SIMPLE SWITCHER® Power Module With 20-V Maximum Input Voltage

1 Features

- Integrated Shielded Inductor
- Simple PCB Layout
- Frequency Synchronization Input (650 kHz to 950 kHz)
- Flexible Start-up Sequencing Using External Soft-Start, Tracking and Precision Enable
- Protection Against Inrush Currents and Faults Such as Input UVLO and Output Short Circuit
- Junction Temperature Range –40°C to 125°C
- Single Exposed Pad for Easy Mounting and Manufacturing
- Fast Transient Response for Powering FPGAs and ASICs
- Fully Enabled for WEBENCH® Power Designer
- Pin Compatible With LMZ23605/LMZ23603/LMZ22003
- Electrical Specifications
  - 30-W Maximum Total Output Power
  - Up to 5-A Output Current
  - Input Voltage Range 6 V to 20 V
  - Output Voltage Range 0.8 V to 6 V
  - Efficiency up to 92%
- Performance Benefits
  - High Efficiency Reduces System Heat Generation
  - Tested to EN55022 Class B(1)
  - Low Component Count, Only 5 External Components
  - Low Output Voltage Ripple
  - Uses PCB as Heat Sink, No Airflow Required

(1) EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007. See AN-2125 SNVA473 and layout for information on device under test. Vin = 12 V, Vo = 3.3 V, Io = 5 A

2 Applications

- Point-of-load Conversions from 12V Input Rail
- Time-Critical Projects
- Space Constrained/High Thermal Requirement Applications
- Negative Output Voltage Applications (see AN-2027 SNVA425)

3 Description

The LMZ22005 SIMPLE SWITCHER® power module is an easy-to-use step-down DC-DC solution capable of driving up to 5-A load. The LMZ22005 is available in an innovative package that enhances thermal performance and allows for hand or machine soldering.

The LMZ22005 can accept an input voltage rail between 6 V and 20 V and can deliver an adjustable and highly accurate output voltage as low as 0.8 V. The LMZ22005 only requires two external resistors and three external capacitors to complete the power solution. The LMZ22005 is a reliable and robust design with the following protection features: thermal shutdown, input undervoltage lockout, output overvoltage protection, short circuit protection, output current limit, and the device allows start-up into a prebiased output. The sync input allows synchronization over the 650- to 950-kHz switching frequency range.

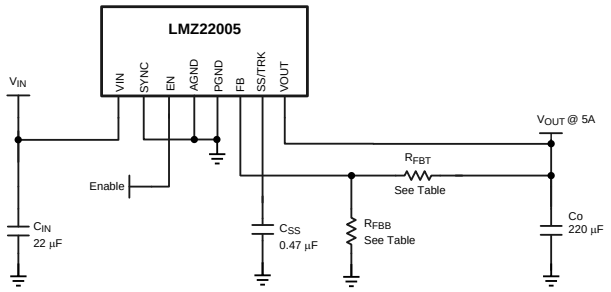
Device Information(1)(2)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMZ22005	NDW (7)	10.16 mm × 9.85 mm

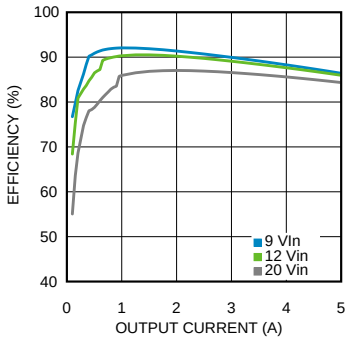
(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Peak reflow temperature equals 245°C. See SNAA214 for more details.

Simplified Application Schematic



Efficiency 5-V Output at 25°C Ambient



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (October 2013) to Revision J **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes, Application and Implementation* section, *Power Supply Recommendations* section, *Layout section, Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision H (March 2013) to Revision I **Page**

- Changed 10 mils ... 23
- Changed 10 mils ... 25
- Added *Power Module SMT Guidelines* ... 26

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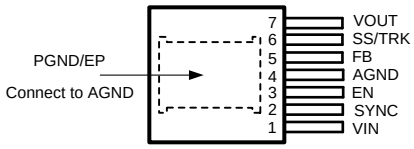
5 Pin Configuration and Functions

NDW Package
7-Pin
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	4	Ground	Analog Ground — Reference point for all stated voltages. Must be externally connected to EP/PGND.
EN	3	Analog	Enable — Input to the precision enable comparator. Rising threshold is 1.279 V typical. Once the module is enabled, a 20-µA source current is internally activated to accommodate programmable hysteresis.
FB	5	Analog	Feedback — Internally connected to the regulation, overvoltage, and short circuit comparators. The regulation reference point is 0.796 V at this input pin. Connect the feedback resistor divider between the output and AGND to set the output voltage.
PGND	—	Ground	Exposed Pad / Power Ground Electrical path for the power circuits within the module. — NOT Internally connected to AGND / pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.
SS/TRK	6	Analog	Soft-Start/Track — To extend the 1.6-ms internal soft-start connect an external soft -start capacitor. For tracking connect to an external resistive divider connected to a higher priority supply rail. See *Design Steps*.
SYNC	2	Analog	Sync Input — Apply a CMOS logic level square wave whose frequency is between 650 kHz and 950 kHz to synchronize the PWM operating frequency to an external frequency source. When not using synchronization connect to ground. The module free running PWM frequency is 812 kHz (typical)
VIN	1	Power	Supply input — Nominal operating range is 6 V to 20 V. A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and exposed pad (PGND).
VOUT	7	Power	Output Voltage — Output from the internal inductor. Connect the output capacitor between this pin and exposed pad.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)(3)

	MIN	MAX	UNIT
VIN to PGND	–0.3	24	V
EN, SYNC to AGND	–0.3	5.5	V
SS/TRK, FB to AGND	–0.3	2.5	V
AGND to PGND	–0.3	0.3	V
Junction temperature		150	°C
Peak reflow case temperature (30 sec)		245	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) For soldering specifications, refer to the following document: SNOA549

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN	6	20	V
EN, SYNC	0	5	V
Operation junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)			LMZ22005 NDW 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	4-layer Evaluation Printed-Circuit-Board, 60 vias, No air flow	19.3	°C/W
		2-layer JEDEC Printed-Circuit-Board, No air flow	21.5	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	No air flow	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Theta JA measured on a 3.5-in × 3.5-in 4-layer board, with 3-oz. copper on outer layers and 2-oz. copper on inner layers, sixty thermal vias, no air flow, and 1-W power dissipation. Refer to application note layout diagrams.

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6.5 Electrical Characteristics

Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V, V_{OUT} = 3.3 V.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
SYSTEM PARAMETERS						
ENABLE CONTROL						
V_{EN}	EN threshold trip point	V_{EN} rising, T_J = 25°C		1.279		V
		V_{EN} rising, T_J = –40°C to +125°C	1.1		1.458	
V_{EN-HYS}	EN input hysteresis current	V_{EN} > 1.279 V		21		µA
SOFT-START						
I_{SS}	SS source current	V_{SS} = 0 V, T_J = 25°C		50		µA
		V_{SS} = 0 V, T_J = –40°C to +125°C	40		60	
t_{SS}	Internal soft-start interval			1.6		ms
CURRENT LIMIT						
I_{CL}	Current limit threshold	DC average, T_J = –40°C to +125°C	5.4			A
INTERNAL SWITCHING OSCILLATOR						
f_{osc}	Free-running oscillator frequency	Sync input connected to ground.	711	812	914	kHz
f_{sync}	Synchronization range		650		950	kHz
$V_{IL-sync}$	Synchronization logic zero amplitude	Relative to AGND, T_J = –40°C to +125°C			0.4	V
$V_{IH-sync}$	Synchronization logic one amplitude	Relative to AGND, T_J = –40°C to +125°C	1.5			V
Sync $_{dc}$	Synchronization duty cycle range		15%	50%	85%	
D_{max}	Maximum Duty Factor			83%		
REGULATION AND OVERVOLTAGE COMPARATOR						
V_{FB}	In-regulation feedback voltage	V_{SS} >+ 0.8 V, I_O = 3 A, T_J = 25°C		0.796		V
		V_{SS} >+ 0.8 V, I_O = 3 A, T_J = –40°C to +125°C	0.776		0.816	
V_{FB-OV}	Feedback overvoltage protection threshold			0.86		V
I_{FB}	Feedback input bias current			5		nA
I_Q	Non-switching input current	V_{FB} = 0.86 V		2.6		mA
I_{SD}	Shutdown quiescent current	V_{EN} = 0 V		70		µA
THERMAL CHARACTERISTICS						
T_{SD}	Thermal shutdown	Rising		165		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis	Falling		15		°C
PERFORMANCE PARAMETERS(3)						
ΔV_O	Output voltage ripple	C_{out} = 220 µF with 7 mΩ ESR + 100 µF X7R + 2 x 0.047 µF BW at 20 MHz		9		mV_{PP}
$\Delta V_O/\Delta V_{IN}$	Line regulation	V_{IN} = 12 V to 20 V, I_O= 0.001 A		±0.02%		
$\Delta V_O/\Delta I_{OUT}$	Load regulation	V_{IN} = 12 V, I_O= 0.001 A to 3 A		1		mV/A
η	Peak efficiency	V_{IN} = 12 V, V_O = 3.3 V, I_O = 1 A		86%		
η	Full load efficiency	V_{IN} = 12 V V_O = 3.3 V, I_O = 3 A		81.5%		

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Refer to BOM in Table 1.

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6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = 2 x 10 µF + 1-µF X7R Ceramic; C_O = 220-µF Specialty Polymer + 10-µF Ceramic; T_A = 25°C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher output ripple – See *Design Steps* section.

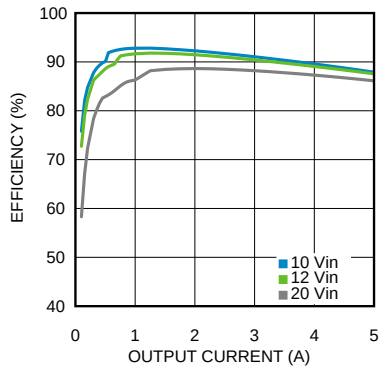

Figure 1. Efficiency 6-V Output at 25°C Ambient

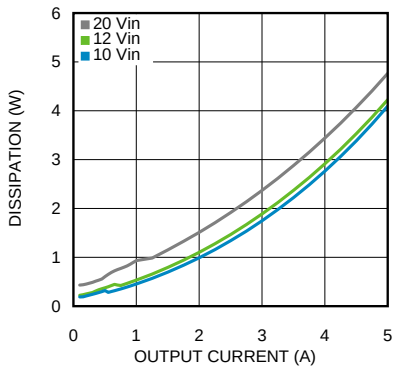

Figure 2. Dissipation 6-V Output at 25°C Ambient

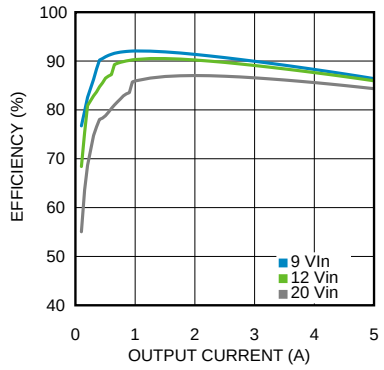

Figure 3. Efficiency 5-V Output at 25°C Ambient

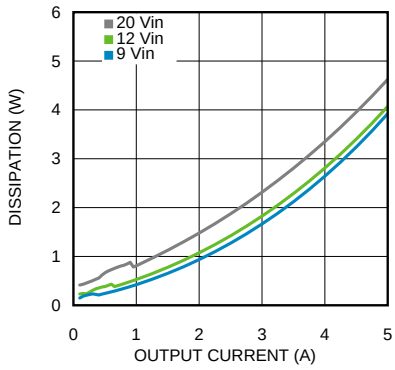

Figure 4. Dissipation 5-V Output at 25°C Ambient

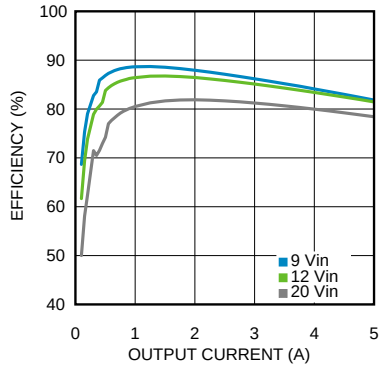

Figure 5. Efficiency 3.3-V Output at 25°C Ambient

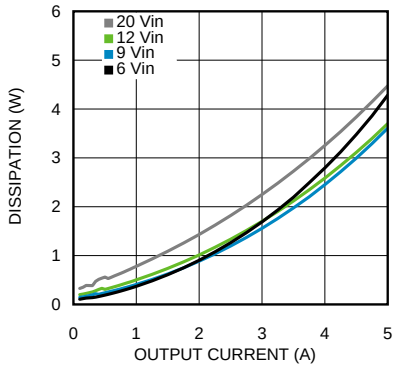

Figure 6. Dissipation 3.3-V Output at 25°C Ambient

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = 2 x 10 µF + 1-µF X7R Ceramic; C_O = 220-µF Specialty Polymer + 10-µF Ceramic; T_A = 25°C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher output ripple – See *Design Steps* section.

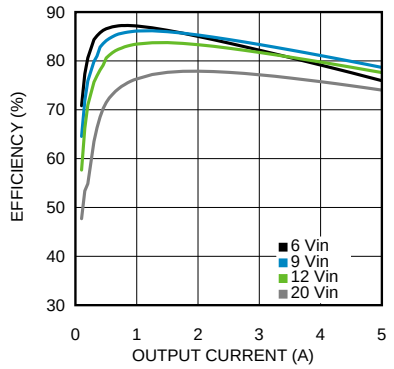

Figure 7. Efficiency 2.5-V Output at 25°C Ambient

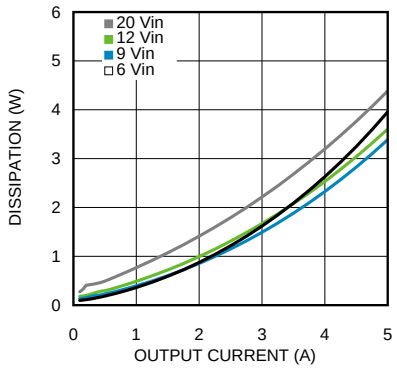

Figure 8. Dissipation 2.5-V Output at 25°C Ambient

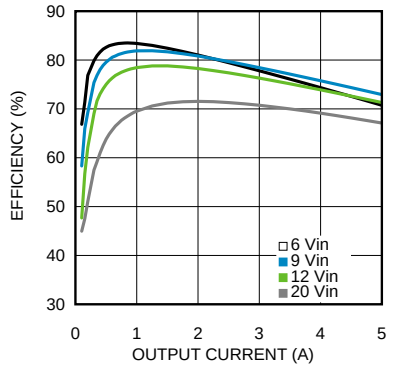

Figure 9. Efficiency 1.8-V Output at 25°C Ambient

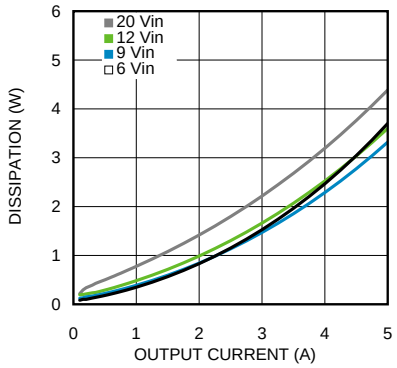

Figure 10. Dissipation 1.8-V Output at 25°C Ambient

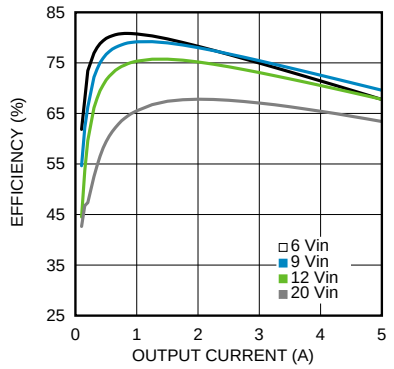

Figure 11. Efficiency 1.5-V Output at 25°C Ambient

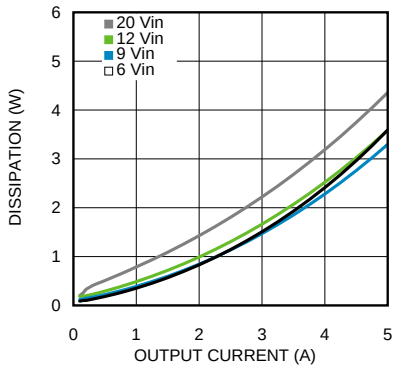

Figure 12. Dissipation 1.5-V Output at 25°C Ambient

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = 2 x 10 µF + 1-µF X7R Ceramic; C_O = 220-µF Specialty Polymer + 10-µF Ceramic; T_A = 25°C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher output ripple – See *Design Steps* section.

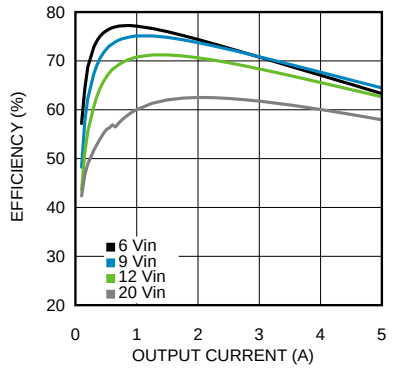

Figure 13. Efficiency 1.2-V Output at 25°C Ambient

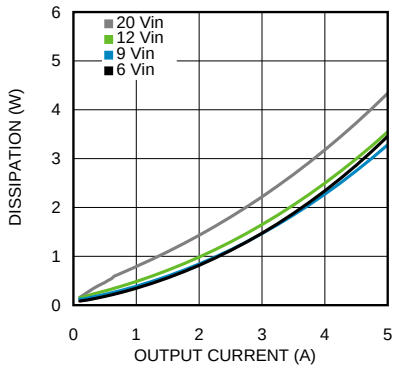

Figure 14. Dissipation 1.2-V Output at 25°C Ambient

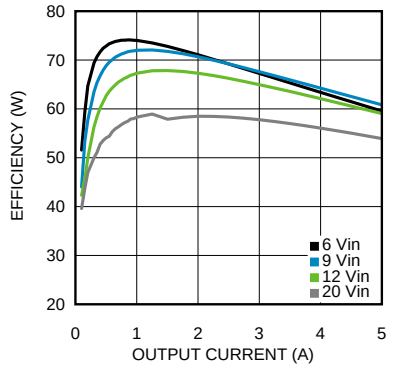

Figure 15. Efficiency 1-V Output at 25°C Ambient

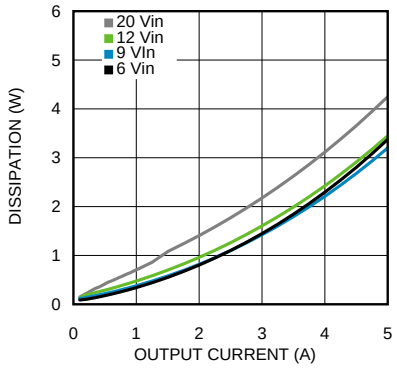

Figure 16. Dissipation 1-V Output at 25°C Ambient

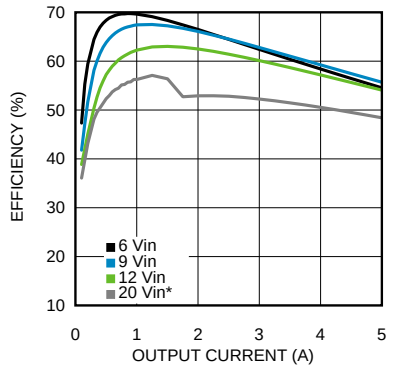

Figure 17. Efficiency 0.8-V Output at 25°C Ambient

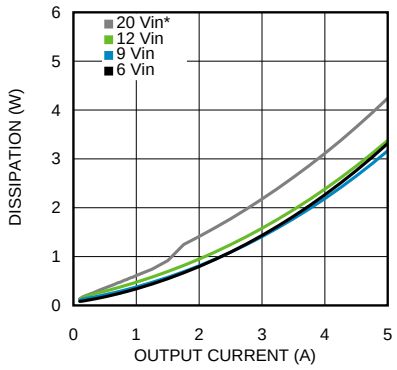

Figure 18. Dissipation 0.8-V Output at 25°C Ambient

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = 2 x 10 µF + 1-µF X7R Ceramic; C_O = 220-µF Specialty Polymer + 10-µF Ceramic; T_A = 25°C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher output ripple – See *Design Steps* section.

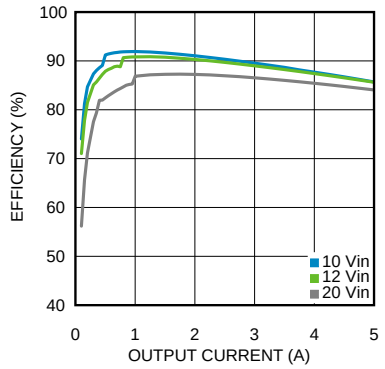

Figure 19. Efficiency 6-V Output at 85°C Ambient

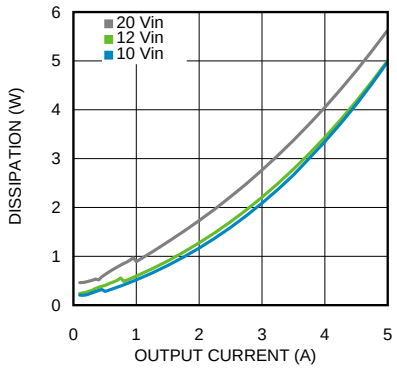

Figure 20. Dissipation 6-V Output at 85°C Ambient

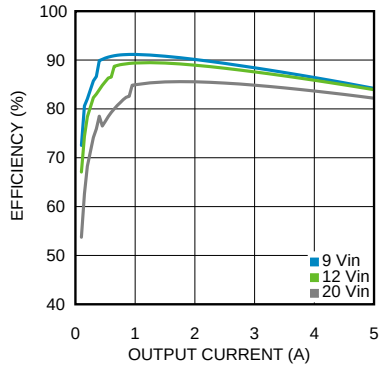

Figure 21. Efficiency 5-V Output at 85°C Ambient

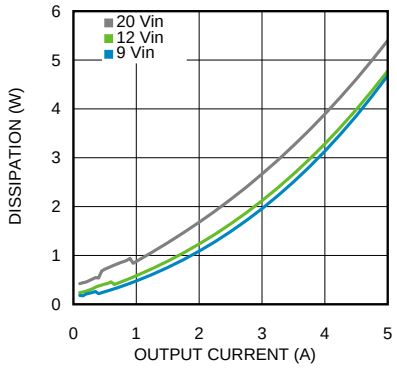

Figure 22. Dissipation 5-V Output at 85°C Ambient

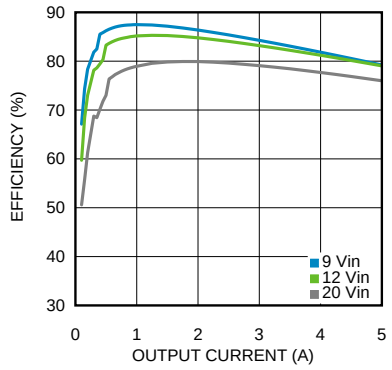

Figure 23. Efficiency 3.3-V Output at 85°C Ambient

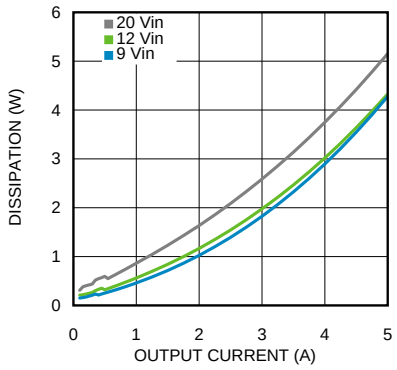

Figure 24. Dissipation 3.3-V Output at 85°C Ambient

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = 2 x 10 µF + 1-µF X7R Ceramic; C_O = 220-µF Specialty Polymer + 10-µF Ceramic; T_A = 25°C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher output ripple – See *Design Steps* section.

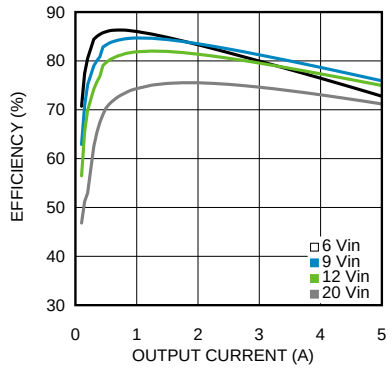

Figure 25. Efficiency 2.5-V Output at 85°C Ambient

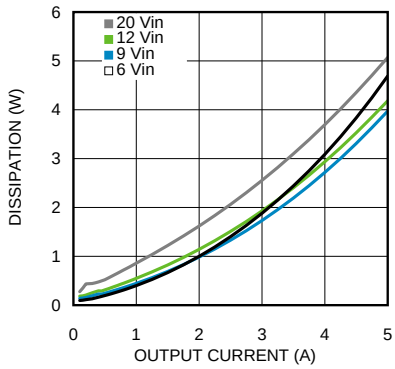

Figure 26. Dissipation 2.5-V Output at 85°C Ambient

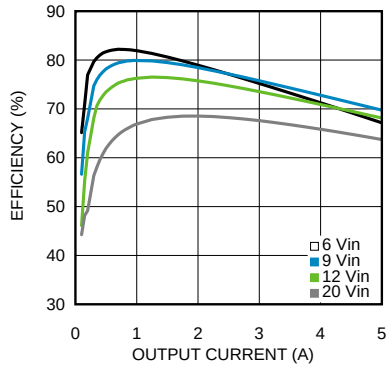

Figure 27. Efficiency 1.8-V Output at 85°C Ambient

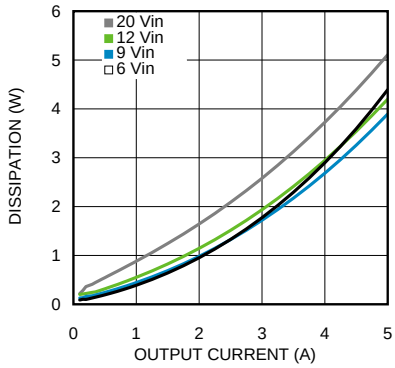

Figure 28. Dissipation 1.8-V Output at 85°C Ambient

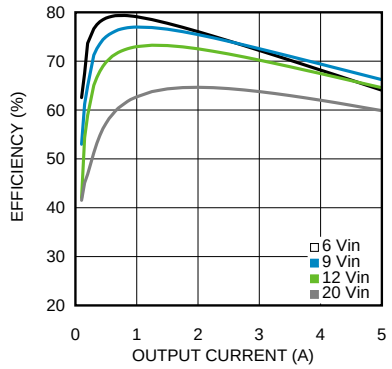

Figure 29. Efficiency 1.5-V Output at 85°C Ambient

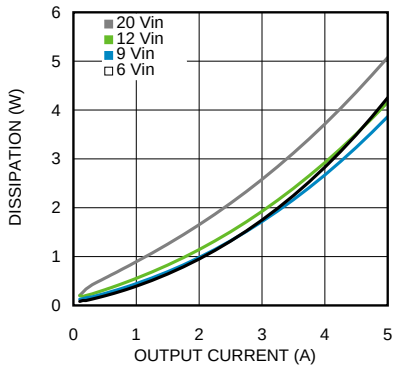

Figure 30. Dissipation 1.5-V Output at 85°C Ambient

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = 2 x 10 µF + 1-µF X7R Ceramic; C_O = 220-µF Specialty Polymer + 10-µF Ceramic; T_A = 25°C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher output ripple – See *Design Steps* section.

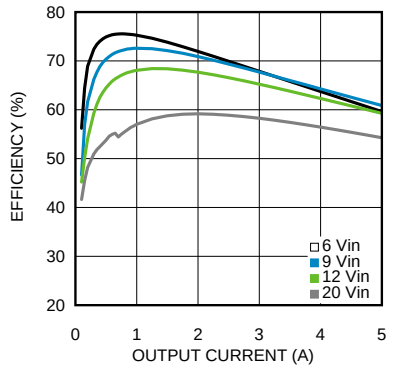

Figure 31. Efficiency 1.2-V Output at 85°C Ambient

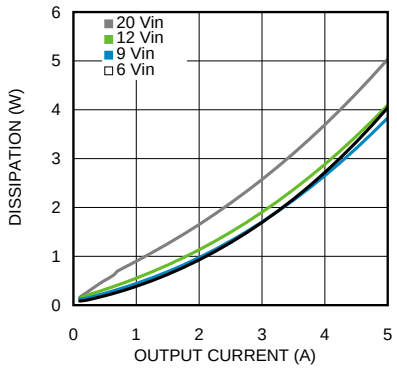

Figure 32. Dissipation 1.2-V Output at 85°C Ambient

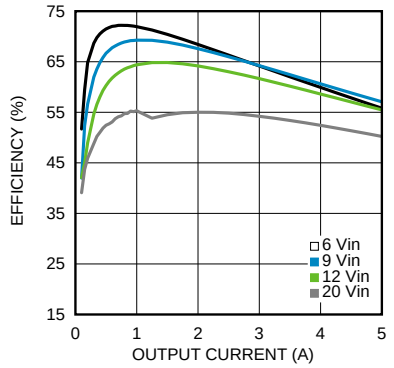

Figure 33. Efficiency 1-V Output at 85°C Ambient

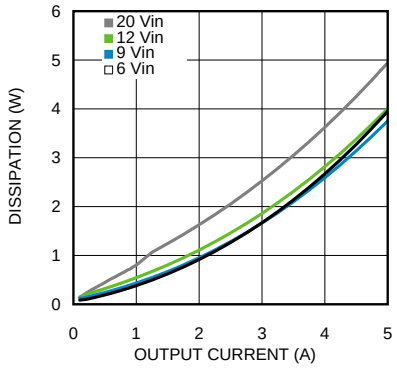

Figure 34. Dissipation 1-V Output at 85°C Ambient

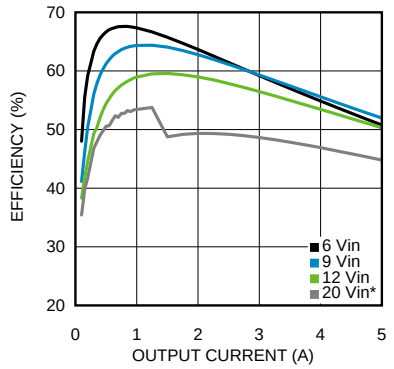

Figure 35. Efficiency 0.8-V at 85°C Ambient

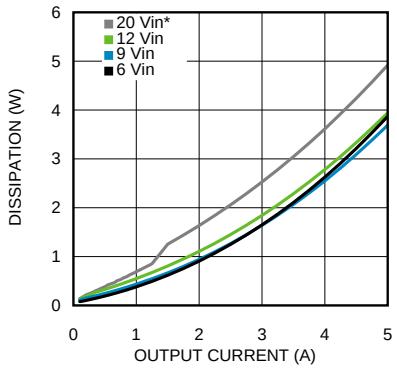

Figure 36. Dissipation 0.8-V Output at 85°C Ambient

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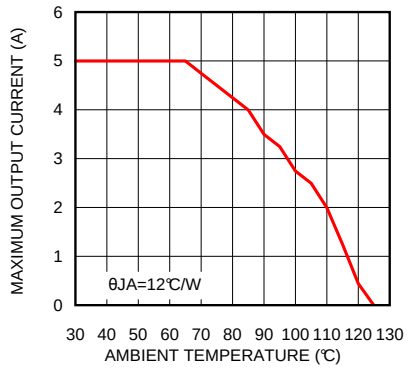
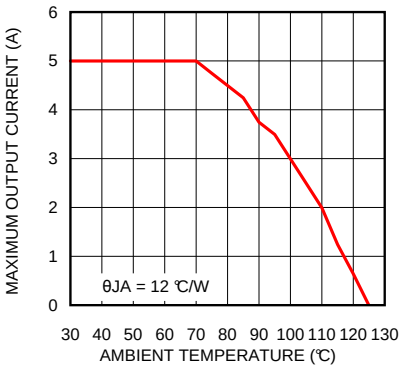
Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = 2 x 10 µF + 1-µF X7R Ceramic; C_O = 220-µF Specialty Polymer + 10-µF Ceramic; T_A = 25°C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher output ripple – See *Design Steps* section.



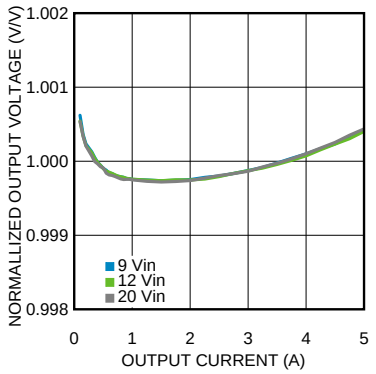
V_{IN} = 12 V, V_{OUT} = 5 V

Figure 37. Thermal Derating



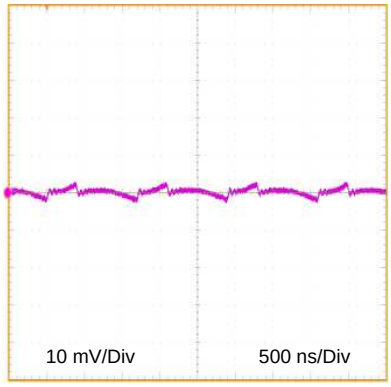
V_{IN}= 12 V, V_{OUT} = 3.3 V

Figure 38. Thermal Derating



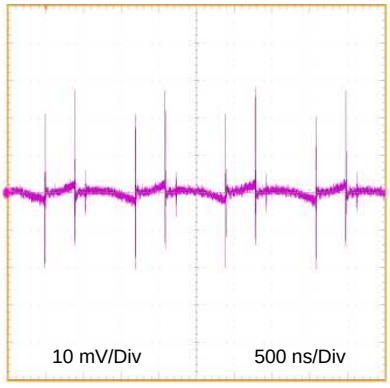
V_{OUT} = 3.3 V

Figure 39. Normalized — Line and Load Regulation



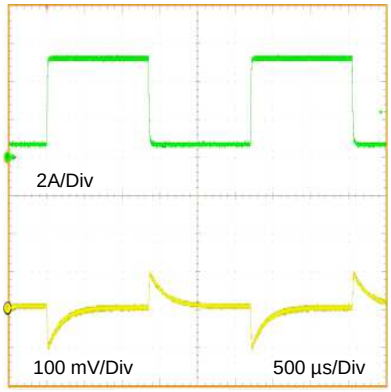
12 V_{IN} 3.3 V_O at 5 A, BW = 20 MHz

Figure 40. Output Ripple



12 V_{IN} 3.3 V_O at 5 A BW = 250 MHz

Figure 41. Output Ripple



12 V_{IN} 3.3 V_O 0.5- to 5-A Step

Figure 42. Transient Response From Evaluation Board

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Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 12 V; C_{IN} = 2 x 10 µF + 1-µF X7R Ceramic; C_O = 220-µF Specialty Polymer + 10-µF Ceramic; T_A = 25°C for waveforms. Efficiency and dissipation plots marked with * have cycle skipping at light loads resulting is slightly higher output ripple – See *Design Steps* section.

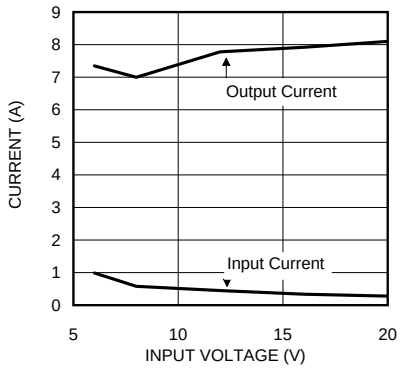


Figure 43. Short Circuit Current vs Input Voltage

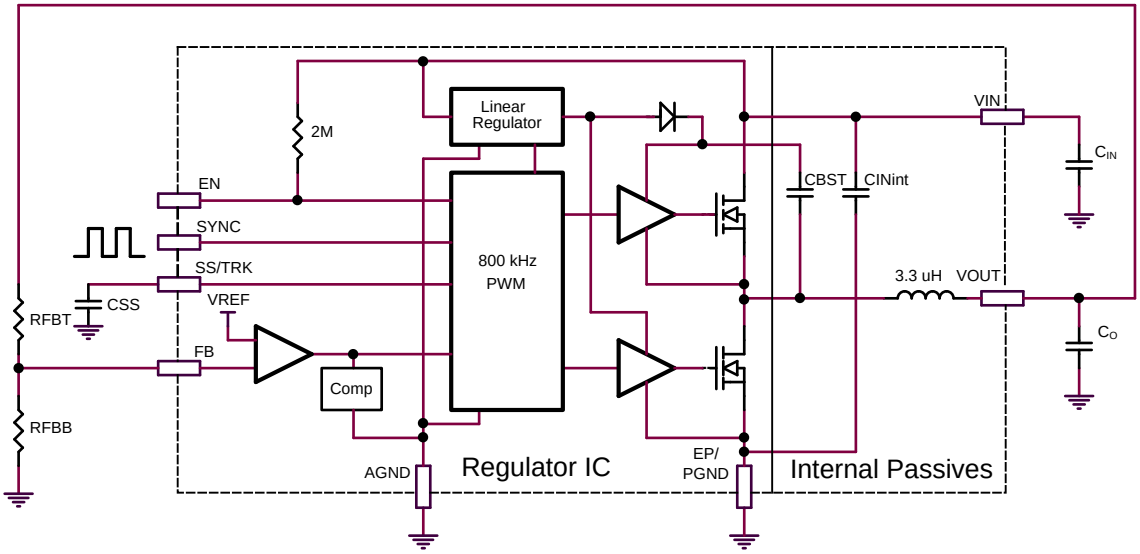
7 Detailed Description

7.1 Overview

The architecture used is an internally compensated emulated peak current mode control, based on a monolithic synchronous SIMPLE SWITCHER core capable of supporting high load currents. The output voltage is maintained through feedback compared with an internal 0.8-V reference. For emulated peak current-mode, the valley current is sampled on the down-slope of the inductor current. This is used as the DC value of current to start the next cycle.

The primary application for emulated peak current-mode is high input voltage to low output voltage operating at a narrow duty cycle. By sampling the inductor current at the end of the switching cycle and adding an external ramp, the minimum ON-time can be significantly reduced, without the need for blanking or filtering which is normally required for peak current-mode control.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Synchronization Input

The PWM switching frequency can be synchronized to an external frequency source. If this feature is not used, connect this input either directly to ground, or connect to ground through a resistor of 1.5 kΩ or less. The allowed synchronization frequency range is 650 kHz to 950 kHz. The typical input threshold is 1.4-V transition level. Ideally the input clock must overdrive the threshold by a factor of 2, so direct drive from 3.3-V logic through a 1.5-kΩ Thevenin source resistance is recommended.

NOTE

Applying a sustained logic 1 corresponds to zero Hz PWM frequency and will cause the module to stop switching.

7.3.2 Output Overvoltage Protection

If the voltage at FB is greater than the 0.86-V internal reference the output of the error amplifier is pulled toward ground causing V_O to fall.

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Feature Description (continued)

7.3.3 Current Limit

The LMZ22005 is protected by both low-side (LS) and high-side (HS) current limit circuitry. The LS current limit detection is carried out during the OFF-time by monitoring the current through the LS synchronous MOSFET. Referring to the *Functional Block Diagram*, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 5.4 A (typical) the current limit comparator disables the start of the next switching period. Switching cycles are prohibited until current drops below the limit.

NOTE

DC current limit is dependent on duty cycle as illustrated in the graph in the *Typical Characteristics* section.

The HS current limit monitors the current of top side MOSFET. Once HS current limit is detected (7 A typical) , the HS MOSFET is shutoff immediately, until the next cycle. Exceeding HS current limit causes V_O to fall. Typical behavior of exceeding LS current limit is that f_{SW} drops to 1/2 of the operating frequency.

7.3.4 Thermal Protection

The junction temperature of the LMZ22005 must not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal thermal shutdown circuit which activates at 165°C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the C_{SS} capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 150°C (typical hysteresis = 15°C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require additional derating at elevated temperatures.

7.3.5 Prebiased Start-Up

The LMZ22005 will properly start up into a prebiased output. This start-up situation is common in multiple rail logic applications where current paths may exist between different power rails during the start-up sequence. Figure 44 shows proper behavior in this mode. Trace one is Enable going high. Trace two is 1.5-V prebias rising to 3.3 V. Rise time determined by C_{SS}, trace three.

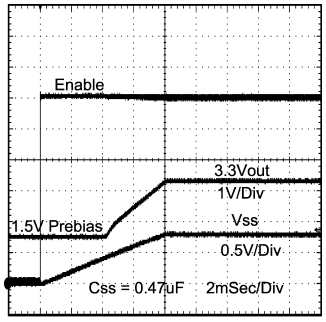


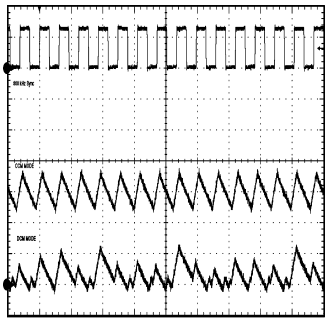
Figure 44. Prebiased Start-Up

7.4 Device Functional Modes

7.4.1 Discontinuous And Continuous Conduction Modes

At light load the regulator will operate in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it will operate in continuous conduction mode (CCM). In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. When operating in DCM, inductor current is maintained to an average value equaling I_{OUT}. Inductor current exhibits normal behavior for the emulated current mode control method used. Output voltage ripple typically increases during this mode of operation.

Figure 45 is a comparison pair of waveforms of the showing both CCM (upper) and DCM operating modes.



V_{IN} = 12 V, V_O = 3.3 V, I_O = 3 A / 0.3 A 2 µs/div

Figure 45. CCM and DCM Operating Modes

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ22005 is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 5 A. The following design procedure can be used to select components for the LMZ22005. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. Please go to www.ti.com for more details.

8.2 Typical Application

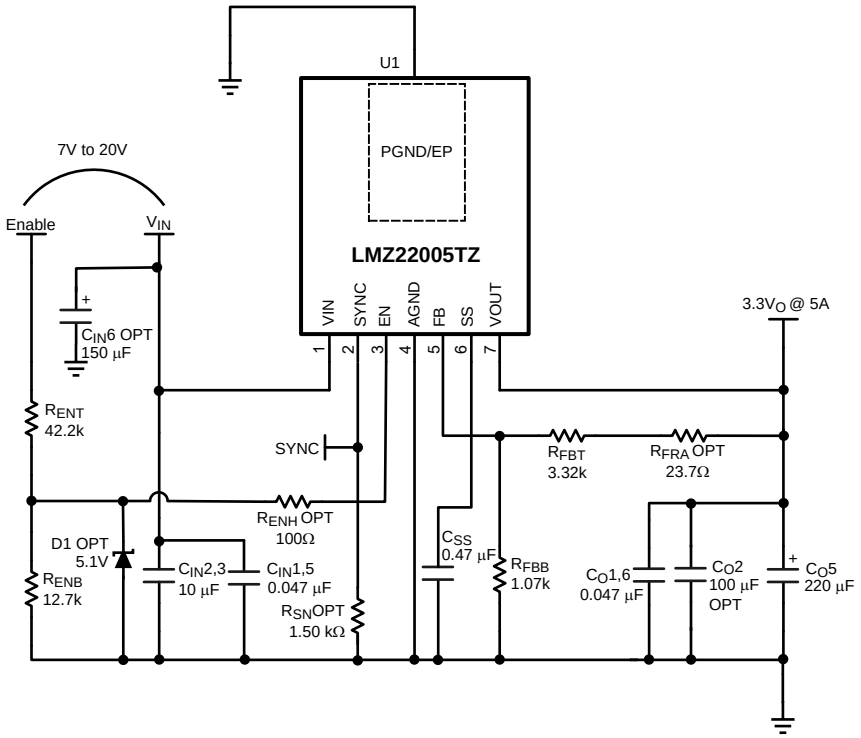

Figure 46. Typical Application Schematic

8.2.1 Design Requirements

For this example the following application parameters exist:

- V_{IN} Range = Up to 20 V
- V_{OUT} = 0.8 V to 6 V
- I_{OUT} = 5 A

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Design Steps

The LMZ22005 is fully supported by WEBENCH which offers: component selection, electrical and thermal simulations. Additionally there is are evaluation and demonstration boards that may be used a starting point for design. The following list of steps can be used to quickly design the LMZ22005 application.

1. Select minimum operating V_{IN} with enable divider resistors
2. Program V_O with resistor divider selection
3. Select C_O
4. Select C_{IN}
5. Determine module power dissipation
6. Layout PCB for required thermal performance

8.2.2.2 Enable Divider, R_{ENT}, R_{ENB} and R_{ENH} Selection

Internal to the module is a 2-MΩ pullup resistor connected from V_{IN} to Enable. For applications not requiring precision undervoltage lockout (UVLO), the Enable input may be left open circuit and the internal resistor will always enable the module. In such case, the internal UVLO occurs typically at 4.3 V (V_{IN} rising).

In applications with separate supervisory circuits Enable can be directly interfaced to a logic source. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ22005 output rail.

Enable provides a precise 1.279-V threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. Additionally there is 21 µA (typical) of switched offset current allowing programmable hysteresis. See Figure 47.

The function of the enable divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable UVLO. The two resistors must be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\ UVLO} / 1.279\ V) - 1 \quad (1)$$

The LMZ22005 typical application shows 12.7 kΩ for R_{ENB} and 42.2 kΩ for R_{ENT} resulting in a rising UVLO of 5.46 V.

NOTE

A midpoint 5.1-V Zener clamp is present to allow setting UVLO to cover an extended range of operation. The Zener clamp is not required if the target application prohibits the maximum Enable input voltage from being exceeded.

Additional enable voltage hysteresis can be added with the inclusion of R_{ENH}. It may be possible to select values for R_{ENT} and R_{ENB} such that R_{ENH} is a value of zero allowing it to be omitted from the design.

Rising threshold can be calculated as follows:

$$V_{EN}(rising) = 1.279\ (\ 1 + R_{ENT} || \ 2\ meg / R_{ENB}) \quad (2)$$

Whereas falling threshold level can be calculated using:

$$V_{EN}(falling) = V_{EN}(rising) - 21\ \mu A\ (\ R_{ENT} || \ 2\ meg \ || \ R_{ENTB} + R_{ENH}\ ) \quad (3)$$

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Typical Application (continued)

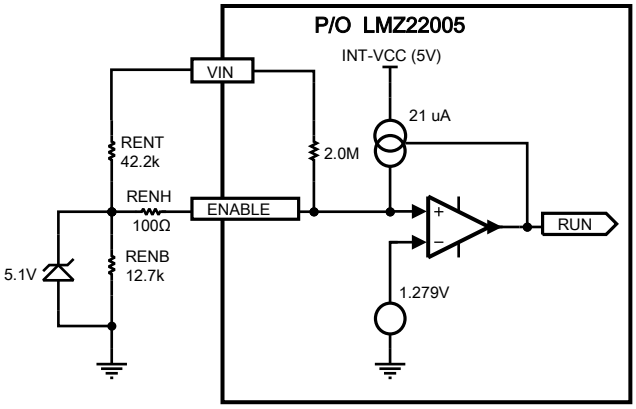

Figure 47. Enable Input Detail

8.2.2.3 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.8\ V \times (1 + R_{FBT} / R_{FBB}) \quad (4)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.796\ V) - 1 \quad (5)$$

These resistors must generally be chosen from values in the range of 1.0 kΩ to 10.0 kΩ.

For V_O = 0.8 V the FB pin can be connected to the output directly and R_{FBB} can be omitted.

Table 1 lists the values for R_{FBT} , and R_{FBB}.

Table 1. Typical Application Bill of Materials

REF DES	DESCRIPTION	CASE SIZE	MANUFACTURER	MANUFACTURER P/N
U1	SIMPLE SWITCHER	PFM-7	Texas Instruments	LMZ22005TZ
C_{in}1,5	0.047 µF, 50 V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_{in}2,3	10 µF, 50 V, X7R	1210	Taiyo Yuden	UMK325BJ106MM-T
C_{in}6 (OPT)	CAP, AL, 150 µF, 50 V	Radial G	Panasonic	EEE-FK1H151P
C_O1,6	0.047 µF, 50 V, X7R	1206	Yageo America	CC1206KRX7R9BB473
C_O2 (OPT)	100 µF, 6.3 V, X7R	1210	TDK	C3225X5R0J107M
C_O5	220 µF, 6.3 V, SP-Cap	(7343)	Panasonic	EEF-UE0J221LR
R_{FBT}	3.32 kΩ	0805	Panasonic	ERJ-6ENF3321V
R_{FBB}	1.07 kΩ	0805	Panasonic	ERJ-6ENF1071V
R_{SN} (OPT)	1.50 kΩ	0805	Vishay Dale	CRCW08051K50FKEA
R_{ENT}	42.2 kΩ	0805	Panasonic	ERJ-6ENF4222V
R_{ENB}	12.7 kΩ	0805	Panasonic	ERJ-6ENF1272V
R_{FRA}(OPT)	23.7Ω	0805	Vishay Dale	CRCW080523R7FKEA
R_{ENH}	100 Ω	0805	Vishay Dale	CRCW0805100RFKEA
C_{FF}	180 pF, ±10%, C0G, 50 V	0805	TDK	08055A181JAT2A
C_{SS}	047 µF, ±10%, X7R, 16 V	0805	AVX	0805YC474KAT2A
D1(OPT)	5.1 V, 0.5 W	SOD-123	Diodes Inc.	MMSZ5231BS-7-F

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8.2.2.4 Soft-start Capacitor Selection

Programmable soft-start permits the regulator to slowly ramp to its steady-state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time.

Upon turnon, after all UVLO conditions have been passed, an internal 2-ms circuit slowly ramps the SS/TRK input to implement internal soft-start. If 1.6 ms is an adequate turnon time then the C_{SS} capacitor can be left unpopulated. Longer soft-start periods are achieved by adding an external capacitor to this input.

Soft-start duration is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / Iss = 0.796\ V \times C_{SS} / 50\ \mu A \quad (6)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 50\ \mu A / 0.796\ V \quad (7)$$

Using a 0.22-µF capacitor results in 3.5-ms typical soft-start duration; and 0.47 µF results in 7.5-ms typical. 0.47 µF is a recommended initial value.

Once the soft-start input exceeds 0.796 V the output of the power stage will be in regulation and the 50-µA current is deactivated. The following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal current sink.

- The Enable input being *pulled low*
- Thermal shutdown condition
- Internal V_{CC} UVLO (Approx 4.3V input to V_{IN})

8.2.2.5 Tracking Supply Divider Option

The tracking function allows the module to be connected as a slave supply to a primary voltage rail (often the 3.3-V system rail) where the slave module output voltage is lower than that of the master. Proper configuration allows the slave rail to power up coincident with the master rail such that the voltage difference between the rails during ramp-up is small (that is, <0.15 V typical). The values for the tracking resistive divider must be selected such that the effect of the internal 50-µA current source is minimized. In most cases the ratio of the tracking divider resistors is the same as the ratio of the output voltage setting divider. Proper operation in tracking mode dictates the soft-start time of the slave rail be shorter than the master rail; a condition that is easy satisfy because the C_{SS} cap is replaced by R_{TKB}. The tracking function is only supported for the power up interval of the master supply; once the SS/TRK rises past 0.8V the input is no longer enabled and the 50-µA internal current source is switched off.

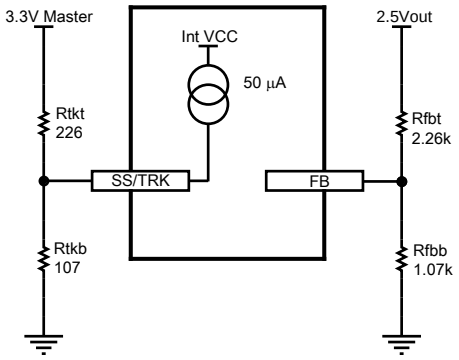

Figure 48. Tracking Option Input Detail

8.2.2.6 C_O Selection

None of the required C_O output capacitance is contained within the module. A minimum value of 200 µF is required based on the values of internal compensation in the error amplifier. Low ESR tantalum, organic semiconductor or specialty polymer capacitor types are recommended for obtaining lowest ripple. The output capacitor C_O may consist of several capacitors in parallel placed in close proximity to the module. The output capacitor assembly must also meet the worst case minimum ripple current rating of 0.5 × I_{LRP-P}, as calculated in Equation 14. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. Loop response verification is also valuable to confirm closed loop behavior.

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For applications with dynamic load steps; the following equation provides a good first pass approximation of C_O for load transient requirements. Where $V_{O\text{-}Tran}$ is 100 mV on a 3.3-V output design.

$$C_O \geq I_{O\text{-}Tran} / (V_{O\text{-}Tran} – ESR \times I_{O\text{-}Tran}) \times (Fsw / V_O) \quad (8)$$

Solving:

$$C_O \geq 4.5\ A / (0.1\ V – 0.007 \times 4.5\ A) \times (\ 800000\ Hz / 3.3\ V) \geq 271\ \mu F \quad (9)$$

NOTE

The stability requirement for 200-µF minimum output capacitance will take precedence.

One recommended output capacitor combination is a 220-µF, 7-mΩ ESR specialty polymer cap in parallel with a 100-µF, 6.3-V X5R ceramic. This combination provides excellent performance that may exceed the requirements of certain applications. Additionally some small ceramic capacitors can be used for high-frequency EMI suppression.

8.2.2.7 C_{IN} Selection

The LMZ22005 module contains only a small amount of input capacitance. Additional input capacitance is required external to the module to handle the input ripple current of the application. The input capacitor can be several capacitors in parallel. This input capacitance must be located in very close proximity to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Input ripple current rating is dictated by the equation:

$$I(C_{IN(RMS)}) \cong 1 / 2 \times I_O \times SQRT\ (D / 1 – D)$$

where

- $D \cong V_O / V_{IN}$ (10)

As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$.

Recommended minimum input capacitance is 22-µF X7R (or X5R) ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI recommends to pay attention to the voltage and temperature derating of the capacitor selected. The ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may have to contact the capacitor manufacturer for this parameter.

If the system design requires a certain minimum value of peak-to-peak input ripple voltage (ΔV_{IN}) be maintained then the following equation may be used.

$$C_{IN} \geq I_O \times D \times (1 – D) / f_{SW\text{-}CCM} \times \Delta V_{IN} \quad (11)$$

If ΔV_{IN} is 1% of V_{IN} for a 12-V input to 3.3-V output application this equals 120 mV and f_{SW} = 812 kHz.

$$C_{IN} \geq 5\ A \times 3.3\ V / 12\ V \times (1 – 3.3\ V / 12\ V) / (812000 \times 0.120\ V) \geq 10.2\ \mu F \quad (12)$$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines. The LMZ22005 typical applications schematic recommends a 150-µF 50-V aluminum capacitor for this function. There are many situations where this capacitor is not necessary.

8.2.2.8 Discontinuous And Continuous Conduction Modes Selection

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O \times (V_{IN} – V_O) / (2 \times 3.3\ \mu H \times f_{SW(CCM)} \times V_{IN}) \quad (13)$$

The inductor internal to the module is 3.3 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\ P\text{-}P} = V_O \times (V_{IN} – V_O) / (3.3\ \mu H \times f_{SW} \times V_{IN})$$

where

- V_{IN} is the maximum input voltage
- And f_{SW} is typically 812 kHz. (14)

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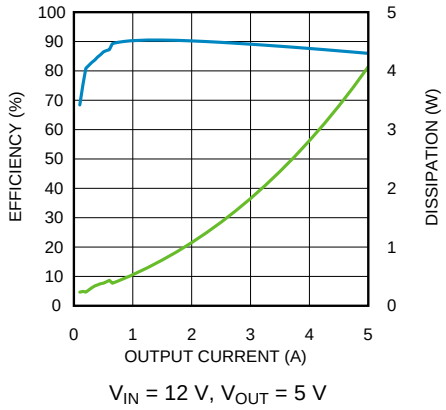
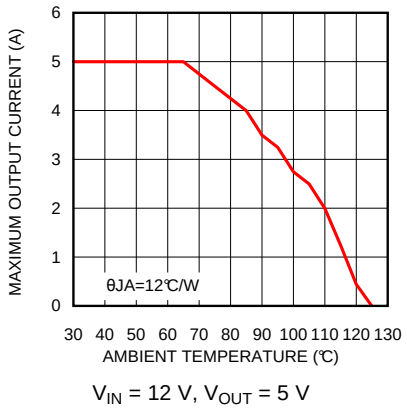
If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined.

8.2.3 Application Curves



V_{IN} = 12 V, V_{OUT} = 5 V

Figure 49. Efficiency



V_{IN} = 12 V, V_{OUT} = 5 V

Figure 50. Thermal Derating Curve

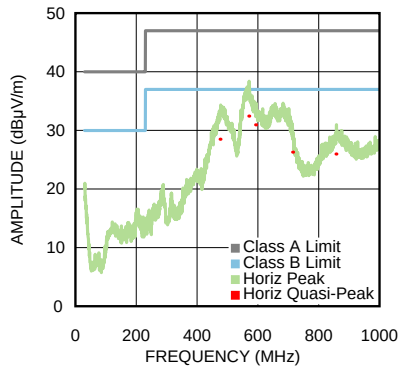


Figure 51. Radiated EMI (EN 55022) of Demo Board (See AN-2125)

9 Power Supply Recommendations

The LMZ22005 device is designed to operate from an input voltage supply range between 6 V and 20 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMZ22005 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is more than a few inches from the LMZ22005, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-µF or 100-µF electrolytic capacitor is a typical choice.

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10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules. A good example layout is shown in Figure 54.

1. **Minimize area of switched current loops.**

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PCB layout as shown in Figure 52. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (C_{IN1}) is placed at a distance away from the LMZ22005. Therefore place C_{IN1} as close as possible to the LMZ22005 VIN and PGND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the PGND exposed pad (EP).

2. **Have a single point ground.**

   The ground connections for the feedback, soft-start, and enable components should be routed to the AGND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Additionally provide the single point ground connection from pin 4 (AGND) to EP/PGND.

3. **Minimize trace length to the FB pin.**

   Both feedback resistors, R_{FBT} and R_{FBB}, and the feed-forward capacitor C_{FF}, must be located close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The traces from R_{FBT}, R_{FBB}, and C_{FF} must be routed away from the body of the LMZ22005 to minimize possible noise pickup.

4. **Make input and output bus connections as wide as possible.**

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. **Provide adequate device heat-sinking.**

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 10 via array with a minimum via diameter of 8 mils thermal vias spaced 39 mils (1.0 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

10.2 Layout Examples

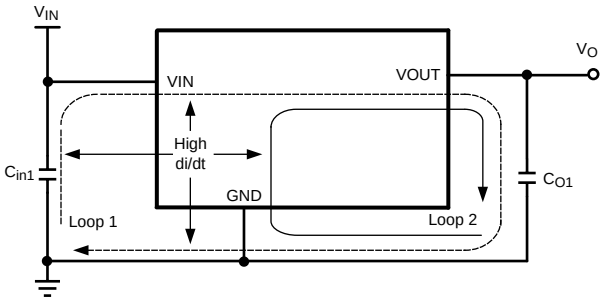

Figure 52. Critical Current Loops to Minimize

Layout Examples (continued)

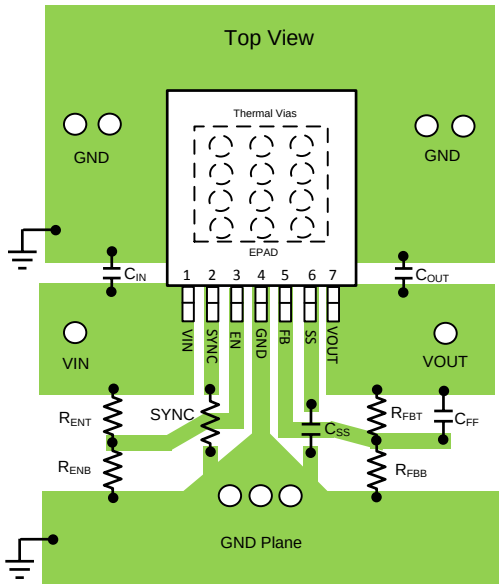

Figure 53. PCB Layout Guide

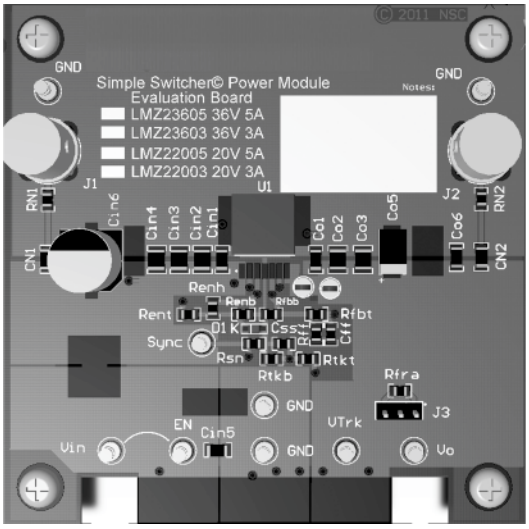

Figure 54. Top View Evaluation Board – See AN–2085 SNVA457

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Layout Examples (continued)

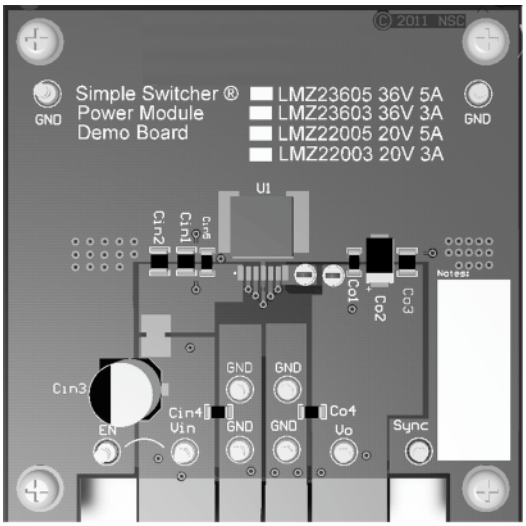

Figure 55. Bottom View Demonstration Board

10.3 Power Dissipation and Thermal Considerations

When calculating module dissipation use the maximum input voltage and the average output current for the application. Many common operating conditions are provided in the characteristic curves such that less common applications can be derived through interpolation. In all designs, the junction temperature must be kept below the rated maximum of 125°C.

For the design case of V_{IN} = 12 V, V_O = 3.3 V, I_O = 5 A, and $T_{AMB(MAX)}$ = 85°C, the module must see a thermal resistance from case to ambient of less than:

$$R_{\theta CA} < (T_{J\text{-}MAX} - T_{A\text{-}MAX}) / P_{IC\text{-}LOSS} - R_{\theta JC} \quad (15)$$

Given the typical thermal resistance from junction to case to be 1.9°C/W. Use the 85°C power dissipation curves in the *Typical Characteristics* section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is 4.3W.

$$R_{\theta CA} = (125 - 85) / 4.3\ W - 1.9 = 7.4 \quad (16)$$

To reach $R_{\theta CA}$ = 7.4, the PCB is required to dissipate heat effectively. With no airflow and no external heat-sink, a good estimate of the required board area covered by 2-oz. copper on both the top and bottom metal layers is:

$$Board\_Area\_cm^2 = 500°C \times cm^2/W / R_{\theta CA} \quad (17)$$

As a result, approximately 67 square cm of 2-oz. copper on top and bottom layers is required for the PCB design. The PCB copper heat sink must be connected to the exposed pad. Approximately sixty, 8 mils thermal vias spaced 39 mils (1.0 mm) apart connect the top copper to the bottom copper. For an example of a high thermal performance PCB layout for SIMPLE SWITCHER power modules, refer to AN-2085 (SNVA457), AN-2125 (SNVA437), AN-2020 (SNVA419) and AN-2026 (SNVA424).

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10.4 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern — Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste — Use a standard SAC Alloy such as SAC 305, type 3 or higher
- Stencil Thickness — 0.125 to 0.15 mm
- Reflow — Refer to solder paste supplier recommendation and optimized per board size and density
- Refer to *Design Summary LMZ1xxx and LMZ2xxx Power Modules Family* (SNAA214) for reflow information
- Maximum number of reflows allowed is one

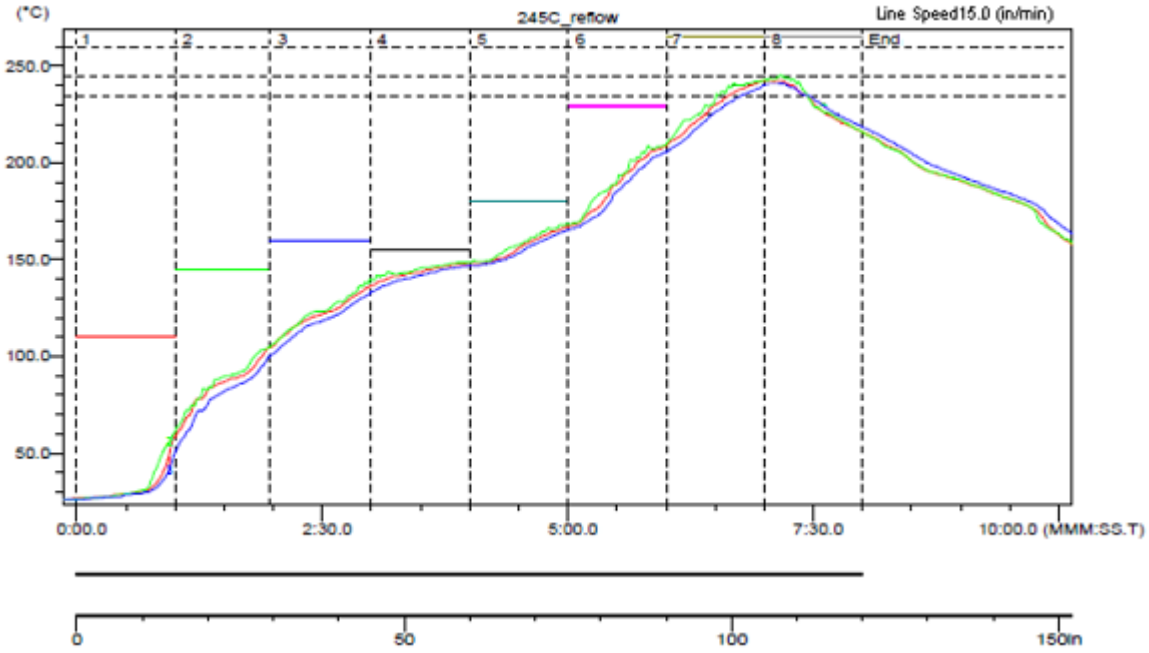

Figure 56. Sample Reflow Profile

Table 2. Sample Reflow Profile Table

PROBE	MAX TEMP (°C)	REACHED MAX TEMP	TIME ABOVE 235°C	REACHED 235°C	TIME ABOVE 245°C	REACHED 245°C	TIME ABOVE 260°C	REACHED 260°C
1	242.5	6.58	0.49	6.39	0.00	–	0.00	–
2	242.5	7.10	0.55	6.31	0.00	7.10	0.00	–
3	241.0	7.09	0.42	6.44	0.00	–	0.00	–

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Development Support

For developmental support, see the following:

WEBENCH Tool, http://www.ti.com/webench

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- AN-2027 *Inverting Application for the LMZ14203 SIMPLE SWITCHER Power Module*, (SNVA425)
- *Absolute Maximum Ratings for Soldering*, (SNOA549)
- AN-2024 *LMZ1420x / LMZ1200x Evaluation Board* (SNVA422)
- AN-2085 *LMZ23605/03, LMZ22005/03 Evaluation Board* (SNVA457)
- AN-2054 *Evaluation Board for LM10000 - PowerWise AVS System Controller* (SNVA437)
- AN-2020 *Thermal Design By Insight, Not Hindsight* (SNVA419)
- AN-2026 *Effect of PCB Design on Thermal Performance of SIMPLE SWITCHER Power Modules* (SNVA424)
- *Design Summary LMZ1xxx and LMZ2xxx Power Modules Family* (SNAA214)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ22005TZ/NOPB	ACTIVE	TO-PMOD	NDW	7	45	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 85	LMZ22005	Samples
LMZ22005TZE/NOPB	ACTIVE	TO-PMOD	NDW	7	250	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 85	LMZ22005	Samples
LMZ22005TZX/NOPB	ACTIVE	TO-PMOD	NDW	7	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 85	LMZ22005	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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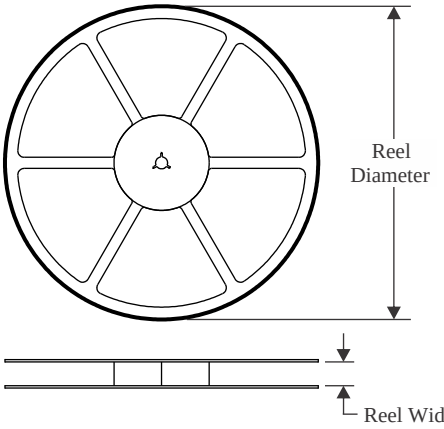
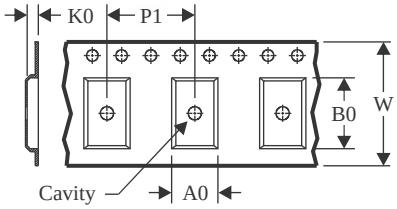
TAPE AND REEL INFORMATION

REEL DIMENSIONS

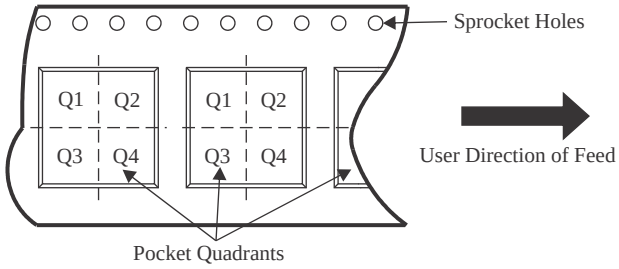


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

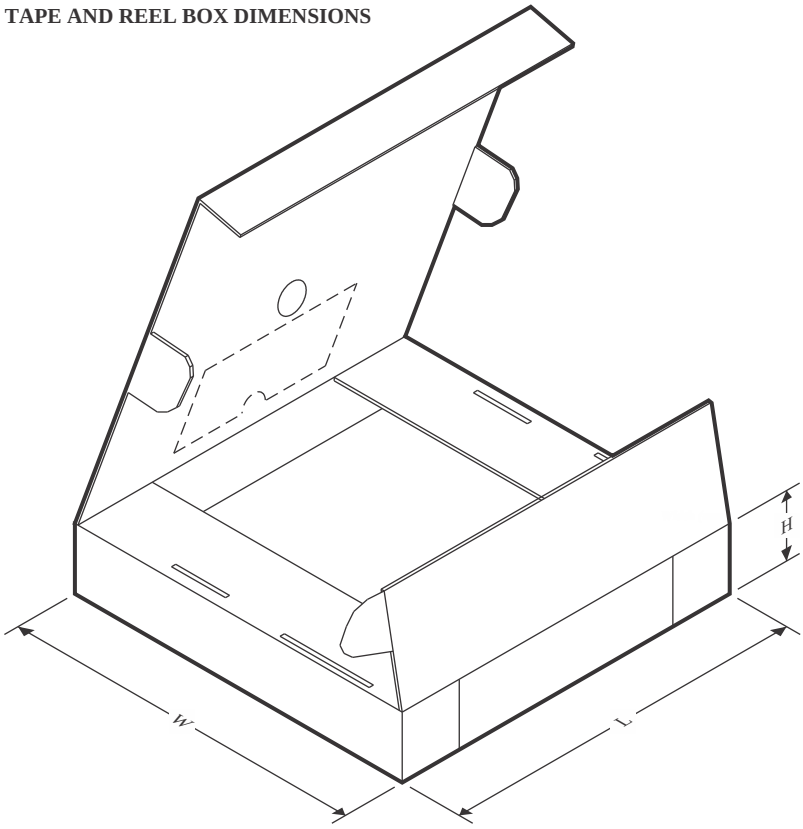
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ22005TZE/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ22005TZX/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

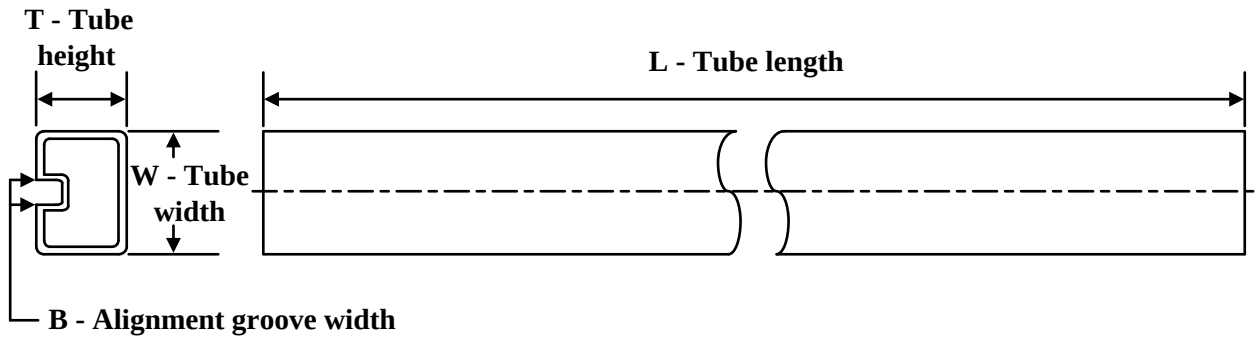
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ22005TZE/NOPB	TO-PMOD	NDW	7	250	356.0	356.0	45.0
LMZ22005TZX/NOPB	TO-PMOD	NDW	7	500	356.0	356.0	45.0

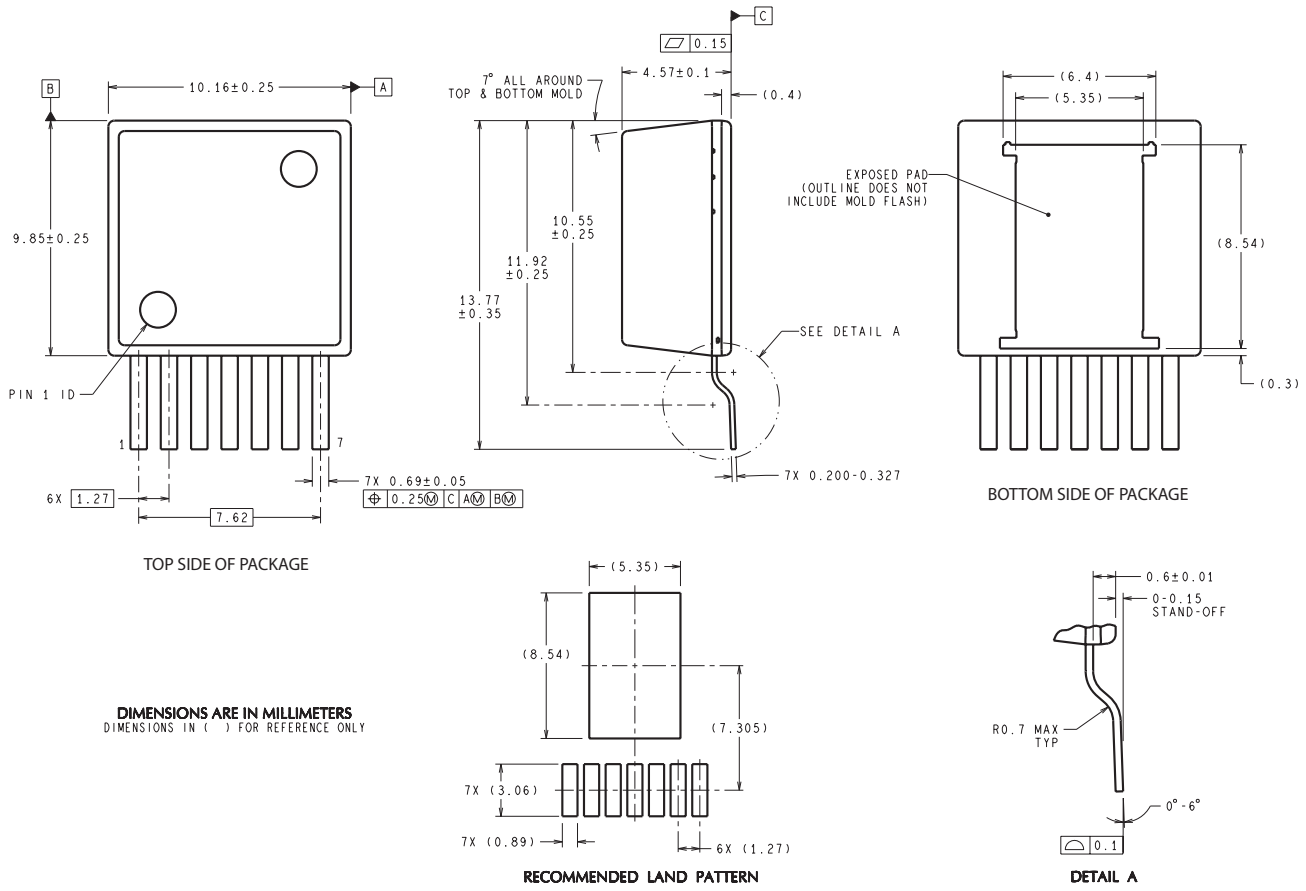
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMZ22005TZ/NOPB	NDW	TO-PMOD	7	45	502	17	6700	8.4

NDW0007A



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