LP5922 2-A Low-Noise, Adjustable LDO With Low Input- and Output-Voltage Capability

1 Features

- Wide Input Voltage Range: 1.3 V to 6 V
- Low V_{IN} Voltage Without Extra Bias Voltage
- Adjustable Output Voltage: 0.5 V to 5 V
- Low Dropout: 200 mV at 2-A Load
- Low Output Voltage Noise: 25 μV_{RMS}
- Output Current: 2 A
- –40˚C to +125°C Operating Junction Temperature
- Programmable Soft Start Limits Inrush Current
- 3-mm × 3-mm × 0.75-mm 10-Pin WSON Package
- Thermal-Overload and Short-Circuit Protection
- Output Voltage Tolerance: ±1.5%
- Shutdown Supply Current : 0.1 µA
- PSRR: 70 dB at 1 kHz
- Power Good Output
- Create a Custom Design Using the LP5922 With the WEBENCH® Power Designer

2 Applications

- Space-Constrained Applications
- Noise- and Ripple-Sensitive High Current Analog or RF Systems
- Target Sectors
  - Medical, Test and Measurement Equipment
  - Portable and Consumer electronics
  - Telecom and Networking Cards
  - Wireless Infrastructure
  - Industrial Applications
- Typical Systems
  - Radio Transceivers, Power Amplifiers, PLL/Synthesizer, Clocking, VCO, GPRS, 3G Modules, FPGAs, DSP, GPUs, and others

3 Description

The LP5922 is 2-A low dropout (LDO) linear regulator with 200-mV typical dropout voltage at maximum current levels. The LP5922 device can operate from a voltage rail down to 1.3 V without additional bias supply. System efficiency is maximized and power dissipation minimized by the low dropout and low V_{IN} capability. The device also features low quiescent current and very low shutdown current.

The LP5922 device was designed to have high PSRR and low output noise to support sensitive analog applications without additional filtering. The output noise can be reduced even further by implementing a small capacitor on the SS/NR pin.

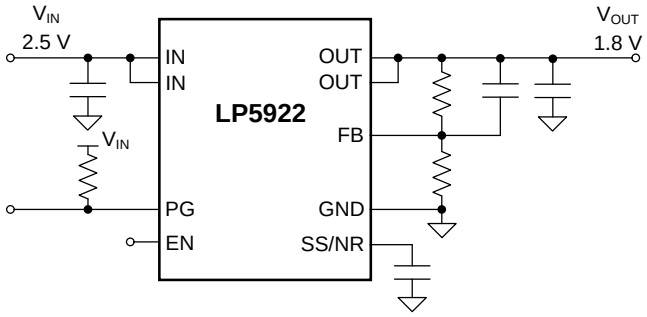
The output voltage is adjustable from 0.5 V to 5 V by an external resistor divider. Enable pin, adjustable soft start and optional Power Good features help with system power sequencing. Inrush current is controlled with the soft start and the device has short circuit and thermal protections.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP5922	WSON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



PSRR

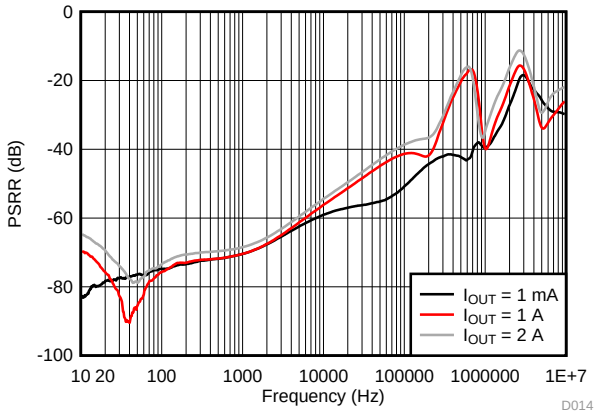


Table of Contents

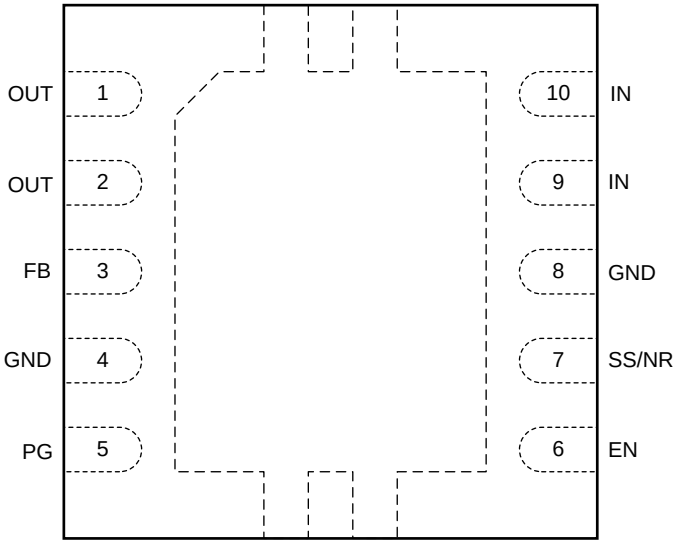
4 Revision History

Changes from Original (November 2016) to Revision A **Page**

- Added links to WEBENCH ... 1
- Changed load transients test conditions from "V_{OUT} = 3.3 V" to "V_{OUT} = 2.8 V" and "t_{RISE} = t_{FALL} = 1 V/µs" to "t_{RISE} = t_{FALL} = 1 A/µs" ... 6
- Changed "t_{fall} = 1 V/µs" to "t_{fall} = 1 A/µs" in legend to Figure 9 ... 8
- Changed scope shot in Figure 10 (was duplicate of Fig 9) and changed condition from "t_{fall} = 1 V/µs" to "t_{fall} = 1 A/µs" ... 8
- Changed t_{fall} = 1 V/µs" to "t_{RISE} =t_{FALL} = 5 µs" in Figure 11 conditions ... 8
- Added *Custom Design With WEBENCH Tools* subsection ... 14

5 Pin Configuration and Functions

DSC Package
10-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT	O	Regulated output voltage, connect directly to pin 2
2	OUT	O	Regulated output voltage, connect directly to pin 1
3	FB	I	Voltage feedback input to the internal error amplifier
4	GND	Ground	Ground; connect to device pin 8.
5	PG	O	Power Good to indicate the status of output voltage. Requires an external pullup resistor. When PG pin voltage is high the output voltage is considered good.
6	EN	I	Enable
7	SS/NR	I/O	Soft-start and noise reduction pin
8	GND	Ground	Ground —connect to device pin 4.
9	IN	I	Supply voltage input — connect directly to pin 10.
10	IN	I	Supply voltage input —connect directly to pin 9.
Exposed pad	Thermal Pad	—	The exposed thermal pad on the bottom of the package must be connected to a copper area under the package on the PCB. Connect to ground potential. Do not connect to any potential other than the same ground potential seen at device pins 4 and 8 (GND). See *Power Dissipation* for more information.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
IN pin voltage, V_{IN}	–0.3	7	V
OUT pin voltage, V_{OUT}		See(3)	
EN pin voltage, V_{EN}	–0.3	7	V
PG pin voltage, V_{PG}	–0.3	7	V
SS/NR pin voltage, $V_{SS/NR}$	–0.3	3.6	V
FB pin voltage, V_{FB}	–0.3	3.6	V
Junction temperature, T_J		150	°C
Continuous power dissipation(4)	Internally limited		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Absolute maximum V_{OUT} is the lesser of V_{IN} + 0.3 V, or 7 V.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, V_{IN}	1.3		6	V
Output voltage, V_{OUT}	0.5		5	V
FB voltage, V_{FB}		0.5		V
EN input voltage, V_{EN}	0		V_{IN}	V
Recommended load current, I_L	0		2	A
Operating junction temperature, $T_{J-MAX-OP}$	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LP5922 DSC (WSON) 10 PINS	UNIT
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance, High K	49.5(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.0	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by *JESD51-7 - High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.*
(3) The PCB for the WSON/DSC package $R_{\theta JA}$ includes four (4) thermal vias, in a 2 × 2 array, under the exposed thermal pad per EIA/JEDEC JESD51-5.

6.5 Electrical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.3 V, whichever is greater; V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor (unless otherwise noted).[1][2][3]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{IN}	Input voltage range		1.3		6	V
UVLO	Undervoltage lock-out threshold	V_{IN} Rising (↑) until output is ON		1.2	1.25	V
ΔUVLO	UVLO hysteresis	V_{IN} Falling (↓) from UVLO threshold until output is OFF		160		mV
OUTPUT VOLTAGE AND REGULATION						
V_{OUT}	Output voltage range		0.5		5	V
ΔV_{OUT}	Line regulation	I_{OUT} = 5 mA, 1.3 V ≤ V_{IN} ≤ 6 V		0.02		%/V
	Load regulation	5 mA ≤ I_{OUT} ≤ 2 A		0.1		%/A
V_{DO}	Dropout voltage[4]	V_{IN} = 1.4 V, I_{OUT} = 2 A		220	400	mV
		V_{IN} = 2.5 V, I_{OUT} = 2 A		100	180	
		V_{IN} = 5.3 V, I_{OUT} = 2 A		90	160	
FB						
V_{FB}	FB voltage	I_{OUT} = 5 mA to 2 A	492.5	500	507.5	mV
I_{FB}	FB pin input current	V_{FB} = 0.5 V	–100		100	nA
CURRENT LEVELS						
I_L	Maximum load current	V_{IN} ≥ 1.3 V	2			A
I_{SC}	Short-circuit current limit[5]		2.2	3	3.8	A
I_{GND}	Ground-current minimum load[6]	V_{IN} = 6 V, I_{OUT} = 0 mA		0.7		mA
	Ground-current maximum load[6]	V_{IN} = 1.3 V, I_{OUT} = 2 A		1	4	
$I_{GND(SD)}$	Shutdown current[7]	V_{IN} = 6 V, V_{EN} = 0 V, V_{PG} = 0 V		0.1	15	µA
V_{IN} to V_{OUT} RIPPLE REJECTION [8]						
PSRR	Power-supply rejection ratio	V_{IN} ≥ 1.4 V, f = 1 kHz, I_{OUT} = 2 A		70		dB
		V_{IN} ≥ 1.4 V, f = 10 kHz, I_{OUT} = 2 A		55		
		V_{IN} ≥ 1.4 V, f = 100 kHz, I_{OUT} = 2 A		40		
		V_{IN} ≥ 1.4 V, f = 1 MHz, I_{OUT} = 2 A		30		
OUTPUT NOISE VOLTAGE						
e_N	Noise voltage[8]	V_{IN}= 2.5 V, V_{OUT}= 1.8 V BW = 10 Hz to 100 kHz		25		μV_{RMS}

(1) All voltages are with respect to the GND pin.
(2) Minimum and maximum limits are design targeted limits over the junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.
(3) C_{IN}, C_{OUT}: Low-ESR surface-mount-ceramic capacitors (MLCCs) used in setting electrical characteristics.
(4) Dropout voltage is the voltage difference between the input and the output at which the FB voltage drops to 97% of its nominal value.
(5) Short-circuit current (I_{SC}) is equivalent to current limit. To minimize thermal effects during testing, I_{SC} is measured with V_{OUT} pulled to 100 mV below its nominal voltage.
(6) Ground current is defined here as the total current flowing to ground as a result of all voltages applied to the device I_{GND} = ((I_{IN} – I_{OUT}) + I_{EN} + $I_{LKG(PG)}$)
(7) Ground current in shutdown mode, $I_{GND(SD)}$, does NOT include current from PG pin.
(8) This specification is verified by design.

Electrical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.3 V, whichever is greater; V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor (unless otherwise noted).(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUT THRESHOLDS						
$V_{IL(EN)}$	EN pin low threshold	V_{EN} falling (↓) until output is OFF			0.35	V
$V_{IH(EN)}$	EN pin high threshold	V_{EN} rising (↑) until output is ON	1.2			V
I_{EN}	Input current at EN pin (9)	V_{IN} = 6 V, V_{EN} = 6 V		3		µA
PG_{HTH}	PG high threshold (% of nominal V_{OUT})	V_{OUT} rising (↑) until PG goes high		94%		
PG_{LTH}	PG low threshold (% of nominal V_{OUT})	V_{OUT} falling (↓) until PG goes low		90%		
$V_{OL(PG)}$	PG pin low-level output voltage	V_{OUT} < PG_{LTH}, sink current = 1 mA			400	mV
$I_{LKG(PG)}$	PG pin leakage current	V_{OUT} > PG_{HTH}, V_{PG} = 6 V			1	µA
SOFT START						
I_{SS}	SS/NR pin charging current			6.2		µA
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			165		°C
ΔT_{SD}	Thermal shutdown hysteresis			15		°C
TRANSITION CHARACTERISTICS						
ΔV_{OUT}	Line transients	ΔV_{IN} = 0.5 V, V_{OUT} = 2.8 V, t_{RISE} = t_{FALL} = 5 µs		3		mV
	Load transients	V_{OUT} = 2.8 V, I_{OUT} = 10 mA to 2 A to 10 mA t_{RISE} = t_{FALL} = 1 A/µs		25		
R_{AD}	Output discharge pull-down resistance	V_{EN} = 0 V, V_{IN} = 2.3 V		400		Ω

(9) There is a 2-MΩ resistor between EN and ground (pulldown) on the device.

6.6 Input and Output Capacitors

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{IN}	Input capacitance(1)			22		µF
C_{OUT}	Output capacitance	V_{OUT} ≤ 0.8 V	34	47		µF
		V_{OUT} > 0.8 V	15	22		

(1) Typically input capacitance placed close to the device is in the same order as output capacitance. See also *Input Capacitor, C_{IN}*.

6.7 Typical Characteristics

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor and T_J = 25°C, unless otherwise stated.

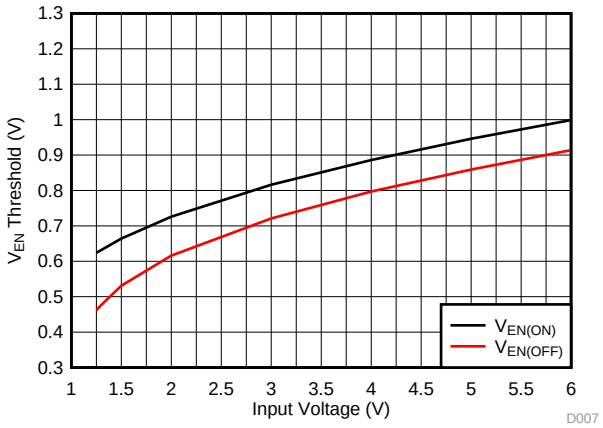


Figure 1. V_{EN} Thresholds vs Input Voltage

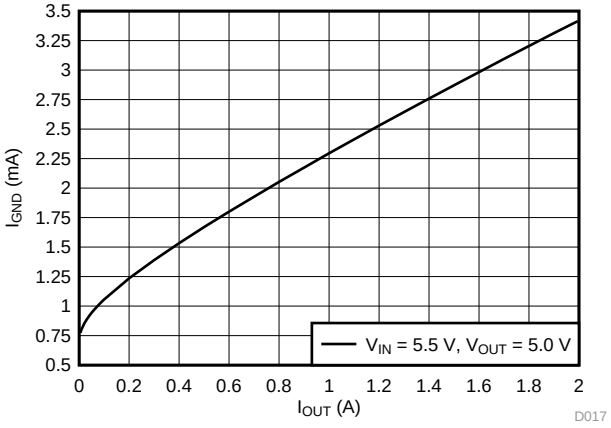
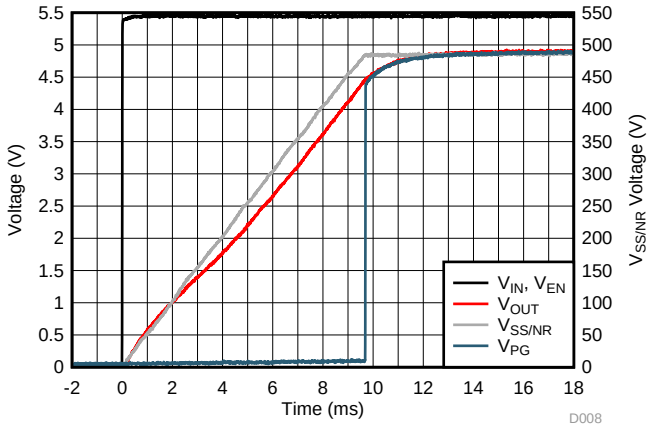
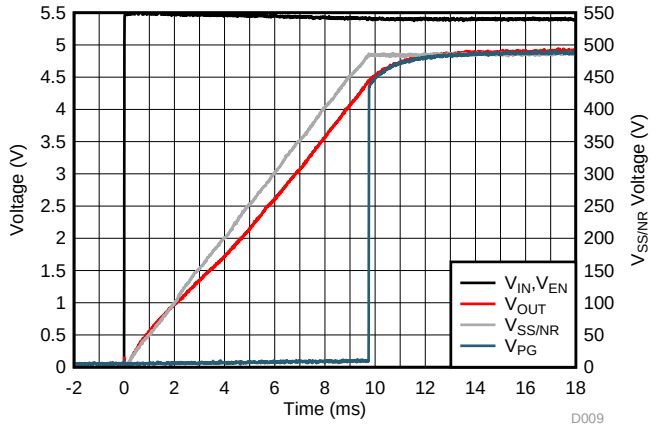


Figure 2. Ground Current vs Output Current



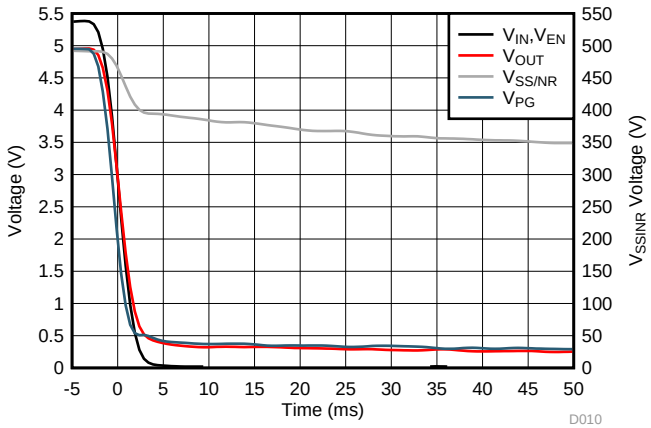
V_{OUT} = 5 V V_{EN} = V_{IN} I_{OUT} = 1 mA

Figure 3. Power Up



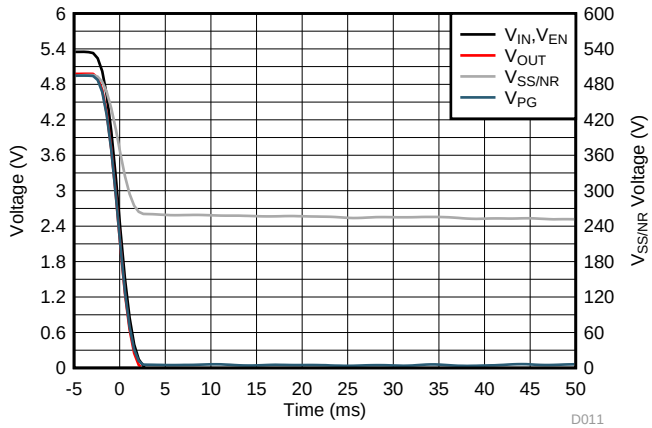
V_{OUT} = 5 V V_{EN} = V_{IN} I_{OUT} = 2 A

Figure 4. Power Up



V_{OUT} = 5 V V_{EN} = V_{IN} I_{OUT} = 1 mA

Figure 5. Power Down

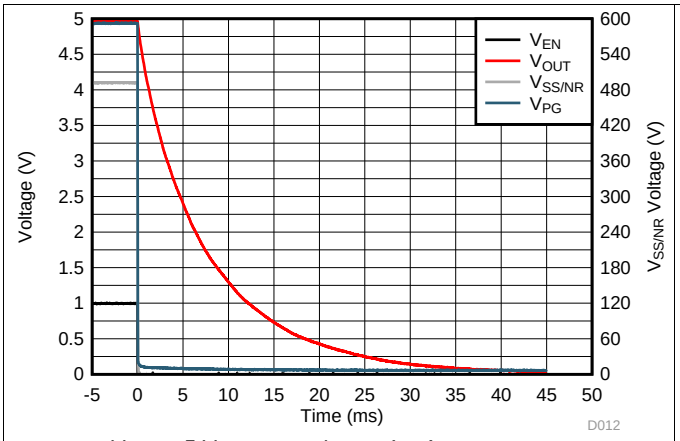


V_{OUT} = 5 V V_{EN} = V_{IN} I_{OUT} = 2 A

Figure 6. Power Down

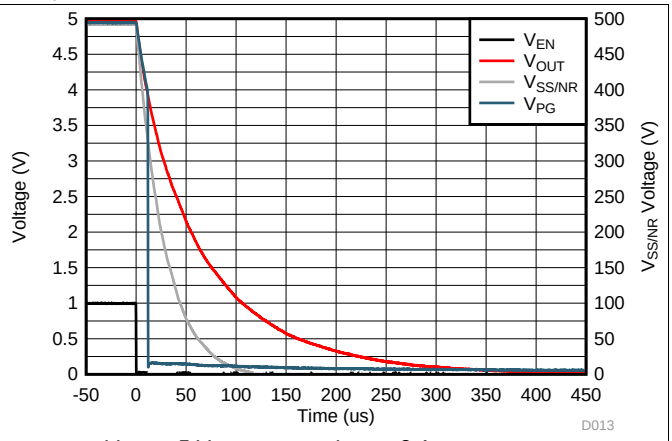
Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor and T_J = 25°C, unless otherwise stated.



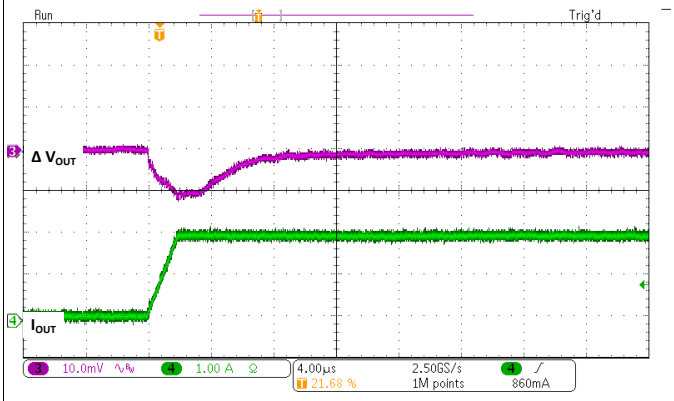
V_{OUT} = 5 V I_{OUT} = 1 mA

Figure 7. Power Down



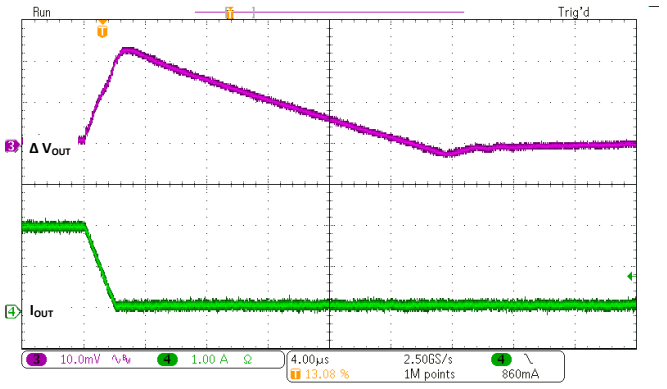
V_{OUT} = 5 V I_{OUT} = 2 A

Figure 8. Power Down



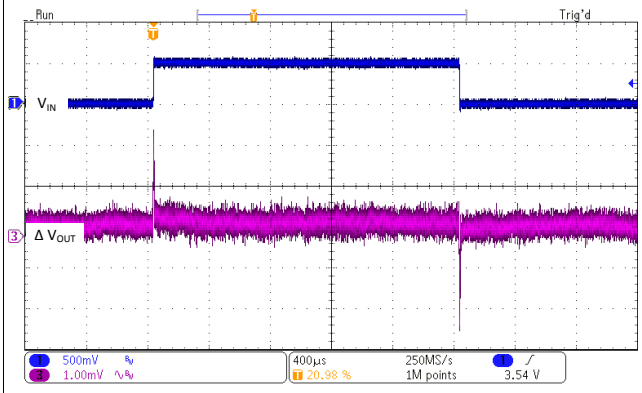
V_{OUT} = 2.8 V I_{OUT} = 10 mA to 2 A t_{rise} = 1 A/µs

Figure 9. Load Transient Response



V_{OUT} = 2.8 V I_{OUT} = 2 A to 10 mA t_{FALL} = 1 A/µs

Figure 10. Load Transient Response



V_{OUT} = 2.8 V t_{RISE} = t_{FALL} = 5 µs
V_{IN} = 3.3 V to 3.8 V to 3.3 V

Figure 11. Line Transient Response

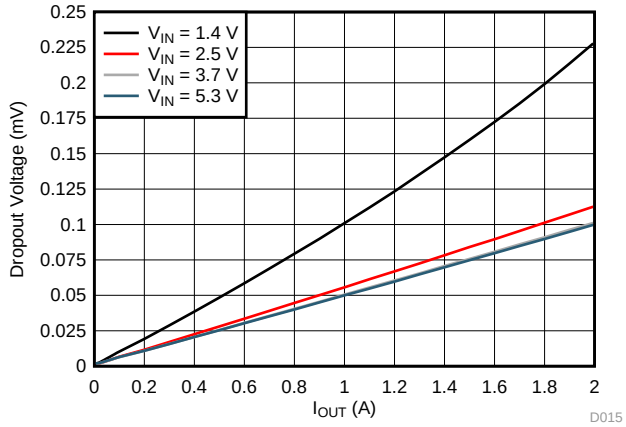
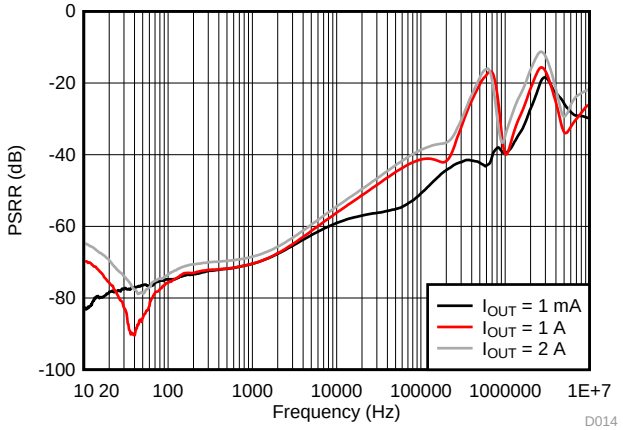


Figure 12. Dropout Voltage (V_{DO}) vs Load Current

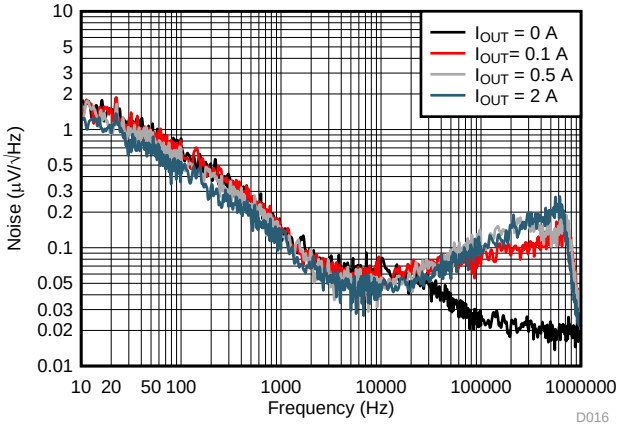
Typical Characteristics (continued)

V_{IN} = V_{OUT} + 0.5 V, V_{EN} = 1.2 V, C_{IN} = 22 µF, C_{OUT} = 22 µF, OUT connected to 50 Ω to GND, V_{FB} = 0.5 V, $C_{SS/NR}$ = 0.12 µF, C_{FF} = 0.01 µF, and PG pin pulled up to V_{IN} by 100-kΩ resistor and T_J = 25°C, unless otherwise stated.



V_{IN} = 5.5 V V_{OUT} = 5 V

Figure 13. PSRR vs Frequency



V_{IN} = 2.5 V V_{OUT} = 1.8 V

Figure 14. Noise Density vs Frequency

7 Detailed Description

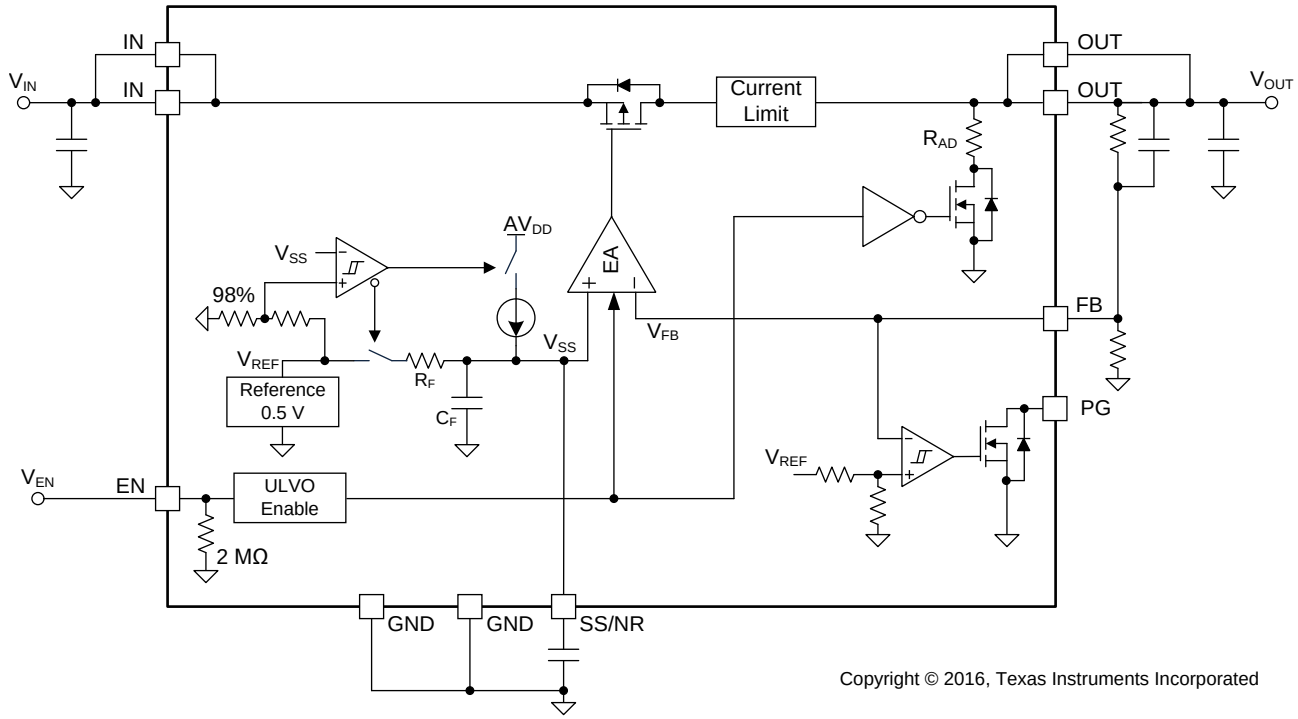
7.1 Overview

The LP5922 is a low-noise, high PSRR, low-dropout regulator capable of sourcing a 2-A load. The LP5922 can operate down to 1.3-V input voltage and 0.5-V output voltage. This combination of low noise, high PSRR, and low output voltage makes the device an ideal low dropout (LDO) regulator to power a multitude of loads from noise-sensitive communication components to battery-powered system.

The LP5922 block diagram contains several features, including:

- Low-noise, 0.5-V reference
- Internal protection circuit, such as current limit and thermal shutdown
- Programmable soft-start circuit
- Power Good output

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Voltage

The LP5922 output voltage can be set to any value from 0.5 V to 5 V using two external resistors shown as R_{UPPER} and R_{LOWER} in Figure 15. The value for the R_{LOWER} should be less than or equal to 100 kΩ for good loop compensation. R_{UPPER} can be selected for a given V_{OUT} using Equation 1:

$$R_{UPPER} = \frac{(V_{OUT} - V_{FB}) \times R_{LOWER}}{V_{FB}} \quad (1)$$

where

- V_{FB} = 0.5 V

Feature Description (continued)

7.3.2 Enable

The LP5922 EN pin is internally held low by a 2-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the VIL threshold to ensure that the device is fully disabled and the automatic output discharge is activated.

7.3.3 Output Automatic Discharge

The LP5922 output employs an internal 400-Ω (typical) pulldown resistance to discharge the output capacitor when the EN pin is low, and the device is disabled.

7.3.4 Programmable Soft Start and Noise Reduction

The output voltage of LP5922 ramps up linearly in a constant slew rate until reaching the target regulating voltage after a stable V_{IN} (greater than V_{OUT} + V_{DO}) is supplied and EN pin is pulled high. The slew rate of V_{OUT} ramping is programmable by an external capacitor on the SS/NR pin; therefore, the duration for soft-start period is programmable as well. Once the LP5922 is enabled, the SS/NR pin sources a constant 6-µA current to charge the external $C_{SS/NR}$ capacitor until the voltage at the SS/NR pin reaches 98% of the internal reference voltage (V_{REF}) of 500 mV typical. The final 2% of $C_{SS/NR}$ charge is determined by a RC time constant. During the soft-start period, the current flowing into the IN pin primarily consists of the sum of the load current at the LDO output and the charging current into the output capacitor. The soft-start period can be calculated by Equation 2:

$$t_{SS} = \frac{C_{SS/NR} \times V_{FB}}{I_{SS}} \quad (2)$$

where

- V_{FB} = 0.5 V - this is the voltage that $C_{SS/NR}$ charges to;
- $C_{SS/NR}$ is the value of the capacitor connected between the SS/NR pin and ground; and
- I_{SS} = 6.2 µA is the typical charging current to the SS/NR pin during start-up period.

The recommended value for $C_{SS/NR}$ is 100 nF or larger. Equation 2 is most accurate for these values. The $C_{SS/NR}$ capacitor is also the filter capacitor for internal reference for noise reduction purpose. An integrated resistor and the $C_{SS/NR}$ capacitor structure a RC low-pass filter to remove the noise on the internal reference voltage.

7.3.5 Internal Current Limit

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate in a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Note also that if a current limit occurs and the resulting output voltage is low, excessive power may be dissipated across the LDO, resulting in a thermal shutdown of the output.

7.3.6 Thermal Overload Protection

Thermal shutdown disables the output when the junction temperature rises to T_{SD} level, which allows the device to cool. When the junction temperature cools by ΔT_{SD}, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the LP5922 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the LP5922 into thermal shutdown degrades device reliability.

Feature Description (continued)

7.3.7 Power Good Output

The LP5922 has a Power-Good function that works by toggling the state of the PG output pin. When the output voltage falls below the PG threshold voltage (PG_{LTH}), the PG pin open-drain output engages (low impedance to GND). When the output voltage rises above the PG threshold voltage (PG_{HTH}), the PG pin becomes high-impedance. By connecting a pullup resistor to an external supply, any downstream device can receive PG as a logic signal. User must make sure that the external pullup supply voltage results in a valid logic signal for the receiving device or devices; use a pullup resistor from 10 kΩ to 100 kΩ for best results.

In Power-Good function, the PG output pin pulled high immediatelly after output voltage rises above the PG threshold voltage.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP5922 enable (EN) pin is internally held low by a 2-MΩ resistor to GND. If the EN pin is open the output is OFF. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. When the EN pin is pulled low, and the output is disabled, the output automatic discharge circuit is activated. Any charge on the OUT pin is discharged to GND through the internal pulldown resistance.

7.4.2 Undervoltage Lockout (UVLO)

The LP5922 incorporates UVLO. The UVLO circuit monitors the input voltage and keeps the LP5922 disabled while a rising V_{IN} is less than 1.2 V (typical). The rising UVLO threshold is approximately 100 mV below the recommended minimum operating V_{IN} of 1.3 V.

7.4.3 Minimum Operating Input Voltage

The LP5922 internal circuit is not fully functional until V_{IN} is at least 1.3 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 1.3 V or (V_{OUT} + V_{DO}).

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP5922 is designed to meet the requirements of RF and analog circuits, by providing low noise, high PSRR, low quiescent current, and low line or load transient response figures. The device offers excellent noise performance without the need for a noise bypass capacitor and is stable with input and output capacitors with a value of 22 µF. The LP5922 delivers this performance in an industry-standard WSON package which, for this device, is specified with an operating junction temperature (T_J) of –40°C to +125°C.

8.2 Typical Application

Figure 15 shows the typical application circuit for the LP5922. Input and output capacitances may need to be increased above 22 µF minimum for some applications.

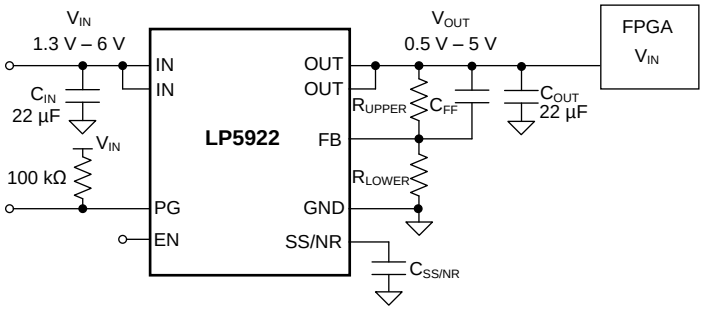


Figure 15. LP5922 Typical Application

8.2.1 Design Requirements

For typical LP5922 applications, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.25 V to 2.75 V
Output voltage	1.8 V
Output current	2000 mA
Output capacitor range	22 µF to 47 µF
Output capacitor ESR range	2 mΩ to 500 mΩ

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LP5922 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 External Capacitors

The LP5922 is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input, output, and the noise-reduction pin (SS/NR). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance. Additionally, the case size has a direct impact on the capacitance versus applied voltage derating.

Regardless of the ceramic capacitor type selected, the actual capacitance varies with the applied operating voltage and temperature. As a rule of thumb, derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a effective capacitance derating of approximately 50%, but at high applied voltage conditions the capacitance derating can be greater than 50% and must be taken into consideration. The minimum capacitance values declared in *Input and Output Capacitors* must be met across the entire expected operating voltage range and temperature range.

8.2.2.3 Input Capacitor, C_{IN}

An input capacitor is required for stability. A capacitor with a value of at least 22 µF must be connected between the LP5922 IN pin and ground for stable operation over full load current range. It is acceptable to have more output capacitance than input, as long as the input is at least 22 µF.

The input capacitor must be located as close as possible to, but at a distance not more than 1 cm from, the IN pin and returned to the device GND pin with a clean analog ground. This will minimize the trace inductance between the capacitor and the device. Any good quality ceramic or tantalum capacitor may be used at the input.

8.2.2.4 Output Capacitor, C_{OUT}

The LP5922 is designed to work specifically with a low ESR ceramic (MLCC) output capacitor, typically 22 µF. A ceramic capacitor (dielectric types X5R or X7R) in the 22-µF to 100-µF range, with an ESR not exceeding 500 mΩ, is suitable in the LP5922 application circuit having an output voltage greater than 0.8 V. For output voltages of 0.8 V or less, the output capacitance must be increased to typically 47 µF. The output capacitor must be connected between the device OUT and GND pins. The output capacitor must meet the requirement for the minimum value of capacitance and have an ESR value that does not exceed 500 mΩ to ensure stability.

It is possible to use tantalum capacitors at the device output, but these are not as attractive for reasons of size, cost, and performance.

A combination of multiple output capacitors in parallel boosts the high-frequency PSRR. The combination of one 0805-sized, 47-µF ceramic capacitor in parallel with two 0805-sized, 10-µF ceramic capacitors with a sufficient voltage rating optimizes PSRR response in the frequency range of 400 kHz to 700 kHz (which is a typical range for dc-dc supply switching frequency). This 47-µF || 10-µF || 10-µF combination also ensures that at high input voltage and high output voltage configurations, the minimum effective capacitance is met. Many 0805-sized, 47-µF ceramic capacitors have a voltage derating of approximately 60% to 75% at 5 V, so the addition of the two 10-µF capacitors ensures that the capacitance is at or above 22 µF.

8.2.2.5 Soft-Start and Noise-Reduction Capacitor, $C_{SS/NR}$

Recommended value for $C_{SS/NR}$ is 100 nF or larger. The soft-start period can be calculated by Equation 2. The $C_{SS/NR}$ capacitor is also the filter capacitor for internal reference for noise reduction purpose.

8.2.2.6 Feed-Forward Capacitor, C_{FF}

Although a feed-forward capacitor (C_{FF}) from the FB pin to the OUT pin is not required to achieve stability, a 10-nF external C_{FF} optimizes the transient, noise, and PSRR performance. A higher capacitance C_{FF} value can be used; however, the start-up time may be longer and the Power-Good signal may incorrectly indicate that the output voltage is settled. The maximum recommended value is 100 nF

To ensure proper PGx functionality, the time constant defined by CNR/SSx must be greater than or equal to the time constant from CFFx. For a detailed description, see the application report *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* (SBVA042).

8.2.2.7 No-Load Stability

The LP5922 remains stable, and in regulation, with no external load.

8.2.2.8 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the exposed thermal pad is critical to ensuring reliable operation. Device power dissipation depends on input voltage, output voltage, and load conditions and can be calculated with Equation 3.

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT} \quad (3)$$

Power dissipation can be minimized, and greater efficiency can be achieved, by using the lowest available voltage drop option that is greater than the dropout voltage (V_{DO}). However, keep in mind that higher voltage drops result in better dynamic (that is, PSRR and transient) performance.

On the WSON (DSC) package, the primary conduction path for heat is through the exposed thermal pad into the PCB. To ensure the device does not overheat, connect the exposed thermal pad, through multiple thermal vias, to an internal ground plane with an appropriate amount of PCB copper area.

Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to Equation 4 or Equation 5:

$$T_{J(MAX)} = T_{A(MAX)} + (R_{\theta JA} \times P_{D(MAX)}) \quad (4)$$

$$P_D = (T_{J(MAX)} - T_{A(MAX)}) / R_{\theta JA} \quad (5)$$

If the $V_{IN} - V_{OUT}$ voltage is known, the maximum allowable output current can be calculated with Equation 6

$$I_{OUT(MAX)} = (((125°C - T_A) / R_{\theta JA}) / (V_{IN} - V_{OUT})) \quad (6)$$

Unfortunately, the $R_{\theta JA}$ value is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the PCB size, total copper area, copper weight, any thermal vias, and location of the planes. The $R_{\theta JA}$ recorded in *Thermal Information* is determined by the specific EIA/JEDEC JESD51-7 standard for PCB and copper spreading area, and is to be used only as a relative measure of package thermal performance. For a well designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JC(bot)}$) plus the thermal resistance contribution by the PCB copper area acting as a heat sink.

8.2.2.9 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the *Thermal Information* table and are used in accordance with Equation 7 and Equation 8.

$$T_{J(MAX)} = T_{TOP} + (\Psi_{JT} \times P_{D(MAX)})$$

where

- T_{TOP} is the temperature measured at the center-top of the device package.
- $P_{D(MAX)}$ is described at Equation 3

(7)

$$T_{J(MAX)} = T_{BOARD} + (\Psi_{JB} \times P_{D(MAX)})$$

where

- T_{BOARD} is the PCB surface temperature measured 1 mm from the device package and centered on the package edge.
- $P_{D(MAX)}$ is described at Equation 3

(8)

For more information about the thermal characteristics Ψ_{JT} and Ψ_{JB}, see *Semiconductor and IC Package Thermal Metrics* ; for more information about measuring T_{TOP} and T_{BOARD}, see *Using New Thermal Metrics* ; and for more information about the EIA/JEDEC JESD51 PCB used for validating $R_{\theta JA}$, see the *TI Application Report Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*. These application notes are available at www.ti.com.

8.2.2.10 Recommended Continuous Operating Area

The continuous operational area of an LDO is limited by the input voltage (V_{IN}), the output voltage (V_{OUT}), the dropout voltage (V_{DO}), the output current (I_{OUT}), and the junction temperature (T_J). The recommended area for continuous operation for a linear regulator can be separated into the following steps, and is shown in Figure 16.

- Limited by dropout: Dropout voltage limits the minimum differential voltage between the input and the output ($V_{IN} – V_{OUT}$) at a given output current level.
- Limited by the rated output current: The rated output current limits the maximum recommended output current level. Exceeding this rating causes the device to fall out of specification.
- Limited by thermals: This portion of the boundary is defined by Equation 6. The slope is nonlinear because the junction temperature of the LDO is controlled by the power dissipation (P_D) across the LDO; therefore, when $V_{IN} – V_{OUT}$ increases, the output current must decrease in order to ensure that the rated maximum operating junction temperature of the device is not exceeded. Exceeding the maximum operating junction temperature rating can cause the device to fall out of specifications, reduces long-term reliability, and may activate the thermal shutdown protection circuitry.
- Limited by V_{IN} range: The rated operating input voltage range governs both the minimum and maximum of $V_{IN} – V_{OUT}$.

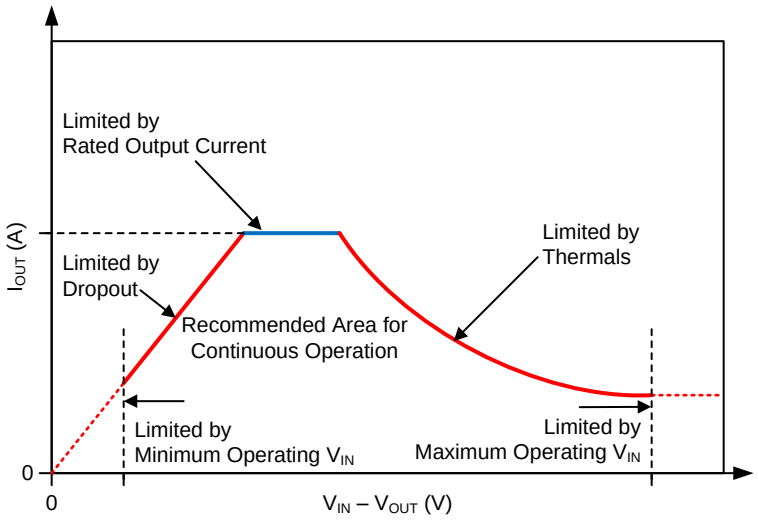


Figure 16. Recommended Continuous Operating Area

Figure 17 to Figure 22 show the recommended continuous operating area boundaries for this device in the WSON (DSC) package mounted to a EIA/JEDEC High-K printed circuit board, as defined by JESD51-7, with an $R_{\theta JA}$ rating of 49.5°C/W.

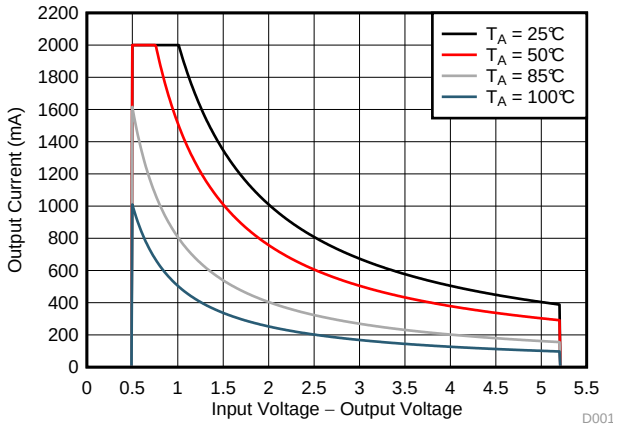


Figure 17. Recommended Continuous Operating Area for V_{OUT} = 0.8 V

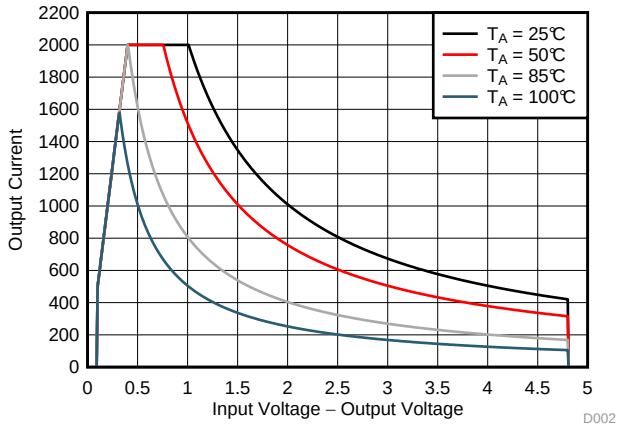


Figure 18. Recommended Continuous Operating Area for V_{OUT} = 1.2 V

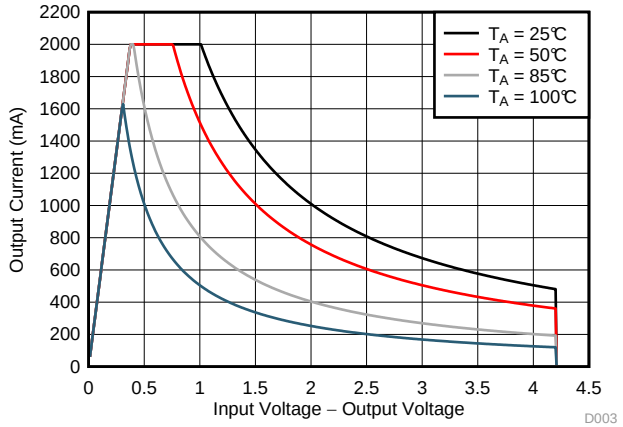


Figure 19. Recommended Continuous Operating Area for V_{OUT} = 1.8 V

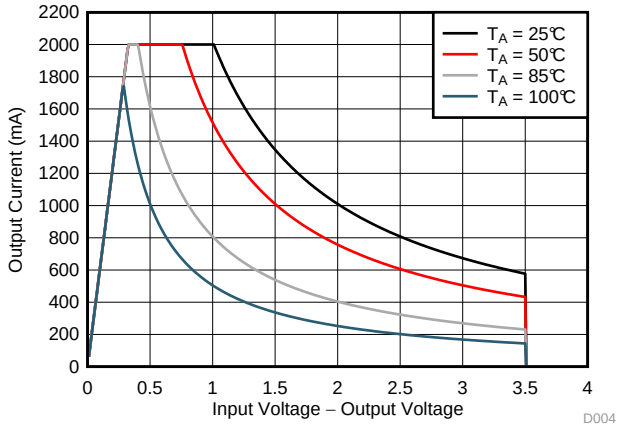


Figure 20. Recommended Continuous Operating Area for V_{OUT} = 2.5 V

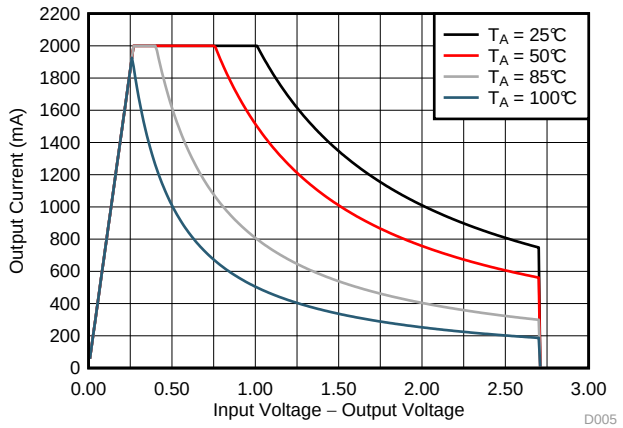


Figure 21. Recommended Continuous Operating Area for V_{OUT} = 3.3 V

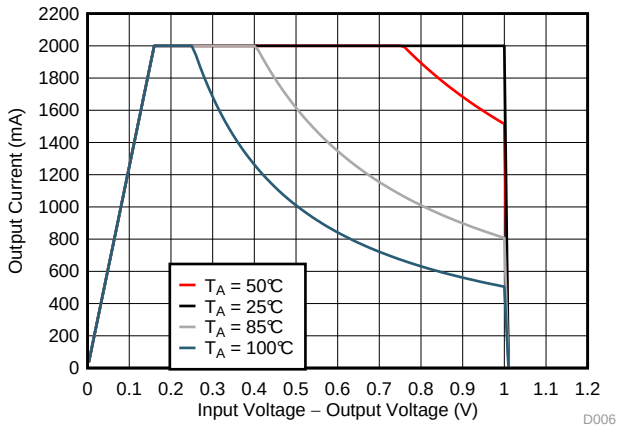


Figure 22. Recommended Continuous Operating Area for V_{OUT} = 5 V

8.2.3 Application Curves

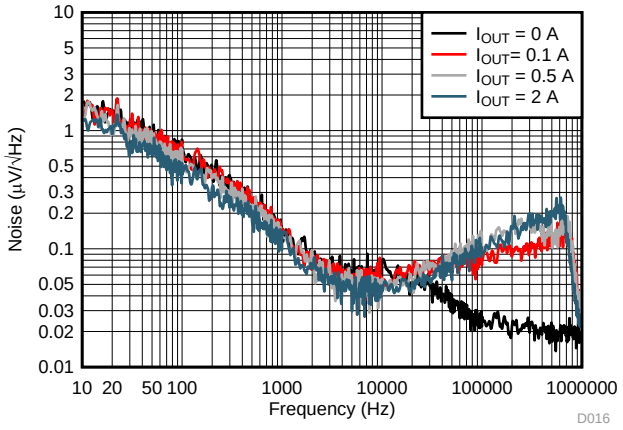


Figure 23. Noise Density vs Frequency

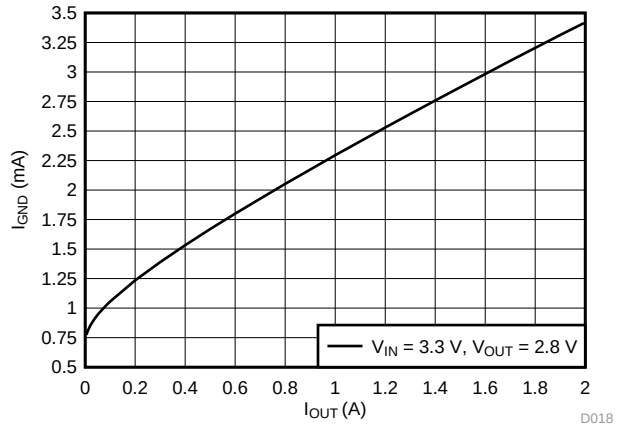


Figure 24. Ground Current vs Output Current

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 1.3 V to 6 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP5922 output voltage is well regulated and dynamic performance is optimum, the input supply must be at least V_{OUT} + 1 V. A minimum capacitor value of 22 μF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP5922 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the LP5922.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP5922 device, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} must be back to the LP5922 GND pin using as wide and as short of a copper trace as is practical.

Avoid connections using long trace lengths, narrow trace widths, or connections through vias. These add parasitic inductances and resistance that results in inferior performance especially during transient conditions

10.2 Layout Example

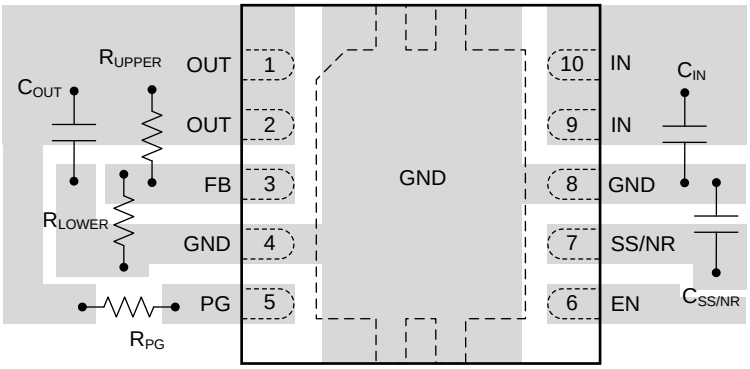


Figure 25. LP5922 Typical Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LP5922 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Related Documentation

For additional information, see the following:

- *Using New Thermal Metrics*
- *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP592201DSCR	NRND	WSON	DSC	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	592201	
LP592201DSCT	NRND	WSON	DSC	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	592201	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

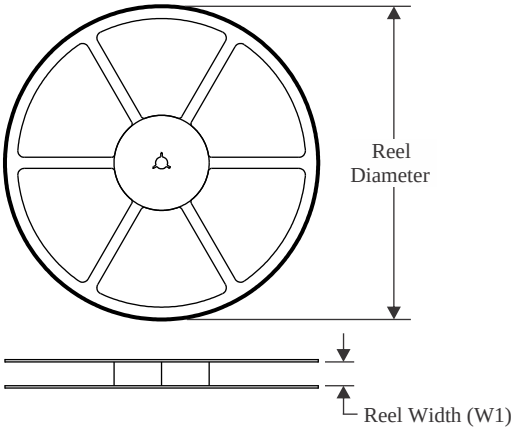
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

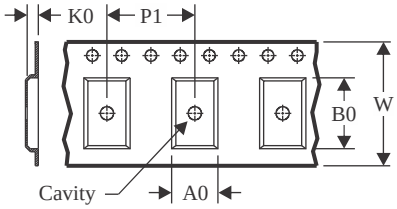
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

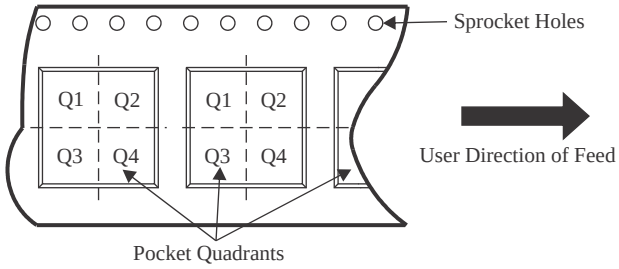


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

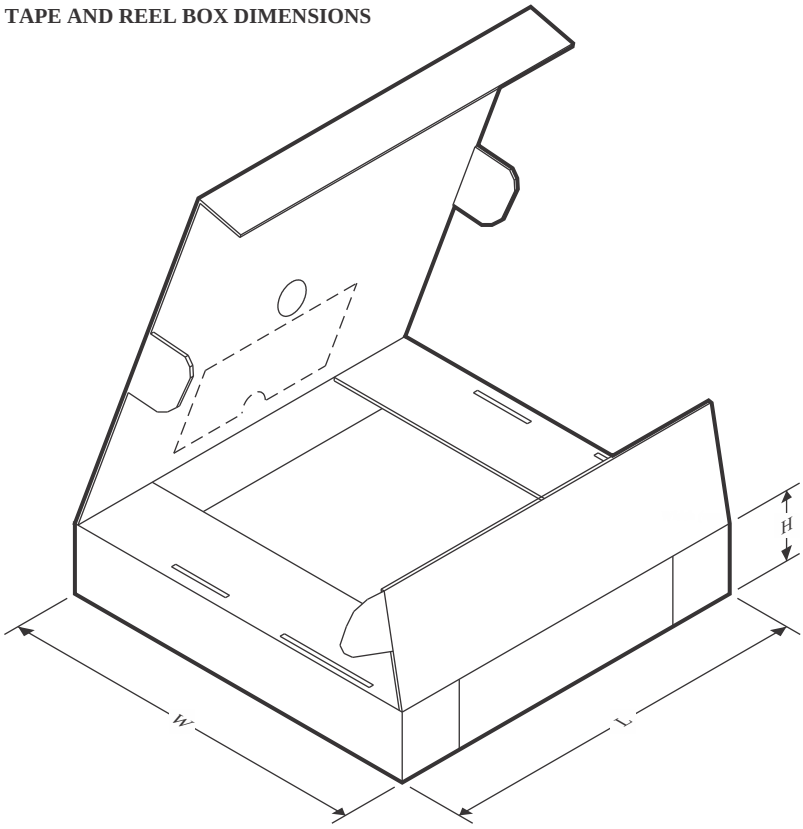
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP592201DSCR	WSON	DSC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP592201DSCT	WSON	DSC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

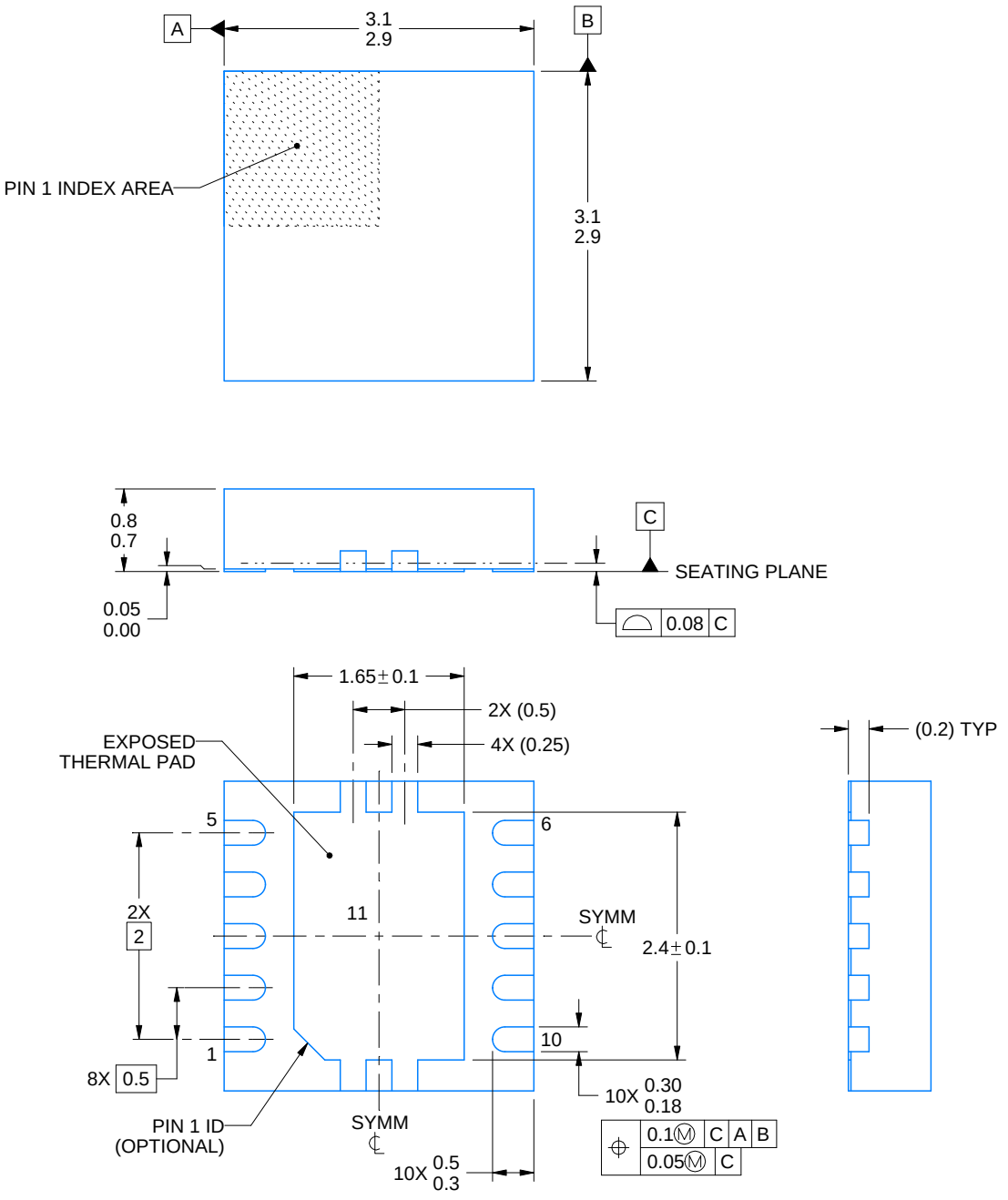
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP592201DSCR	WSON	DSC	10	3000	367.0	367.0	35.0
LP592201DSCT	WSON	DSC	10	250	210.0	185.0	35.0

DSC0010J

PACKAGE OUTLINE

WSON - 0.8 mm max height

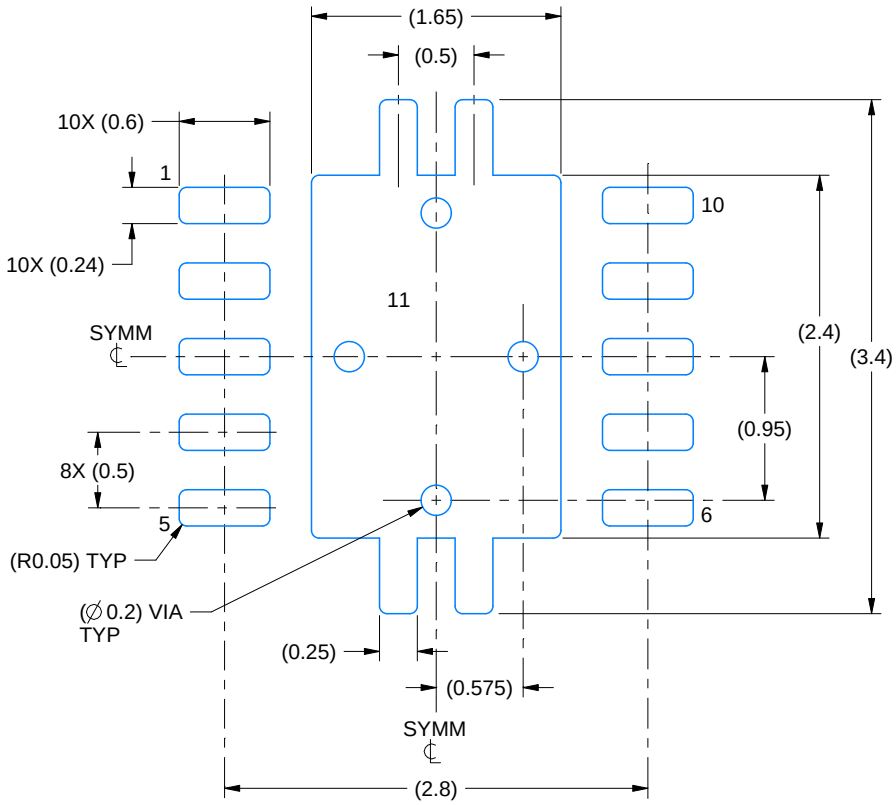
PLASTIC SMALL OUTLINE - NO LEAD



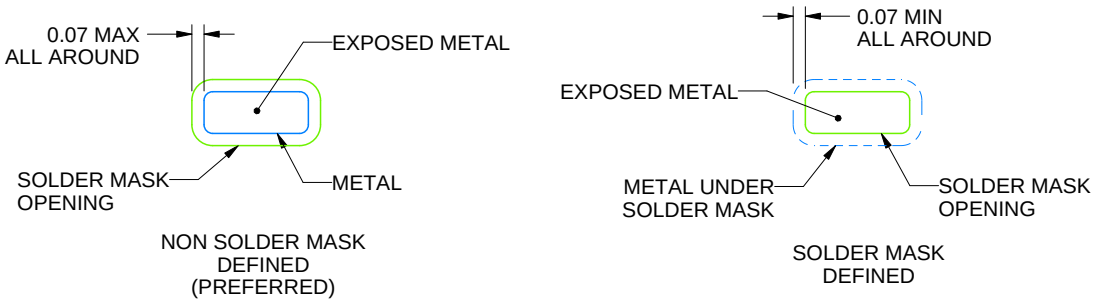
4221826/D 08/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

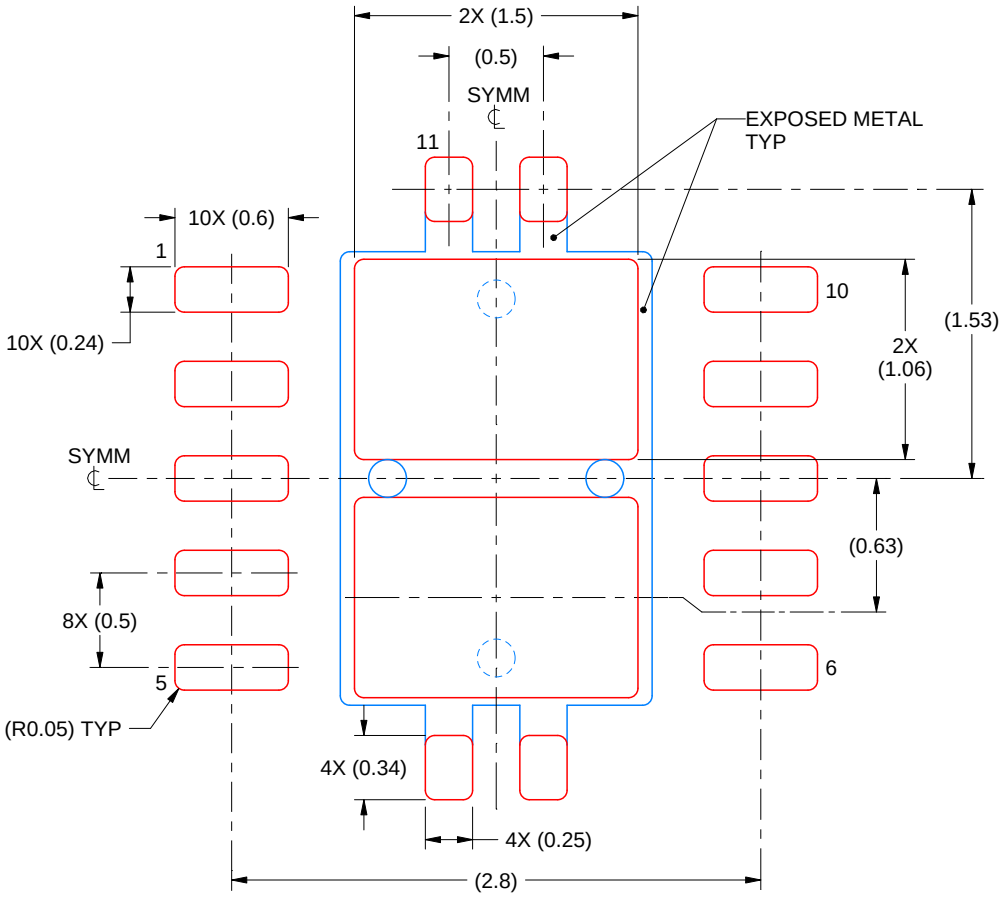


SOLDER MASK DETAILS

4221826/D 08/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4221826/D 08/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265