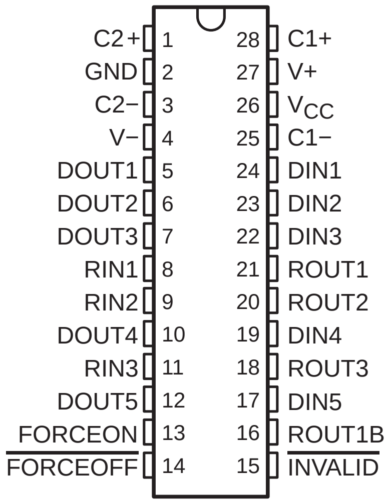
MAX3238
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ±15-kV ESD (HBM) PROTECTION

SLLS349J − JUNE 1999 − REVISED MARCH 2004

- **RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)**
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates With 3-V to 5.5-V V_{CC} Supply**
- **Operates Up To 250 kbit/s**
- **Five Drivers and Three Receivers**
- **Low Standby Current . . . 1 μA Typical**
- **External Capacitors . . . 4 × 0.1 μF**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Always-Active Noninverting Receiver Output (ROUT1B)**
- **Alternative High-Speed Pin-Compatible Device (1 Mbit/s)**
  - **SNx5C3238**
- **Applications**
  - **Battery-Powered Systems, PDAs, Notebooks, Subnotebooks, Laptops, Palmtop PCs, Hand-Held Equipment, Modems, and Printers**

DB OR PW PACKAGE
(TOP VIEW)



description/ordering information

The MAX3238 consists of five line drivers, three line receivers, and a dual charge-pump circuit with ±15-kV ESD (HBM) protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between notebook and subnotebook computer applications. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT1B), which allows applications using the ring indicator to transmit data while the device is powered down. These devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/μs driver output slew rate.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−0°C to 70°C	SSOP (DB)	Tube of 50	MAX3238CDB	MAX3238C
		Reel of 2000	MAX3238CDBR	
	TSSOP (PW)	Tube of 50	MAX3238CPW	MA3238C
		Reel of 2000	MAX3238CPWR	
−40°C to 85°C	SSOP (DB)	Tube of 50	MAX3238IDB	MAX3238I
		Reel of 2000	MAX3238IDBR	
	TSSOP (PW)	Tube of 50	MAX3238IPW	MB3238I
		Reel of 2000	MAX3238IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

Flexible control options for power management are featured when the serial port and driver inputs are inactive. The auto-powerdown plus feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense valid signal transitions on all receiver and driver inputs for approximately 30 s, the built-in charge pump and drivers are powered down, reducing the supply current to 1 µA. By disconnecting the serial port or placing the peripheral drivers off, auto-powerdown plus occurs if there is no activity in the logic levels for the driver inputs. Auto-powerdown plus can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-powerdown plus enabled, the device activates automatically when a valid signal is applied to any receiver or driver input. $\overline{\text{INVALID}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than −2.7 V, or has been between −0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INVALID}}$ is low (invalid data) if all receiver input voltages are between −0.3 V and 0.3 V for more than 30 µs. Refer to Figure 5 for receiver input levels.

Function Tables

EACH DRIVER

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	
L	L	H	<30 s	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 s	L	
L	L	H	>30 s	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 s	Z	

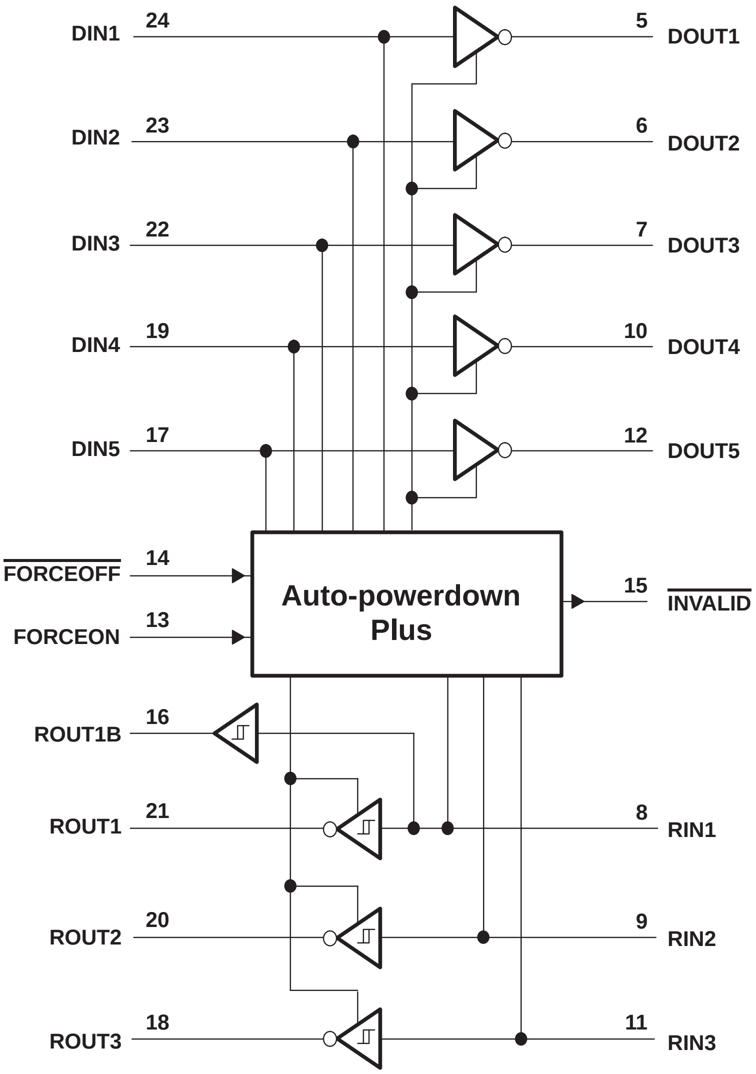
H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER

INPUTS				OUTPUTS		RECEIVER STATUS
RIN1	RIN2−RIN3	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT1B	ROUT	
L	X	L	X	L	Z	Powered off while ROUT1B is active
H	X	L	X	H	Z	
L	L	H	<30 s	L	H	Normal operation with auto-powerdown plus disabled/enabled
L	H	H	<30 s	L	L	
H	L	H	<30 s	H	H	
H	H	H	<30 s	H	L	
Open	Open	H	>30 s	L	H	

H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1)	−0.3 V to 7 V
Negative output supply voltage range, V− (see Note 1)	0.3 V to −7 V
Supply voltage difference, V+ − V− (see Note 1)	13 V
Input voltage range, V_I: Driver ($\overline{\text{FORCEOFF}}$, FORCEON)	−0.3 V to 6 V
Receiver	−25 V to 25 V
Output voltage range, V_O: Driver	−13.2 V to 13.2 V
Receiver ($\overline{\text{INVALID}}$)	−0.3 V to V_{CC} + 0.3 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package	62°C/W
PW package	62°C/W
Operating virtual junction temperature, T_J	150°C
Storage temperature range, T_{stg}	−65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.

2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 6)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
			V_{CC} = 5 V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_{CC} = 3.3 V	2			V
			V_{CC} = 5 V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			−25		25	V
T_A	Operating free-air temperature		MAX3238C	0		70	°C
			MAX3238I	−40		85	

NOTE 4: Testing supply conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER			TEST CONDITIONS	MIN	TYP[‡]	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±1	µA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown plus disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}		0.5	2	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	µA
		Auto-powerdown plus enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

[‡] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

NOTE 4: Testing supply conditions are C1−C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 µF and C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND		5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND		−5	−5.4		V
I_{IH}	High-level input current	$V_I = V_{CC}$			±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	μA
I_{OS}	Short-circuit output current[‡]	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V		±40	±100	
r_o	Output resistance	V_{CC}, V+, and V− = 0 V,	V_O = ±2 V	300	10M		Ω
I_{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = GND	V_O = ±12 V, V_{CC} = 3 V to 3.6 V			±25	μA
			V_O = ±10 V, V_{CC} = 4.5 V to 5.5 V			±25	

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[‡] Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Testing supply conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ, See Figure 1	150	250		kbit/s
$t_{sk(p)}$	Pulse skew[§]	C_L = 150 pF to 2500 pF	R_L = 3 kΩ to 7 kΩ, See Figure 2		100		ns
SR(tr)	Slew rate, transition region (see Figure 1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF	6		30	V/μs
			C_L = 150 pF to 2500 pF	4		30	

[†] All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

[§] Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

NOTE 4: Testing supply conditions are C1−C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1−C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA	$V_{CC}-0.6$ V	$V_{CC}-0.1$ V		V
V_{OL}	Low-level output voltage	$I_{OL} = 1.6$ mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	$V_{CC} = 3.3$ V		1.5	2.4	V
		$V_{CC} = 5$ V		1.8	2.4	
V_{IT-}	Negative-going input threshold voltage	$V_{CC} = 3.3$ V	0.6	1.2		V
		$V_{CC} = 5$ V	0.8	1.5		
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.3		V
I_{off}	Output leakage current (except ROUT1B)	$\overline{\text{FORCEOFF}} = 0$ V		±0.05	±10	μA
r_i	Input resistance	$V_I = \pm 3$ V to ±25 V	3	5	7	kΩ

[†] All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25°C$.

NOTE 4: Testing supply conditions are C1−C4 = 0.1 μF at $V_{CC} = 3.3$ V ± 0.15 V; C1−C4 = 0.22 μF at $V_{CC} = 3.3$ V ± 0.3 V; and C1 = 0.047 μF and C2−C4 = 0.33 μF at $V_{CC} = 5$ V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 150$ pF, See Figure 3		150		ns
t_{PHL}	Propagation delay time, high- to low-level output			150		ns
t_{en}	Output enable time	$C_L = 150$ pF, $R_L = 3$ kΩ, See Figure 4		200		ns
t_{dis}	Output disable time			200		ns
$t_{sk(p)}$	Pulse skew[‡]	See Figure 3		50		ns

[†] All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25°C$.

[‡] Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

NOTE 4: Testing supply conditions are C1−C4 = 0.1 μF at $V_{CC} = 3.3$ V ± 0.15 V; C1−C4 = 0.22 μF at $V_{CC} = 3.3$ V ± 0.3 V; and C1 = 0.047 μF and C2−C4 = 0.33 μF at $V_{CC} = 5$ V ± 0.5 V.

AUTO-POWERDOWN PLUS SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}			2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	−2.7			V
$V_{T(invalid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	−0.3		0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	I_{OH} = −1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}	V_{CC}−0.6			V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_{CC}			0.4	V

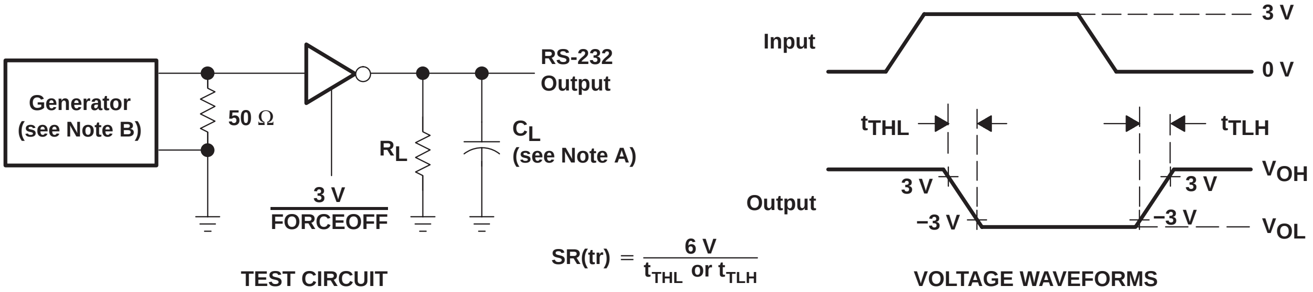
† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

PARAMETER		MIN	TYP†	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		0.1		µs
$t_{invalid}$	Propagation delay time, high- to low-level output		50		µs
t_{en}	Supply enable time		25		µs
t_{dis}	Receiver or driver edge to auto-powerdown plus	15	30	60	s

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

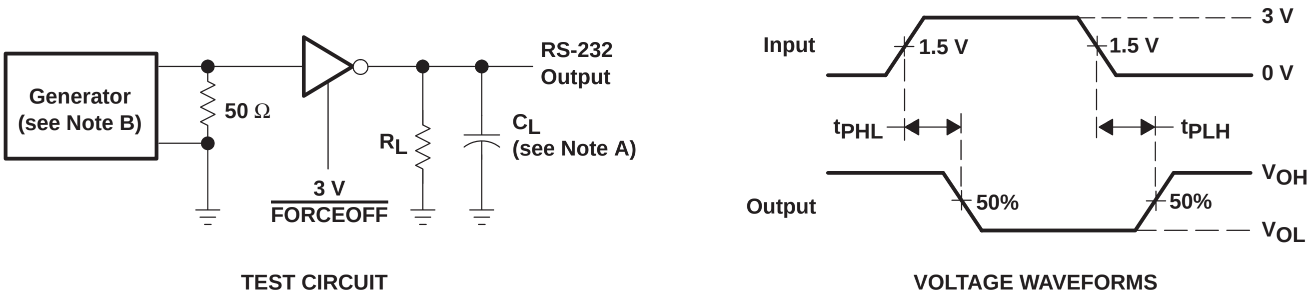


$$SR(tr) = \frac{6\ V}{t_{THL}\ \text{or}\ t_{TLH}}$$

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

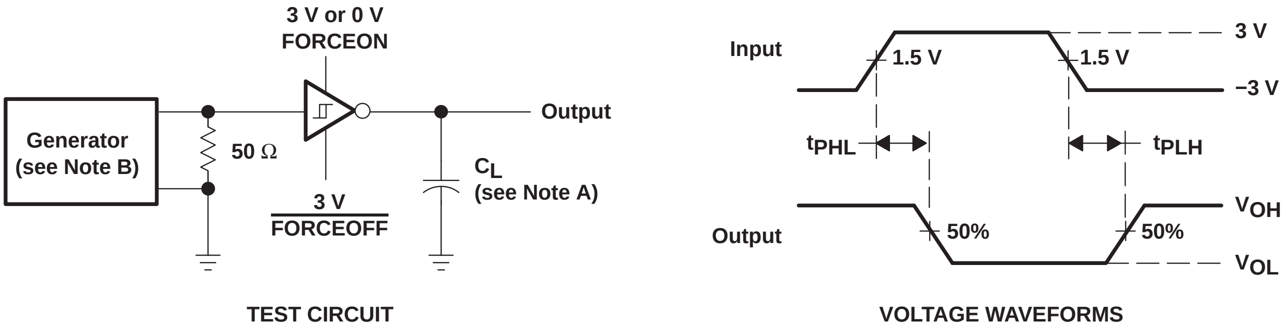
Figure 1. Driver Slew Rate

PARAMETER MEASUREMENT INFORMATION



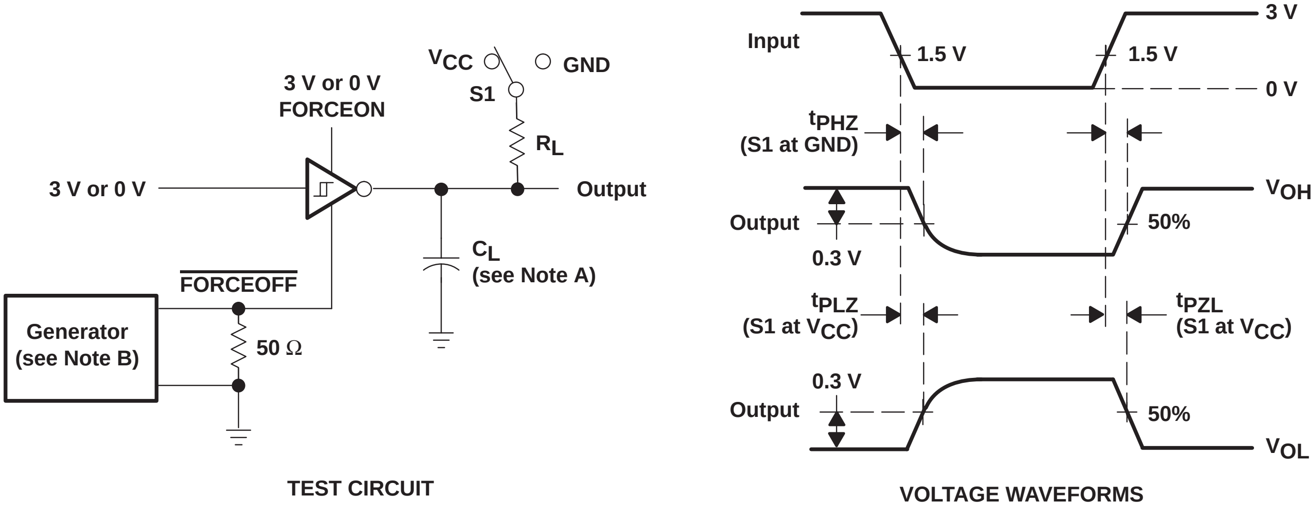
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

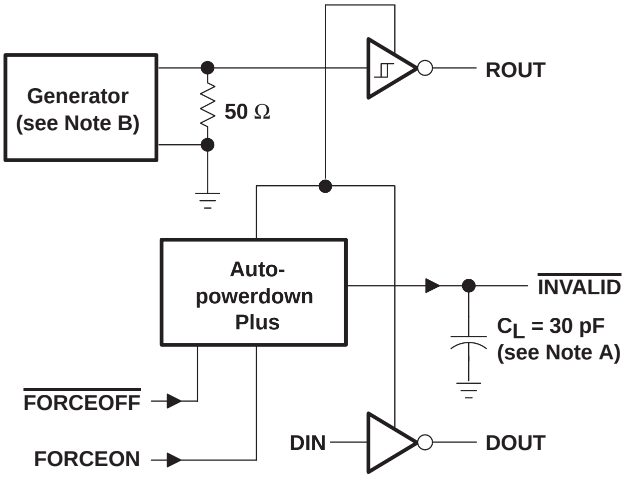
Figure 3. Receiver Propagation Delay Times



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

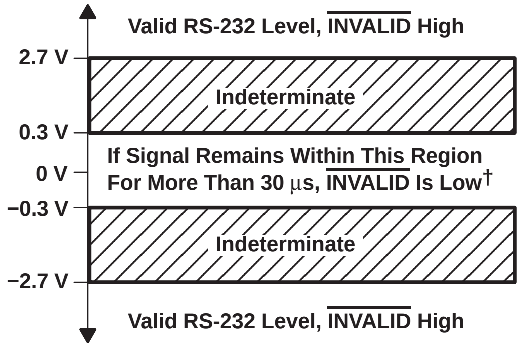
Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION

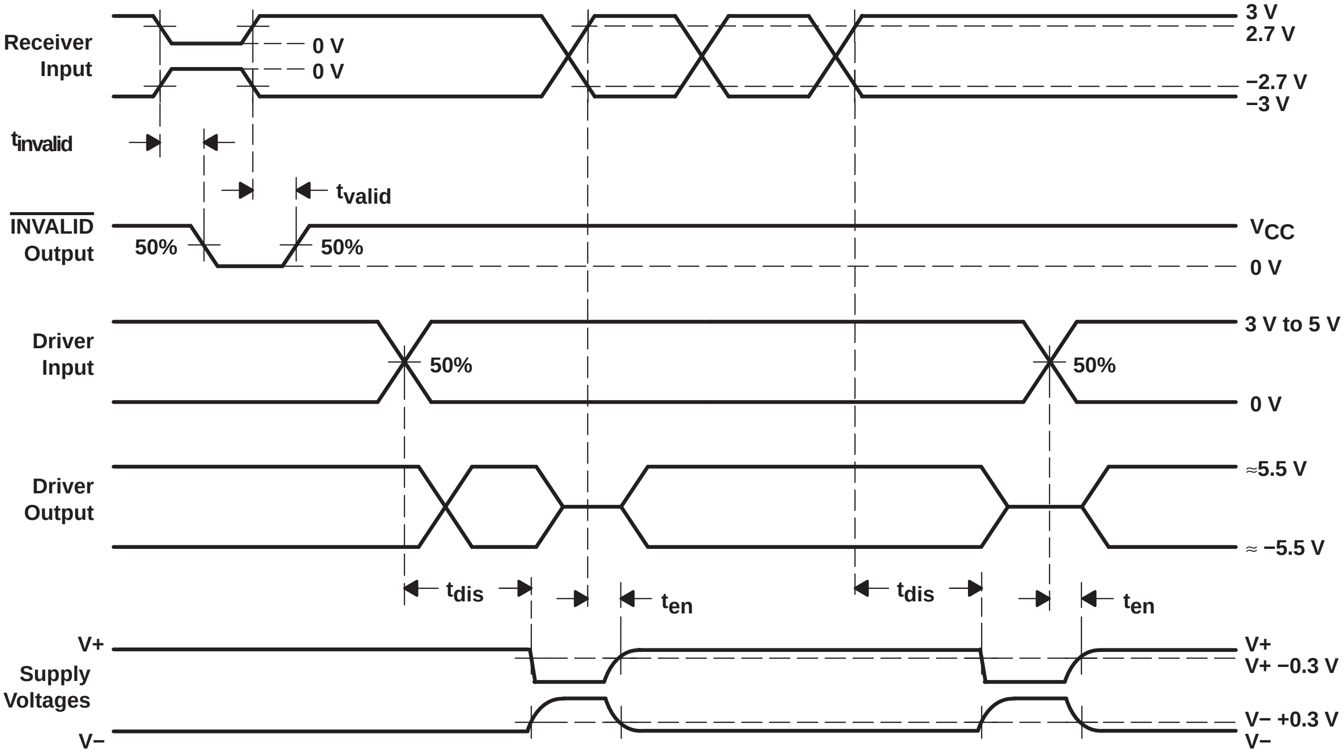


TEST CIRCUIT

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.



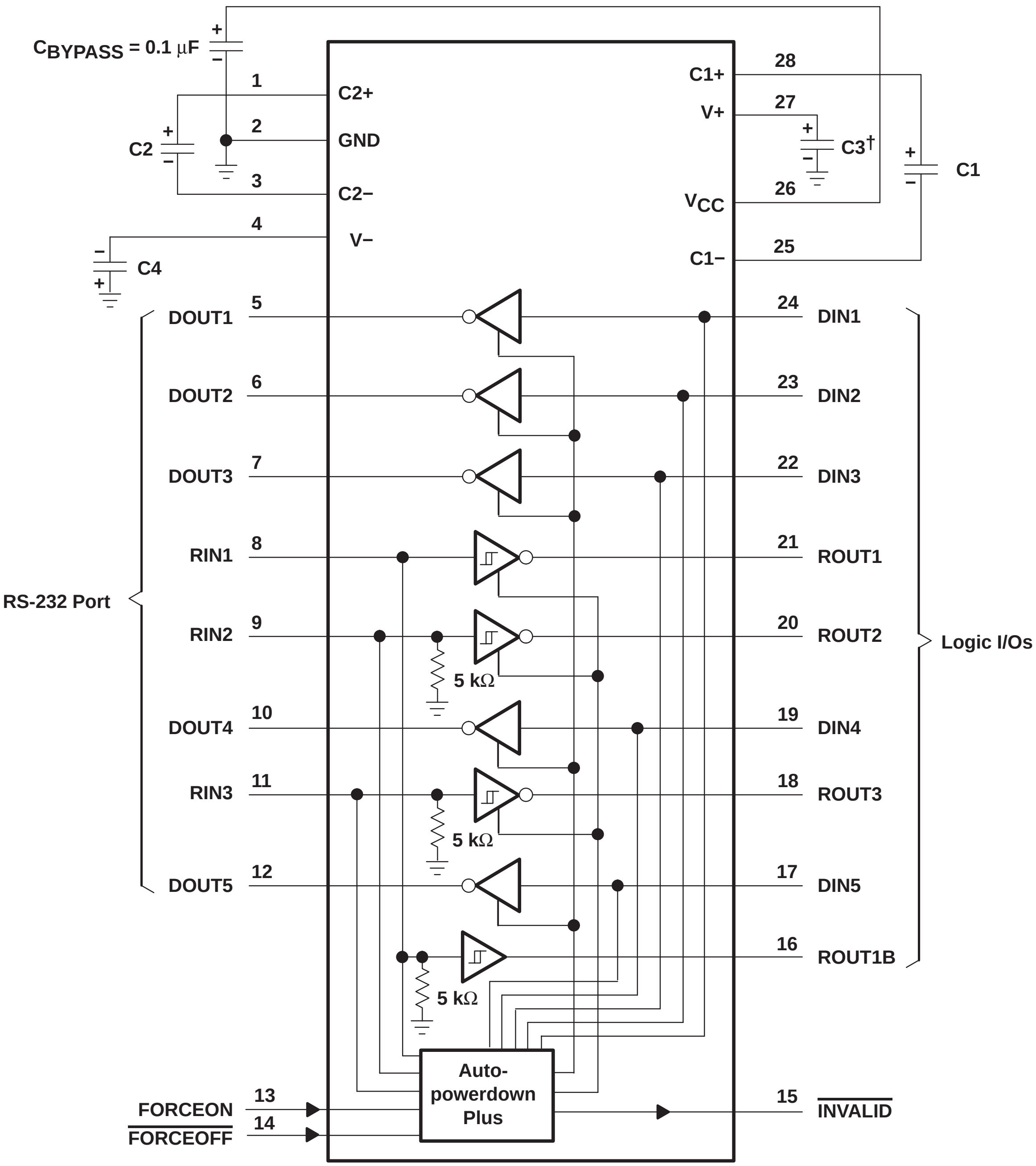
† Auto-powerdown plus disables drivers and reduces supply current to 1 μA.



Voltage Waveforms and Timing Diagrams

Figure 5. $\overline{\text{INVALID}}$ Propagation-Delay Times and Supply-Enabling Time

APPLICATION INFORMATION



V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.15 V	0.1 µF	0.1 µF
3.3 V ± 0.3 V	0.22 µF	0.22 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.22 µF	1 µF

† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 6. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3238CDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3238C	Samples
MAX3238CDBRE4	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3238C	Samples
MAX3238CPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MA3238C	Samples
MAX3238IDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3238I	Samples
MAX3238IPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MB3238I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF MAX3238 :

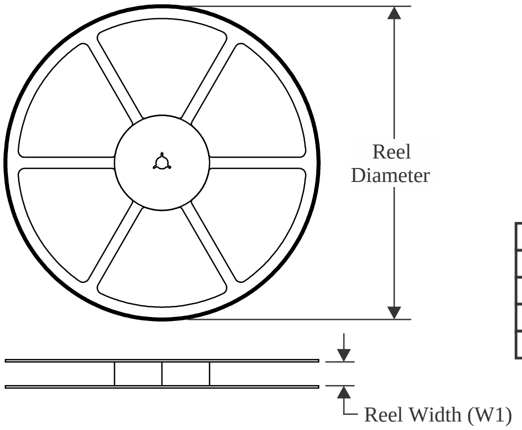
- Automotive : MAX3238-Q1

NOTE: Qualified Version Definitions:

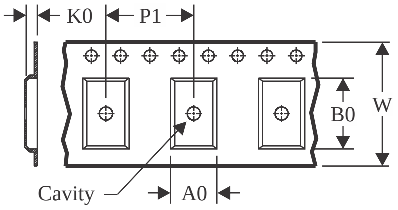
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

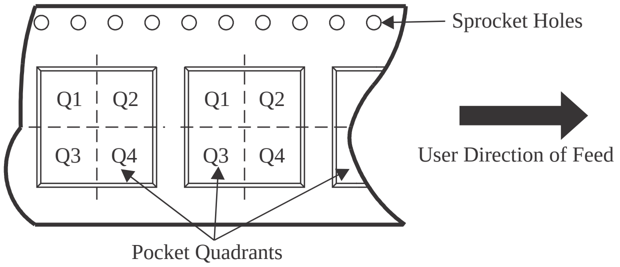


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

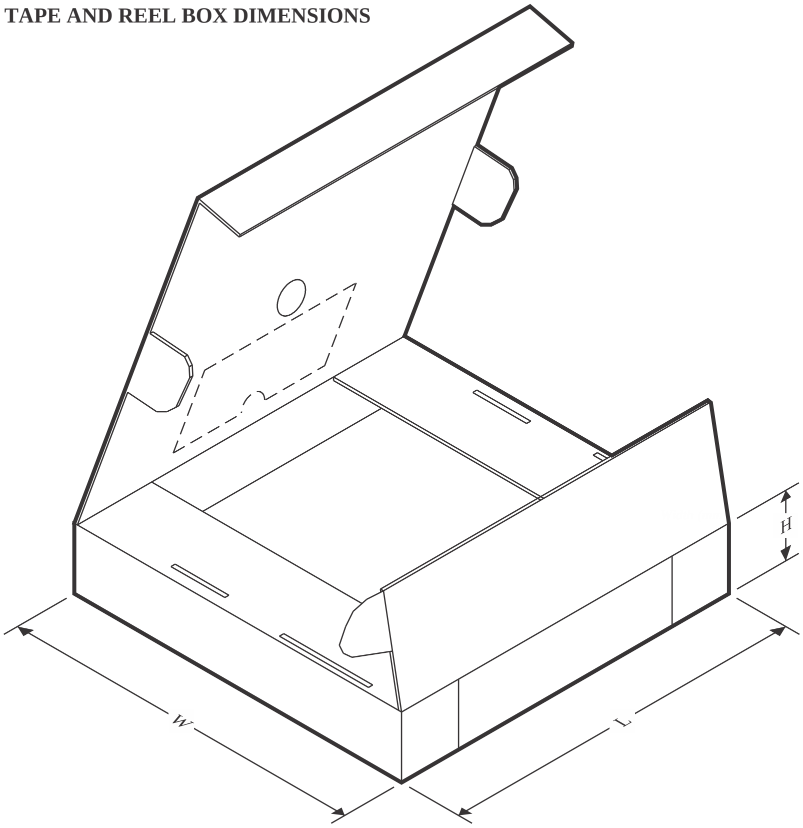
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3238CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX3238CPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MAX3238IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
MAX3238IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

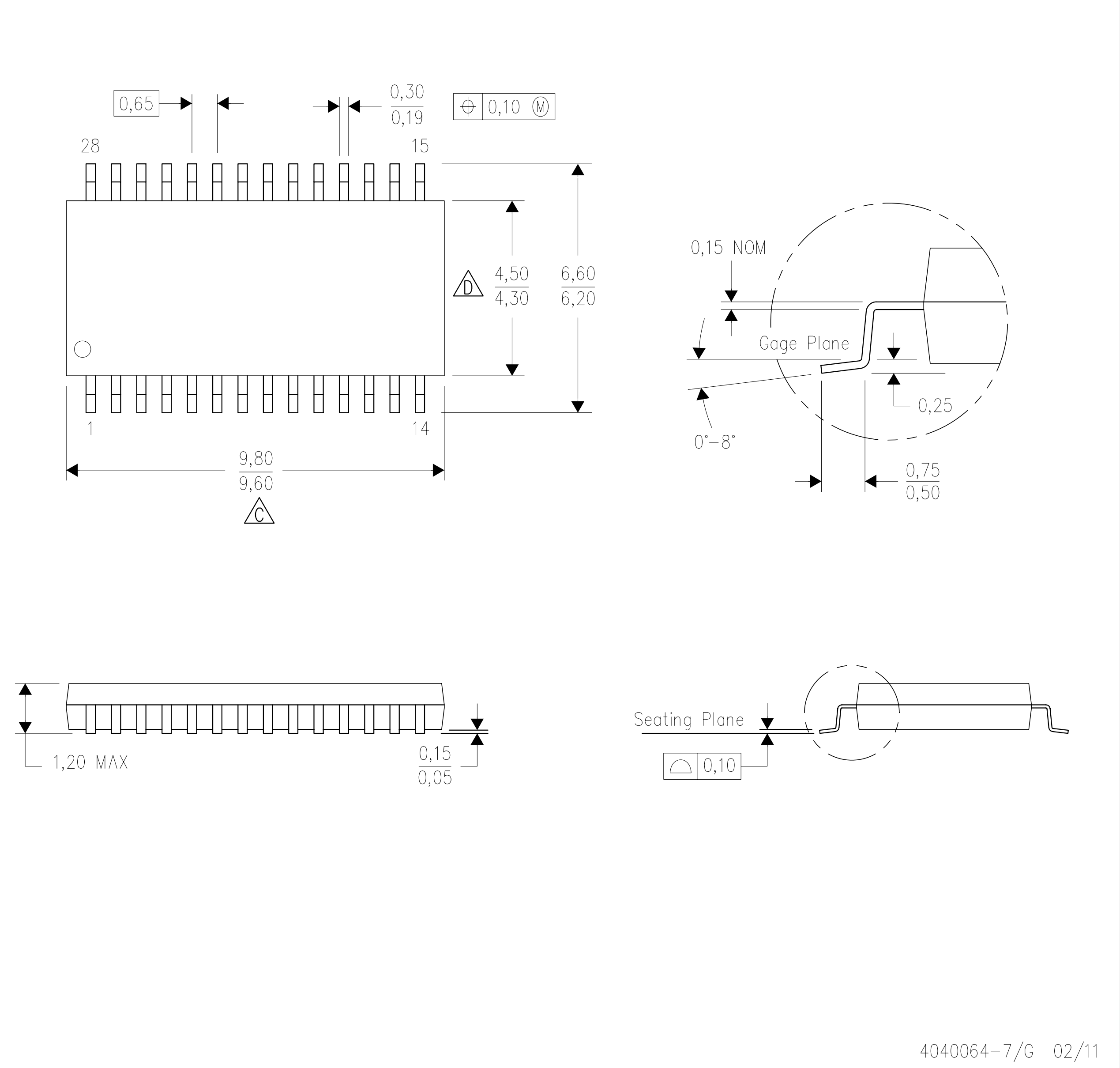
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

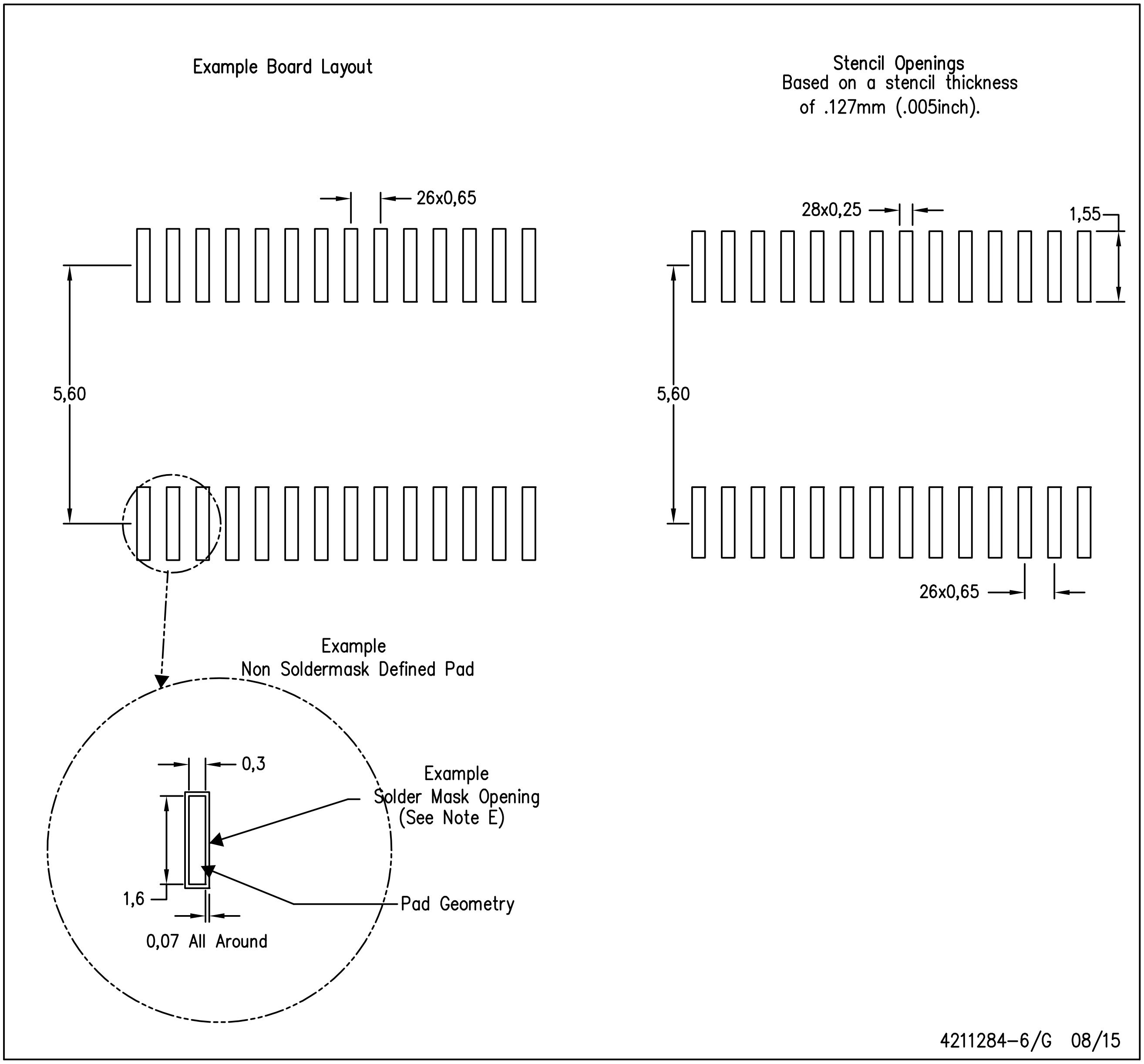
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3238CDBR	SSOP	DB	28	2000	356.0	356.0	35.0
MAX3238CPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
MAX3238IDBR	SSOP	DB	28	2000	356.0	356.0	35.0
MAX3238IPWR	TSSOP	PW	28	2000	356.0	356.0	35.0

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G28) PLASTIC SMALL OUTLINE



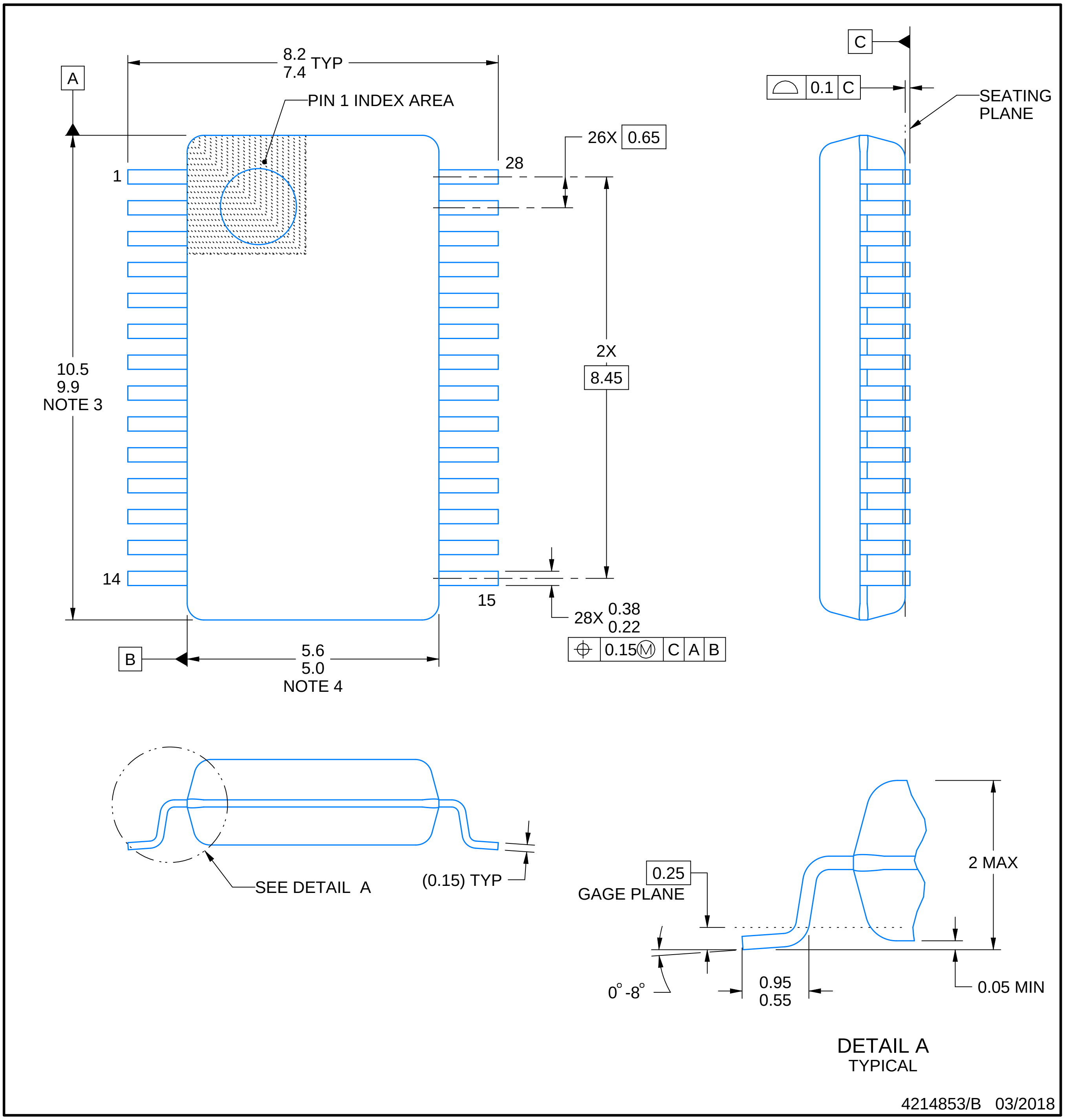
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0028A

PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



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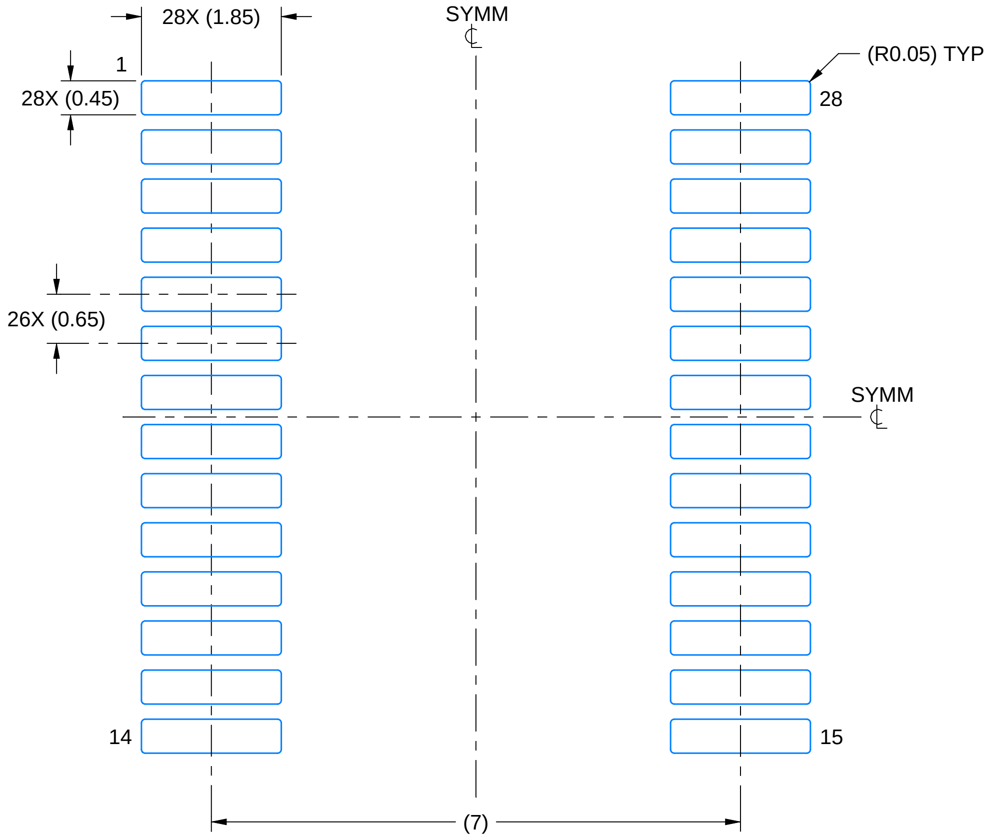
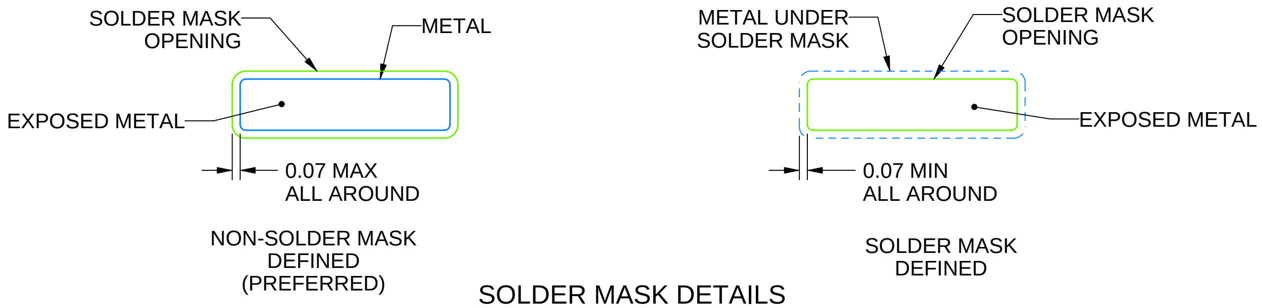
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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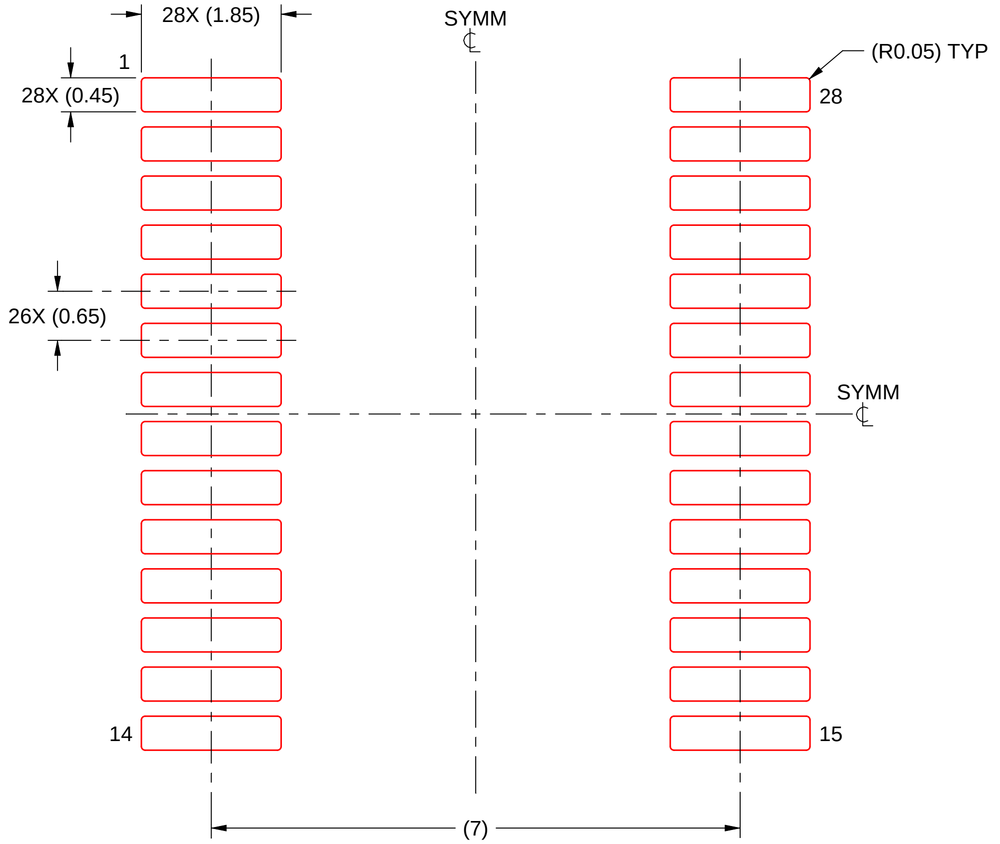
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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